LPC5410x

32-bit ARM Cortex-M4F/M0+ MCU; 104 KB SRAM; 512 KB flash, 3 x I2C, 2 x SPI, 4 x USART, 32-bit counter/timers, SCTimer/PWM, ADC

Rev. 1.1 — 18 November 2014 **Product data sheet**

1. General description

The LPC5410x are ARM Cortex-M4F based microcontrollers for embedded applications. These devices include an optional ARM Cortex-M0+ coprocessor, 104 KB of on-chip SRAM, 512 KB on-chip flash, five general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I^{2}C-bus interfaces with high-speed slave mode, and one 12-bit 4.8 Msamples/sec ADC.

The ARM Cortex-M4 is a 32-bit core that offers system enhancements such as low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. The Cortex-M4F is the Cortex-M4 with the inclusion of the 32-bit Floating Point Unit.

The ARM Cortex-M0+ coprocessor is an energy-efficient and easy-to-use 32-bit core which is code- and tool-compatible with the Cortex-M4F core. The Cortex-M0+ coprocessor offers up to 100 MHz performance with a simple instruction set and reduced code size.

2. Features and benefits

- Dual processor cores: ARM Cortex-M4 and ARM Cortex-M0+. The M0+ core runs at the same frequency as the M4 core. Both cores operate up to a maximum frequency of 100 MHz.
- ARM Cortex-M4F core (version r0p1):
  - ARM Cortex-M4 processor, running at a frequency of up to 100 MHz.
  - Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with eight breakpoints and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.
- ARM Cortex-M0+ core (version r0p1):
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).

  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 512 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - 104 KB SRAM for code and data use.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - Power control API.
- Serial interfaces:
  - Four USART interfaces with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs include a FIFO buffer and share a fractional baud-rate generator.
  - Two SPI interfaces, each with four slave selects and flexible data configuration. The SPIs include a FIFO buffer. The slave function is able to wake up the device from Deep-sleep and Power-down modes.
  - Three I^{2}C-bus interfaces supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Each I^{2}C-bus interface also supports High Speed Mode (3.4 Mbit/s) as a slave. The slave function is able to wake up the device from Deep-sleep and Power-down modes.
- Digital peripherals:
  - DMA controller with 22 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 50 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input/output inverter.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
  - Up to eight GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.
- Timers:
  - Five 32-bit general purpose timers/counters, with up to 4 capture inputs and 4 compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
  - One State Configurable Timer/PWM (SCT) with 6 input and 8 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to/from selected peripherals. Internally, the SCT supports 13 captures/matches, 13 events and 13 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including Deep power-down, with 1 ms resolution. The RTC is clocked by the 32 kHz oscillator.

  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Ultra-low power Micro-tick Timer, running from the Watchdog oscillator, that can be used to wake up the device from low power modes.
  - Repetitive Interrupt Timer (RIT) for debug time-stamping and general-purpose use.
- Analog peripheral: 12-bit, 12-channel, Analog-to-Digital Converter (ADC) supporting 4.8 Msamples/s. The ADC supports two independent conversion sequences.
- Clock generation:
  - 12 MHz internal RC oscillator.
  - External clock input for clock frequencies of up to 24 MHz.
  - Internal low-power, watchdog oscillator with a nominal frequency of 500 kHz (WDOSC).
  - 32 kHz low-power RTC oscillator.
  - System PLL allows CPU operation up to the maximum CPU rate. May be run from the internal RC oscillator, the external clock input CLKIN, or the RTC oscillator.
  - Clock output function for monitoring internal clocks.
  - Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Wake-up from Deep-sleep and Power-down modes via activity on the USART, SPI, and I^{2}C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes using the RTC alarm.
  - The Micro-tick Timer can wake-up the device from the Deep power-down mode by using the watchdog oscillator when no other on-chip resources are running.
- Single power supply 1.62 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- Unique device serial number for identification.
- Operating temperature range –40 °C to 105 °C.
- Available in a 3.288 x 3.288 mm WLCSP49 package and LQFP64 package.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54102J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J512UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54101J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.288 x 3.288 x 0.54 mm	-
LPC54102J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54102J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J512BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54101J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	Total SRAM/KB	Core M4 w/ FPU	Core M0+	GPIO
LPC54102J512UK49	512	104	1	1	39
LPC54102J256UK49	256	104	1	1	39
LPC54101J512UK49	512	104	1	0	39
LPC54101J256UK49	256	104	1	0	39
LPC54102J512BD64	512	104	1	1	50
LPC54102J256BD64	256	104	1	1	50
LPC54101J512BD64	512	104	1	0	50
LPC54101J256BD64	256	104	1	0	50

[1] All of the parts include five general-purpose timers, one State-Configurable Timer with PWM capabilities (SCTimer/PWM), one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), four USARTs, two SPIs, three Fast-mode plus I2C-bus interfaces with high-speed slave mode, and one 12-bit 4.8 Msamples/sec ADC.

4. Marking

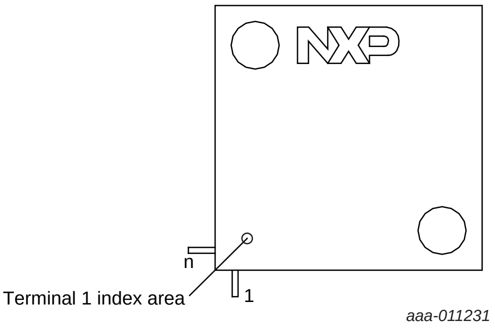


Fig 1. LQFP64 package marking

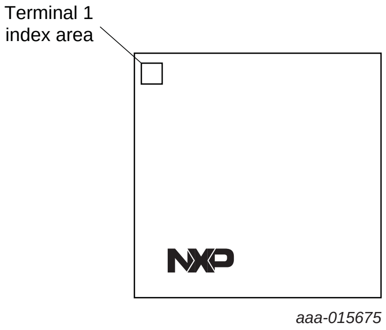


Fig 2. WLCSP49 package marking

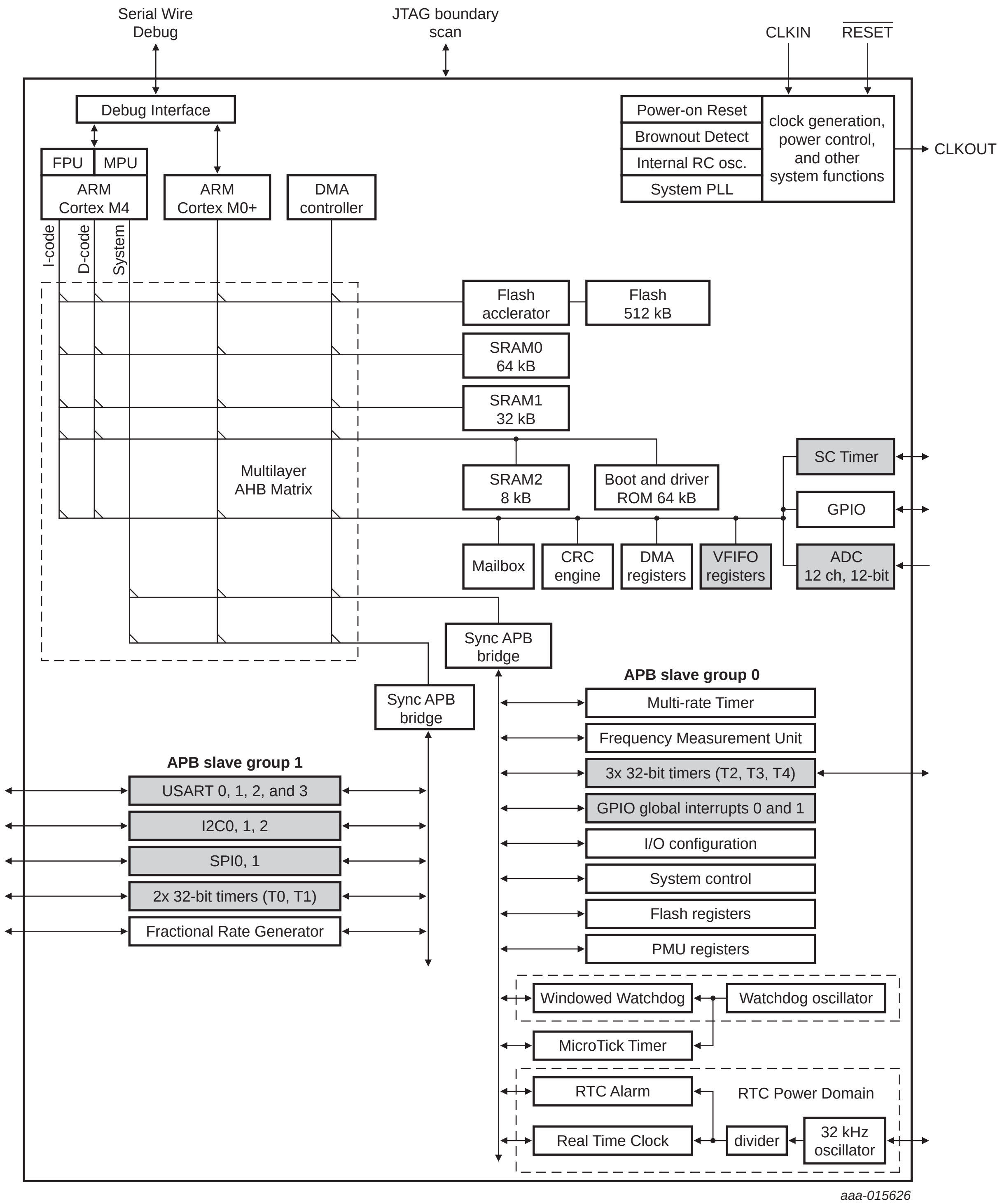
The LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJ512
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - R = Chip revision.

The LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
- Second line: J512UK49
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]x
  - R = Chip revision.

5. Block diagram



Gray-shaded peripheral blocks provide dedicated request lines or triggers for DMA transfers.

Fig 3. LPC5410x Block diagram

6. Pinning information

6.1 Pinning

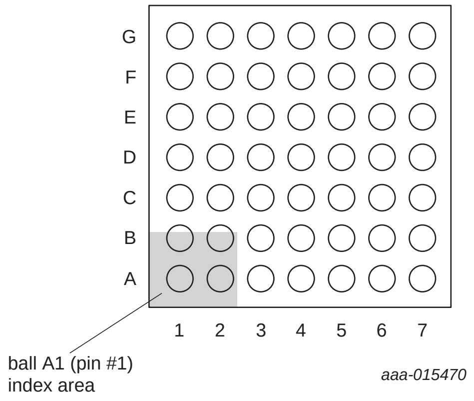


Fig 4. WLCSP49 Pin configuration

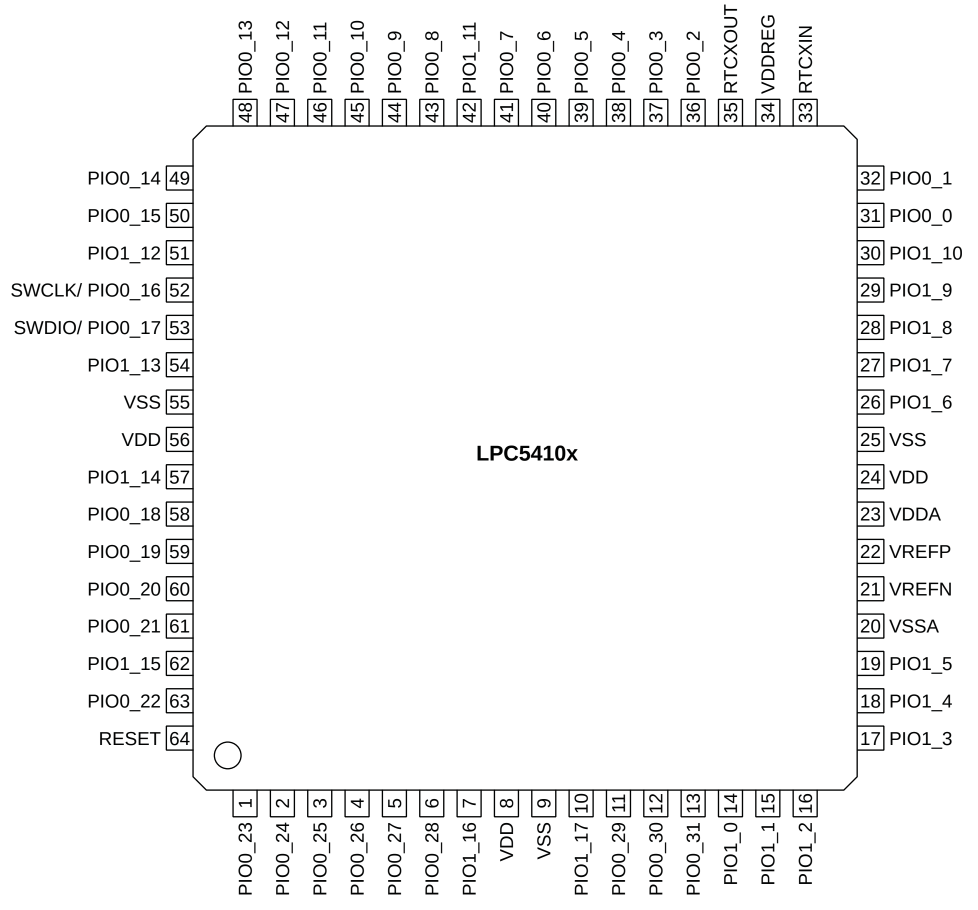


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Fig 5. LQFP64 Pin configuration

6.2 Pin description

On the LPC5410x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 3. Pin description

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO0_0	A6	31	[2]	Z	I/O	**PIO0_0** — General-purpose digital input/output pin.
					I	**U0_RXD** — Receiver input for USART0.
					I/O	**SPI0_SSEL0** — Slave Select 0 for SPI0.
					I	**CT32B0_CAP0** — 32-bit timer0 capture input 0.
					I	**R** — Reserved.
					O	**SCT0_OUT3** — SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	Z	I/O	**PIO0_1** — General-purpose digital input/output pin.
					O	**U0_TXD** — Transmitter output for USART0.
					I/O	**SPI0_SSEL1** — Slave Select 1 for SPI0.
					I	**CT32B0_CAP1** — 32-bit timer0 capture input 1.
					I	**R** — Reserved.
					O	**SCT0_OUT1** — SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	Z	I/O	**PIO0_2** — General-purpose digital input/output pin.
					I	**$\overline{\text{U0\_CTS}}$** — Clear To Send input for USART0.
					I	**R** — Reserved.
					I	**CT32B2_CAP1** — 32-bit timer2 capture input 1.
					I	**R** — Reserved.
PIO0_3	-	37	[2]	Z	I/O	**PIO0_3** — General-purpose digital input/output pin.
					O	**$\overline{\text{U0\_RTS}}$** — Request To Send output for USART0.
					I	**R** — Reserved.
					O	**CT32B1_MAT3** — 32-bit timer1 match output 3.
					I	**R** — Reserved.
PIO0_4	C7	38	[2]	Z	I/O	**PIO0_4** — General-purpose digital input/output pin.
					I/O	**U0_SCLK** — USART0 clock in synchronous USART mode.
					I/O	**SPI0_SSEL2** — Slave Select 2 for SPI0.
					I	**CT32B0_CAP2** — 32-bit timer0 capture input 2.
					I	**R** — Reserved.
PIO0_5	C6	39	[2]	Z	I/O	**PIO0_5** — General-purpose digital input/output pin.
					I	**U1_RXD** — Receiver input for USART1.
					O	**SCT0_OUT6** — SCT0 output 6. PWM output 6.
					O	**CT32B0_MAT0** — 32-bit timer0 match output 0.
					I	**R** — Reserved.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO0_6	D7	40	[2]	Z	I/O	**PIO0_6 —** General-purpose digital input/output pin.
					O	**U1_TXD —** Transmitter output for USART1.
					I	**R —** Reserved.
					O	**CT32B0_MAT1 —** 32-bit timer0 match output 1.
					I	**R —** Reserved.
PIO0_7	D6	41	[2]	Z	I/O	**PIO0_7 —** General-purpose digital input/output pin.
					I/O	**U1_SCLK —** USART1 clock in synchronous USART mode.
					O	**SCT0_OUT0 —** SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT2 —** 32-bit timer0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit timer0 capture input 2.
PIO0_8	D5	43	[2]	Z	I/O	**PIO0_8 —** General-purpose digital input/output pin.
					I	**U2_RXD —** Receiver input for USART2.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT3 —** 32-bit timer0 match output 3.
					I	**R —** Reserved.
PIO0_9	E7	44	[2]	Z	I/O	**PIO0_9 —** General-purpose digital input/output pin.
					O	**U2_TXD —** Transmitter output for USART2.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					I	**CT32B3_CAP0 —** 32-bit timer3 capture input 0.
					I	**R —** Reserved.
					I/O	**SPI0_SSEL0 —** Slave Select 0 for SPI0.
PIO0_10	E6	45	[2]	Z	I/O	**PIO0_10 —** General-purpose digital input/output pin.
					I/O	**U2_SCLK —** USART2 clock in synchronous USART mode.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CT32B3_MAT0 —** 32-bit timer3 match output 0.
					I	**R —** Reserved.
PIO0_11	E5	46	[2]	Z	I/O	**PIO0_11 —** General-purpose digital input/output pin.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**U1_RXD —** Receiver input for USART1.
					O	**CT32B2_MAT1 —** 32-bit timer2 match output 1.
					I	**R —** Reserved.
PIO0_12	F7	47	[2]	Z	I/O	**PIO0_12 —** General-purpose digital input/output pin.
					I/O	**SPI0_MOSI —** Master Out Slave in for SPI0.
					O	**U1_TXD —** Transmitter output for USART1.
					O	**CT32B2_MAT3 —** 32-bit timer2 match output 3.
					I	**R —** Reserved.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO0_13	G7	48	[2]	Z	I/O	**PIO0_13** — General-purpose digital input/output pin.
					I/O	**SPI0_MISO** — Master In Slave Out for SPI0.
					O	**SCT0_OUT4** — SCT0 output 4. PWM output 4.
					O	**CT32B2_MAT0** — 32-bit timer2 match output 0.
					I	**R** — Reserved.
PIO0_14/ TCK	F6	49	[2]	Z	I/O	**PIO0_14** — General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock).
					I/O	**SPI0_SSEL0** — Slave Select 0 for SPI0.
					O	**SCT0_OUT5** — SCT0 output 5. PWM output 5.
					O	**CT32B2_MAT1** — 32-bit timer2 match output 1.
					I	**R** — Reserved.
PIO0_15	G6	50	[2]	Z	I/O	**PIO0_15** — General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out).
					I/O	**SPI0_SSEL1** — Slave Select 1 for SPI0.
					I/O	**SWO** — Serial wire trace output.
					O	**CT32B2_MAT2** — 32-bit timer2 match output 2.
					I	**R** — Reserved.
SWCLK/ PIO0_16	F5	52	[2]	Z	I/O	**PIO0_16** — General-purpose digital input/output pin. After booting, this pin is connected to the SWCLK.
					I/O	**SPI0_SSEL2** — Slave Select 2 for SPI0.
					I	**$\overline{\text{U1\_CTS}}$** — Clear To Send input for USART1.
					O	**CT32B3_MAT1** — 32-bit timer3 match output 1.
					I	**R** — Reserved.
					I/O	**SWCLK** — Serial Wire Clock. JTAG Test Clock. This is the default function after booting.
SWDIO/ PIO0_17	G5	53	[2]	Z	I/O	**PIO0_17** — General-purpose digital input/output pin. After booting, this pin is connected to SWDIO.
					I/O	**SPI0_SSEL3** — Slave Select 3 for SPI0.
					O	**$\overline{\text{U1\_RTS}}$** — Request To Send output for USART1.
					O	**CT32B3_MAT2** — 32-bit timer3 match output 2.
					I	**R** — Reserved.
					I/O	**SWDIO** — Serial Wire Debug I/O. This is the default function after booting.
PIO0_18/ $\overline{\text{TRST}}$	G4	58	[2]	Z	I/O	**PIO0_18** — General-purpose digital input/output pin. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset).
					O	**U3_TXD** — Transmitter output for USART3.
					O	**SCT0_OUT0** — SCT0 output 0. PWM output 0.
					O	**CT32B0_MAT0** — 32-bit timer0 match output 0.
					I	**R** — Reserved.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO0_19/ TDI	G3	59	[2]	Z	I/O	**PIO0_19** — General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In).
					I/O	**U3_SCLK** — USART3 clock in synchronous USART mode.
					O	**SCT0_OUT1** — SCT0 output 1. PWM output 1.
					O	**CT32B0_MAT1** — 32-bit timer0 match output 1.
					I	**R** — Reserved.
PIO0_20	F3	60	[2]	Z	I/O	**PIO0_20** — General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select).
					I	**U3_RXD** — Receiver input for USART3.
					I/O	**U0_SCLK** — USART0 clock in synchronous USART mode.
					I	**CT32B3_CAP0** — 32-bit timer3 capture input 0.
					I	**R** — Reserved.
PIO0_21	E3	61	[2]	Z	I/O	**PIO0_21** — General-purpose digital input/output pin.
					O	**CLKOUT** — Clockout pin.
					O	**U0_TXD** — Transmitter output for USART0.
					O	**CT32B3_MAT0** — 32-bit timer3 match output 0.
					I	**R** — Reserved.
PIO0_22	G2	63	[2]	Z	I/O	**PIO0_22** — General-purpose digital input/output pin.
					I	**CLKIN** — Clock input.
					I	**U0_RXD** — Receiver input for USART0.
					O	**CT32B3_MAT3** — 32-bit timer3 match output 3.
					I	**R** — Reserved.
PIO0_23	F2	1	[3]	Z	I/O	**PIO0_23** — General-purpose digital input/output pin.
					I/O	**I2C0_SCL** — I^{2}C0 clock input/output.
					I	**R** — Reserved.
					I	**CT32B0_CAP0** — 32-bit timer0 capture input 0.
					I	**R** — Reserved.
PIO0_24	F1	2	[3]	Z	I/O	**PIO0_24** — General-purpose digital input/output pin.
					I/O	**I2C0_SDA** — I^{2}C0 data input/output.
					I	**R** — Reserved.
					I	**CT32B0_CAP1** — 32-bit timer0 capture input 1.
					I	**R** — Reserved.
					O	**CT32B0_MAT0** — 32-bit timer0 match output 0.
PIO0_25	E2	3	[3]	Z	I/O	**PIO0_25** — General-purpose digital input/output pin.
					I/O	**I2C1_SCL** — I^{2}C1 clock input/output.
					I	**U1_$\overline{\text{CTS}}$** — Clear To Send input for USART1.
					I	**CT32B0_CAP2** — 32-bit timer0 capture input 2.
					I	**R** — Reserved.
					I	**CT32B1_CAP1** — 32-bit timer1 capture input 1.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO0_26	E1	4	[3]	Z	I/O	**PIO0_26 —** General-purpose digital input/output pin.
					I/O	**I2C1_SDA —** I^{2}C1 data input/output.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit timer0 capture input 3.
					I	**R —** Reserved.
PIO0_27	D2	5	[3]	Z	I/O	**PIO0_27 —** General-purpose digital input/output pin.
					I/O	**I2C2_SCL —** I^{2}C2 clock input/output.
					I	**R —** Reserved.
					I	**CT32B2_CAP0 —** 32-bit timer2 capture input 0.
					I	**R —** Reserved.
PIO0_28	D1	6	[3]	Z	I/O	**PIO0_28 —** General-purpose digital input/output pin.
					I/O	**I2C2_SDA —** I^{2}C2 data input/output.
					I	**R —** Reserved.
					O	**CT32B2_MAT0 —** 32-bit timer2 match output 0.
					I	**R —** Reserved.
PIO0_29/ ADC0_0	D3	11	[4]	Z	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin (default). ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT2 —** SCT0 output 2.
					O	**CT32B0_MAT3 —** 32-bit timer0 match output 3.
					I	**R —** Reserved.
					I	**CT32B0_CAP1 —** 32-bit timer0 capture input 1.
					O	**CT32B0_MAT1 —** 32-bit timer0 match output 1.
PIO0_30/ ADC0_1	C1	12	[4]	Z	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin (default). ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3.
					O	**CT32B0_MAT2 —** 32-bit timer0 match output 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP2 —** 32-bit timer0 capture input 2.
PIO0_31/ ADC0_2	C2	13	[4]	Z	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin (default). ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
					-	**R —** Reserved.
					I	**U2_$\overline{\text{CTS}}$ —** Clear To Send input for USART2.
					I	**CT32B2_CAP2 —** 32-bit timer2 capture input 2.
					I	**R —** Reserved.
					I	**CT32B0_CAP3 —** 32-bit timer0 capture input 3.
					O	**CT32B0_MAT3 —** 32-bit timer0 match output 3.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO1_0/ ADC0_3	C3	14	[4]	Z	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin (default). ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					O	**U2_RTS —** Request To Send output for USART2.
					O	**CT32B3_MAT1 —** 32-bit timer3 match output 1.
					I	**R —** Reserved.
					I	**CT32B0_CAP0 —** 32-bit timer0 capture input 0.
PIO1_1/ ADC0_4	B1	15	[4]	Z	I/O; AI	**PIO1_1/ADC0_4 —** General-purpose digital input/output pin (default). ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SWO —** Serial wire trace output.
					O	**SCT0_OUT4 —** SCT0 output 4.
PIO1_2/ ADC0_5	A1	16	[4]	Z	I/O; AI	**PIO1_2/ADC0_5 —** General-purpose digital input/output pin (default). ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL3 —** Slave Select 3 for SPI1.
					O	**SCT0_OUT5 —** SCT0 output 5.
PIO1_3/ ADC0_6	B2	17	[4]	Z	I/O; AI	**PIO1_3/ADC0_6 —** General-purpose digital input/output pin (default). ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL2 —** Slave Select 2 for SPI1.
					O	**SCT0_OUT6 —** SCT0 output 6.
					I	**R —** Reserved.
					I/O	**SPI0_SCK —** Serial clock for SPI0.
					I	**CT32B0_CAP1 —** 32-bit timer0 capture input 1.
PIO1_4/ ADC0_7	A2	18	[4]	Z	I/O; AI	**PIO1_4/ADC0_7 —** General-purpose digital input/output pin (default). ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL1 —** Slave Select 1 for SPI1.
					O	**SCT0_OUT7 —** SCT0 output 7.
					I	**R —** Reserved.
					I/O	**SPI0_MISO —** Master In Slave Out for SPI0.
					O	**CT32B0_MAT1 —** 32-bit timer0 match output 1.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO1_5/ ADC0_8	B3	19	[4]	Z	I/O; AI	**PIO1_5/ADC0_8 —** General-purpose digital input/output pin (default). ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SSEL0 —** Slave Select 0 for SPI1.
					I	**CT32B1_CAP0 —** 32-bit timer1 capture input 0.
					I	**R —** Reserved.
					O	**CT32B1_MAT3 —** 32-bit timer1 match output 3.
					I	**R —** Reserved.
PIO1_6/ ADC0_9	A5	26	[4]	Z	I/O; AI	**PIO1_6/ADC0_9 —** General-purpose digital input/output pin (default). ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_SCK —** Serial clock for SPI1.
					I	**CT32B1_CAP2 —** 32-bit timer1 capture input 2.
					-	**R —** Reserved.
					O	**CT32B1_MAT2 —** 32-bit timer1 match output 2.
					I	**R —** Reserved.
PIO1_7/ ADC0_10	B5	27	[4]	Z	I/O; AI	**PIO1_7/ADC0_10 —** General-purpose digital input/output pin (default). ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MOSI —** Master Out Slave in for SPI1.
					O	**CT32B1_MAT2 —** 32-bit timer1 match output 2.
					-	**R —** Reserved.
					I	**CT32B1_CAP2 —** 32-bit timer1 capture input 2.
					I	**R —** Reserved.
PIO1_8/ ADC0_11	C5	28	[4]	Z	I/O; AI	**PIO1_8/ADC0_11 —** General-purpose digital input/output pin (default). ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					-	**R —** Reserved.
					I/O	**SPI1_MISO —** Master In Slave Out for SPI1.
					O	**CT32B1_MAT3 —** 32-bit timer1 match output 3.
					I	**R —** Reserved.
					I	**CT32B1_CAP3 —** 32-bit timer1 capture input 3.
					I	**R —** Reserved.
PIO1_9	-	29	[2]	Z	I/O	**PIO1_9 —** General-purpose digital input/output pin.
					I	**R —** Reserved.
					I/O	**SPI0_MOSI —** Master Out Slave In for SPI0.
					I	**CT32B0_CAP2 —** 32-bit timer0 capture input 2.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
PIO1_10	-	30	[2]	Z	I/O	**PIO1_10** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					O	**U1_TXD** — Transmitter output for USART1.
					O	**SCT0_OUT4** — SCT0 output 4.
PIO1_11	-	42	[2]	Z	I/O	**PIO1_11** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					O	**$\overline{\text{U1\_RTS}}$** — Request To Send output for USART1.
					I	**CT32B1_CAP0** — 32-bit timer1 capture input 0.
PIO1_12	-	51	[2]	Z	I/O	**PIO1_12** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					I	**U3_RXD** — Receiver input for USART3.
					O	**CT32B1_MAT0** — 32-bit timer1 match output 0.
					I/O	**SPI1_SCK** — Serial clock for SPI1.
PIO1_13	-	54	[2]	Z	I/O	**PIO1_13** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					O	**U3_TXD** — Transmitter output for USART3.
					O	**CT32B1_MAT1** — 32-bit timer1 match output 1.
					I/O	**SPI1_MOSI** — Master Out Slave In for SPI1.
PIO1_14	-	57	[2]	Z	I/O	**PIO1_14** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					I	**U2_RXD** — Receiver input for USART2.
					O	**SCT0_OUT7** — SCT0 output 7.
					I/O	**SPI1_MISO** — Master In Slave Out for SPI1.
PIO1_15	-	62	[2]	Z	I/O	**PIO1_15** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					O	**SCT0_OUT5** — SCT0 output 5.
					I	**CT32B1_CAP3** — 32-bit timer1 capture input 3.
					I/O	**SPI1_SSEL0** — Slave Select 0 for SPI1.
PIO1_16	-	7	[2]	Z	I/O	**PIO1_16** — General-purpose digital input/output pin.
					I	**R** — Reserved.
					O	**CT32B0_MAT0** — 32-bit timer0 match output 0.
					I	**CT32B0_CAP0** — 32-bit timer0 capture input 0.
					I/O	**SPI1_SSEL1** — Slave Select 1 for SPI1.
PIO1_17	-	10	[2]	Z	I/O	**PIO1_17** — General-purpose digital input/output pin.
$\overline{\text{RESET}}$	G1	64	[5]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. Wakes up the part from Deep power-down mode. Pull-up enabled.
RTCXIN	A7	33				RTC oscillator input.
RTCXOUT	B7	35				RTC oscillator output.

Table 3. Pin description *…continued*

Symbol	WLCSP49	LQFP64		Reset state [1]	Type	Description
VREFP	B4	22		-		ADC positive reference voltage.
VREFN	-	21		-	-	ADC negative reference voltage.
VDDA	A4	23		-		Analog supply voltage 1.62 V to 3.6 V.
VDD	C4; F4	8, 24, 56, 34		-	-	Single digital 1.62 V to 3.6 V power supply.
VSS	D4; E4	9, 25, 55		-	-	Ground.
VSSA	A3	20				Analog ground.

[1] Z = high-impedance; pull-up/pull-down disabled (inputs can float); I = input, O = output, IA = inactive; PD = pull-down enabled, PU = pull-up enabled (weak pull-up resistor pulls up pin to V_{DD}); Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength (see Figure 11).

[3] Specialized I2C pads.

[4] Digital I/O pad with analog functionality.

[5] Reset pad.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4F includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC5410x uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4F processor

The ARM Cortex-M4F is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4F offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 ARM Cortex-M0+ co-processor

The ARM Cortex-M0+ co-processor offers high performance and very low power consumption. This processor uses a 2-stage pipeline von Neumann architecture and a small but powerful instruction set providing high-end processing hardware. The processor includes a single-cycle multiplier, an NVIC with 32 interrupts and a separate system tick timer.

7.5 Memory Protection Unit (MPU)

The Cortex-M4F includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4F

The NVIC is an integral part of the Cortex-M4F. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M4F includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the IRC or the Cortex-M4F core clock.

7.9 On-chip static RAM

The LPC5410x support 104 KB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC5410x supports 512 KB of on-chip flash memory.

7.11 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming.
- Power control API for configuring power consumption and PLL settings.

7.12 Memory mapping

The LPC5410x incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals.Each peripheral is allocated 16 kB of space simplifying the address decoding. The registers incorporated into the CPU, such as NVIC, SysTick, and sleep mode control, are located on the private peripheral bus.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.

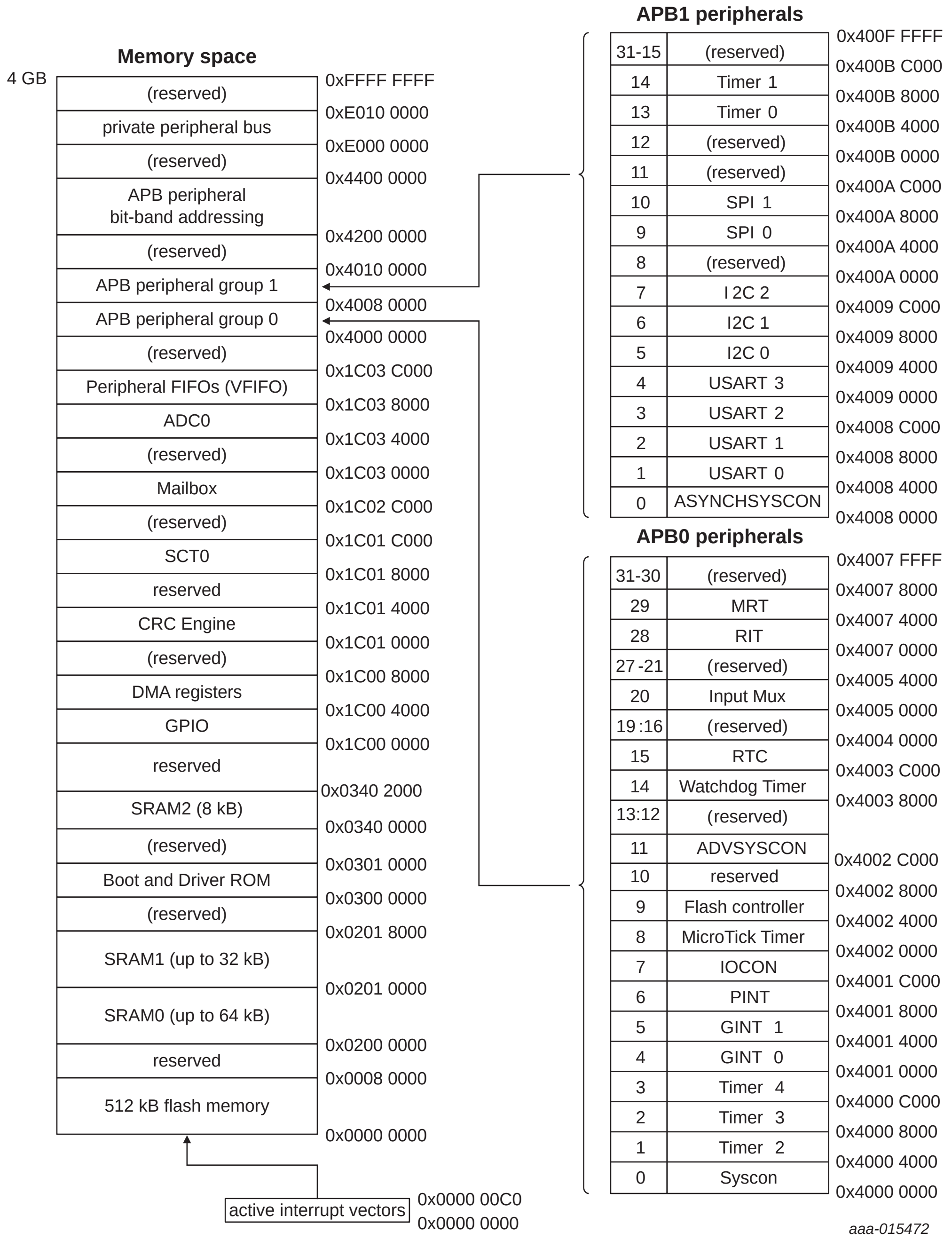


Fig 6. LPC5410x Memory mapping

7.13 General Purpose I/O (GPIO)

The LPC5410x provides two GPIO ports with a total of 50 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 3 for the default state on reset.

7.13.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge- or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.14 AHB peripherals

7.14.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.14.1.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.15 Digital serial peripherals

7.15.1 USART

7.15.1.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.15.2 SPI serial I/O controller

7.15.2.1 Features

- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.

- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Four Slave Select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in slave mode allows wake-up from Deep-sleep and Power-down modes on any enabled interrupt.

7.16 I2C-bus interface

The I^{2}C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.16.1 Features

- All I2Cs support standard, fast mode, and Fast-mode Plus with data rates of up to 1 Mbit/s.
- All I2Cs support high-speed slave mode with data rates of up to 3.4 Mbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^{2}C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^{2}C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Activity on the I2C in slave mode allows wake-up from Deep-sleep and Power-down modes on any enabled interrupt.

7.17 Counter/timers

7.17.1 General-purpose 32-bit timers/external event counter

The LPC5410x includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.17.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.

- Up to three 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to two external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM mode using up to two match channels for PWM output.

7.17.2 State Configurable Timer/PWM (SCTimer/PWM) subsystem

The SCTimer/PWM (SCT0) allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCT, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.17.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).

- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCT states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:
  - 6 inputs
  - up to 8 outputs
  - 13 match/capture registers
  - 13 events
  - 13 states
- PWM capabilities including dead time and emergency abort functions

7.17.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.17.3.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the WDOSC as the clock source.

7.17.4 RTC timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32 kHz clock input to create a 1 Hz or 1 kHz clock.

7.17.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.17.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat and one-shot interrupt modes.

7.18 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 4.8 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCT, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCT.

7.19 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 4.8 MHz. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger

7.20 System control

7.20.1 Clock sources

The LPC5410x supports one external and two internal clock sources:

- The Internal RC (IRC).
- Watchdog oscillator (WDOSC).
- External clock source from the digital I/O pin CLKIN.

7.20.1.1 Internal RC oscillator (IRC)

The IRC can be used as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up or any chip reset, the LPC5410x uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The nominal output frequency is 500 kHz.

7.20.1.3 Clock input

An external square-wave clock source can be supplied on the digital I/O pin CLKIN.

7.20.2 System PLL

The system PLL accepts an input clock frequency in the range of 32 kHz to 12 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.20.3 Clock Generation

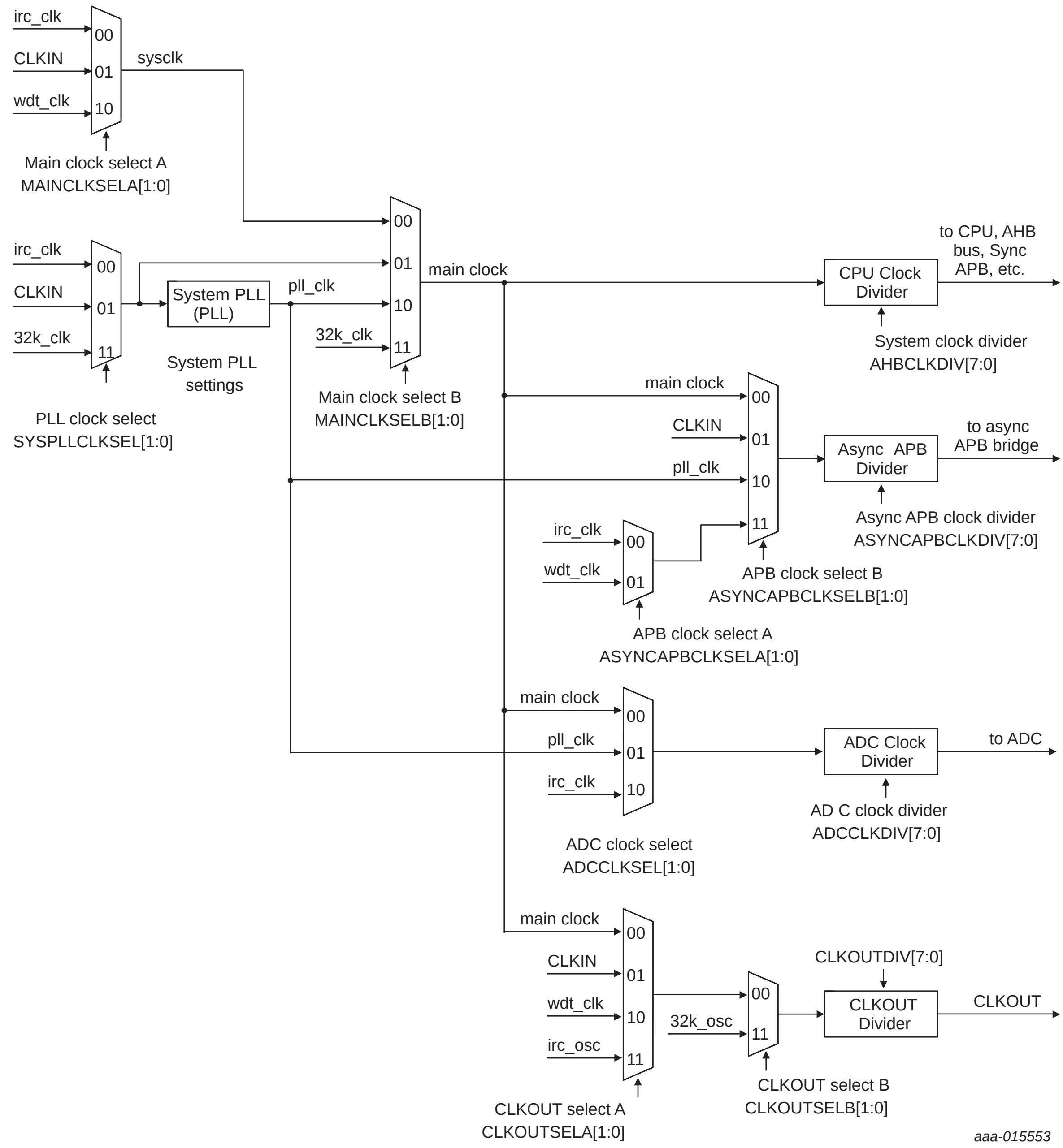


Fig 7. LPC5410x clock generation

7.20.4 Power control

The LPC5410x supports four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down modes.

7.20.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped along with any unused peripherals. Waking up from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals.

7.20.4.2 Deep-sleep mode

In Deep-sleep mode, all peripheral clocks and all clock sources are off with the option of keeping the IRC, the 32 kHz clock, and the WDOSC running. In addition, all analog blocks are shut down and the flash is put in stand-by mode. In Deep-sleep mode, the application can keep some of the internal clocks and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC5410x can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer interrupt, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals. For wake-up from Deep-sleep mode, the SPI and I2C peripherals must be configured in slave mode.

Any interrupt used for waking up from Deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

In Deep-sleep mode, the state of the LPC5410x is retained. Deep-sleep mode allows for very low quiescent power and fast wake-up options.

7.20.4.3 Power-down mode

In Power-down mode, all peripheral clocks and all clock sources are off with the option of keeping the 32 kHz clock, and the WDOSC running. In addition, all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC5410x can wake up from Power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, RTC alarm, Micro-tick, a watchdog timer interrupt, or an interrupt from the USART (in 32 kHz mode or synchronous slave mode), the SPI, or any of the I2C peripherals.

In power-down mode, the state of the LPC5410x is retained. Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.20.4.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the RTC power domain, the $\overline{\text{RESET}}$ pin, and the Micro-tick timer if enabled. The LPC5410x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin, the RTC alarm, or, without an external signal, by using the time-out of the Micro-tick timer.

7.20.5 Brownout detection

The LPC5410x includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold level can be selected to cause chip reset.

7.20.6 Safety

The LPC5410x includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.21 Code security (Code Read Protection - CRP)

This feature of the LPC5410x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the LPC5410x LOW on reset. This pin is called the ISP entry pin.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user’s application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.22 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4F and ARM Cortex-M0+. Serial wire debug and trace functions are supported. The ARM Cortex-M4F is configured to support up to eight breakpoints and four watch points. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points. In addition, a boundary scan mode is provided.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	on pin VDD	[2]	–0.5	+4.6	V
V_{DDA}	analog supply voltage	on pin VDDA		–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP	-	–0.5	+4.6	V
V_I	input voltage	only valid when the $V_{DD} > 1.8$ V; 5 V tolerant I/O pins	[6][7]	–0.5	5.0	V
V_I	input voltage	on I2C open-drain pins	[5]	–0.5	+5.0	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[8][9]	–0.5	V_{DD}	V
I_{DD}	supply current	per supply pin	[3]	-	100	mA
I_{SS}	ground current	per ground pin	[3]	-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
$V_{i(rtcx)}$	32 kHz oscillator input voltage		[2]	–0.5	+4.6	V
T_{stg}	storage temperature		[10]	–65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 11.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 11) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \tag{1}$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 5. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP64 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	58 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		18 ± 15 %	°C/W
WLCSP49 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		0.3 ± 15 %	°C/W

10. Static characteristics

10.1 General operating conditions

Table 6. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	100	MHz
V_{DD}	supply voltage (core and external rail)			1.62	3.3	3.6	V
V_{DDA}	analog supply voltage			1.62	3.3	3.6	V
RTC oscillator pins							
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN		−0.5	-	+3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT		−0.5	-	+3.6	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Excluding bonding pad capacitance. Based on simulation, not tested in production.

10.2 CoreMark score

Table 7. CoreMark score

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4F in active mode; ARM Cortex-M0+ in sleep mode				
CoreMark score	CoreMark code executed from SRAM; CCLK = 12 MHz	[1][3][4]	2.5	(Iterations/s) / MHz
	CCLK = 84 MHz	[2][3][4]	2.6	(Iterations/s) / MHz
	CCLK = 96 MHz	[2][3][4]	2.6	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz	[1][3][4]	2.5	(Iterations/s) / MHz
	CCLK = 84 MHz	[2][3][4]	2.2	(Iterations/s) / MHz
	CCLK = 96 MHz	[2][3][4]	2.2	(Iterations/s) / MHz

[1] Clock source 12 MHz IRC. PLL disabled.

[2] Clock source 12 MHz IRC. PLL enabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision v.5.1.0, optimization level 3, optimized for time on.

10.3 Power consumption

Power measurements in Active, Sleep, Deep-sleep, and Power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 8. Static characteristics: Power consumption in active and sleep modes
T_{amb} = –40 °C to +105 °C, unless otherwise specified.1.62 V <= V_{DD} <= 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4F in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM;					
		CCLK = 12 MHz	[2][4]	-	1.4	-	mA
		CCLK = 84 MHz	[3][4]	-	4.6	-	mA
		CCLK = 96 MHz	[3][4]	-	5.2	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz	[2][4]	-	1.6	-	mA
		CCLK = 84 MHz	[3][4]	-	5.4	-	mA
		CCLK = 96 MHz	[3][4]	-	6.0	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash;					
		CCLK = 12 MHz	[2][4][5]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][5]	-	6.2	-	mA
		CCLK = 96 MHz	[3][4][5]	-	7.2	-	mA

Table 8. Static characteristics: Power consumption in active and sleep modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V <= V_{DD} <= 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M4F in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAM;					
		CCLK = 12 MHz	[2][4][6]	-	1.5	-	mA
		CCLK = 84 MHz	[3][4][6]	-	7.9	-	mA
		CCLK = 96 MHz	[3][4][6]	-	9.2	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from SRAM;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz	[2][4][6]	-	2.1	-	mA
		CCLK = 84 MHz	[3][4][6]	-	9.0	-	mA
		CCLK = 96 MHz	[3][4][6]	-	10.4	-	mA
I_{DD}	supply current	Calculating Fibonacci numbers executed from flash;					
		CCLK = 12 MHz	[2][4][5]	-	1.7	-	mA
		CCLK = 84 MHz	[3][4][5]	-	8.0	-	mA
		CCLK = 96 MHz	[3][4][5]	-	9.4	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source 12 MHz IRC. PLL disabled.

[3] Clock source 12 MHz IRC. PLL enabled.

[4] Characterized through bench measurements using typical samples.

[5] Compiler settings: Keil µVision v.5.10, optimization level 0, optimized for time off.

[6] Compiler settings: Keil µVision v.5.12, optimization level 0, optimized for time off.

Table 9. Static characteristics: Power consumption in deep-sleep, power-down, and deep power-down modes

T_{amb} = –40 °C to +105 °C, unless otherwise specified.V_{DD} = 3.3 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	deep-sleep mode; all SRAM on	[2]	-	317	-	µA
		power-down mode; first 8 KB in SRAM0 powered	[2]	-	3.5	-	µA
		SRAM0 (64 KB) powered		-	5	-	µA
		SRAM0 (64 KB), SRAM1 (32 KB) powered		-	6	-	µA
		SRAM0 (64 KB), SRAM1 (32 KB), SRAM2 (8 KB) powered		-	6.2	-	µA
		deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled)	[2]	-	135	-	nA
		RTC oscillator running with external crystal		-	280	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), nominal supply voltages.

[2] Characterized through bench measurements using typical samples.

Table 10. Static characteristics: Power consumption in deep-sleep, power-down, and deep power-down modes

T_{amb} = –40 °C to +105 °C, unless otherwise specified.V_{DD} = 1.62 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	deep-sleep mode; all SRAM on	[2]	-	238	-	µA
		power-down mode; first 8 KB in SRAM0 powered	[2]	-	3	-	µA
		SRAM0 (64 KB) powered		-	4	-	µA
		SRAM0 (64 KB), SRAM1 (32 KB) powered		-	5	-	µA
		SRAM0 (64 KB), SRAM1 (32 KB), SRAM2 (8 KB) powered		-	5.3	-	µA
		deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled)	[2]	-	84	-	nA
		RTC oscillator running with external crystal		-	114	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), nominal supply voltages.

[2] Characterized through bench measurements using typical samples.

10.4 Pin characteristics

Table 11. Static characteristics: pin characteristics

T_{amb} = 25 °C, 1.62 V <= V_{DD} <= 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × (V_{DD})	-	5.0	V
V_{IL}	LOW-level input voltage			–0.5	-	0.3 × (V_{DD})	V
V_{hys}	hysteresis voltage			0.05 × (V_{DD})	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	-	10[2]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	-	10[2]	nA
V_I	input voltage	pin configured to provide a digital function;	[5]				
		V_{DD} > 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.62 V <= V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V <= V_{DD} <= 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.62 V <= V_{DD} < 2.7 V		–0.5	-	+0.4	V
		2.7 V <= V_{DD} <= 3.6 V		–0.5	-	+0.8	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	-	10[2]	nA
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 1.62 V <= V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = 6 mA; 2.7 V <= V_{DD} <= 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.62 V <= V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V <= V_{DD} <= 3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.62 V <= V_{DD} < 2.7 V		4	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V <= V_{DD} <= 3.6 V		6	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.62 V <= V_{DD} < 2.7 V		4	-	-	mA
		V_{OL} = 0.4 V; 2.7 V <= V_{DD} <= 3.6 V		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground; 2.7 V <= V_{DD} <= 3.6 V	[6]	-	-	87	mA
		1.62 V <= V_{DD} <= 1.98 V		-	-	35	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to V_{DD}; 2.7 V <= V_{DD} <= 3.6 V	[6]	-	-	77	mA
		1.62 V <= V_{DD} <= 1.98 V		-	-	30	mA

Table 11. Static characteristics: pin characteristics *...continued*

T_{amb} = 25 °C, 1.62 V <= V_{DD} <= 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Open-drain I²C pins							
V_{IH}	HIGH-level input voltage			0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[7]	-	4.5	-	µA
		V_I = 5 V		-	-	10	µA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4 V; pin configured for Fast-mode Plus		20.0	-	-	mA
Pin capacitance							
C_{io}	input/output capacitance	I²C-bus pins	[8]	-	-	6.0	pF
		pins with digital functions only	[8]	-	-	2.0	pF

[1] Typical ratings are not guaranteed.

[2] Based on characterization. Not tested in production.

[3] Not characterized on samples or in production.

[4] Characterized on the bench for typical samples.

[5] With respect to ground.

[6] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[7] To V_{SS}.

[8] Excluding bonding capacitance. Simulated values.

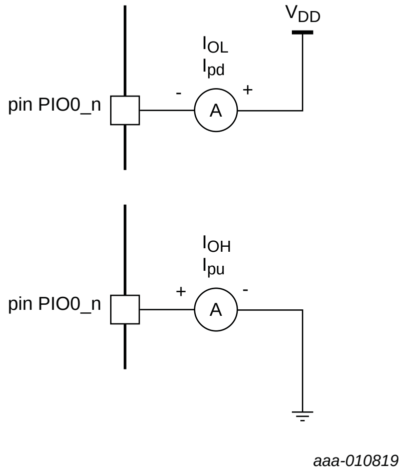


Fig 8. Pin input/output current measurement

11. Dynamic characteristics

11.1 Flash memory

Table 12. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.62 V to 3.6 V for read operations; V_{DD} = 2.7V to 3.6V for erase/program operations.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	sector erase/program	[1]	10000	-	-	cycles
		page erase/program; page in large sector		1000	-	-	cycles
		page erase/program; page in small sector		10000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[2]	-	1	-	ms

[1] Number of erase/program cycles.

[2] Programming times are given for writing 512 bytes from RAM to the flash. Data must be written to the flash in blocks of 512 bytes. T_{amb} = 25 °C.

11.2 I/O pins

Table 13. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C; 1.62 V ≤ $V_{DD(IO)}$ ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V <= V_{DD} <= 3.6 V		1.0	-	2.5	ns
		1.62 V <= V_{DD} <= 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V <= V_{DD} <= 3.6 V		0.9	-	2.5	ns
		1.62 V <= V_{DD} <= 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V <= V_{DD} <= 3.6 V		1.9	-	4.3	ns
		1.62 V <= V_{DD} <= 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V <= V_{DD} <= 3.6 V		1.9	-	4.0	ns
		1.62 V <= V_{DD} <= 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC54xxx user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

11.3 Wake-up process

Table 14. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 ℃; using IRC as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2][3]	-	1.6	-	µs
		from Deep-sleep mode with full SRAM retention:	[2]				
		to code executing in flash		-	18	-	µs
		to code executing in SRAM	[2]	-		-	µs
		from Power-down mode	[2]				
		to code executing in flash		-	70	-	µs
		to code executing in SRAM	[2]		18	-	µs
		from deep power-down,mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4]	-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] IRC enabled, all peripherals off.

[4] RTC disabled. Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

11.4 IRC

Table 15. Dynamic characteristic: IRC oscillator

T_{amb} = 25 ℃; 1.62 V $\leq V_{DD} \leq$ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-		11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 RTC oscillator

See Section 13.3 for connecting the RTC oscillator to an external clock source.

Table 16. Dynamic characteristic: RTC oscillator

1.62 $\leq V_{DD} \leq$ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 Watchdog oscillator

Table 17. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency		[2]	-	500	-	kHz
D_{clkout}	clkout duty cycle			48	-	52	%
$J_{PP\text{-}CC}$	peak-peak period jitter		[3][4]	-	1	20	ns
t_{start}	start-up time		[4]	-	4	-	μs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

11.7 I^{2}C-bus

Table 18. Dynamic characteristic: I^{2}C-bus pins[1]

T_{amb} = –40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	μs
			Fast-mode	0.6	-	μs
			Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	μs
			Fast-mode	0	-	μs
			Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I^{2}C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

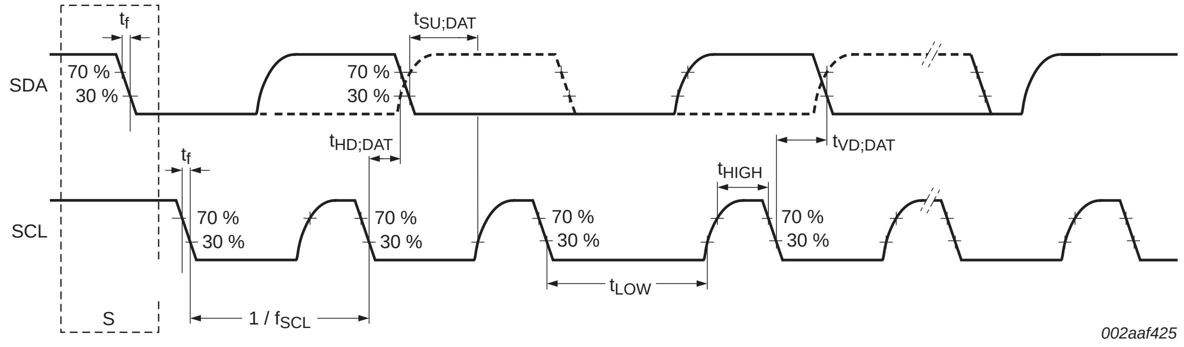


Fig 9. I^{2}C-bus pins clock timing

12. Analog characteristics

12.1 12-bit ADC characteristics

Table 19. 12-bit ADC static characteristics

T_{amb} = 25 °C; V_{DD} = 3.3 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}. ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions	Min	Typ [2]	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
$f_{clk(ADC)}$	ADC clock frequency				72	MHz
f_s	sampling frequency		-	-	4.8	Msamples/s
E_D	differential linearity error	[1][3]	-	± 0.8		LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	± 1.4		LSB
E_O	offset error	calibration enabled [1][5]	-	± 1.3		LSB
$V_{err(FS)}$	full-scale error voltage	[1][6]	-	± 0.06		%

[1] Based on characterization; not tested in production.

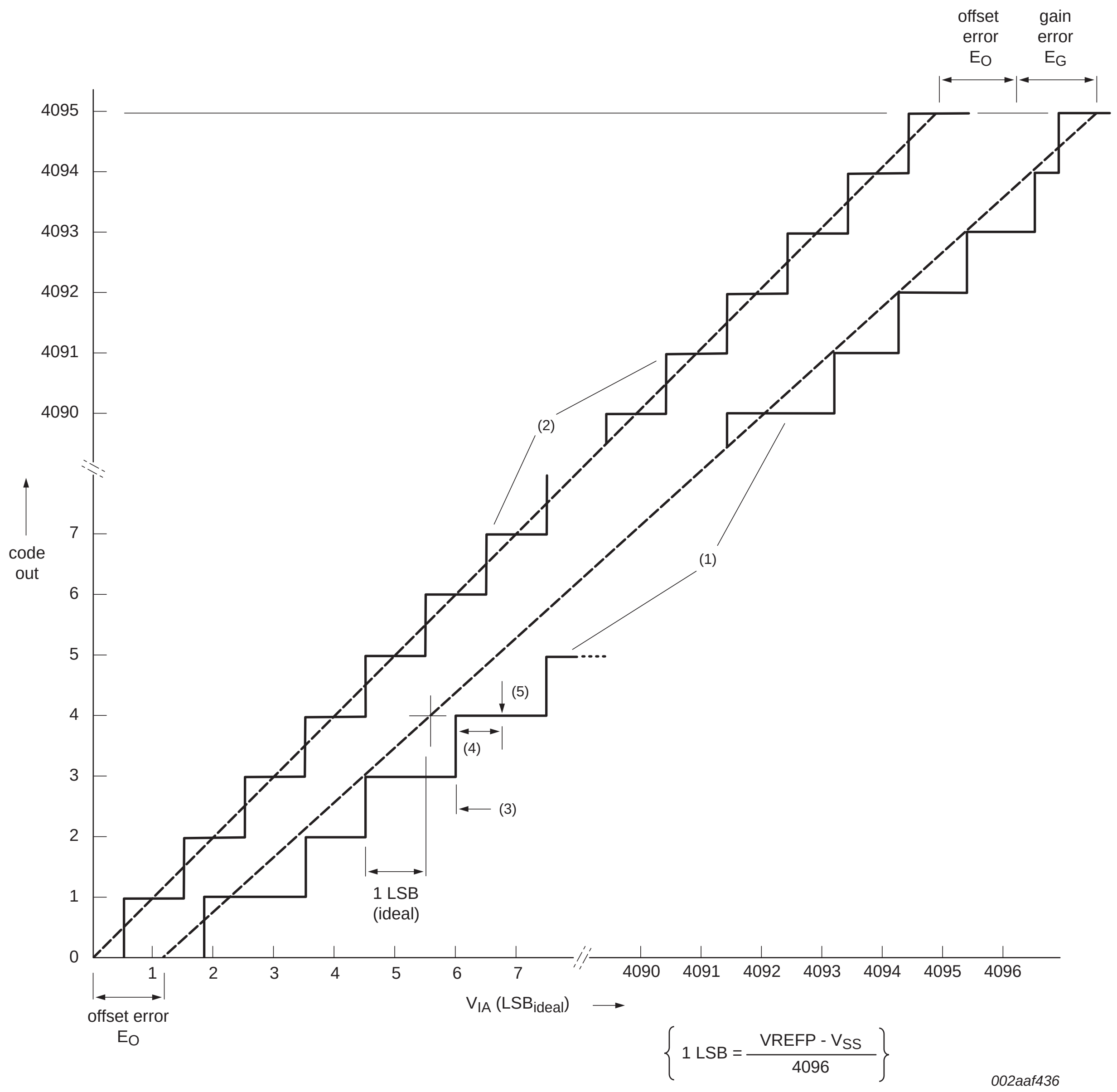
[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 10.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 10.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 10.

[6] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 10.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 10. 12-bit ADC characteristics

Table 20. ADC sampling times[1]

-40 °C <= T_{amb} <= 85 °C; 1.62 V <= V_{DDA} <= 3.6 V; 1.62 V <= V_{DD} <= 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		47	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		38	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		30	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		22	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		74	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		105	-	-	ns

Table 20. ADC sampling times[1] *…continued*

-40 °C <= T_{amb} <= 85 °C; 1.62 V <= V_{DDA} <= 3.6 V; 1.62 V <= V_{DD} <= 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		61	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		48	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		36	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

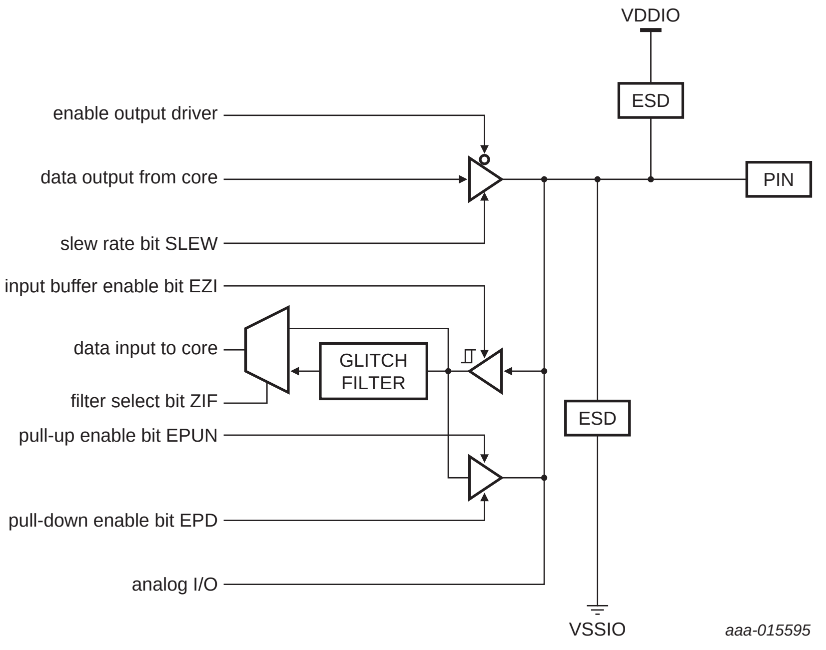
13. Application information

13.1 Standard I/O pin configuration

Figure 11 shows the possible pin modes for standard I/O pins:

- Digital output driver: enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Z mode; High impedance (no cross-bar currents for floating inputs).

The default configuration for standard I/O pins is Z mode. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.



The glitch filter rejects pulses of typical 12 ns width.

Fig 11. Standard I/O and $\overline{\text{RESET}}$ pin configuration

13.2 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 11 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 11, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 11 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2}$ = 20 (typical) ± 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

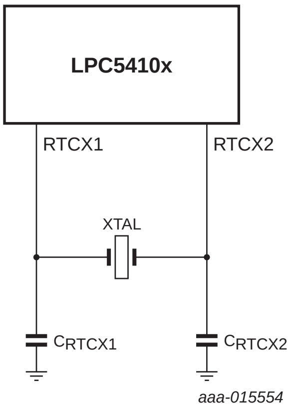
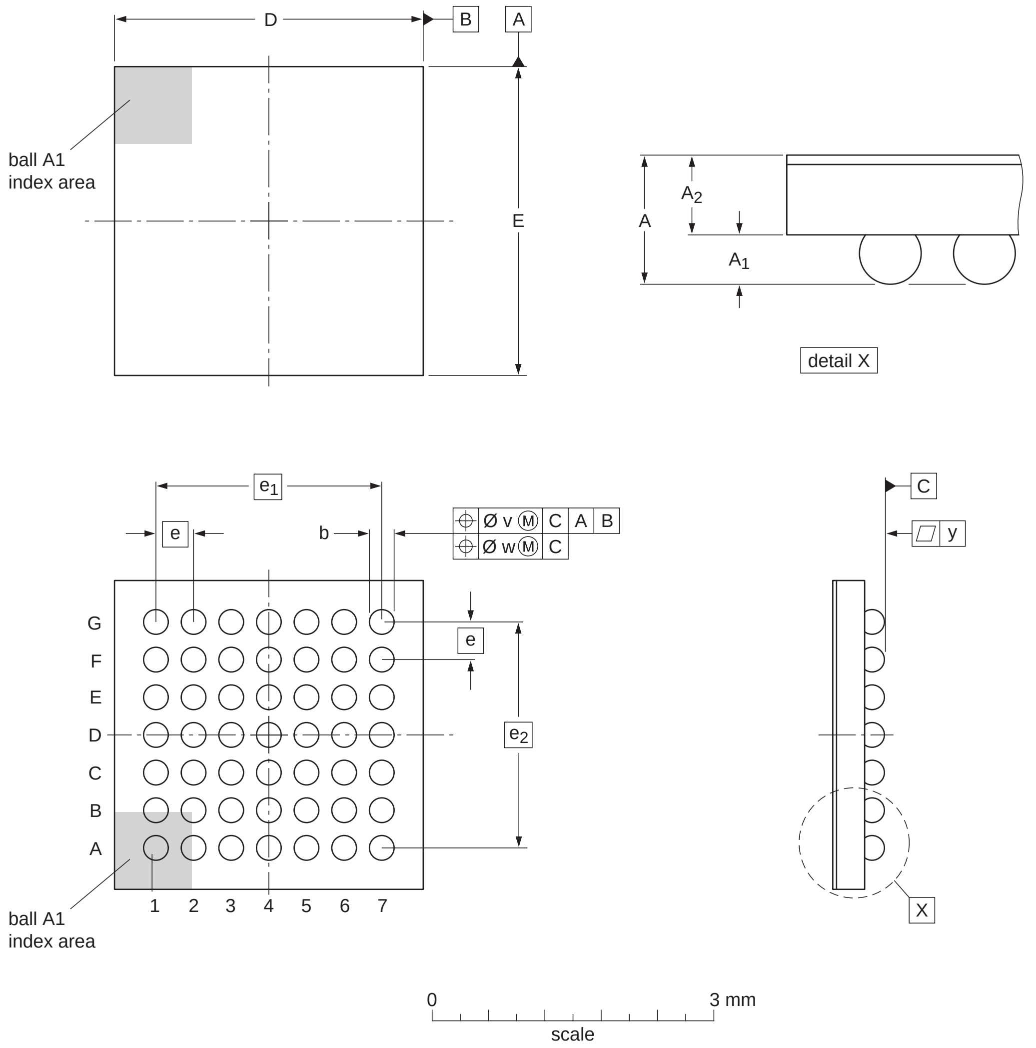


Fig 12. RTC 32 kHz oscillator circuit

14. Package outline

WLCSP49: wafer level chip-scale package; 49 bumps; 3.29 x 3.29 x 0.54 mm (backside coating included) **LPC5410**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.58	0.23	0.37	0.29	3.318	3.318						
mm	nom	0.54	0.20	0.34	0.26	3.288	3.288	0.4	2.4	2.4	0.05	0.015	0.03
	min	0.50	0.17	0.31	0.23	3.258	3.258						

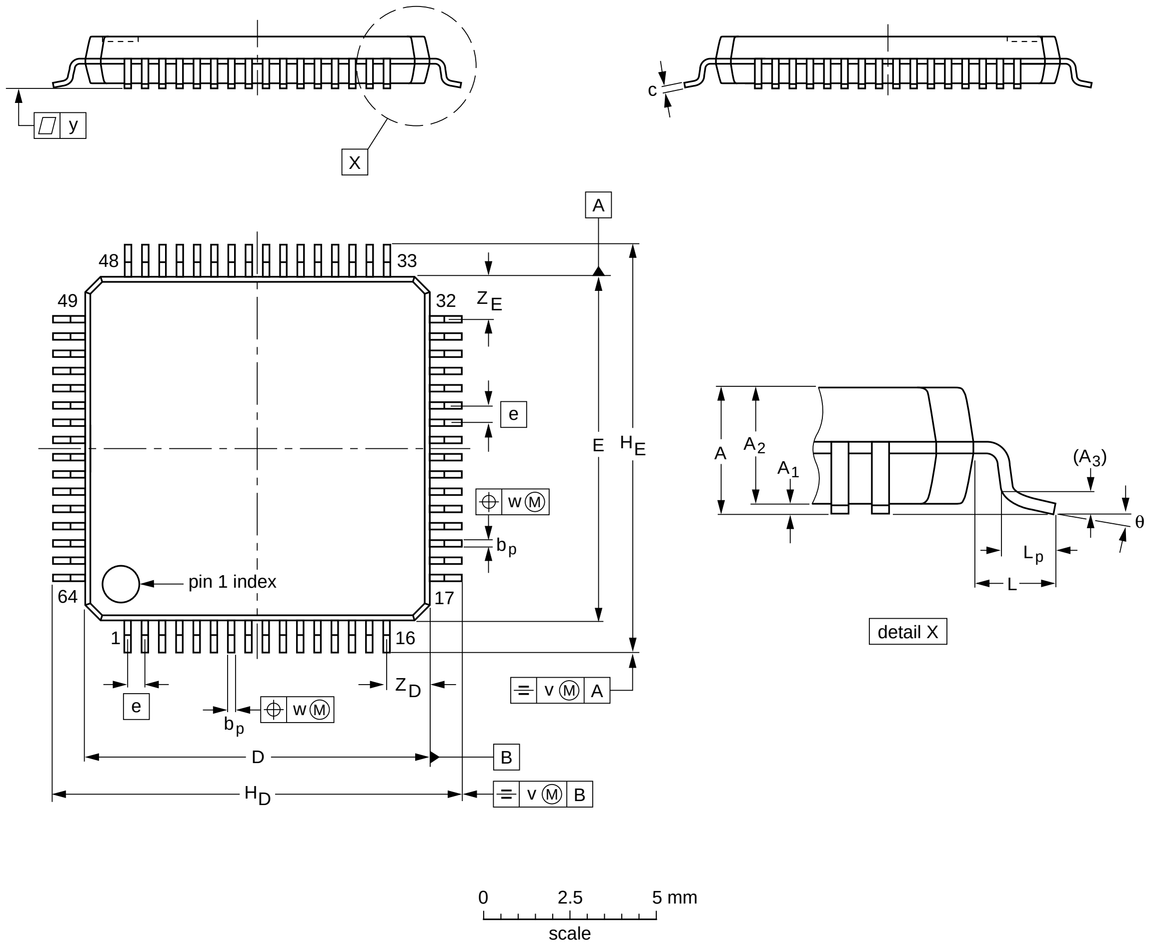
Note
Backside coating 40 µm

wlcsp49_lpc5410_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
LPC5410		- - -				~~13-09-16~~ 14-11-03

Fig 13. WLCSP49 Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

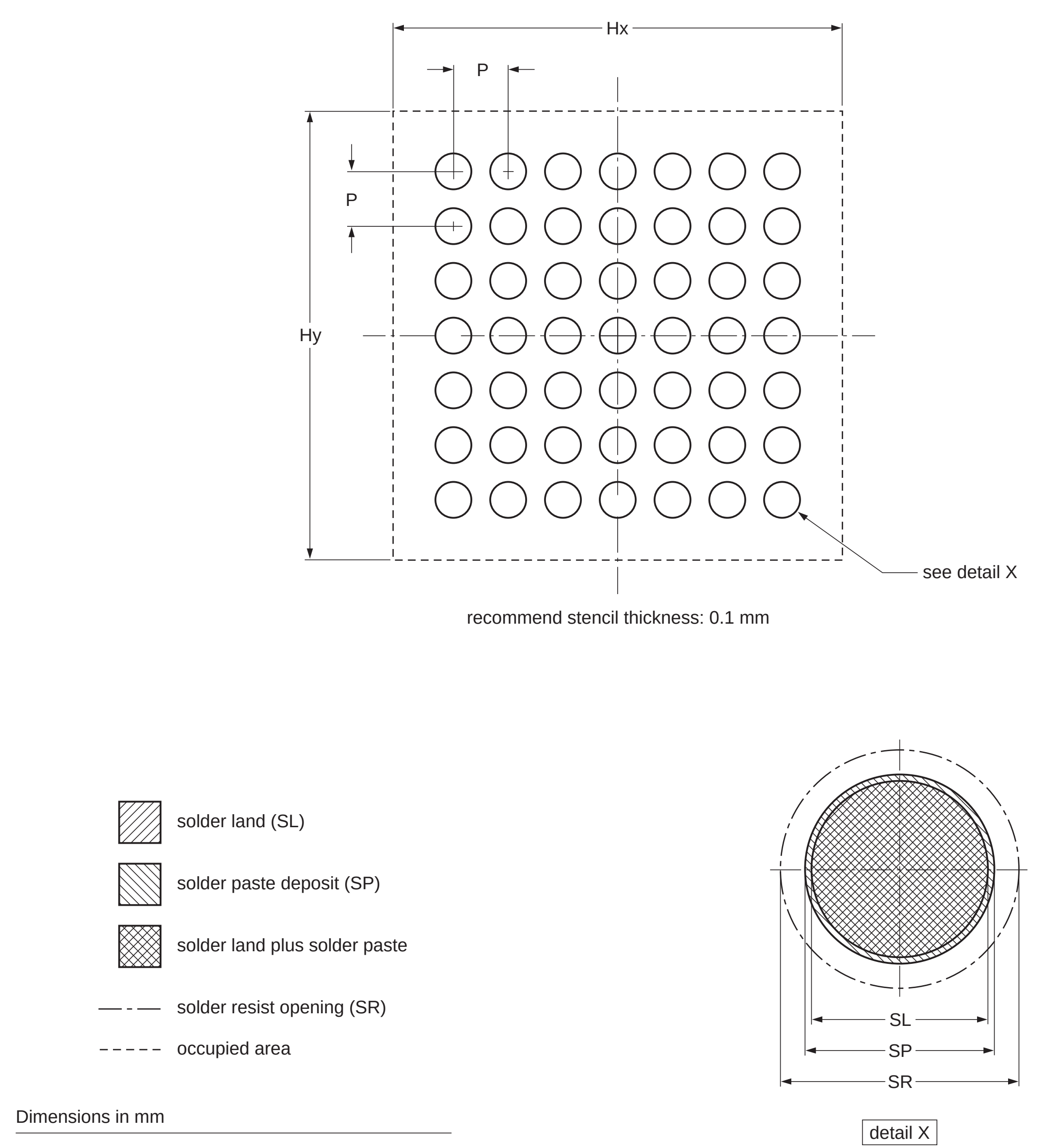
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 14. LQFP64 Package outline

15. Soldering

Footprint information for reflow soldering of WLCSP49 package **LPC5410_NSMD**



Dimensions in mm

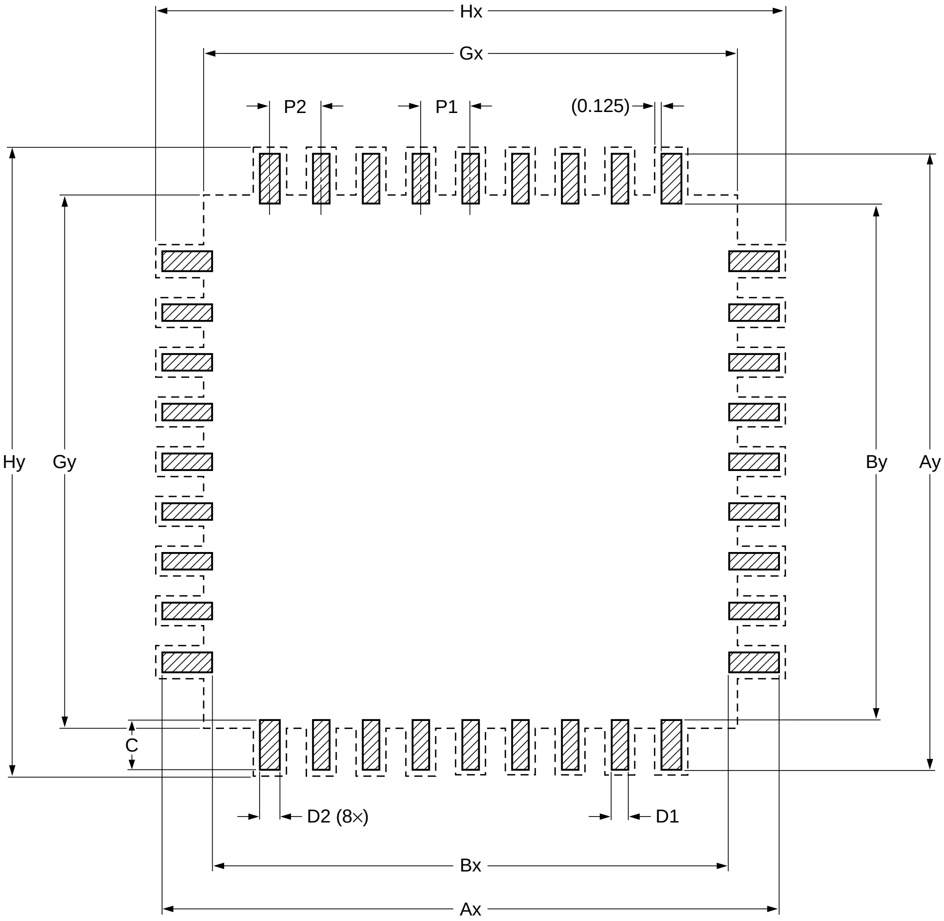
P	SL	SP	SR	Hx	Hy
0.4	0.24	0.27	0.31	3.5	3.5

Issue date ~~14-04-08~~
14-11-05

wlcsp49_lpc5410_fr

Fig 15. WLCSP49 Soldering footprint

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

▨ solder land

- - - - occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 16. LQFP64 Soldering footprint

16. Abbreviations

Table 21. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
LSB	Least Significant Bit
MCU	MicroController Unit
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC5410x v1.1	20141118	Product data sheet	-	LPC5410x v1.0
Modification:	• Minor editorial update in Section 1.			
LPC5410x v1.0	20141106	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	**Product status**[3]	**Definition**
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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