

# ESD237-B1-W0201

## Protection devices

TVS (Transient Voltage Suppressor)

Bi-directional, 8 V, 7 pF, 0201, RoHS and Halogen Free compliant

Quality Requirement Category: Standard

## Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 16$  kV (air),  $\pm 16$  kV (contact discharge)
  - IEC61000-4-4 (EFT):  $\pm 2$  kV /  $\pm 40$  A (5/50 ns)
  - IEC61000-4-5 (surge):  $\pm 3$  A (8/20  $\mu$ s)
- Bi-directional working voltage up to:  $V_{RWM} = \pm 8$  V
- Line capacitance:  $C_L = 7$  pF (typical) at  $f = 1$  MHz
- Clamping voltage:  $V_{CL} = 13$  V (typical) at  $I_{TLP} = 16$  A with  $R_{DYN} = 0.21 \Omega$  (typical)
- Very low reverse current:  $I_R < 1$  nA (typical)
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 0201 and low profile 0.58 mm x 0.28 mm x 0.15 mm
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package

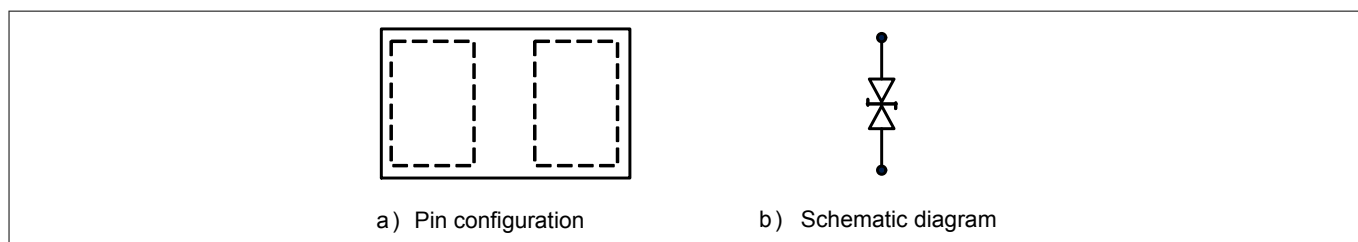


Guidelines for optimized PCB design and assembly process are available in [\[2\]](#).

## Application examples

- ESD Protection of highly susceptible IC/ASICs serving a wider usable voltage headroom
- Dedicated solution for audio PA lines to preserve uncompressed clean audio

## Device information



**Figure 1** Pin configuration and schematic diagram

**Table 1** Part information

| Type            | Package | Configuration          | Marking code     |
|-----------------|---------|------------------------|------------------|
| ESD237-B1-W0201 | WLL-2-1 | 1 line, bi-directional | YY <sup>1)</sup> |

<sup>1</sup> The device does not have any marking on the device top. The marking code is on the pads.

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## Maximum ratings

### 1 Maximum ratings

Note:  $T_A = 25\text{ °C}$ , unless otherwise specified <sup>1)</sup>

Table 2 Maximum Rating

| Parameter                        | Symbol              | Values     | Unit |
|----------------------------------|---------------------|------------|------|
| Reverse working voltage          | $V_{RWM}$           | $\pm 8$    | V    |
| ESD discharge <sup>2)</sup>      | $V_{ESD}$ (contact) | $\pm 16$   | kV   |
|                                  | $V_{ESD}$ (air)     | $\pm 16$   |      |
| Peak pulse power <sup>3)</sup>   | $P_{PK}$            | 42         | W    |
| Peak pulse current <sup>3)</sup> | $I_{PP}$            | $\pm 3$    | A    |
| Operating temperature range      | $T_{OP}$            | -55 to 85  | °C   |
| Storage temperature              | $T_{stg}$           | -55 to 150 | °C   |

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component.

<sup>1</sup> Device is electrically symmetrical

<sup>2</sup>  $V_{ESD}$  according to IEC61000-4-2 (R = 330  $\Omega$ , C = 150 pF discharge network)

<sup>3</sup> Stress pulse: 8/20 $\mu$ s current waveform according to IEC61000-4-5

Electrical characteristics

## 2 Electrical characteristics

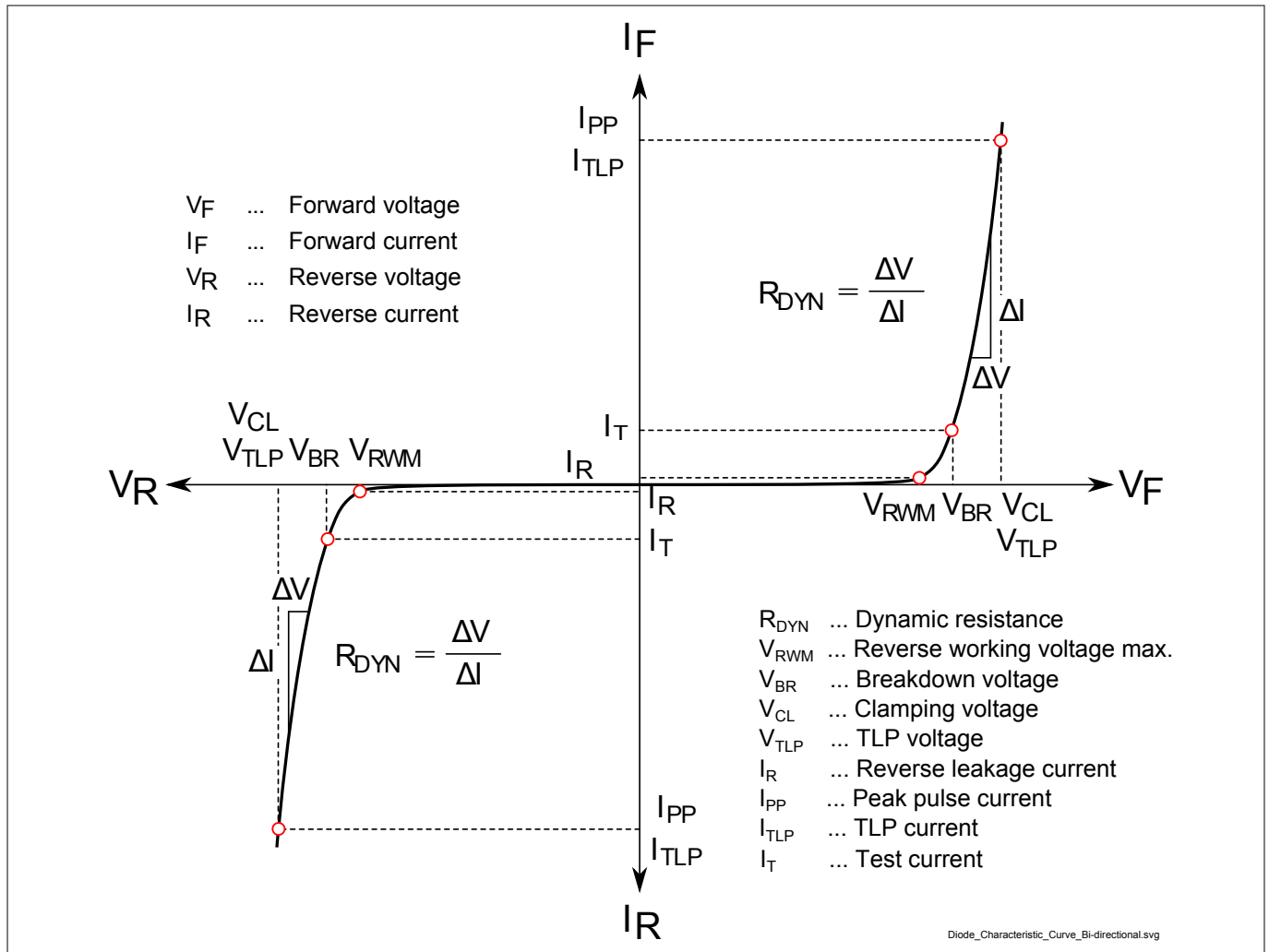


Figure 2 Definitions of electrical characteristics

## Electrical characteristics

**Table 3 DC characteristics ( $T_A = 25\text{ °C}$ , unless otherwise specified) <sup>1)</sup>**

| Parameter         | Symbol   | Values |      |      | Unit | Note or test condition |
|-------------------|----------|--------|------|------|------|------------------------|
|                   |          | Min.   | Typ. | Max. |      |                        |
| Breakdown voltage | $V_{BR}$ | 9      | 10.5 | 12   | V    | $I_T = 1\text{ mA}$    |
| Reverse current   | $I_R$    | –      | –    | 100  | nA   | $V_R = 8\text{ V}$     |

**Table 4 AC characteristics ( $T_A = 25\text{ °C}$ , unless otherwise specified)**

| Parameter        | Symbol | Values |      |      | Unit | Note or test condition                  |
|------------------|--------|--------|------|------|------|-----------------------------------------|
|                  |        | Min.   | Typ. | Max. |      |                                         |
| Line capacitance | $C_L$  | –      | 7    | –    | pF   | $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ |
|                  |        | –      | 7    | –    |      | $V_R = 0\text{ V}$ , $f = 1\text{ GHz}$ |

**Table 5 ESD and surge characteristics ( $T_A = 25\text{ °C}$ , unless otherwise specified) <sup>1)</sup>**

| Parameter                        | Symbol           | Values |      |      | Unit | Note or test condition                           |  |
|----------------------------------|------------------|--------|------|------|------|--------------------------------------------------|--|
|                                  |                  | Min.   | Typ. | Max. |      |                                                  |  |
| Clamping voltage <sup>2)</sup>   | V <sub>CL</sub>  | –      | 13   | –    | V    | I <sub>TLP</sub> = 16 A, t <sub>p</sub> = 100 ns |  |
|                                  |                  | –      | 17   | –    |      | I <sub>TLP</sub> = 30 A, t <sub>p</sub> = 100 ns |  |
| Clamping voltage <sup>3)</sup>   |                  | –      | 10   | –    |      | I <sub>PP</sub> = 1 A, t <sub>p</sub> = 8/20 μs  |  |
|                                  |                  | –      | 12   | –    |      | I <sub>PP</sub> = 3 A, t <sub>p</sub> = 8/20 μs  |  |
| Dynamic resistance <sup>2)</sup> | R <sub>DYN</sub> | –      | 0.21 |      | Ω    | t <sub>p</sub> = 100 ns                          |  |

<sup>1)</sup> Device is electrically symmetrical

<sup>2)</sup> Please refer to Application Note AN210 [\[1\]](#). TLP parameters:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 0.6\text{ ns}$ .

<sup>3)</sup> Stress pulse: 8/20 $\mu\text{s}$  current waveform according to IEC61000-4-5

Typical characteristics diagrams

### 3 Typical characteristics diagrams

Note:  $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

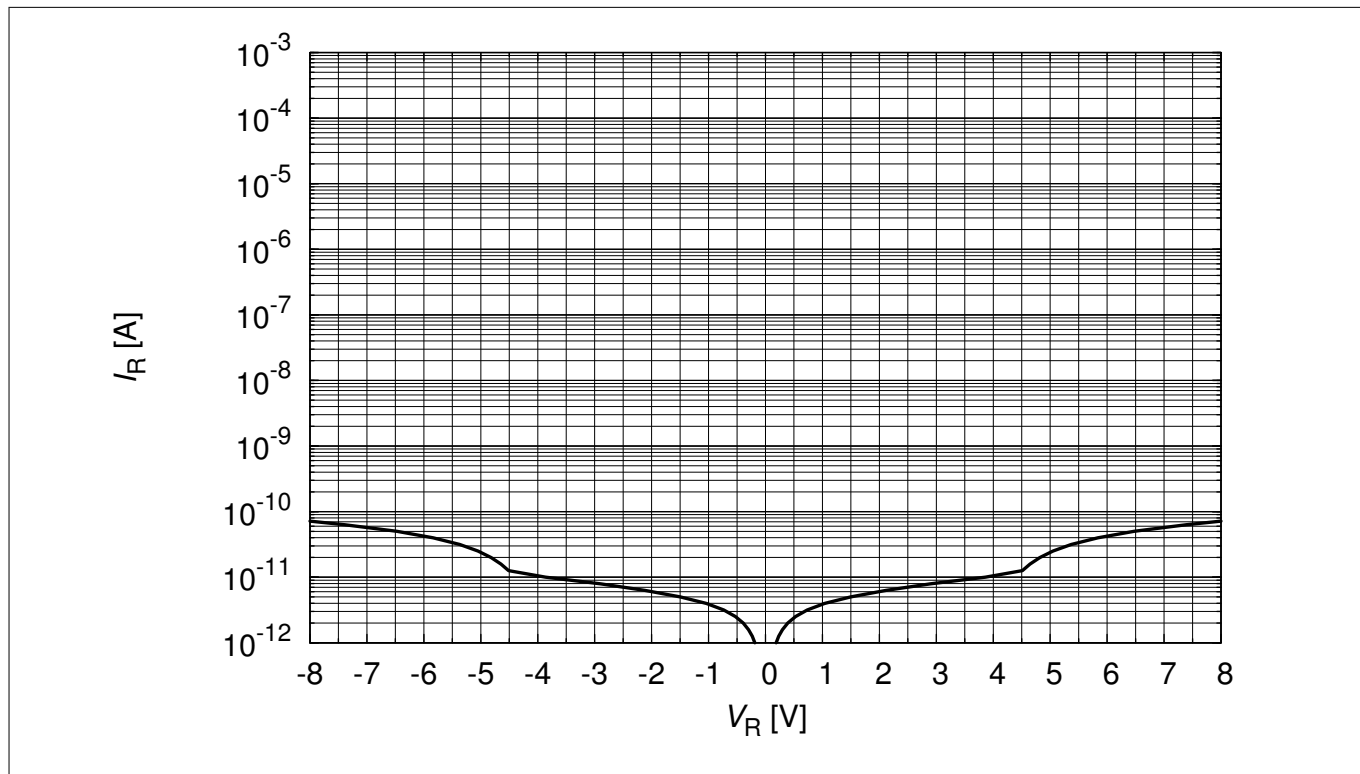


Figure 3 Reverse leakage current:  $I_R = f(V_R)$

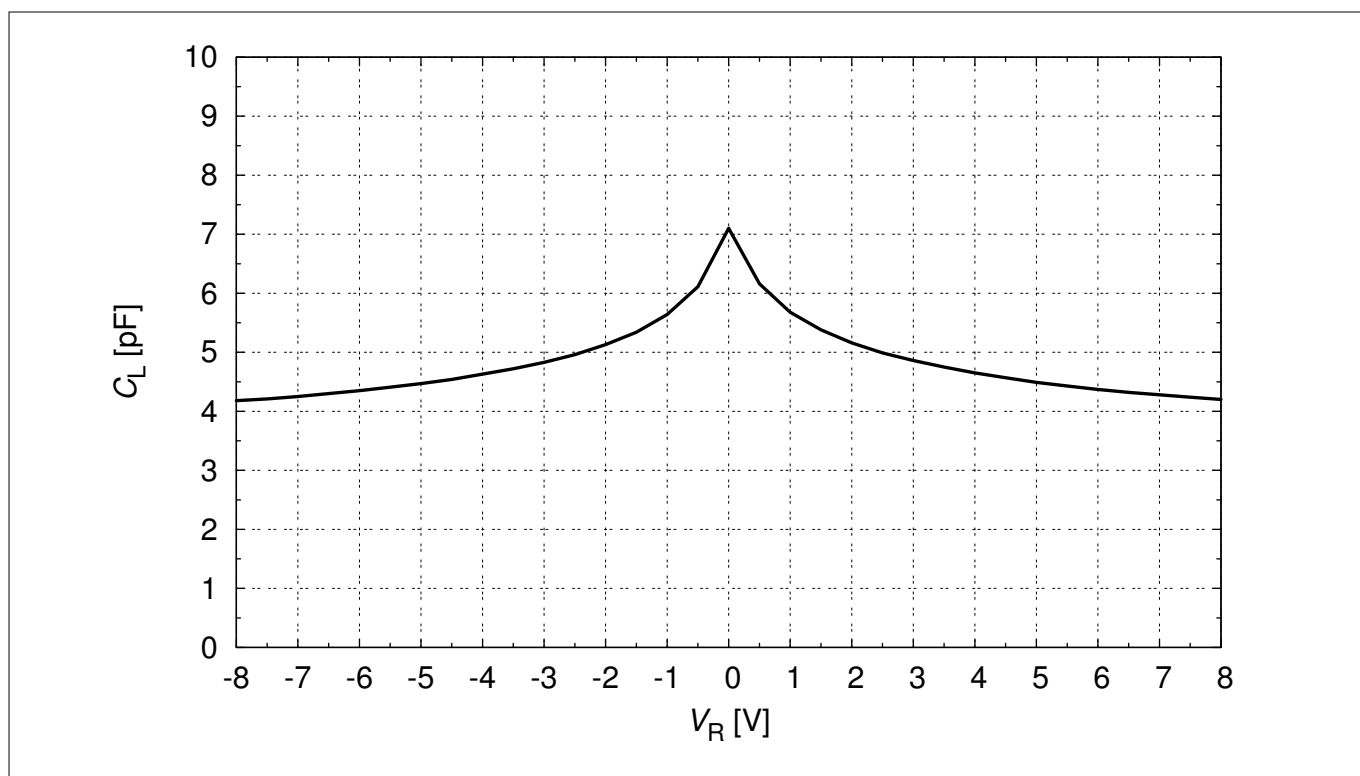


Figure 4 Line capacitance:  $C_L = f(V_R)$ ,  $f = 1\text{ MHz}$

Typical characteristics diagrams

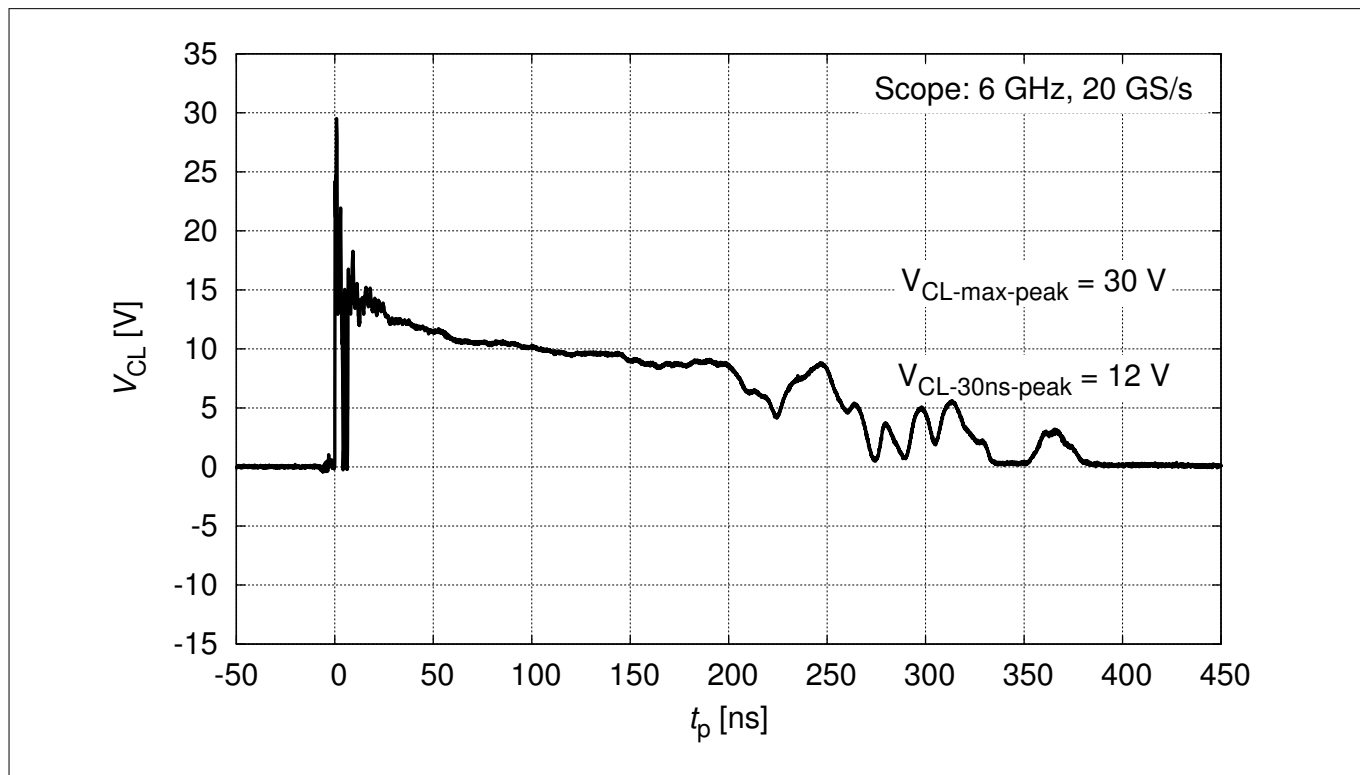


Figure 5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positive pulse

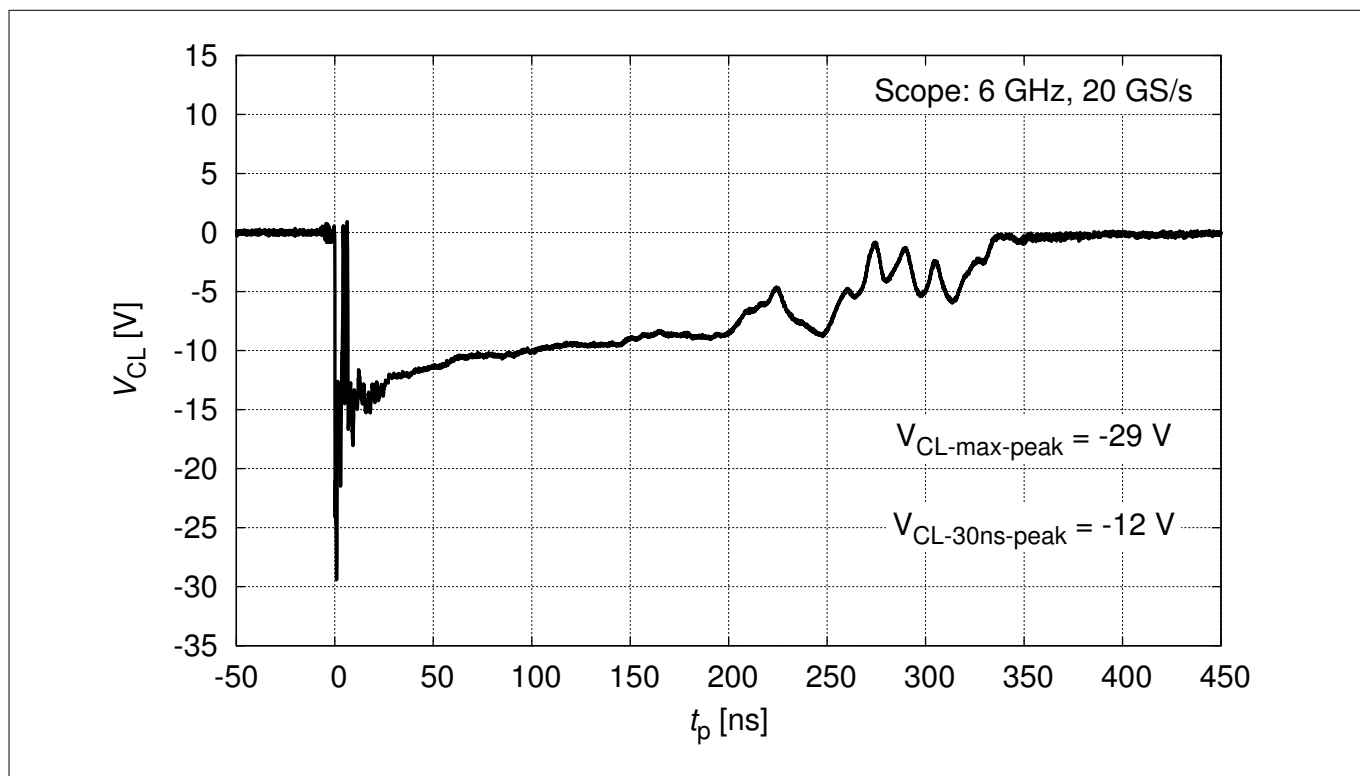


Figure 6 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV negative pulse

Typical characteristics diagrams

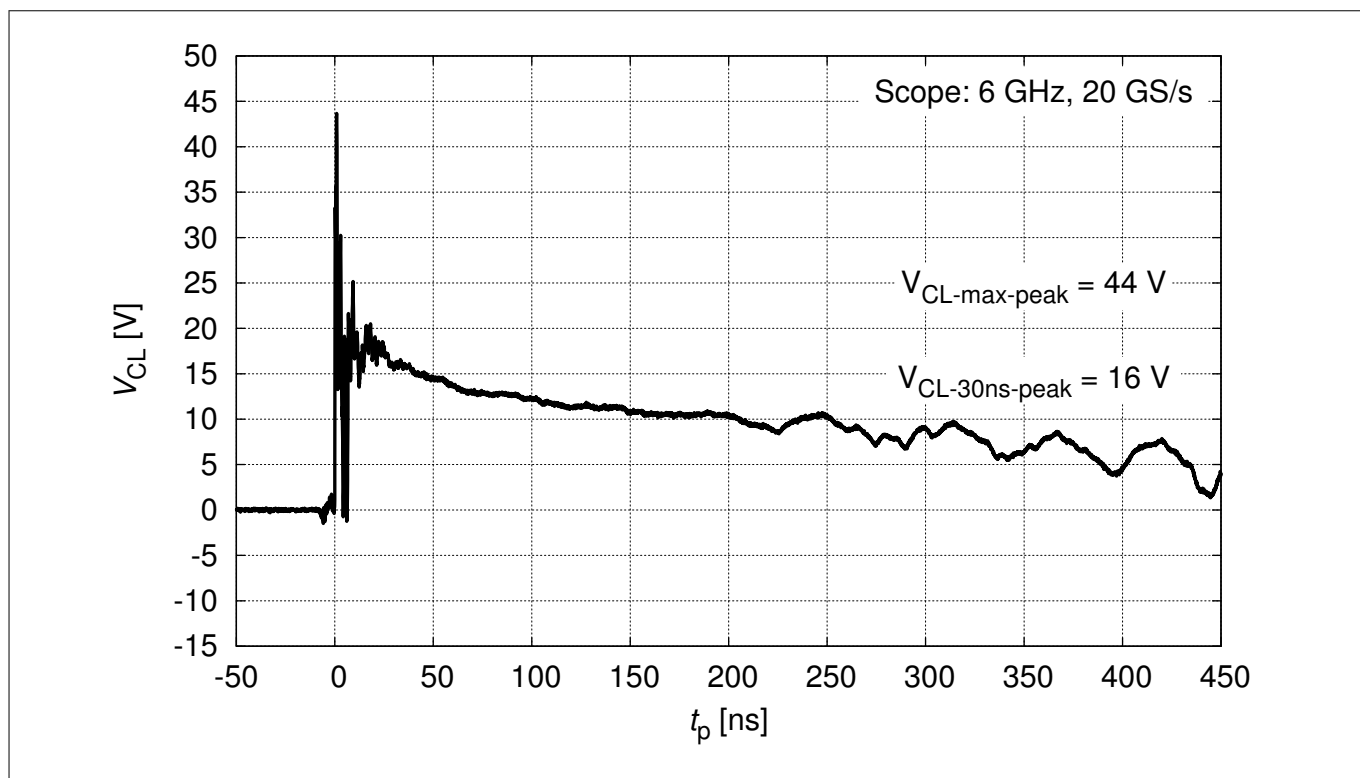


Figure 7 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV positive pulse

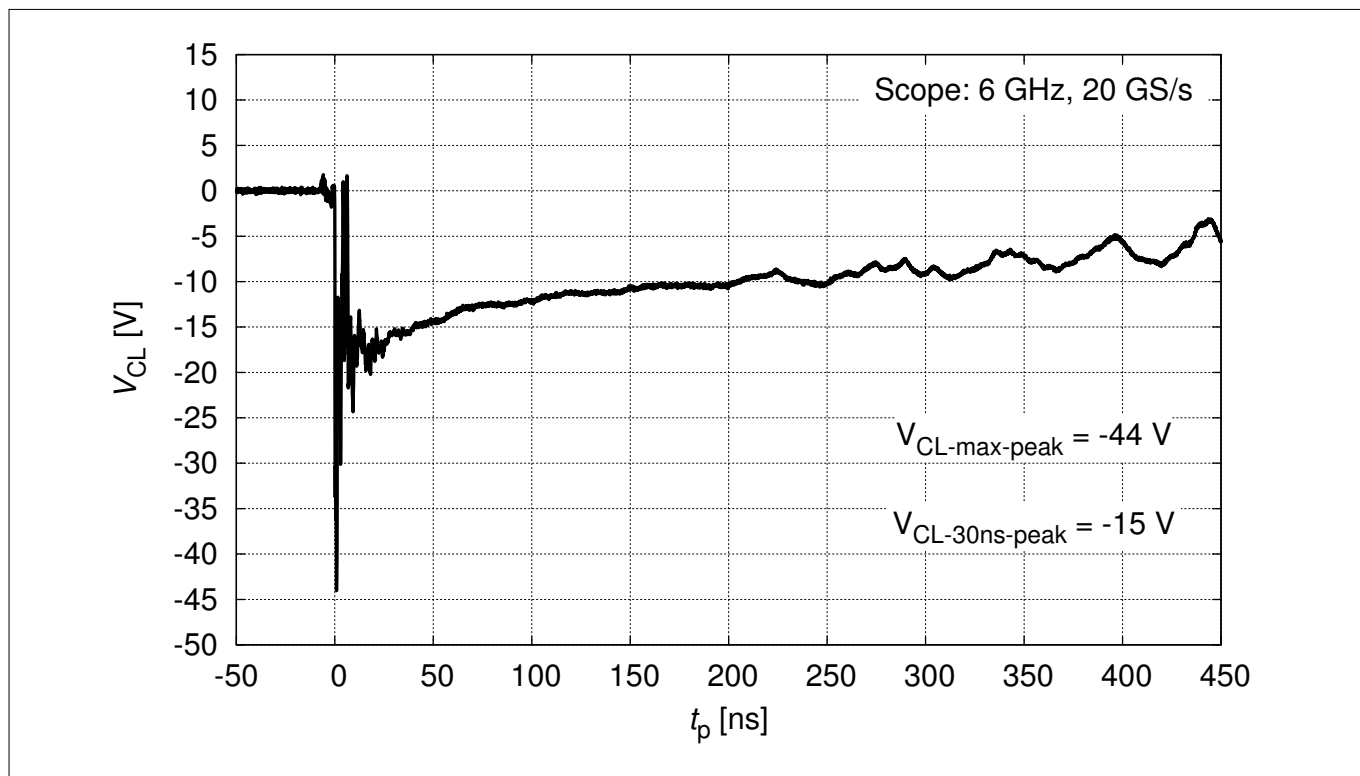


Figure 8 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV negative pulse



Typical characteristics diagrams

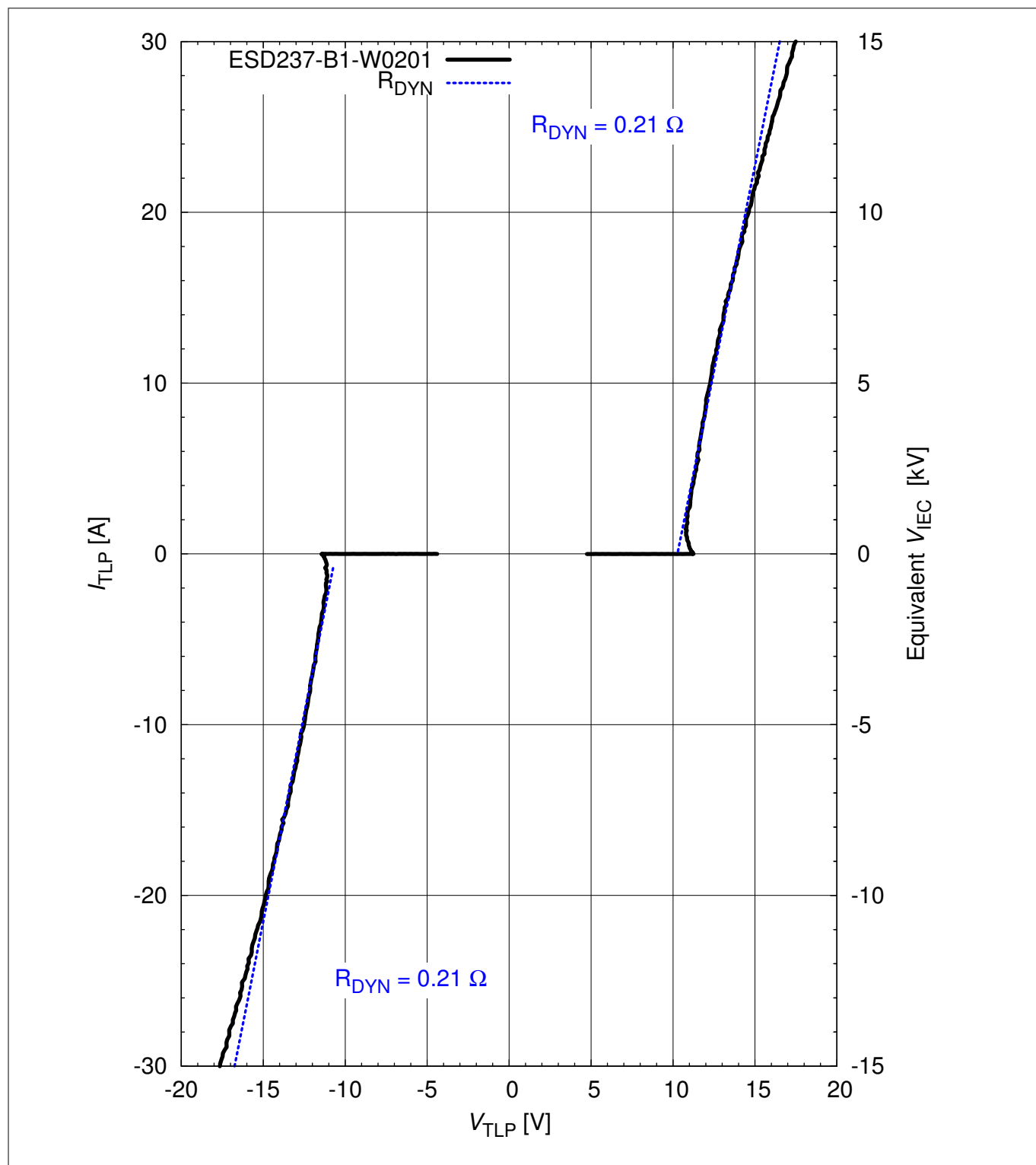


Figure 9 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  [1]

Typical characteristics diagrams

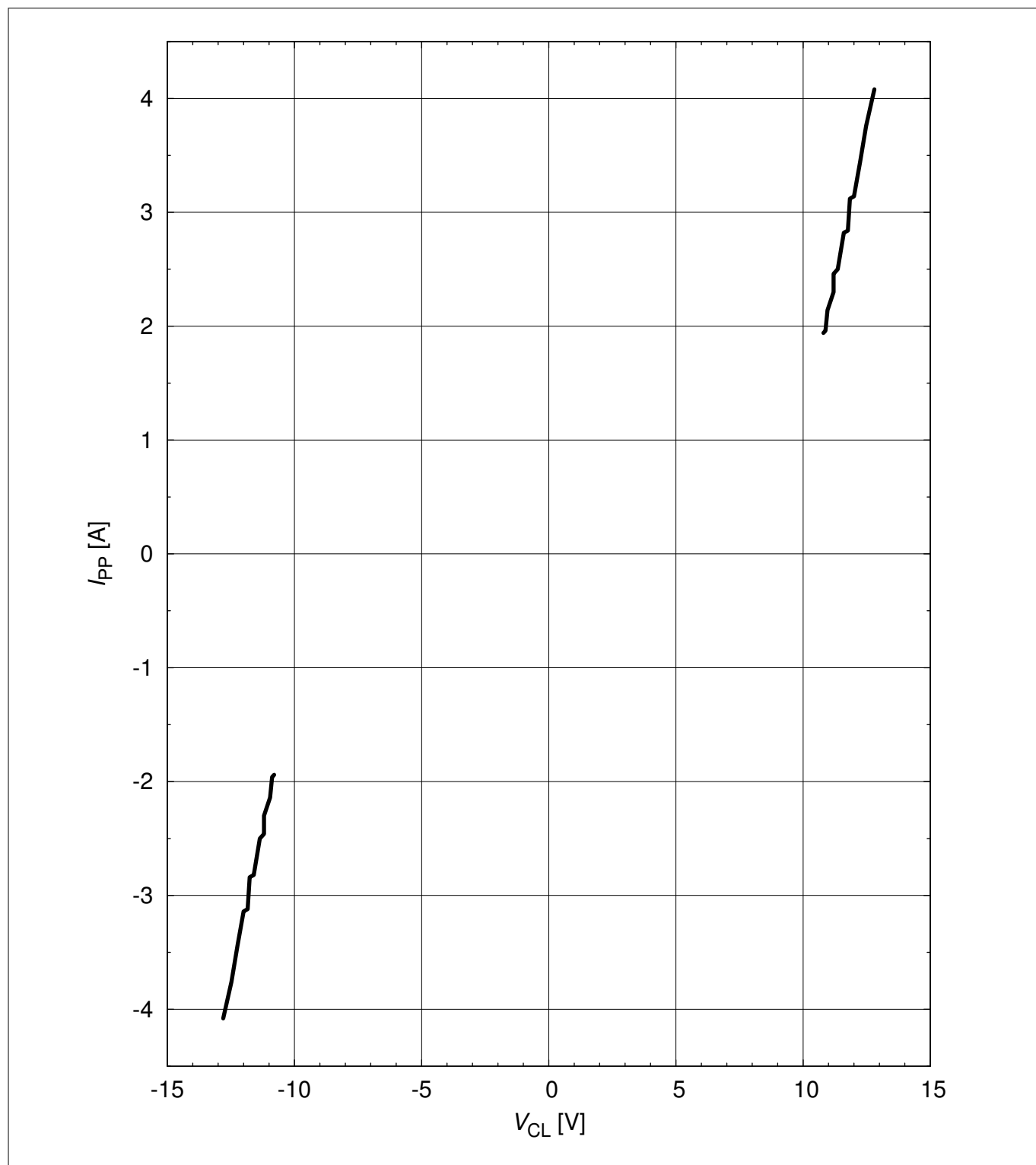
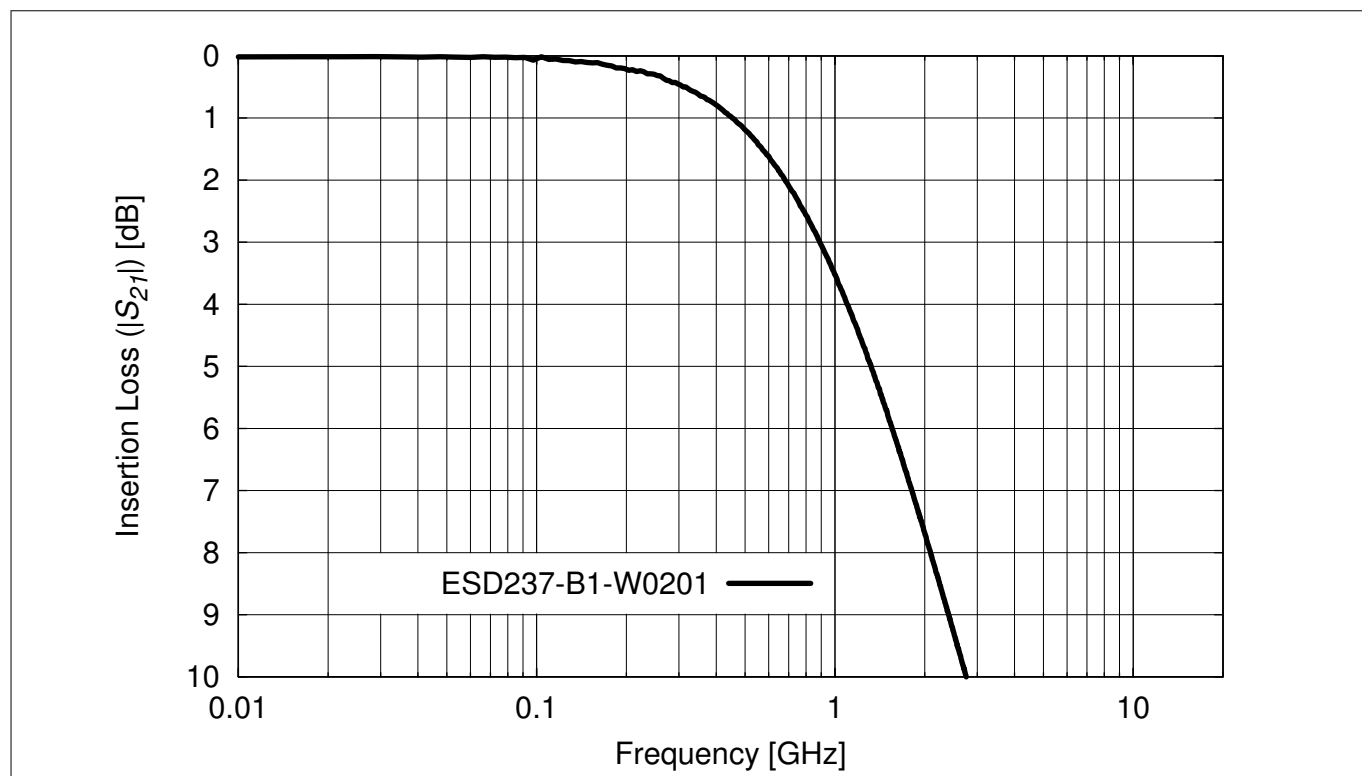


Figure 10 Clamping voltage (Surge):  $I_{PP} = f(V_{CL})$  [1]

Typical characteristics diagrams



**Figure 11** Insertion loss vs. frequency in a 50  $\Omega$  system

Package information

4 Package information

4.1 WLL-2-1 package

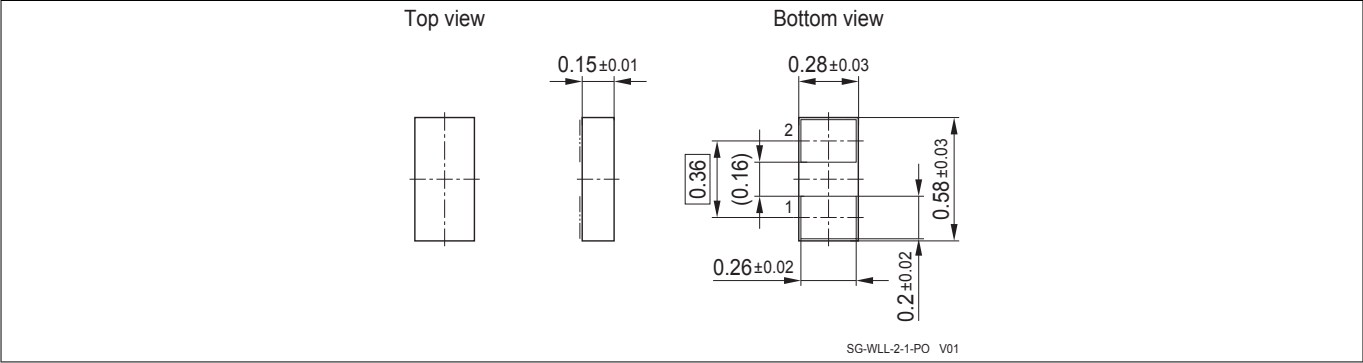


Figure 12 WLL-2-1 package outline (dimension in mm)

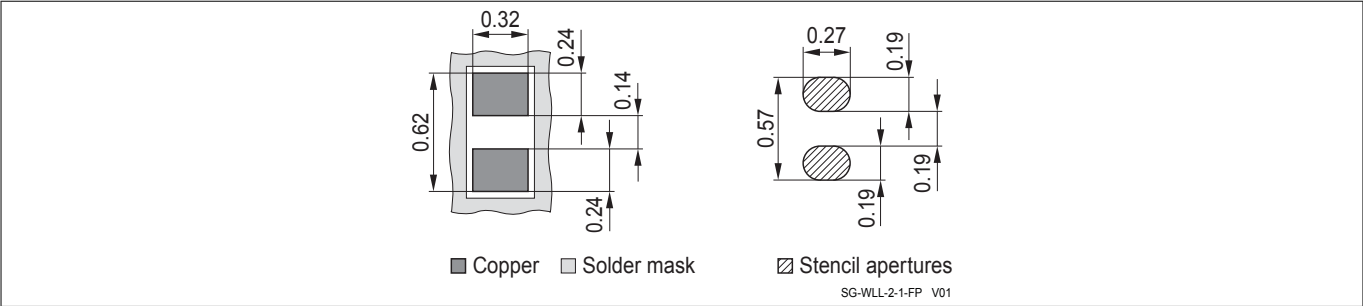


Figure 13 WLL-2-1 footprint (dimension in mm), Recommendations for Printed Circuit Board Assembly see [2]

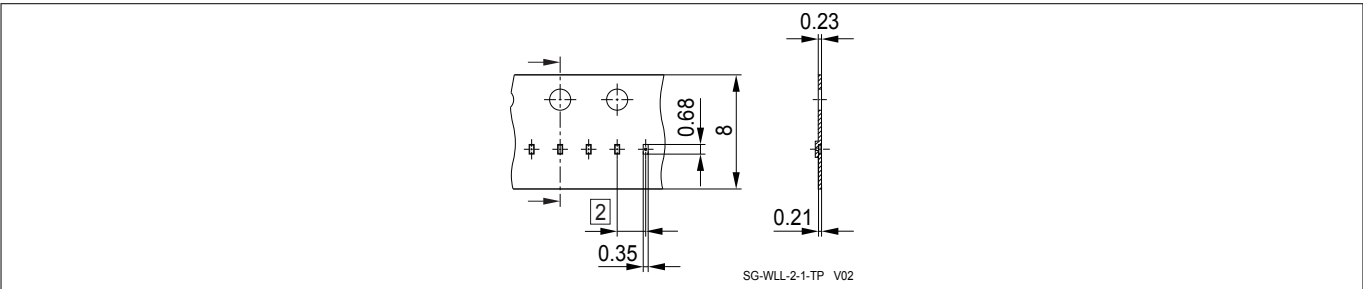


Figure 14 WLL-2-1 packing (dimension in mm)

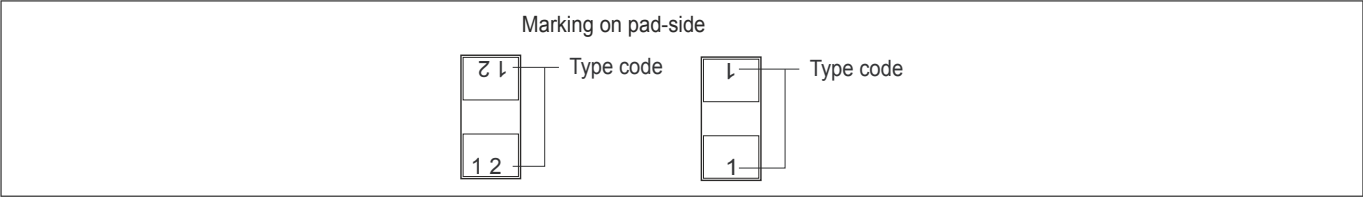


Figure 15 WLL-2-1 marking example (see also Table 1)

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## References

## 5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages  
[http://www.infineon.com/Packageinformation\\_WLL](http://www.infineon.com/Packageinformation_WLL)
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

## Revision History

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### Revision History: Rev.0.3, 2016-01-15

| Page or Item             | Subjects (major changes since previous revision) |
|--------------------------|--------------------------------------------------|
| Revision 1.0, 2016-10-18 |                                                  |
| All                      | Status change to final                           |
|                          |                                                  |

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