



PMH950UPE

20 V, P-channel Trench MOSFET

5 April 2019

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0606-3 (SOT8001) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 1 kV HBM
- Leadless ultra small and ultra thin SMD plastic package: 0.62 × 0.62 × 0.37 mm

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

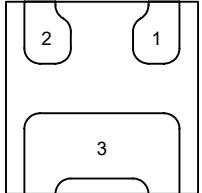
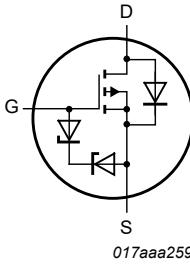
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}$; $T_{amb} = 25^\circ\text{C}$	[1]	-	-	-530	mA
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$; $I_D = -500\text{ mA}$; $T_j = 25^\circ\text{C}$		-	1	1.4	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN0606-3 (SOT8001)	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMH950UPE	DFN0606-3	plastic, leadless ultra small package; 3 terminals; body 0.62 x 0.62 x 0.37 mm	SOT8001

7. Marking

Table 4. Marking codes

Type number	Marking code
PMH950UPE	0001 0100

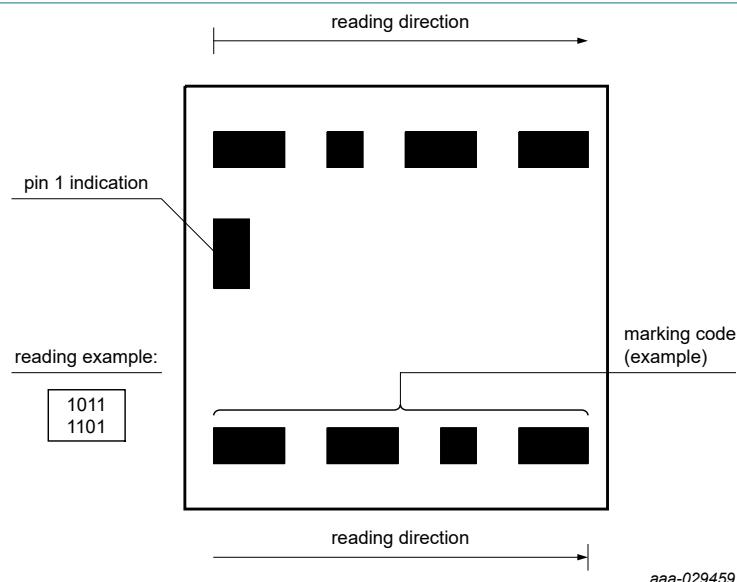


Fig. 1. DFN0606-3 (SOT8001) binary marking code description

8. Limiting values

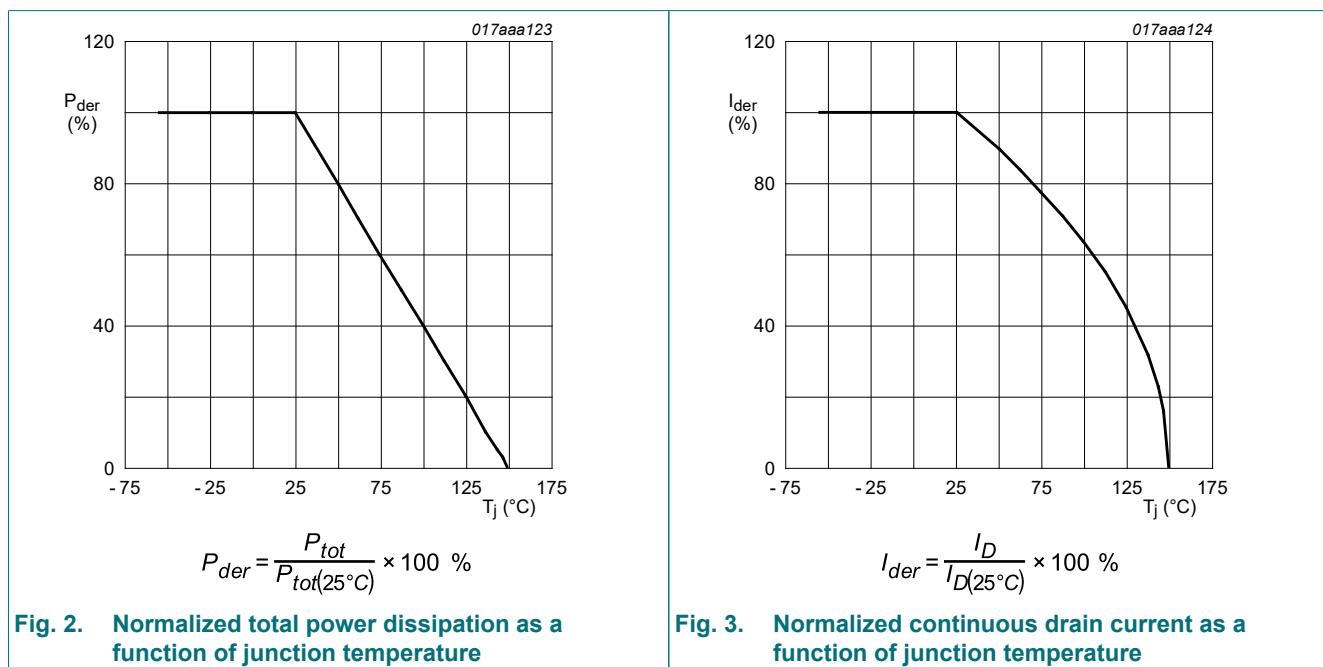
Table 5. Limiting values

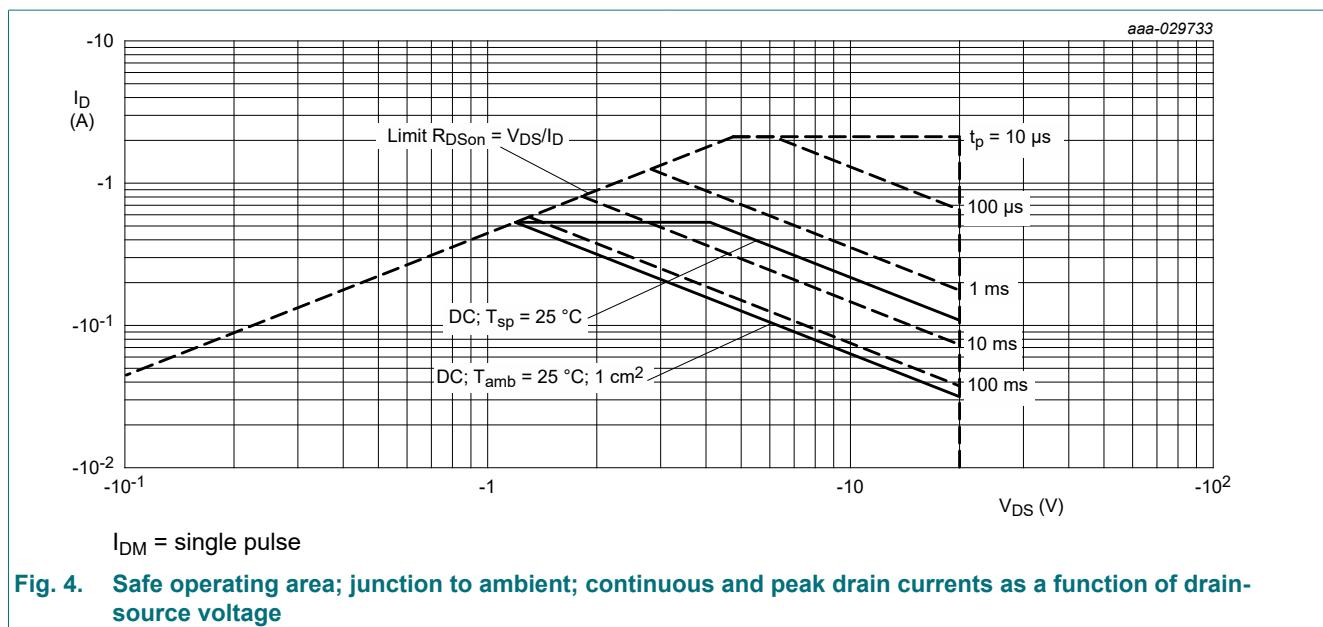
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	-530	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100^\circ\text{C}$	[1]	-	-360	mA
I_{DM}	peak drain current	$T_{amb} = 25^\circ\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-2	A
P_{tot}	total power dissipation	$T_{amb} = 25^\circ\text{C}$	[2]	-	370	mW
			[1]	-	625	mW
		$T_{sp} = 25^\circ\text{C}$		-	2.2	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_s	source current	$T_{amb} = 25^\circ\text{C}$	[1]	-	-530	mA

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





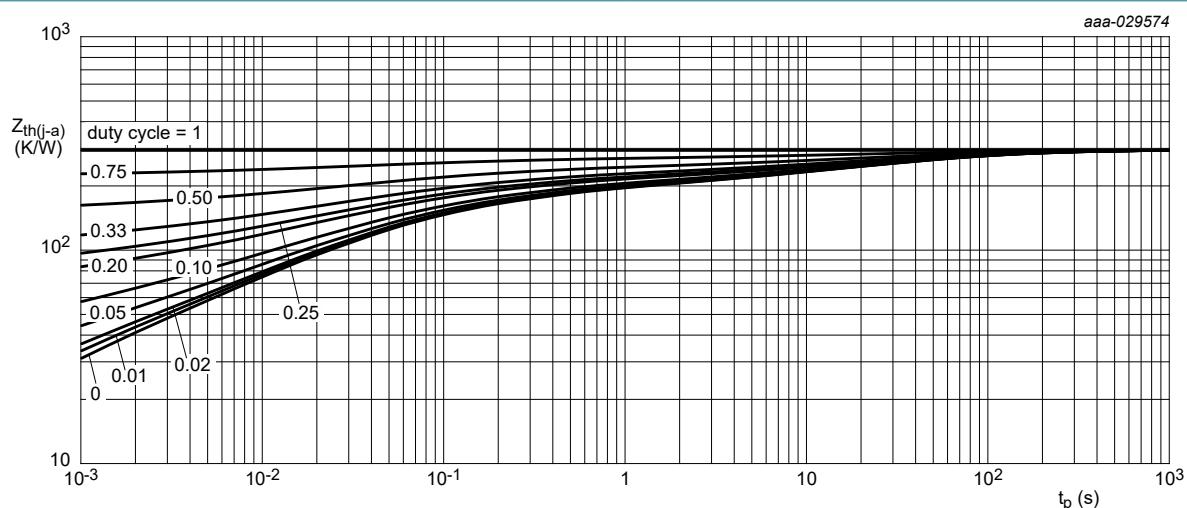
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	300	340	K/W
			[2]	-	175	200	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	50	58	K/W

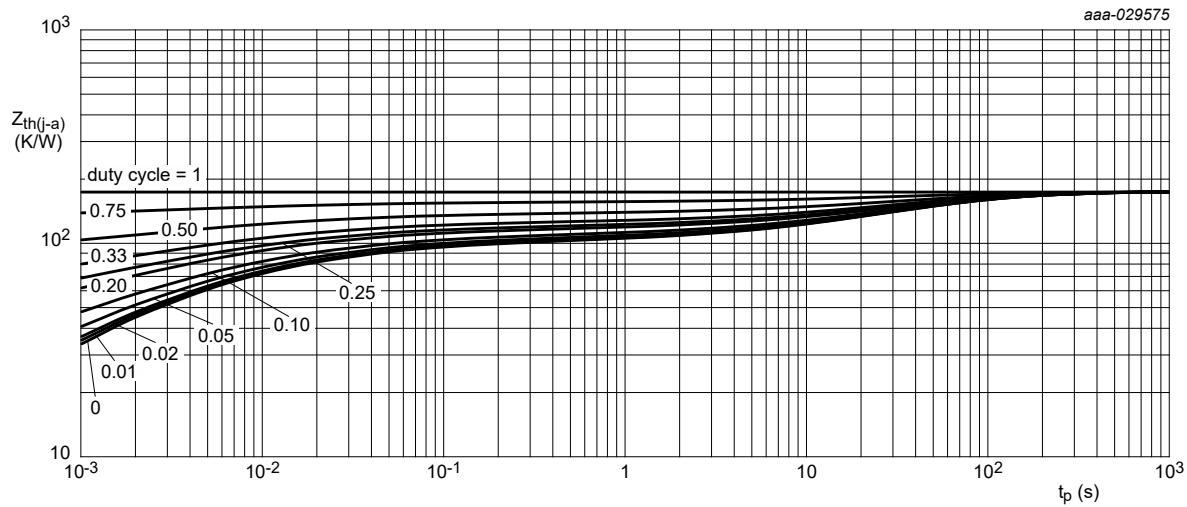
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



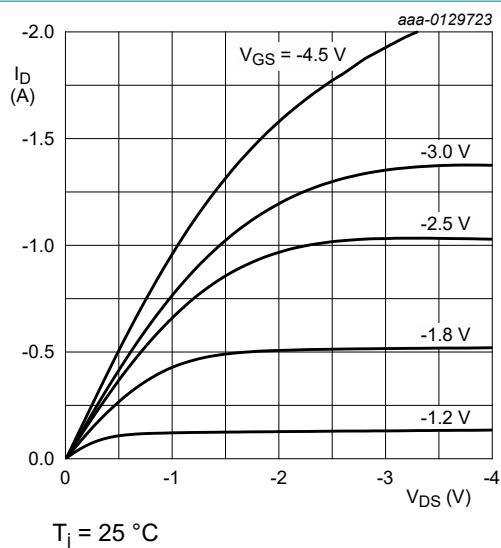
FR4 PCB, mounting pad for drain 1 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

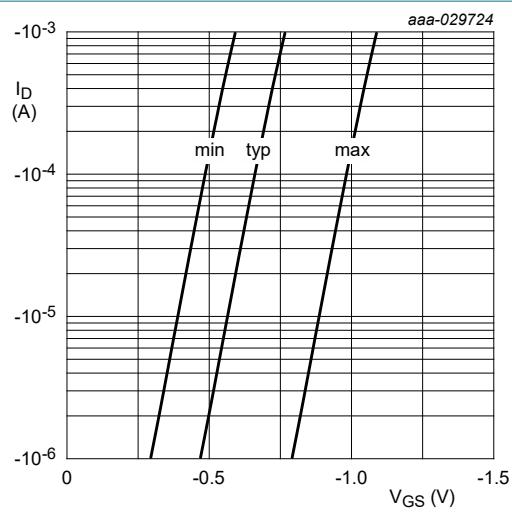
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$		-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$		-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25^\circ C$		-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-10	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	1	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-1	μA
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	100	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25^\circ C$		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -500 mA; T_j = 25^\circ C$		-	1	1.4	Ω
		$V_{GS} = -4.5 V; I_D = -500 mA; T_j = 150^\circ C$		-	1.6	2.3	Ω
		$V_{GS} = -2.5 V; I_D = -200 mA; T_j = 25^\circ C$		-	1.4	2.2	Ω
		$V_{GS} = -1.8 V; I_D = -40 mA; T_j = 25^\circ C$		-	1.8	3.3	Ω
		$V_{GS} = -1.5 V; I_D = -40 mA; T_j = 25^\circ C$		-	2.1	5.5	Ω
		$V_{GS} = -1.2 V; I_D = -10 mA; T_j = 25^\circ C$		-	2.9	-	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -600 mA; T_j = 25^\circ C$		-	700	-	mS
R_G	gate resistance	$f = 1 MHz$		-	3.7	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -600 mA; V_{GS} = -4 V; T_j = 25^\circ C$		-	0.29	0.5	nC
Q_{GS}	gate-source charge			-	0.08	-	nC
Q_{GD}	gate-drain charge			-	0.08	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25^\circ C$		-	36	-	pF
C_{oss}	output capacitance			-	6.3	-	pF
C_{rss}	reverse transfer capacitance			-	4.7	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V; I_D = -600 mA; V_{GS} = -4 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$		-	1	-	ns
t_r	rise time			-	2	-	ns
$t_{d(off)}$	turn-off delay time			-	4	-	ns
t_f	fall time			-	6	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = -600 mA; V_{GS} = 0 V; T_j = 25^\circ C$		-	-0.7	-1.2	V



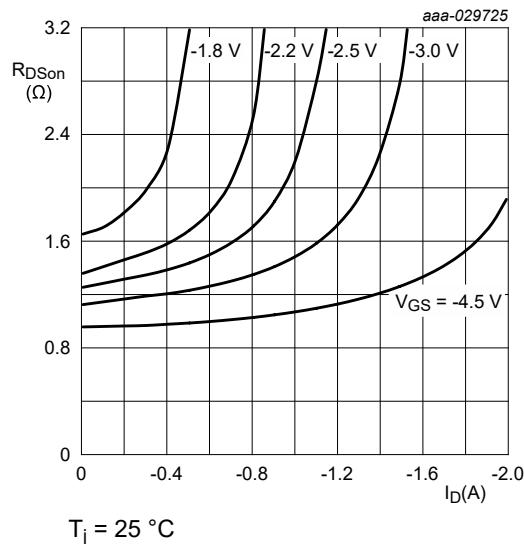
$T_j = 25^\circ\text{C}$

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



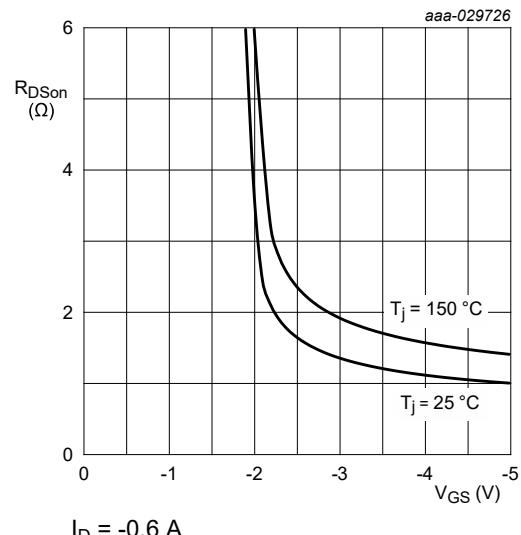
$V_{DS} = -5\text{ V}$
 $T_j = 25^\circ\text{C}$

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



$I_D = -0.6\text{ A}$

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

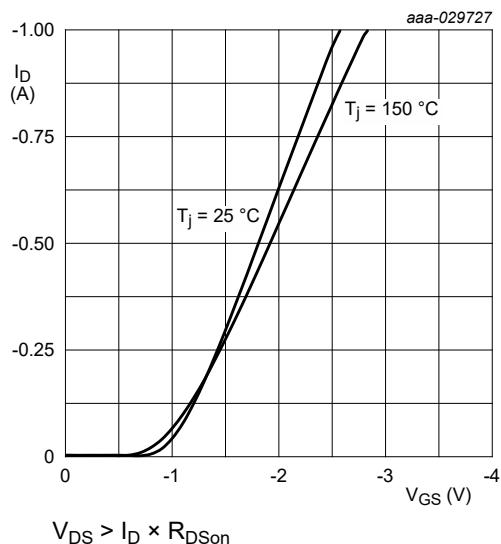


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

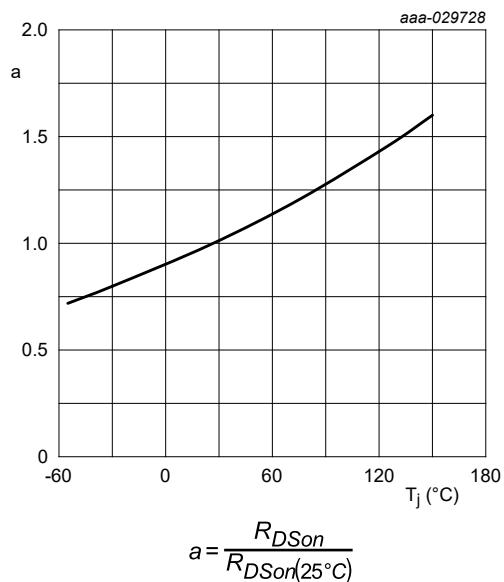


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

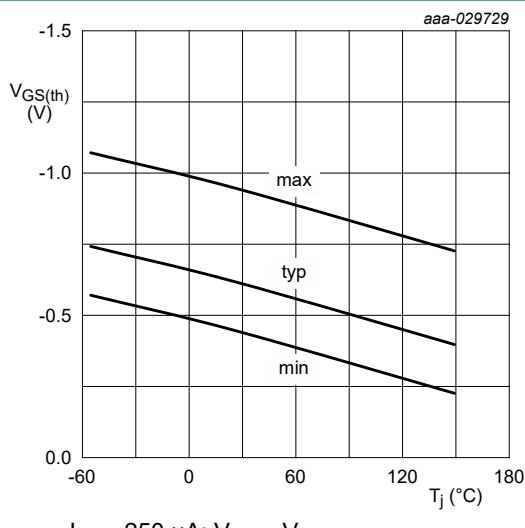


Fig. 13. Gate-source threshold voltage as a function of junction temperature

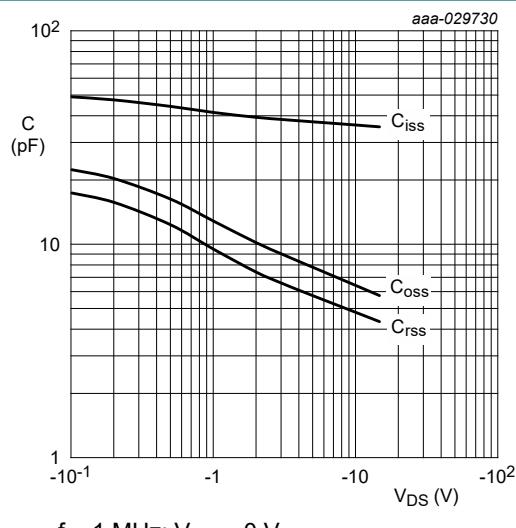


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

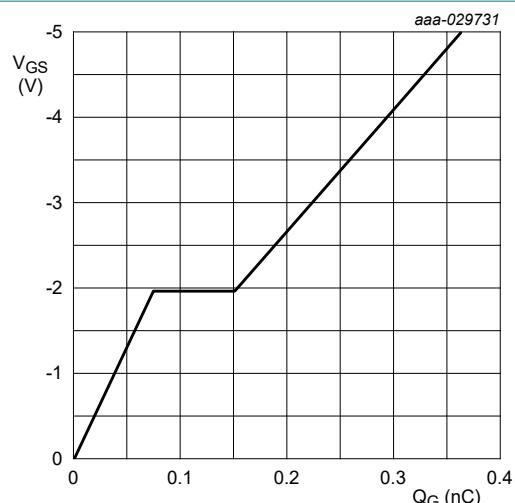


Fig. 15. Gate-source voltage as a function of gate charge; typical values

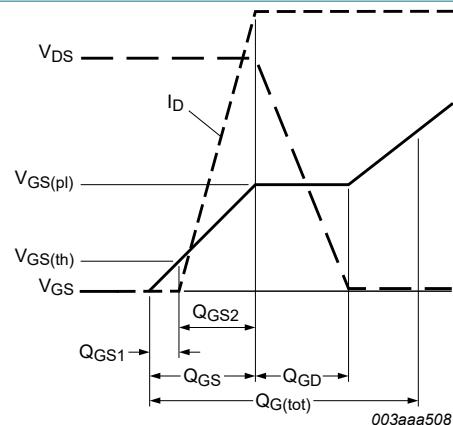
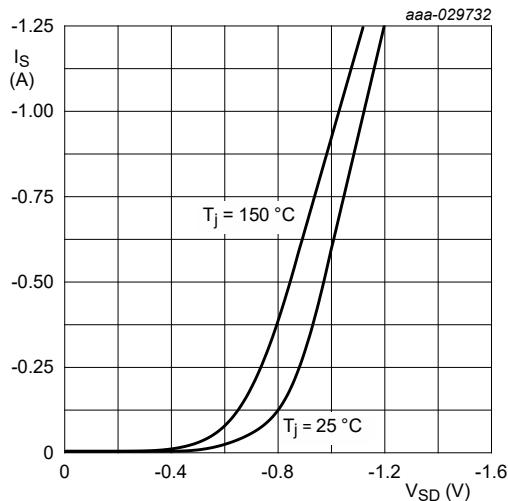


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

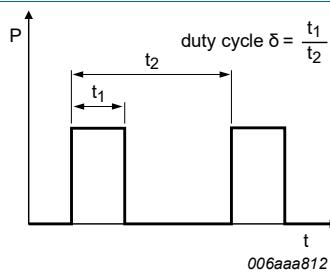
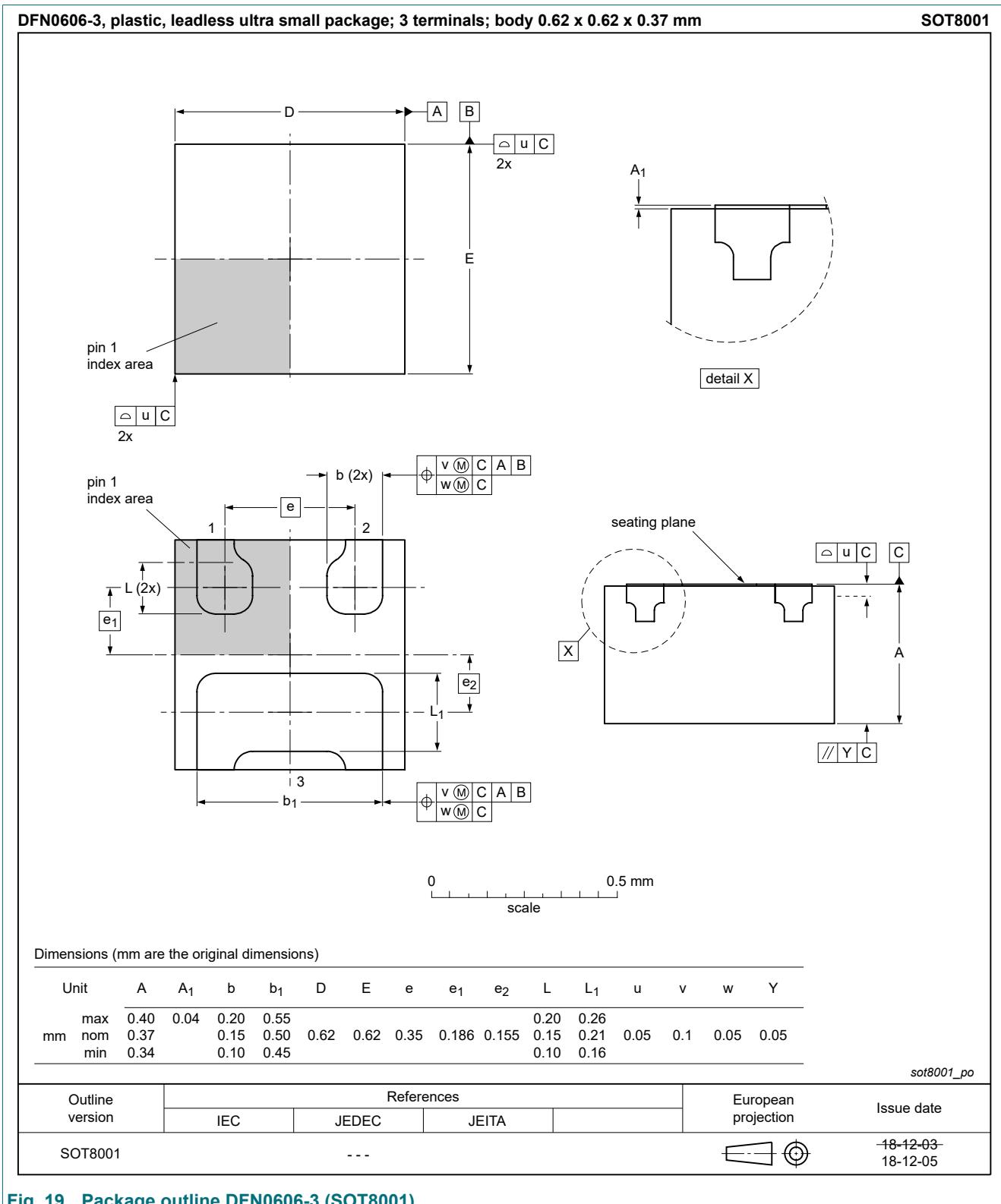


Fig. 18. Duty cycle definition

12. Package outline



13. Soldering

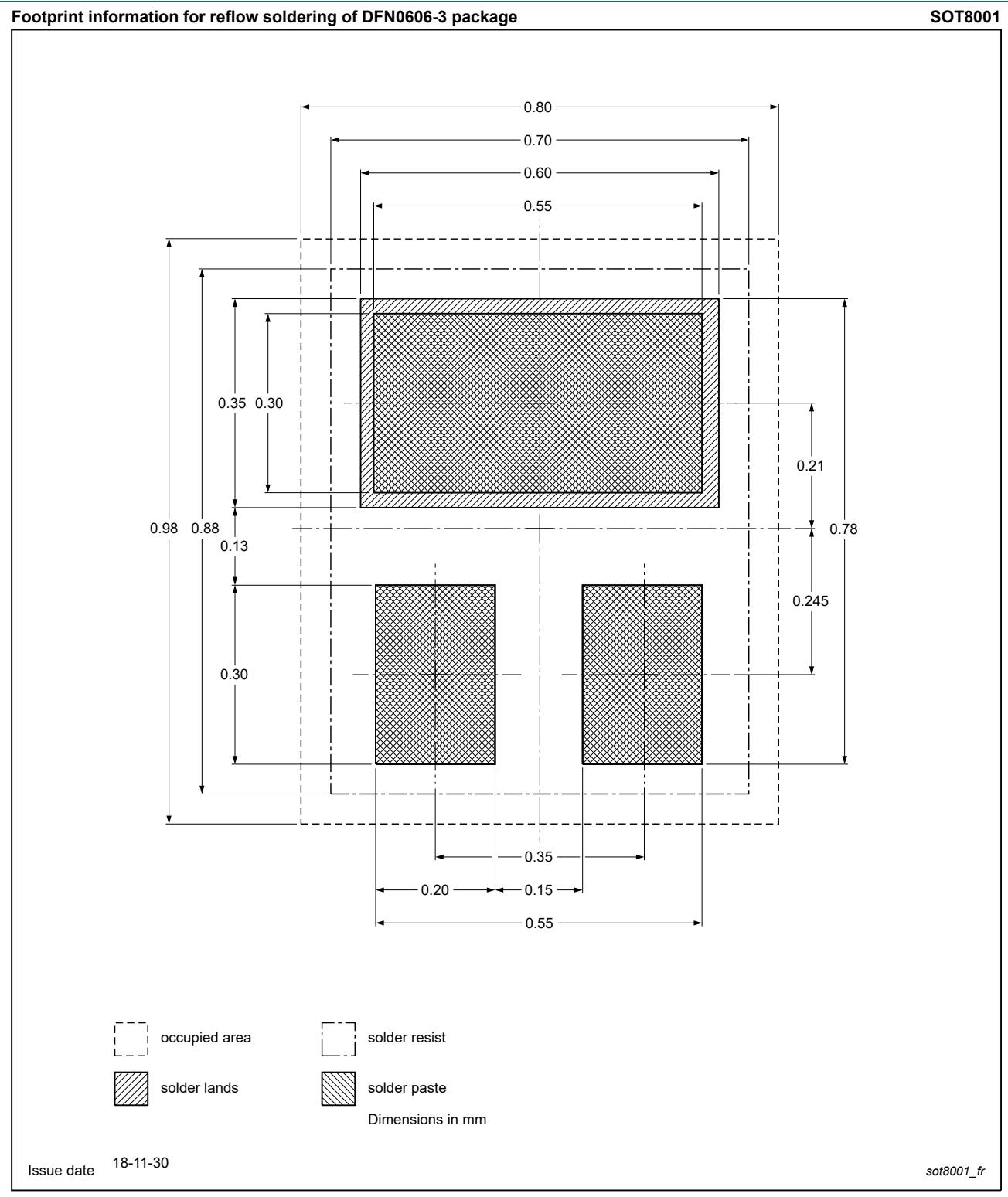


Fig. 20. Reflow soldering footprint for DFN0606-3 (SOT8001)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 5 April 2019



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