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32-Bit Traveo™ Family

S6J3110 Series Microcontroller Datasheet

The S6J3110 series is a set of 32-bit microcontrollers designed for in-vehicle use. It uses the Arm® Cortex®-R5 CPU as a CPU.

Features

This section explains the features of the S6J3110 series.

Cortex-R5 Core

This section explains the Cortex-R5 CPU core.

- Arm® Cortex®-R5
- 32-bit Arm architecture
 - 2-instruction issuance super scalar
 - 8-stage pipeline
- Arm v7/Thumb®-2 instruction set
- MPU (memory protection) equipped
 - 16-area support
- ECC support for the TCM ports for RAM
 - 1-bit error correction and 2-bit error detection (SEC-DED)
- TCM ports
 - 2 TCM ports
 - ATCM port
 - BTCM port (BOTCM, B1TCM)
- Caches
 - Instruction cache 16 KB
 - Data cache 16 KB
- VIC port
 - Low latency interrupt
- AXI master interface
 - 64-bit AXI interface (instruction/data access)
 - 32-bit AXI interface (I/O access)
- AXI slave interface
 - 64-bit AXI interface (TCM port access)
- ETM-R5 trace

Peripheral Functions

This section explains peripheral functions.

- Clock generation
 - Main clock oscillation (4 MHz)
 - No sub clock oscillation
 - CR oscillation (100 kHz)
 - CR oscillation (4 MHz)
- Built-in flash memory size
 - Program: 4096 K + 64 KB (S6J311EyzC*) / 3072K + 64KB (S6J311DyAC*)
 - Work: 112 KB (S6J311EyzC*) / 112 KB (S6J311DyAC*)

* y: J/H, z: A/B

- Built-in RAM size
 - TCRAM 64 KB
 - System SRAM 256 KB (S6J311EyzC*) / 192 KB (S6J311DyAC*)
 - Backup RAM 64 KB (S6J311EyzC*) / 64 KB (S6J311DyAC*)

* y: J/H, z: A/B
- General-purpose ports: 150 channels (S6J311xJAC*)/116 channels (S6J311xHzC*)
 - * x: E/D, z: A/B
- DMA controller
 - Up to 16 channels can be activated simultaneously.
- A/D converter (successive approximation type)
 - 12-bit resolution, 2 units mounted: Max 64 channels (32 channels + 32 channels)
- External interrupt input: 16 channels
 - Level ("H"/"L") and edge (rising/falling) can be detected.
- Multi-function serial (transmission and reception FIFOs mounted): Max 22 channels
 - <I²C>
 - Full-duplex double buffering system, 64-byte transmission FIFO, 64-byte reception FIFO.
 - Standard mode (Max. 100kbps) is supported only.
 - DMA transfer is supported (only for ch.0 to ch.7).
 - <UART (asynchronous serial interface)>
 - Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
 - Parity check can be enabled/disabled.
 - Built-in dedicated baud rate generator
 - An external clock can be used as a transfer clock.
 - Parity, frame, overrun error detection functions are available.
 - DMA transfer is supported (only for ch.0 to 7).
 - <CSIO (synchronous serial interface)>
 - Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
 - Support for SPI. Both master and slave roles are supported. Data length in bits can be set to a value from 5 to 16 or one of the values of 20, 24, and 32.
 - Built-in dedicated baud rate generator (master operation)
 - External clock input is enabled (slave operation).
 - Overrun error detection function is available.
 - DMA transfer is supported (only for ch.0 to ch.7).
 - Serial chip select SPI function

<LIN-UART (asynchronous serial interface for LIN)>

- Full duplex, double buffering system; 64-byte transmission FIFO, 64-byte reception FIFO
- Support for LIN protocol revision 2.1
- Both master and slave roles are supported.
- Framing error and overrun error detection
- LIN Synch break generation and detection, LIN Synch Delimiter generation
- Built-in dedicated baud rate generator
- The external clock can be adjusted by the reload counter.
- DMA transfer is supported (only for ch.0 to ch.7).
- CAN controller: CAN-FD Max 2 channel
 - CAN-FD (V3.2.0)
 - CAN transfer speed: 1Mbps
 - CAN Clock: Max 40MHz
 - 192 message buffers/channel (reception message buffer size)
 - 32 message buffer/channel (transmission message buffer size)
- Base timer: MAX 30 channels
 - 16-bit Timer.
 - It is selectable by 4 functions of the PWM/PPG/PWC/Reload Timer.
 - 2-channel cascade connection enables operation as a 32-bit timer.(PWC and Reload Timer)
- Free-run timer: Max 6 channels
 - 32-bit Timer.
 - Main clock oscillation and CR oscillation are available.
 - Free-run timer output can work in combination with an input capture and an output compare.
- Input capture: Max 12 channels
 - 32-bit Timer.
- Output compare: Max 12 channels
 - 32-bit Timer.
- Real time clock (RTC) (day/hour/minute/second)
 - Main clock oscillation or CR oscillation (100 kHz) can be selected as an operation clock.
- Calibration: Real time clock (RTC) driven by the CR clock
 - Correction can be done by configuring the prescaler of the real time clock based on the ratio between the main clock and the CR clock.
- Clock supervisor
 - Abnormality (such as damaged crystal) of the main clock oscillation (4 MHz) can be monitored.
 - The clock can switch to the CR clock when an abnormality is detected.
 - PLL abnormality can be detected.
- CRC generation
 - Fixed-length CRC
 - CCITT CRC16 generator polynomial: 0x1021
 - IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7
- Watchdog timer
 - Hardware watchdog
 - Software watchdog
- NMI
- I/O relocation
 - Peripheral function pin locations can be changed.
- Low-power consumption control
 - Standby function
 - Power-off function
 - Partial wakeup function
- Power-on reset
- Low-voltage detection reset
- Security
 - Flash security
 - Interface security (JTAG + test port)
 - SHE
 - Unique device ID
- Package:
 - LEP176 (S6J311xJAC*) * x: E/D
 - LES144 (S6J311xHzC*) * x: E/D, z: A/B
- CMOS 55 nm technology
- Power supply
 - 5 V single power supply
 - The voltage step-down circuit generates internal 1.2 V from 5 V.
 - 5 V power supply is used for I/O.

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1. Product Lineup

The following table lists the models available in the S6J3110 series.

Table 1-1 Memory Size

| | S6J311EyzC* | S6J311DyAC* |
|-------------------|--|--|
| Flash (Program) | 4096K bytes + small sector (8KB x 8) | 3072K bytes + small sector (8KB x 8) |
| Flash (Work) | 112K bytes | |
| RAM (TCRAM) | 64K bytes | |
| RAM (System SRAM) | 256K bytes | 192K bytes |
| RAM (Backup RAM) | 64K bytes | |

* y: J/H, z: A/B

Table 1-2 SHE Option

| | S6J311xyAC* | S6J311EHBC |
|----------------|--------------------|-------------------|
| Security (SHE) | ON | OFF |

* x: E/D, y: J/H

Table 1-3 Comparison of models Available

| | S6J311xJAC* * x:E/D | S6J311xHzC* * x:E/D, z: A/B |
|--|------------------------------------|---------------------------------------|
| CPU core | Cortex-R5 | |
| CMOS 55 nm technology | 55 nm | |
| Package | LEP176 | LES144 |
| Main clock | 4 MHz | |
| Built-in CR oscillator | 100 kHz | |
| | 4 MHz | |
| Maximum CPU operating frequency | 144 MHz (target) | |
| Watchdog timer | 1 channel (hardware) | |
| | 1 channel (software) | |
| Clock supervisor | Available | |
| External power supply, low-voltage detection reset | Available | |
| Internal power supply, low-voltage detection reset | Available | |
| NMI request | Available | |
| External interrupt | 16 channels | |
| DMA controller | 16 channels | |
| CAN-FD | 2 channels (192 msg buffers/ch) | 1 channel (192 msg buffers/ch) |
| Multi-function serial | 22 channels | 4 channels |
| A/D converter | 12-bit (2 units) | 12-bit (2 units) |
| | Unit 0 x 32 channels | Unit 0 x 25 channels |
| | Unit 1 x 32 channels | Unit 1 x 31 channels |
| Free-run timer | 6 channels | |
| Input capture | 12 channels | |
| Output compare | 12 channels | |
| Base timer (16-bit) | 30 channels | |
| Real time clock (RTC) | 1 channel | |
| CR clock calibration | Available | |
| CRC generation | Available | |
| Low-power consumption mode | Standby function | |
| | Power-off function | |
| | Partial wakeup function | |
| General-purpose port GPIO | 150 channels | 116 channels |
| Power supply | 5 V + 5% to 10% | |
| Operation assurance temperature (Ta) | -40 °C to +105 °C | |
| On-chip debugger (JTAG) | Available | |

2. Pin Assignment

The following figures show the pin assignment of the S6J3110 series.

Figure 2-1 Pin Assignment for S6J311xJAC*

* x: E/D

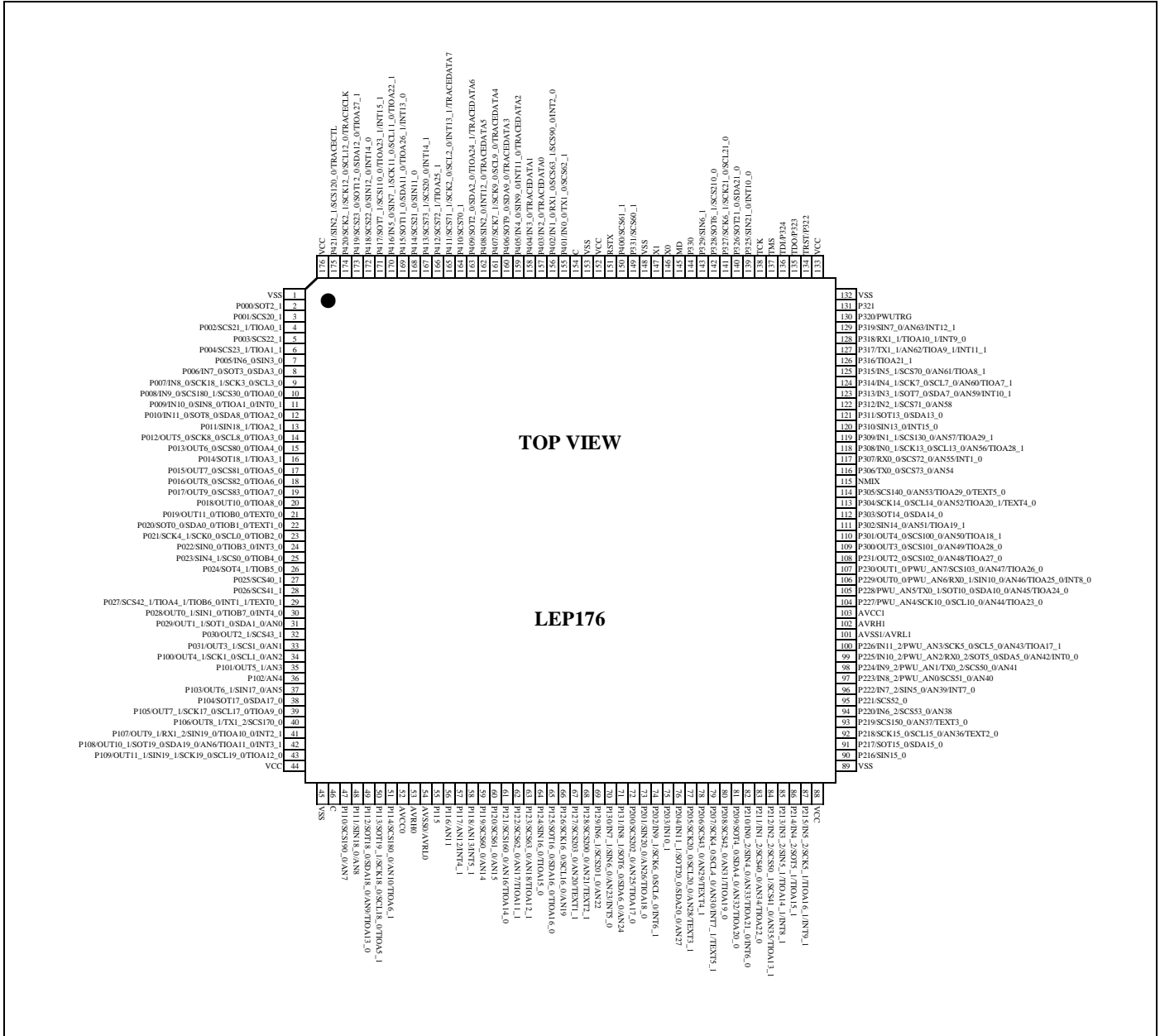
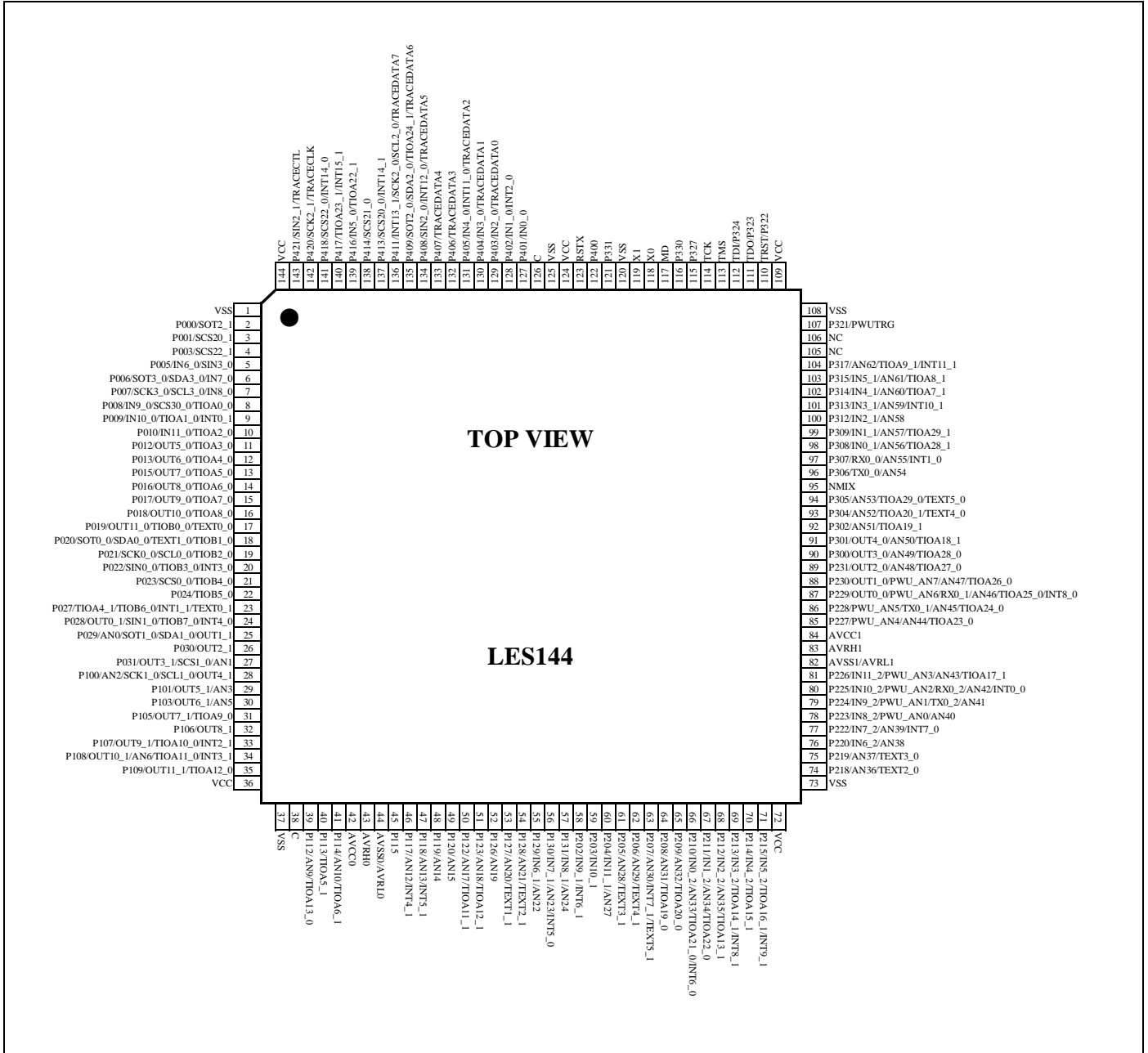


Figure 2-2 Pin Assignment for S6J311xHzC*

* x: E/D, z: A/B



3. Pin Description

This section provides a list of the pin functions of the S6J3110 series

Table 3-1 S6J311xJAC* Pin Functions

* x: E/D

| Pin No. S6J311xJAC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|---|-----------------------|------------------------|--|
| 2 | P000 SOT2_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 serial data output pin (1) |
| 3 | P001 SCS20_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 chip select 0 I/O pin (1) |
| 4 | P002 SCS21_1 TIOA0_1 | - - - | P | General-purpose I/O port Multi-function serial ch.2 chip select 1 output pin (1) Base timer ch.0 TIOA output pin (1) |
| 5 | P003 SCS22_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 chip select 2 output pin (1) |
| 6 | P004 SCS23_1 TIOA1_1 | - - - | P | General-purpose I/O port Multi-function serial ch.3 chip select 2 output pin (1) Base timer ch.1 TIOA output pin (1) |
| 7 | P005 IN6_0 SIN3_0 | - - - | P | General-purpose I/O port Input capture ch.6 input pin (0) Multi-function serial ch.3 serial data input pin (0) |
| 8 | P006 IN7_0 SOT3_0 SDA3_0 | - - - - | P | General-purpose I/O port Input capture ch.7 input pin (0) Multi-function serial ch.3 serial data output pin (0) I ² C bus ch.3 serial data I/O pin |
| 9 | P007 IN8_0 SCK18_1 SCK3_0 SCL3_0 | - - - - - | P | General-purpose I/O port Input capture ch.8 input pin (0) Multi-function serial ch.18 clock I/O pin (1) Multi-function serial ch.3 clock I/O pin (0) I ² C bus ch.3 serial clock I/O pin |
| 10 | P008 IN9_0 SCS180_1 SCS30_0 TIOA0_0 | - - - - - | P | General-purpose I/O port Input capture ch.9 input pin (0) Multi-function serial ch.18 chip select 0 I/O pin (1) Multi-function serial ch.3 chip select 0 I/O pin (0) Base timer ch.0 TIOA output pin (0) |
| 11 | P009 IN10_0 SIN8_0 TIOA1_0 INT0_1 | - - - - - | P | General-purpose I/O port Input capture ch.10 input pin (0) Multi-function serial ch.8 serial data input pin (0) Base timer ch.1 TIOA I/O pin (0) INT0 external interrupt input pin (1) |
| 12 | P010 IN11_0 SOT8_0 SDA8_0 TIOA2_0 | - - - - - | P | General-purpose I/O port Input capture ch.11 input pin (0) Multi-function serial ch.8 serial data output pin (0) I ² C bus ch.8 serial data I/O pin Base timer ch.2 TIOA output pin (0) |
| 13 | P011 SIN18_1 TIOA2_1 | - - - | P | General-purpose I/O port Multi-function serial ch.18 serial data input pin (1) Base timer ch.2 TIOA output pin (1) |
| 14 | P012 SCK8_0 SCL8_0 TIOA3_0 OUT5_0 | - - - - - | P | General-purpose I/O port Multi-function serial ch.8 clock I/O pin (0) I ² C bus ch.8 serial clock I/O pin Base timer ch.3 TIOA I/O pin (0) Output compare ch.5 output pin (0) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|--|----------------------------|------------------------|---|
| 15 | P013 SCS80_0 TIOA4_0 OUT6_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.8 chip select 0 I/O pin (0) Base timer ch.4 TIOA output pin (0) Output compare ch.6 output pin (0) |
| 16 | P014 SOT18_1 TIOA3_1 | - - - | P | General-purpose I/O port Multi-function serial ch.18 serial data output pin (1) Base timer ch.3 TIOA output pin (1) |
| 17 | P015 SCS81_0 TIOA5_0 OUT7_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.8 chip select 1 output pin (0) Base timer ch.5 TIOA I/O pin (0) Output compare ch.7 output pin (0) |
| 18 | P016 SCS82_0 TIOA6_0 OUT8_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.8 chip select 2 output pin (0) Base timer ch.6 TIOA output pin (0) Output compare ch.8 output pin (0) |
| 19 | P017 SCS83_0 TIOA7_0 OUT9_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.8 chip select 3 output pin (0) Base timer ch.7 TIOA I/O pin (0) Output compare ch.9 output pin (0) |
| 20 | P018 TIOA8_0 OUT10_0 | - - - | P | General-purpose I/O port Base timer ch.8 TIOA output pin (0) Output compare ch.10 output pin (0) |
| 21 | P019 OUT11_0 TIOB0_0 TEXT0_0 | - - - - | P | General-purpose I/O port Output compare ch.11 output pin (0) Base timer ch.0 TIOB input pin (0) Free-run timer 0 clock input pin (0) |
| 22 | P020 SOT0_0 SDA0_0 TIOB1_0 TEXT1_0 | - - - - - | P | General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I ² C bus ch.0 serial data I/O pin Base timer ch.1 TIOB input pin (0) Free-run timer 1 clock input pin (0) |
| 23 | P021 SCK4_1 TIOB2_0 SCK0_0 SCL0_0 | - - - - - | P | General-purpose I/O port Multi-function serial ch.4 clock I/O pin (1) Base timer ch.2 TIOB input pin (0) Multi-function serial ch.0 clock I/O pin (0) I ² C bus ch.0 serial clock I/O pin |
| 24 | P022 SIN0_0 TIOB3_0 INT3_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0) INT3 external interrupt input pin (0) |
| 25 | P023 SIN4_1 SCS0_0 TIOB4_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.4 serial data input pin (1) Multi-function serial ch.0 chip select I/O pin (0) Base timer ch.4 TIOB input pin (0) |
| 26 | P024 SOT4_1 TIOB5_0 | - - - | P | General-purpose I/O port Multi-function serial ch.4 serial data output pin (1) Base timer ch.5 TIOB input pin (0) |
| 27 | P025 SCS40_1 | - - | P | General-purpose I/O port Multi-function serial ch.4 chip select 0 I/O pin (1) |
| 28 | P026 SCS41_1 | - - | P | General-purpose I/O port Multi-function serial ch.4 chip select 1 output pin (1) |
| 29 | P027 SCS42_1 TIOA4_1 TIOB6_0 INT1_1 TEXT0_1 | - - - - - - | P | General-purpose I/O port Multi-function serial ch.4 chip select 2 output pin (1) Base timer ch.4 TIOA output pin (1) Base timer ch.6 TIOB input pin (0) INT1 external interrupt input pin (1) Free-run timer 0 clock input pin (1) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|--|---------------------------------|------------------------|--|
| 30 | P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1 | - - - - - | P | General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1) |
| 31 | P029 SOT1_0 SDA1_0 AN0 OUT1_1 | - - - - - | A | General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I ² C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1) |
| 32 | P030 SCS43_1 OUT2_1 | - - - | P | General-purpose I/O port Multi-function serial chip ch.4 select 3 output pin (1) Output compare ch.2 output pin (1) |
| 33 | P031 SCS1_0 AN1 OUT3_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.1 chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1) |
| 34 | P100 SCK1_0 SCL1_0 AN2 OUT4_1 | - - - - - | A | General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I ² C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1) |
| 35 | P101 AN3 OUT5_1 | - - - | A | General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1) |
| 36 | P102 AN4 | - - | A | General-purpose I/O port ADC analog 4 input pin |
| 37 | P103 SIN17_0 AN5 OUT6_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.17 serial data input pin (0) ADC analog 5 input pin Output compare ch.6 output pin (1) |
| 38 | P104 SOT17_0 SDA17_0 | - - - | P | General-purpose I/O port Multi-function serial ch.17 serial data output pin (0) I ² C bus ch.17 serial data I/O pin |
| 39 | P105 SCK17_0 SCL17_0 TIOA9_0 OUT7_1 | - - - - - | P | General-purpose I/O port Multi-function serial ch.17 clock I/O pin (0) I ² C bus ch.17 serial clock I/O pin Base timer ch.9 TIOA output pin (0) Output compare ch.7 output pin (1) |
| 40 | P106 TX1_2 SCS170_0 OUT8_1 | - - - - | P | General-purpose I/O port CAN transmission data 1 output pin (2) Multi-function serial ch.17 chip select 0 I/O pin (0) Output compare ch.8 output pin (1) |
| 41 | P107 RX1_2 SIN19_0 TIOA10_0 INT2_1 OUT9_1 | - - - - - - | P | General-purpose I/O port CAN reception data 1 input pin (2) Multi-function serial ch.19 serial data input pin (0) Base timer ch.10 TIOA output pin (0) INT2 external interrupt input pin (1) Output compare ch.9 output pin (1) |
| 42 | P108 SOT19_0 SDA19_0 AN6 TIOA11_0 INT3_1 OUT10_1 | - - - - - - - | A | General-purpose I/O port Multi-function serial ch.19 serial data output pin (0) I ² C bus ch.19 serial data I/O pin ADC analog 6 input pin Base timer ch.11 TIOA output pin (0) INT3 external interrupt input pin (1) Output compare ch.10 output pin (1) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|----------|----------|------------------------|---|
| 43 | P109 | - | P | General-purpose I/O port |
| | SIN19_1 | - | | Multi-function serial ch.19 serial data input pin (1) |
| | SCK19_0 | - | | Multi-function serial ch.19 clock I/O pin (0) |
| | SCL19_0 | - | | I ² C bus ch.19 serial clock I/O pin |
| | TIOA12_0 | - | | Base timer ch.12 TIOA output pin (0) |
| | OUT11_1 | - | | Output compare ch.11 output pin (1) |
| 47 | P110 | - | A | General-purpose I/O port |
| | SCS190_0 | - | | Multi-function serial ch.19 chip select 0 I/O pin (0) |
| | AN7 | - | | ADC analog 7 input pin |
| 48 | P111 | - | A | General-purpose I/O port |
| | SIN18_0 | - | | Multi-function serial ch.18 serial data input pin (0) |
| | AN8 | - | | ADC analog 8 input pin |
| 49 | P112 | - | A | General-purpose I/O port |
| | SOT18_0 | - | | Multi-function serial ch.18 serial data output pin (0) |
| | SDA18_0 | - | | I ² C bus ch.18 serial data I/O pin |
| | AN9 | - | | ADC analog 9 input pin |
| | TIOA13_0 | - | | Base timer ch.13 TIOA output pin (0) |
| 50 | P113 | - | P | General-purpose I/O port |
| | SOT19_1 | - | | Multi-function serial ch.19 serial data output pin (1) |
| | SCK18_0 | - | | Multi-function serial ch.18 clock I/O pin (0) |
| | SCL18_0 | - | | I ² C bus ch.18 serial clock I/O pin |
| | TIOA5_1 | - | | Base timer ch.5 TIOA output pin (1) |
| 51 | P114 | - | A | General-purpose I/O port |
| | SCS180_0 | - | | Multi-function serial ch.18 chip select 0 I/O pin (0) |
| | AN10 | - | | ADC analog 10 input pin |
| | TIOA6_1 | - | | Base timer ch.6 TIOA output pin (1) |
| 55 | P115 | - | P | General-purpose I/O port |
| 56 | P116 | - | A | General-purpose I/O port |
| | AN11 | - | | ADC analog 11 input pin |
| 57 | P117 | - | A | General-purpose I/O port |
| | AN12 | - | | ADC analog 12 input pin |
| | INT4_1 | - | | INT4 external interrupt input pin (1) |
| 58 | P118 | - | A | General-purpose I/O port |
| | AN13 | - | | ADC analog 13 input pin |
| | INT5_1 | - | | INT5 external interrupt input pin (1) |
| 59 | P119 | - | A | General-purpose I/O port |
| | SCS60_0 | - | | Multi-function serial ch.6 chip select 0 I/O pin (0) |
| | AN14 | - | | ADC analog 14 input pin |
| 60 | P120 | - | A | General-purpose I/O port |
| | SCS61_0 | - | | Multi-function serial ch.6 chip select 1 output pin (0) |
| | AN15 | - | | ADC analog 15 input pin |
| 61 | P121 | - | A | General-purpose I/O port |
| | SCS160_0 | - | | Multi-function serial ch.16 chip select 0 I/O pin (0) |
| | AN16 | - | | ADC analog 16 input pin |
| | TIOA14_0 | - | | Base timer ch.14 TIOA output pin (0) |
| 62 | P122 | - | A | General-purpose I/O port |
| | SCS62_0 | - | | Multi-function serial ch.6 chip select 2 output pin (0) |
| | AN17 | - | | ADC analog 17 input pin |
| | TIOA11_1 | - | | Base timer ch.11 TIOA output pin (1) |
| 63 | P123 | - | A | General-purpose I/O port |
| | SCS63_0 | - | | Multi-function serial ch.6 chip select 3 output pin (0) |
| | AN18 | - | | ADC analog 18 input pin |
| | TIOA12_1 | - | | Base timer ch.12 TIOA output pin (1) |
| 64 | P124 | - | P | General-purpose I/O port |
| | SIN16_0 | - | | Multi-function serial ch.16 serial data input pin (0) |
| | TIOA15_0 | - | | Base timer ch.15 TIOA output pin (0) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|---|-----------------------|------------------------|---|
| 65 | P125 SOT16_0 SDA16_0 TIOA16_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.16 serial data output pin (0) I ² C bus ch.16 serial data I/O pin Base timer ch.16 TIOA output pin (0) |
| 66 | P126 SCK16_0 SCL16_0 AN19 | - - - - | A | General-purpose I/O port Multi-function serial ch.16 clock I/O pin (0) I ² C bus ch.16 serial clock I/O pin ADC analog 19 input pin |
| 67 | P127 SCS203_0 AN20 TEXT1_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.20 chip select 3 output pin (0) ADC analog 20 input pin Free-run timer 1 clock input pin (1) |
| 68 | P128 SCS200_0 AN21 TEXT2_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.20 chip select 0 I/O pin (0) ADC analog 21 input pin Free-run timer 2 clock input pin (1) |
| 69 | P129 IN6_1 SCS201_0 AN22 | - - - - | A | General-purpose I/O port Input capture ch.6 input pin (1) Multi-function serial ch.20 chip select 1 output pin (0) ADC analog 22 input pin |
| 70 | P130 IN7_1 SIN6_0 AN23 INT5_0 | - - - - - | A | General-purpose I/O port Input capture ch.7 input pin (1) Multi-function serial ch.6 serial data input pin (0) ADC analog 23 input pin INT5 external interrupt input pin (0) |
| 71 | P131 IN8_1 SOT6_0 SDA6_0 AN24 | - - - - - | A | General-purpose I/O port Input capture ch.8 input pin (1) Multi-function serial ch.6 serial data output pin (0) I ² C bus ch.6 serial data I/O pin ADC analog 24 input pin |
| 72 | P200 SCS202_0 AN25 TIOA17_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.20 chip select 2 output pin (0) ADC analog 25 input pin Base timer ch.17 TIOA output pin (0) |
| 73 | P201 SIN20_0 AN26 TIOA18_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.20 serial data input pin (0) ADC analog 26 input pin Base timer ch.18 TIOA output pin (0) |
| 74 | P202 IN9_1 SCK6_0 SCL6_0 INT6_1 | - - - - - | P | General-purpose I/O port Input capture ch.9 input pin (1) Multi-function serial ch.6 clock I/O pin (0) I ² C bus ch.6 serial clock I/O pin INT6 external interrupt input pin (1) |
| 75 | P203 IN10_1 | - - | P | General-purpose I/O port Input capture ch.10 input pin (1) |
| 76 | P204 IN11_1 SOT20_0 SDA20_0 AN27 | - - - - - | A | General-purpose I/O port Input capture ch.11 input pin (1) Multi-function serial ch.20 serial data output pin (0) I ² C bus ch.20 serial data I/O pin ADC analog 27 input pin |
| 77 | P205 SCK20_0 SCL20_0 AN28 TEXT3_1 | - - - - - | A | General-purpose I/O port Multi-function serial ch.20 clock I/O pin (0) I ² C bus ch.20 serial clock I/O pin ADC analog 28 input pin Free-run timer 3 clock input pin (1) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|---|----------------------------|------------------------|--|
| 78 | P206 SCS43_0 AN29 TEXT4_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.4 chip select 3 output pin (0) ADC analog 29 input pin Free-run timer 4 clock input pin (1) |
| 79 | P207 SCK4_0 SCL4_0 AN30 INT7_1 TEXT5_1 | - - - - - - | A | General-purpose I/O port Multi-function serial ch.4 clock I/O pin (0) I ² C bus ch.4 serial clock I/O pin ADC analog 30 input pin INT7 external interrupt input pin (1) Free-run timer 5 clock input pin (1) |
| 80 | P208 SCS42_0 AN31 TIOA19_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.4 chip select 2 output pin (0) ADC analog 31 input pin Base timer ch.19 TIOA output pin (0) |
| 81 | P209 SOT4_0 SDA4_0 AN32 TIOA20_0 | - - - - - | A | General-purpose I/O port Multi-function serial ch.4 serial data output pin (0) I ² C bus ch.4 serial data I/O pin ADC analog 32 input pin Base timer ch.20 TIOA output pin (0) |
| 82 | P210 IN0_2 SIN4_0 AN33 TIOA21_0 INT6_0 | - - - - - - | A | General-purpose I/O port Input capture ch.0 input pin (2) Multi-function serial ch.4 serial data input pin (0) ADC analog 33 input pin Base timer ch.21 TIOA output pin (0) INT6 external interrupt input pin (0) |
| 83 | P211 IN1_2 SCS40_0 AN34 TIOA22_0 | - - - - - | A | General-purpose I/O port Input capture ch.1 input pin (2) Multi-function serial ch.4 chip select 0 I/O pin (0) ADC analog 34 input pin Base timer ch.22 TIOA output pin (0) |
| 84 | P212 IN2_2 SCS50_1 SCS41_0 AN35 TIOA13_1 | - - - - - - | A | General-purpose I/O port Input capture ch.2 input pin (2) Multi-function serial ch.5 chip select 0 I/O pin (1) Multi-function serial ch.4 chip select 1 output pin (0) ADC analog 35 input pin Base timer ch.13 TIOA output pin (1) |
| 85 | P213 IN3_2 SIN5_1 TIOA14_1 INT8_1 | - - - - - | P | General-purpose I/O port Input capture ch.3 input pin (2) Multi-function serial ch.5 serial data input pin (1) Base timer ch.14 TIOA output pin (1) INT8 external interrupt input pin (1) |
| 86 | P214 IN4_2 SOT5_1 TIOA15_1 | - - - - | P | General-purpose I/O port Input capture ch.4 input pin (2) Multi-function serial ch.5 serial data output pin (1) Base timer ch.15 TIOA output pin (1) |
| 87 | P215 IN5_2 SCK5_1 TIOA16_1 INT9_1 | - - - - - | P | General-purpose I/O port Input capture ch.5 input pin (2) Multi-function serial ch.5 clock I/O pin (1) Base timer ch.16 TIOA output pin (1) INT9 external interrupt input pin (1) |
| 90 | P216 SIN15_0 | - - | P | General-purpose I/O port Multi-function serial ch.15 serial data input pin (0) |
| 91 | P217 SOT15_0 SDA15_0 | - - - | P | General-purpose I/O port Multi-function serial ch.15 serial data output pin (0) I ² C bus ch.15 serial data I/O pin |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|--|---------------------------------|------------------------|--|
| 92 | P218 SCK15_0 SCL15_0 AN36 TEXT2_0 | - - - - - | A | General-purpose I/O port Multi-function serial ch.15 clock I/O pin (0) I ² C bus ch.15 serial clock I/O pin ADC analog 36 input pin Free-run timer 2 clock input pin (0) |
| 93 | P219 SCS150_0 AN37 TEXT3_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.15 chip select 0 I/O pin (0) ADC analog 37 input pin Free-run timer 3 clock input pin (0) |
| 94 | P220 IN6_2 SCS53_0 AN38 | - - - - | A | General-purpose I/O port Input capture ch.6 input pin (2) Multi-function serial ch.5 chip select 3 output pin (0) ADC analog 38 input pin |
| 95 | P221 SCS52_0 | - - | P | General-purpose I/O port Multi-function serial ch.5 chip select 2 output pin (0) |
| 96 | P222 IN7_2 SIN5_0 AN39 INT7_0 | - - - - - | A | General-purpose I/O port Input capture ch.7 input pin (2) Multi-function serial ch.5 serial data input pin (0) ADC analog 39 input pin INT7 external interrupt input pin (0) |
| 97 | P223 IN8_2 PWU_AN0 SCS51_0 AN40 | - - - - - | A | General-purpose I/O port Input capture ch.8 input pin (2) Partial wakeup ADC analog 0 input pin Multi-function serial ch.5 chip select 1 output pin (0) ADC analog 40 input pin |
| 98 | P224 IN9_2 PWU_AN1 TX0_2 SCS50_0 AN41 | - - - - - - | A | General-purpose I/O port Input capture ch.9 input pin (2) Partial wakeup ADC analog 1 input pin CAN transmission data 0 output pin (2) Multi-function serial ch.5 chip select 0 I/O pin (0) ADC analog 41 input pin |
| 99 | P225 IN10_2 PWU_AN2 RX0_2 SOT5_0 SDA5_0 AN42 INT0_0 | - - - - - - - | A | General-purpose I/O port Input capture ch.10 input pin (2) Partial wakeup ADC analog 2 input pin CAN reception data 0 input pin (2) Multi-function serial ch.5 serial data output pin (0) I ² C bus ch.5 serial data I/O pin ADC analog 42 input pin INT0 external interrupt input pin (0) |
| 100 | P226 IN11_2 PWU_AN3 SCK5_0 SCL5_0 AN43 TIOA17_1 | - - - - - - | A | General-purpose I/O port Input capture ch.11 input pin (2) Partial wakeup ADC analog 3 input pin Multi-function serial ch.5 clock I/O pin (0) I ² C bus ch.5 serial clock I/O pin ADC analog 43 input pin Base timer ch.17 TIOA output pin (1) |
| 104 | P227 PWU_AN4 SCK10_0 SCL10_0 AN44 TIOA23_0 | - - - - - - | A | General-purpose I/O port Partial wakeup ADC analog 4 input pin Multi-function serial ch.10 clock I/O pin (0) I ² C bus ch.10 serial clock I/O pin ADC analog 44 input pin Base timer ch.23 TIOA output pin (0) |
| 105 | P228 PWU_AN5 TX0_1 SOT10_0 SDA10_0 AN45 TIOA24_0 | - - - - - - | A | General-purpose I/O port Partial wakeup ADC analog 5 input pin CAN transmission data 0 output pin (1) Multi-function serial ch.10 serial data output pin (0) I ² C bus ch.10 serial data I/O pin ADC analog 45 input pin Base timer ch.24 TIOA output pin (0) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|---|---------------------------------|------------------------|--|
| 106 | P229 PWU_AN6 RX0_1 SIN10_0 AN46 TIOA25_0 INT8_0 OUT0_0 | - - - - - - - | A | General-purpose I/O port Partial wakeup ADC analog 6 input pin CAN reception data 0 input pin (1) Multi-function serial ch.10 serial data input pin (0) ADC analog 46 input pin Base timer ch.25 TIOA output pin (0) INT8 external interrupt input pin (0) Output compare ch.0 output pin (0) |
| 107 | P230 PWU_AN7 SCS103_0 AN47 TIOA26_0 OUT1_0 | - - - - - | A | General-purpose I/O port Partial wakeup ADC analog 7 input pin Multi-function serial ch.10 chip select 3 output pin (0) ADC analog 47 input pin Base timer ch.26 TIOA output pin (0) Output compare ch.1 output pin (0) |
| 108 | P231 SCS102_0 AN48 TIOA27_0 OUT2_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.10 chip select 2 output pin (0) ADC analog 48 input pin Base timer ch.27 TIOA output pin (0) Output compare ch.2 output pin (0) |
| 109 | P300 SCS101_0 AN49 TIOA28_0 OUT3_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.10 chip select 1 output pin (0) ADC analog 49 input pin Base timer ch.28 TIOA output pin (0) Output compare ch.3 output pin (0) |
| 110 | P301 SCS100_0 AN50 TIOA18_1 OUT4_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.10 chip select 0 I/O pin (0) ADC analog 50 input pin Base timer ch.18 TIOA output pin (1) Output compare ch.4 output pin (0) |
| 111 | P302 SIN14_0 AN51 TIOA19_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.14 serial data input pin (0) ADC analog 51 input pin Base timer ch.19 TIOA output pin (1) |
| 112 | P303 SOT14_0 SDA14_0 | - - - | P | General-purpose I/O port Multi-function serial ch.14 serial data output pin (0) I ² C bus ch.14 serial data I/O pin |
| 113 | P304 SCK14_0 SCL14_0 AN52 TIOA20_1 TEXT4_0 | - - - - - | A | General-purpose I/O port Multi-function serial ch.14 clock I/O pin (0) I ² C bus ch.14 serial clock I/O pin ADC analog 52 input pin Base timer ch.20 TIOA output pin (1) Free-run timer 4 clock input pin (0) |
| 114 | P305 SCS140_0 AN53 TIOA29_0 TEXT5_0 | - - - - | A | General-purpose I/O port Multi-function serial ch.14 chip select 0 I/O pin (0) ADC analog 53 input pin Base timer ch.29 TIOA output pin (0) Free-run timer 5 clock input pin (0) |
| 115 | NMIX | N | F | Non-maskable interrupt input pin |
| 116 | P306 TX0_0 SCS73_0 AN54 | - - - - | A | General-purpose I/O port CAN transmission data 0 output pin (0) Multi-function serial ch.7 chip select 3 output pin (0) ADC analog 54 input pin |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|---|----------------------------|------------------------|---|
| 117 | P307 RX0_0 SCS72_0 AN55 INT1_0 | - - - - - | A | General-purpose I/O port CAN reception data 0 input pin (0) Multi-function serial ch.7 chip select 2 output pin (0) ADC analog 55 input pin INT1 external interrupt input pin (0) |
| 118 | P308 IN0_1 SCK13_0 SCL13_0 AN56 TIOA28_1 | - - - - - - | A | General-purpose I/O port Input capture ch.0 input pin (1) Multi-function serial ch.13 clock I/O pin (0) I ² C bus ch.13 serial clock I/O pin ADC analog 56 input pin Base timer ch.28 TIOA output pin (1) |
| 119 | P309 IN1_1 SCS130_0 AN57 TIOA29_1 | - - - - - | A | General-purpose I/O port Input capture ch.1 input pin (1) Multi-function serial ch.13 chip select 0 I/O pin (0) ADC analog 57 input pin Base timer ch.29 TIOA output pin (1) |
| 120 | P310 SIN13_0 INT15_0 | - - - | P | General-purpose I/O port Multi-function serial ch.13 serial data input pin (0) INT15 external interrupt input pin (0) |
| 121 | P311 SOT13_0 SDA13_0 | - - - | P | General-purpose I/O port Multi-function serial ch.13 serial data output pin (0) I ² C bus ch.13 serial data I/O pin |
| 122 | P312 IN2_1 SCS71_0 AN58 | - - - - | A | General-purpose I/O port Input capture ch.2 input pin (1) Multi-function serial ch.7 chip select 1 output pin (0) ADC analog 58 input pin |
| 123 | P313 IN3_1 SOT7_0 SDA7_0 AN59 INT10_1 | - - - - - - | A | General-purpose I/O port Input capture ch.3 input pin (1) Multi-function serial ch.7 serial data output pin (0) I ² C bus ch.7 serial data I/O pin ADC analog 59 input pin INT10 external interrupt input pin (1) |
| 124 | P314 IN4_1 SCK7_0 SCL7_0 AN60 TIOA7_1 | - - - - - - | A | General-purpose I/O port Input capture ch.4 input pin (1) Multi-function serial ch.7 clock I/O pin (0) I ² C bus ch.7 serial clock I/O pin ADC analog 60 input pin Base timer ch.7 TIOA output pin (1) |
| 125 | P315 IN5_1 SCS70_0 AN61 TIOA8_1 | - - - - - | A | General-purpose I/O port Input capture ch.5 input pin (1) Multi-function serial ch.7 chip select 0 I/O pin (0) ADC analog 61 input pin Base timer ch.8 TIOA output pin (1) |
| 126 | P316 TIOA21_1 | - - | P | General-purpose I/O port Base timer ch.21 TIOA output pin (1) |
| 127 | P317 TX1_1 AN62 TIOA9_1 INT11_1 | - - - - - | A | General-purpose I/O port CAN transmission data 1 output pin (1) ADC analog 62 input pin Base timer ch.9 TIOA output pin (1) INT11 external interrupt input pin (1) |
| 128 | P318 RX1_1 TIOA10_1 INT9_0 | - - - - | P | General-purpose I/O port CAN reception data 1 input pin (1) Base timer ch.10 TIOA output pin (1) INT9 external interrupt input pin (0) |
| 129 | P319 SIN7_0 AN63 INT12_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.7 serial data input pin (0) ADC analog 63 input pin INT12 external interrupt input pin (1) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|--|----------------------------|------------------------|--|
| 130 | P320 PWUTRG | - - | P | General-purpose I/O port Partial wakeup trigger output pin |
| 131 | P321 | - | D | General-purpose output port |
| 134 | TRST P322 | N - | J | JTAG test reset input pin General-purpose output port |
| 135 | TDO P323 | - - | I | JTAG test data output pin General-purpose output port |
| 136 | TDI P324 | - - | D | JTAG test data input pin General-purpose output port |
| 137 | TMS | - | E | JTAG test mode state input pin |
| 138 | TCK | - | E | JTAG test clock input pin |
| 139 | P325 SIN21_0 INT10_0 | - - - | P | General-purpose I/O port Multi-function serial ch.21 serial data input pin (0) INT10 external interrupt input pin (0) |
| 140 | P326 SOT21_0 SDA21_0 | - - - | P | General-purpose I/O port Multi-function serial ch.21 serial data output pin (0) I ² C bus ch.21 serial data I/O pin |
| 141 | P327 SCK6_1 SCK21_0 SCL21_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.6 clock I/O pin (1) Multi-function serial ch.21 clock I/O pin (0) I ² C bus ch.21 serial clock I/O pin |
| 142 | P328 SOT6_1 SCS210_0 | - - - | P | General-purpose I/O port Multi-function serial ch.6 serial data output pin (1) Multi-function serial ch.21 chip select 0 I/O pin (0) |
| 143 | P329 SIN6_1 | - - | P | General-purpose I/O port Multi-function serial ch.6 serial data input pin (1) |
| 144 | P330 | - | P | General-purpose I/O port |
| 145 | MD | - | C | Mode pin |
| 146 | X0 | - | G | Main clock oscillation input pin |
| 147 | X1 | - | G | Main clock oscillation output pin |
| 149 | P331 SCS60_1 | - - | P | General-purpose I/O port Multi-function serial ch.6 chip select 0 I/O pin (1) |
| 150 | P400 SCS61_1 | - - | P | General-purpose I/O port Multi-function serial ch.6 chip select 1 output pin (1) |
| 151 | RSTX | N | F | External reset input pin |
| 155 | P401 IN0_0 TX1_0 SCS62_1 | - - - - | Q | General-purpose I/O port Input capture ch.0 input pin (0) CAN transmission data 1 output pin (0) Multi-function serial ch.6 chip select 2 output pin (1) |
| 156 | P402 IN1_0 RX1_0 SCS63_1 SCS90_0 INT2_0 | - - - - - - | Q | General-purpose I/O port Input capture ch.1 input pin (0) CAN reception data 1 input pin (0) Multi-function serial ch.6 chip select 3 output pin (1) Multi-function serial ch.9 chip select 0 I/O pin (0) INT2 external interrupt input pin (0) |
| 157 | P403 IN2_0 TRACEDATA0 | - - - | Q | General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin |
| 158 | P404 IN3_0 TRACEDATA1 | - - - | Q | General-purpose I/O port Input capture ch.3 input pin (0) Trace data 1 output pin |

| Pin No. S6J311xJAC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|--|----------------------------|------------------------|--|
| 159 | P405 IN4_0 SIN9_0 INT11_0 TRACEDATA2 | - - - - - | Q | General-purpose I/O port Input capture ch.4 input pin (0) Multi-function serial ch.9 serial data input pin (0) INT11 external interrupt input pin (0) Trace data 2 output pin |
| 160 | P406 SOT9_0 SDA9_0 TRACEDATA3 | - - - - | Q | General-purpose I/O port Multi-function serial ch.9 serial data output pin (0) I ² C bus ch.9 serial data I/O pin Trace data 3 output pin |
| 161 | P407 SCK7_1 SCK9_0 SCL9_0 TRACEDATA4 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.7 clock I/O pin (1) Multi-function serial ch.9 clock I/O pin (0) I ² C bus ch.9 serial clock I/O pin Trace data 4 output pin |
| 162 | P408 SIN2_0 INT12_0 TRACEDATA5 | - - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data input pin (0) INT12 external interrupt input pin (0) Trace data 5 output pin |
| 163 | P409 SOT2_0 SDA2_0 TIOA24_1 TRACEDATA6 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data output pin (0) I ² C bus ch.2 serial data I/O pin Base timer ch.24 TIOA output pin (1) Trace data 6 output pin |
| 164 | P410 SCS70_1 | - - | Q | General-purpose I/O port Multi-function serial ch.7 chip select 0 I/O pin (1) |
| 165 | P411 SCS71_1 SCK2_0 SCL2_0 INT13_1 TRACEDATA7 | - - - - - - | Q | General-purpose I/O port Multi-function serial ch.7 chip select 1 output pin (1) Multi-function serial ch.2 clock I/O pin (0) I ² C bus ch.2 serial clock I/O pin INT13 external interrupt input pin (1) Trace data 7 output pin |
| 166 | P412 SCS72_1 TIOA25_1 | - - - | Q | General-purpose I/O port Multi-function serial ch.7 chip select 2 output pin (1) Base timer ch.25 TIOA output pin (1) |
| 167 | P413 SCS73_1 SCS20_0 INT14_1 | - - - - | Q | General-purpose I/O port Multi-function serial ch.7 chip select 3 output pin (1) Multi-function serial ch.2 chip select 0 I/O pin (0) INT14 external interrupt input pin (1) |
| 168 | P414 SCS21_0 SIN11_0 | - - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 1 output pin (0) Multi-function serial ch.11 serial data input pin (0) |
| 169 | P415 SOT11_0 SDA11_0 TIOA26_1 INT13_0 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.11 serial data output pin (0) I ² C bus ch.11 serial data I/O pin Base timer ch.26 TIOA output pin (1) INT13 external interrupt input pin (0) |
| 170 | P416 IN5_0 SIN7_1 SCK11_0 SCL11_0 TIOA22_1 | - - - - - - | Q | General-purpose I/O port Input capture ch.5 input pin (0) Multi-function serial ch.7 serial data input pin (1) Multi-function serial ch.11 clock I/O pin (0) I ² C bus ch.11 serial clock I/O pin Base timer ch.22 TIOA output pin (1) |
| 171 | P417 SOT7_1 SCS110_0 TIOA23_1 INT15_1 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.7 serial data output pin (1) Multi-function serial ch.11 chip select 0 I/O pin (0) Base timer ch.23 TIOA output pin (1) INT15 external interrupt input pin (1) |

| Pin No. S6J311xJA C | Pin Name | Polarity | I/O Circuit Type | Function |
|---------------------------|---|-----------------------|------------------------|---|
| 172 | P418 SCS22_0 SIN12_0 INT14_0 | - - - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 2 output pin (0) Multi-function serial ch.12 serial data input pin (0) INT14 external interrupt input pin (0) |
| 173 | P419 SCS23_0 SOT12_0 SDA12_0 TIOA27_1 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 3 output pin (0) Multi-function serial ch.12 serial data output pin (0) I ² C bus ch.12 serial data I/O pin Base timer ch.27 TIOA output pin (1) |
| 174 | P420 SCK2_1 SCK12_0 SCL12_0 TRACECLK | - - - - - | Q | General-purpose I/O port Multi-function serial ch.2 clock I/O pin (1) Multi-function serial ch.12 clock I/O pin (0) I ² C bus ch.12 serial clock I/O pin Trace clock |
| 175 | P421 SIN2_1 SCS120_0 TRACECTL | - - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data input pin (1) Multi-function serial ch.12 chip select 0 I/O pin (0) Trace control |
| 52 | AVCC0 | - | - | Analog power supply pin for AD converter unit 0 |
| 103 | AVCC1 | - | - | Analog power supply pin for AD converter unit 1 |
| 53 | AVRH0 | - | - | Upper-limit reference voltage pin for AD converter unit 0 |
| 102 | AVRH1 | - | - | Upper-limit reference voltage pin for AD converter unit 1 |
| 54 | AVSS0 AVRL0 | - - | - | GND pin for AD converter unit 0 Lower-limit reference voltage pin for AD converter unit 0 |
| 101 | AVSS1 AVRL1 | - - | - | GND pin for AD converter unit 1 Lower-limit reference voltage pin for AD converter unit 1 |
| 46 | C | - | - | External capacity connection output pin |
| 154 | | | | |
| 44 | VCC | - | - | Power supply pin |
| 88 | | | | |
| 133 | | | | |
| 152 | | | | |
| 176 | | | | |
| 1 | VSS | - | - | GND |
| 45 | | | | |
| 89 | | | | |
| 132 | | | | |
| 148 | | | | |
| 153 | | | | |

Table 3-2 S6J311xHzC* Pin Functions

* x: E/D, z: A/B

| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|---------------------------------------|------------------|------------------------|--|
| 2 | P000 SOT2_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 serial data output pin (1) |
| 3 | P001 SCS20_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 chip select 0 I/O pin (1) |
| 4 | P003 SCS22_1 | - - | P | General-purpose I/O port Multi-function serial ch.2 chip select 2 output pin (1) |
| 5 | P005 IN6_0 SIN3_0 | - - - | P | General-purpose I/O port Input capture ch.6 input pin (0) Multi-function serial ch.3 serial data input pin (0) |
| 6 | P006 IN7_0 SOT3_0 SDA3_0 | - - - - | P | General-purpose I/O port Input capture ch.7 input pin (0) Multi-function serial ch.3 serial data output pin (0) I ² C bus ch.3 serial data I/O pin |
| 7 | P007 IN8_0 SCK3_0 SCL3_0 | - - - - | P | General-purpose I/O port Input capture ch.8 input pin (0) Multi-function serial ch.3 clock I/O pin (0) I ² C bus ch.3 serial clock I/O pin |
| 8 | P008 IN9_0 SCS30_0 TIOA0_0 | - - - - | P | General-purpose I/O port Input capture ch.9 input pin (0) Multi-function serial ch.3 chip select 0 I/O pin (0) Base timer ch.0 TIOA output pin (0) |
| 9 | P009 IN10_0 TIOA1_0 INT0_1 | - - - - | P | General-purpose I/O port Input capture ch.10 input pin (0) Base timer ch.1 TIOA I/O pin (0) INT0 external interrupt input pin (1) |
| 10 | P010 IN11_0 TIOA2_0 | - - - | P | General-purpose I/O port Input capture ch.11 input pin (0) Base timer ch.2 TIOA output pin (0) |
| 11 | P012 TIOA3_0 OUT5_0 | - - - | P | General-purpose I/O port Base timer ch.3 TIOA I/O pin (0) Output compare ch.5 output pin (0) |
| 12 | P013 TIOA4_0 OUT6_0 | - - - | P | General-purpose I/O port Base timer ch.4 TIOA output pin (0) Output compare ch.6 output pin (0) |
| 13 | P015 TIOA5_0 OUT7_0 | - - - | P | General-purpose I/O port Base timer ch.5 TIOA I/O pin (0) Output compare ch.7 output pin (0) |
| 14 | P016 TIOA6_0 OUT8_0 | - - - | P | General-purpose I/O port Base timer ch.6 TIOA output pin (0) Output compare ch.8 output pin (0) |
| 15 | P017 TIOA7_0 OUT9_0 | - - - | P | General-purpose I/O port Base timer ch.7 TIOA I/O pin (0) Output compare ch.9 output pin (0) |
| 16 | P018 TIOA8_0 OUT10_0 | - - - | P | General-purpose I/O port Base timer ch.8 TIOA output pin (0) Output compare ch.10 output pin (0) |
| 17 | P019 OUT11_0 TIOB0_0 TEXT0_0 | - - - - | P | General-purpose I/O port Output compare ch.11 output pin (0) Base timer ch.0 TIOB input pin (0) Free-run timer 0 clock input pin (0) |

| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|---|-----------------------|------------------------|--|
| 18 | P020 SOT0_0 SDA0_0 TIOB1_0 TEXT1_0 | - - - - - | P | General-purpose I/O port Multi-function serial ch.0 serial data output pin (0) I ² C bus ch.0 serial data I/O pin Base timer ch.1 TIOB input pin (0) Free-run timer 1 clock input pin (0) |
| 19 | P021 SCK0_0 SCL0_0 TIOB2_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.0 clock I/O pin (0) I ² C bus ch.0 serial clock I/O pin Base timer ch.2 TIOB input pin (0) |
| 20 | P022 SIN0_0 TIOB3_0 INT3_0 | - - - - | P | General-purpose I/O port Multi-function serial ch.0 serial data input pin (0) Base timer ch.3 TIOB input pin (0) INT3 external interrupt input pin (0) |
| 21 | P023 SCS0_0 TIOB4_0 | - - - | P | General-purpose I/O port Multi-function serial ch.0 chip select I/O pin (0) Base timer ch.4 TIOB input pin (0) |
| 22 | P024 TIOB5_0 | - - | P | General-purpose I/O port Base timer ch.5 TIOB input pin (0) |
| 23 | P027 TIOA4_1 TIOB6_0 INT1_1 TEXT0_1 | - - - - - | P | General-purpose I/O port Base timer ch.4 TIOA output pin (1) Base timer ch.6 TIOB input pin (0) INT1 external interrupt input pin (1) Free-run timer 0 clock input pin (1) |
| 24 | P028 SIN1_0 TIOB7_0 INT4_0 OUT0_1 | - - - - - | P | General-purpose I/O port Multi-function serial ch.1 serial data input pin (0) Base timer ch.7 TIOB input pin (0) INT4 external interrupt input pin (0) Output compare ch.0 output pin (1) |
| 25 | P029 SOT1_0 SDA1_0 AN0 OUT1_1 | - - - - - | A | General-purpose I/O port Multi-function serial ch.1 serial data output pin (0) I ² C bus ch.1 serial data I/O pin ADC analog 0 input pin Output compare ch.1 output pin (1) |
| 26 | P030 OUT2_1 | - - | P | General-purpose I/O port Output compare ch.2 output pin (1) |
| 27 | P031 SCS1_0 AN1 OUT3_1 | - - - - | A | General-purpose I/O port Multi-function serial ch.1 chip select I/O pin (0) ADC analog 1 input pin Output compare ch.3 output pin (1) |
| 28 | P100 SCK1_0 SCL1_0 AN2 OUT4_1 | - - - - - | A | General-purpose I/O port Multi-function serial ch.1 clock I/O pin (0) I ² C bus ch.1 serial clock I/O pin ADC analog 2 input pin Output compare ch.4 output pin (1) |
| 29 | P101 AN3 OUT5_1 | - - - | A | General-purpose I/O port ADC analog 3 input pin Output compare ch.5 output pin (1) |
| 30 | P103 AN5 OUT6_1 | - - - | A | General-purpose I/O port ADC analog 5 input pin Output compare ch.6 output pin (1) |
| 31 | P105 TIOA9_0 OUT7_1 | - - - | P | General-purpose I/O port Base timer ch.9 TIOA output pin (0) Output compare ch.7 output pin (1) |
| 32 | P106 OUT8_1 | - - | P | General-purpose I/O port Output compare ch.8 output pin (1) |

| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|--|-----------------------|------------------------|--|
| 33 | P107 TIOA10_0 INT2_1 OUT9_1 | - - - - | P | General-purpose I/O port Base timer ch.10 TIOA output pin (0) INT2 external interrupt input pin (1) Output compare ch.9 output pin (1) |
| 34 | P108 AN6 TIOA11_0 INT3_1 OUT10_1 | - - - - - | A | General-purpose I/O port ADC analog 6 input pin Base timer ch.11 TIOA output pin (0) INT3 external interrupt input pin (1) Output compare ch.10 output pin (1) |
| 35 | P109 TIOA12_0 OUT11_1 | - - - | P | General-purpose I/O port Base timer ch.12 TIOA output pin (0) Output compare ch.11 output pin (1) |
| 39 | P112 AN9 TIOA13_0 | - - - | A | General-purpose I/O port ADC analog 9 input pin Base timer ch.13 TIOA output pin (0) |
| 40 | P113 TIOA5_1 | - - | P | General-purpose I/O port Base timer ch.5 TIOA output pin (1) |
| 41 | P114 AN10 TIOA6_1 | - - - | A | General-purpose I/O port ADC analog 10 input pin Base timer ch.6 TIOA output pin (1) |
| 45 | P115 | - | P | General-purpose I/O port |
| 46 | P117 AN12 INT4_1 | - - - | A | General-purpose I/O port ADC analog 12 input pin INT4 external interrupt input pin (1) |
| 47 | P118 AN13 INT5_1 | - - - | A | General-purpose I/O port ADC analog 13 input pin INT5 external interrupt input pin (1) |
| 48 | P119 AN14 | - - | A | General-purpose I/O port ADC analog 14 input pin |
| 49 | P120 AN15 | - - | A | General-purpose I/O port ADC analog 15 input pin |
| 50 | P122 AN17 TIOA11_1 | - - - | A | General-purpose I/O port ADC analog 17 input pin Base timer ch.11 TIOA output pin (1) |
| 51 | P123 AN18 TIOA12_1 | - - - | A | General-purpose I/O port ADC analog 18 input pin Base timer ch.12 TIOA output pin (1) |
| 52 | P126 AN19 | - - | A | General-purpose I/O port ADC analog 19 input pin |
| 53 | P127 AN20 TEXT1_1 | - - - | A | General-purpose I/O port ADC analog 20 input pin Free-run timer 1 clock input pin (1) |
| 54 | P128 AN21 TEXT2_1 | - - - | A | General-purpose I/O port ADC analog 21 input pin Free-run timer 2 clock input pin (1) |
| 55 | P129 IN6_1 AN22 | - - - | A | General-purpose I/O port Input capture ch.6 input pin (1) ADC analog 22 input pin |
| 56 | P130 IN7_1 AN23 INT5_0 | - - - - | A | General-purpose I/O port Input capture ch.7 input pin (1) ADC analog 23 input pin INT5 external interrupt input pin (0) |
| 57 | P131 IN8_1 AN24 | - - - | A | General-purpose I/O port Input capture ch.8 input pin (1) ADC analog 24 input pin |

| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|---|-----------------------|------------------------|--|
| 58 | P202 IN9_1 INT6_1 | - - - | P | General-purpose I/O port Input capture ch.9 input pin (1) INT6 external interrupt input pin (1) |
| 59 | P203 IN10_1 | - - | P | General-purpose I/O port Input capture ch.10 input pin (1) |
| 60 | P204 IN11_1 AN27 | - - - | A | General-purpose I/O port Input capture ch.11 input pin (1) ADC analog 27 input pin |
| 61 | P205 AN28 TEXT3_1 | - - - | A | General-purpose I/O port ADC analog 28 input pin Free-run timer 3 clock input pin (1) |
| 62 | P206 AN29 TEXT4_1 | - - - | A | General-purpose I/O port ADC analog 29 input pin Free-run timer 4 clock input pin (1) |
| 63 | P207 AN30 INT7_1 TEXT5_1 | - - - - | A | General-purpose I/O port ADC analog 30 input pin INT7 external interrupt input pin (1) Free-run timer 5 clock input pin (1) |
| 64 | P208 AN31 TIOA19_0 | - - - | A | General-purpose I/O port ADC analog 31 input pin Base timer ch.19 TIOA output pin (0) |
| 65 | P209 AN32 TIOA20_0 | - - - | A | General-purpose I/O port ADC analog 32 input pin Base timer ch.20 TIOA output pin (0) |
| 66 | P210 IN0_2 AN33 TIOA21_0 INT6_0 | - - - - - | A | General-purpose I/O port Input capture ch.0 input pin (2) ADC analog 33 input pin Base timer ch.21 TIOA output pin (0) INT6 external interrupt input pin (0) |
| 67 | P211 IN1_2 AN34 TIOA22_0 | - - - - | A | General-purpose I/O port Input capture ch.1 input pin (2) ADC analog 34 input pin Base timer ch.22 TIOA output pin (0) |
| 68 | P212 IN2_2 AN35 TIOA13_1 | - - - - | A | General-purpose I/O port Input capture ch.2 input pin (2) ADC analog 35 input pin Base timer ch.13 TIOA output pin (1) |
| 69 | P213 IN3_2 TIOA14_1 INT8_1 | - - - - | P | General-purpose I/O port Input capture ch.3 input pin (2) Base timer ch.14 TIOA output pin (1) INT8 external interrupt input pin (1) |
| 70 | P214 IN4_2 TIOA15_1 | - - - | P | General-purpose I/O port Input capture ch.4 input pin (2) Base timer ch.15 TIOA output pin (1) |
| 71 | P215 IN5_2 TIOA16_1 INT9_1 | - - - - | P | General-purpose I/O port Input capture ch.5 input pin (2) Base timer ch.16 TIOA output pin (1) INT9 external interrupt input pin (1) |
| 74 | P218 AN36 TEXT2_0 | - - - | A | General-purpose I/O port ADC analog 36 input pin Free-run timer 2 clock input pin (0) |
| 75 | P219 AN37 TEXT3_0 | - - - | A | General-purpose I/O port ADC analog 37 input pin Free-run timer 3 clock input pin (0) |
| 76 | P220 IN6_2 AN38 | - - - | A | General-purpose I/O port Input capture ch.6 input pin (2) ADC analog 38 input pin |

| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|--|----------------------------|------------------------|---|
| 77 | P222 IN7_2 AN39 INT7_0 | - - - - | A | General-purpose I/O port Input capture ch.7 input pin (2) ADC analog 39 input pin INT7 external interrupt input pin (0) |
| 78 | P223 IN8_2 AN40 PWU_AN0 | - - - | A | General-purpose I/O port Input capture ch.8 input pin (2) ADC analog 40 input pin Partial wakeup ADC analog 0 input pin |
| 79 | P224 IN9_2 TX0_2 AN41 PWU_AN1 | - - - - | A | General-purpose I/O port Input capture ch.9 input pin (2) CAN transmission data 0 output pin (2) ADC analog 41 input pin Partial wakeup ADC analog 1 input pin |
| 80 | P225 IN10_2 RX0_2 AN42 PWU_AN2 INT0_0 | - - - - - | A | General-purpose I/O port Input capture ch.10 input pin (2) CAN reception data 0 input pin (2) ADC analog 42 input pin Partial wakeup ADC analog 2 input pin INT0 external interrupt input pin (0) |
| 81 | P226 IN11_2 AN43 PWU_AN3 TIOA17_1 | - - - - | A | General-purpose I/O port Input capture ch.11 input pin (2) ADC analog 43 input pin Partial wakeup ADC analog 3 input pin Base timer ch.17 TIOA output pin (1) |
| 85 | P227 AN44 PWU_AN4 TIOA23_0 | - - - | A | General-purpose I/O port ADC analog 44 input pin Partial wakeup ADC analog 4 input pin Base timer ch.23 TIOA output pin (0) |
| 86 | P228 TX0_1 AN45 PWU_AN5 TIOA24_0 | - - - - | A | General-purpose I/O port CAN transmission data 0 output pin (1) ADC analog 45 input pin Partial wakeup ADC analog 5 input pin Base timer ch.24 TIOA output pin (0) |
| 87 | P229 RX0_1 AN46 PWU_AN6 TIOA25_0 INT8_0 OUT0_0 | - - - - - - | A | General-purpose I/O port CAN reception data 0 input pin (1) ADC analog 46 input pin Partial wakeup ADC analog 6 input pin Base timer ch.25 TIOA output pin (0) INT8 external interrupt input pin (0) Output compare ch.0 output pin (0) |
| 88 | P230 AN47 PWU_AN7 TIOA26_0 OUT1_0 | - - - - | A | General-purpose I/O port ADC analog 47 input pin Partial wakeup ADC analog 7 input pin Base timer ch.26 TIOA output pin (0) Output compare ch.1 output pin (0) |
| 89 | P231 AN48 TIOA27_0 OUT2_0 | - - - | A | General-purpose I/O port ADC analog 48 input pin Base timer ch.27 TIOA output pin (0) Output compare ch.2 output pin (0) |
| 90 | P300 AN49 TIOA28_0 OUT3_0 | - - - | A | General-purpose I/O port ADC analog 49 input pin Base timer ch.28 TIOA output pin (0) Output compare ch.3 output pin (0) |
| 91 | P301 AN50 TIOA18_1 OUT4_0 | - - - | A | General-purpose I/O port ADC analog 50 input pin Base timer ch.18 TIOA output pin (1) Output compare ch.4 output pin (0) |
| 92 | P302 AN51 TIOA19_1 | - - | A | General-purpose I/O port ADC analog 51 input pin Base timer ch.19 TIOA output pin (1) |

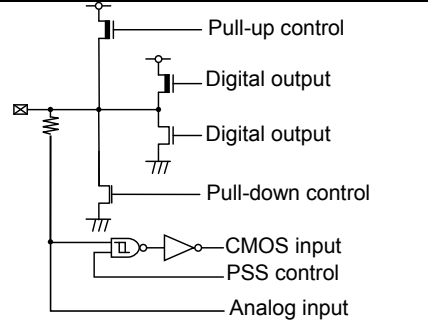
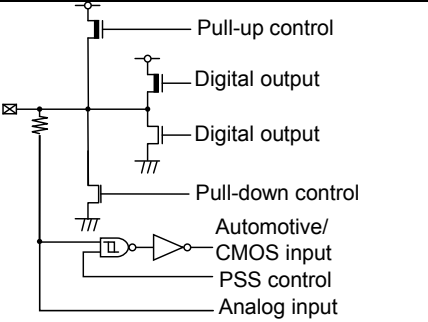
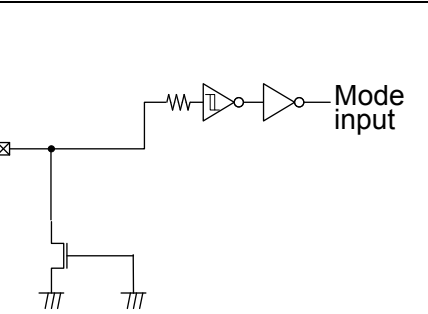
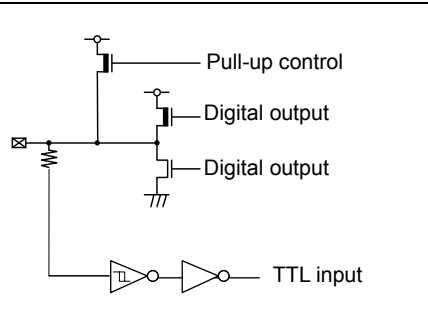
| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|-------------------------------------|------------------|------------------------|--|
| 93 | P304 AN52 TIOA20_1 TEXT4_0 | - - - - | A | General-purpose I/O port ADC analog 52 input pin Base timer ch.20 TIOA output pin (1) Free-run timer 4 clock input pin (0) |
| 94 | P305 AN53 TIOA29_0 TEXT5_0 | - - - - | A | General-purpose I/O port ADC analog 53 input pin Base timer ch.29 TIOA output pin (0) Free-run timer 5 clock input pin (0) |
| 95 | NMIX | N | F | Non-maskable interrupt input pin |
| 96 | P306 TX0_0 AN54 | - - - | A | General-purpose I/O port CAN transmission data 0 output pin (0) ADC analog 54 input pin |
| 97 | P307 RX0_0 AN55 INT1_0 | - - - - | A | General-purpose I/O port CAN reception data 0 input pin (0) ADC analog 55 input pin INT1 external interrupt input pin (0) |
| 98 | P308 IN0_1 AN56 TIOA28_1 | - - - - | A | General-purpose I/O port Input capture ch.0 input pin (1) ADC analog 56 input pin Base timer ch.28 TIOA output pin (1) |
| 99 | P309 IN1_1 AN57 TIOA29_1 | - - - - | A | General-purpose I/O port Input capture ch.1 input pin (1) ADC analog 57 input pin Base timer ch.29 TIOA output pin (1) |
| 100 | P312 IN2_1 AN58 | - - - | A | General-purpose I/O port Input capture ch.2 input pin (1) ADC analog 58 input pin |
| 101 | P313 IN3_1 AN59 INT10_1 | - - - - | A | General-purpose I/O port Input capture ch.3 input pin (1) ADC analog 59 input pin INT10 external interrupt input pin (1) |
| 102 | P314 IN4_1 AN60 TIOA7_1 | - - - - | A | General-purpose I/O port Input capture ch.4 input pin (1) ADC analog 60 input pin Base timer ch.7 TIOA output pin (1) |
| 103 | P315 IN5_1 AN61 TIOA8_1 | - - - - | A | General-purpose I/O port Input capture ch.5 input pin (1) ADC analog 61 input pin Base timer ch.8 TIOA output pin (1) |
| 104 | P317 AN62 TIOA9_1 INT11_1 | - - - - | A | General-purpose I/O port ADC analog 62 input pin Base timer ch.9 TIOA output pin (1) INT11 external interrupt input pin (1) |
| 107 | P321 PWUTRG | - - | R | General-purpose output port Partial wakeup trigger output pin |
| 110 | TRST P322 | N - | J | JTAG test reset input pin General-purpose output port |
| 111 | TDO P323 | - - | I | JTAG test data output pin General-purpose output port |
| 112 | TDI P324 | - - | D | JTAG test data input pin General-purpose output port |
| 113 | TMS | - | E | JTAG test mode state input pin |
| 114 | TCK | - | E | JTAG test clock input pin |
| 115 | P327 | - | P | General-purpose I/O port |
| 116 | P330 | - | P | General-purpose I/O port |

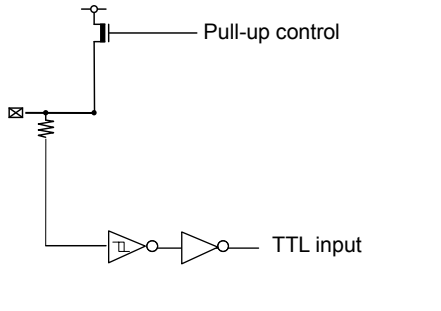
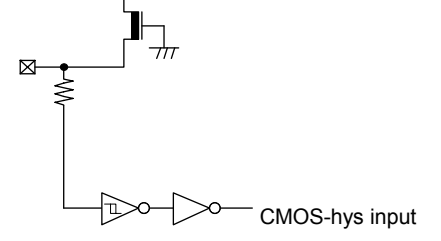
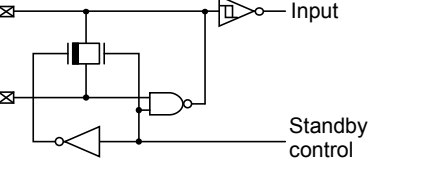
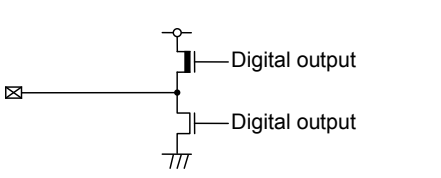
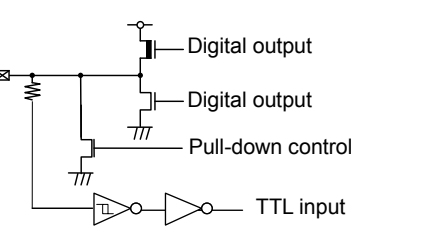
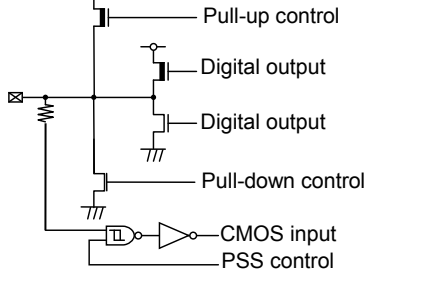
| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|--|-----------------------|------------------------|---|
| 117 | MD | - | C | Mode pin |
| 118 | X0 | - | G | Main clock oscillation input pin |
| 119 | X1 | - | G | Main clock oscillation output pin |
| 121 | P331 | - | P | General-purpose I/O port |
| 122 | P400 | - | P | General-purpose I/O port |
| 123 | RSTX | N | F | External reset input pin |
| 127 | P401 IN0_0 | - - | Q | General-purpose I/O port Input capture ch.0 input pin (0) |
| 128 | P402 IN1_0 INT2_0 | - - - | Q | General-purpose I/O port Input capture ch.1 input pin (0) INT2 external interrupt input pin (0) |
| 129 | P403 IN2_0 TRACEDATA0 | - - - | Q | General-purpose I/O port Input capture ch.2 input pin (0) Trace data 0 output pin |
| 130 | P404 IN3_0 TRACEDATA1 | - - - | Q | General-purpose I/O port Input capture ch.3 input pin (0) Trace data 1 output pin |
| 131 | P405 IN4_0 INT11_0 TRACEDATA2 | - - - - | Q | General-purpose I/O port Input capture ch.4 input pin (0) INT11 external interrupt input pin (0) Trace data 2 output pin |
| 132 | P406 TRACEDATA3 | - - | Q | General-purpose I/O port Trace data 3 output pin |
| 133 | P407 TRACEDATA4 | - - | Q | General-purpose I/O port Trace data 4 output pin |
| 134 | P408 SIN2_0 INT12_0 TRACEDATA5 | - - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data input pin (0) INT12 external interrupt input pin (0) Trace data 5 output pin |
| 135 | P409 SOT2_0 SDA2_0 TIOA24_1 TRACEDATA6 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data output pin (0) I ² C bus ch.2 serial data I/O pin Base timer ch.24 TIOA output pin (1) Trace data 6 output pin |
| 136 | P411 SCK2_0 SCL2_0 INT13_1 TRACEDATA7 | - - - - - | Q | General-purpose I/O port Multi-function serial ch.2 clock I/O pin (0) I ² C bus ch.2 serial clock I/O pin INT13 external interrupt input pin (1) Trace data 7 output pin |
| 137 | P413 SCS20_0 INT14_1 | - - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 0 I/O pin (0) INT14 external interrupt input pin (1) |
| 138 | P414 SCS21_0 | - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 1 output pin (0) |
| 139 | P416 IN5_0 TIOA22_1 | - - - | Q | General-purpose I/O port Input capture ch.5 input pin (0) Base timer ch.22 TIOA output pin (1) |
| 140 | P417 TIOA23_1 INT15_1 | - - - | Q | General-purpose I/O port Base timer ch.23 TIOA output pin (1) INT15 external interrupt input pin (1) |
| 141 | P418 SCS22_0 INT14_0 | - - - | Q | General-purpose I/O port Multi-function serial ch.2 chip select 2 output pin (0) INT14 external interrupt input pin (0) |

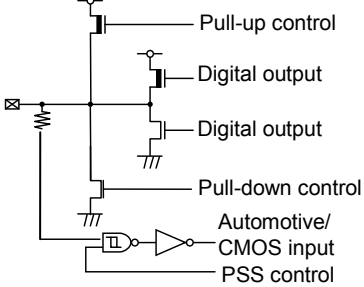
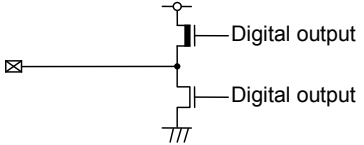
| Pin No. S6J311xHzC | Pin Name | Polarity | I/O Circuit Type | Function |
|-----------------------|----------------------------|-------------|------------------------|---|
| 142 | P420 SCK2_1 TRACECLK | - - - | Q | General-purpose I/O port Multi-function serial ch.2 clock I/O pin (1) Trace clock |
| 143 | P421 SIN2_1 TRACECTL | - - - | Q | General-purpose I/O port Multi-function serial ch.2 serial data input pin (1) Trace control |
| 42 | AVCC0 | - | - | Analog power supply pin for AD converter unit 0 |
| 84 | AVCC1 | - | - | Analog power supply pin for AD converter unit 1 |
| 43 | AVRH0 | - | - | Upper-limit reference voltage pin for AD converter unit 0 |
| 83 | AVRH1 | - | - | Upper-limit reference voltage pin for AD converter unit 1 |
| 44 | AVSS0 AVRL0 | - - | - | GND pin for AD converter unit 0 Lower-limit reference voltage pin for AD converter unit 0 |
| 82 | AVSS1 AVRL1 | - - | - | GND pin for AD converter unit 1 Lower-limit reference voltage pin for AD converter unit 1 |
| 105 | N.C | - | - | Non connection |
| 106 | | | | |
| 38 | C | - | - | External capacity connection output pin |
| 126 | | | | |
| 36 | VCC | - | - | Power supply pin |
| 72 | | | | |
| 109 | | | | |
| 124 | | | | |
| 144 | | | | |
| 1 | VSS | - | - | GND |
| 37 | | | | |
| 73 | | | | |
| 108 | | | | |
| 120 | | | | |
| 125 | | | | |

4. I/O Circuit Types

This section explains I/O circuit types.

| Type | Circuit | Overview |
|------|---|--|
| A |  | <ul style="list-style-type: none"> - General-purpose I/O port with analog input - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis input |
| B |  | <ul style="list-style-type: none"> - General-purpose I/O port with analog input - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable |
| C |  | <ul style="list-style-type: none"> - Mode input - CMOS hysteresis input |
| D |  | <ul style="list-style-type: none"> - JTAG - General-purpose output port - Output of 2 mA - 50 kΩ with pull-up resistor control - TTL input |

| Type | Circuit | Overview |
|------|---|--|
| E |  | <ul style="list-style-type: none"> - JTAG - 50 kΩ with pull-up resistor control - TTL input |
| F |  | <ul style="list-style-type: none"> - CMOS hysteresis input - 50 kΩ with pull-up resistor |
| G |  | <ul style="list-style-type: none"> - Main oscillation I/O |
| I |  | <ul style="list-style-type: none"> - JTAG - Output of 2 mA |
| J |  | <ul style="list-style-type: none"> - JTAG - General-purpose output port - Output of 2 mA - 50 kΩ with pull-down resistor control - TTL input |
| P |  | <ul style="list-style-type: none"> - General-purpose I/O port - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis input |

| Type | Circuit | Overview |
|------|---|--|
| Q |  <p> Pull-up control Digital output Digital output Pull-down control Automotive/ CMOS input PSS control </p> | <ul style="list-style-type: none"> - General-purpose I/O port - Output of 1 mA or 2 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - Automotive/CMOS hysteresis input selectable |
| R |  <p> Digital output Digital output </p> | <ul style="list-style-type: none"> - Output of 2 mA |

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.
Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%.
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

For Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC or lower than VSS; or the voltage applied between a VCC pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also be careful that analog power supplies (AVCC0, AVCC1, AVRH0, and AVRH1) and analog inputs do not exceed the digital power supply (VCC) at the analog system power-on and power-off times.

The power-on sequence is as follows. Simultaneously turn on the digital supply voltage (VCC) and analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1), or turn on the digital supply voltage (VCC) and then the analog supply voltages (AVCC0, AVCC1, AVRH0, and AVRH1).

About Handling Unused Pins

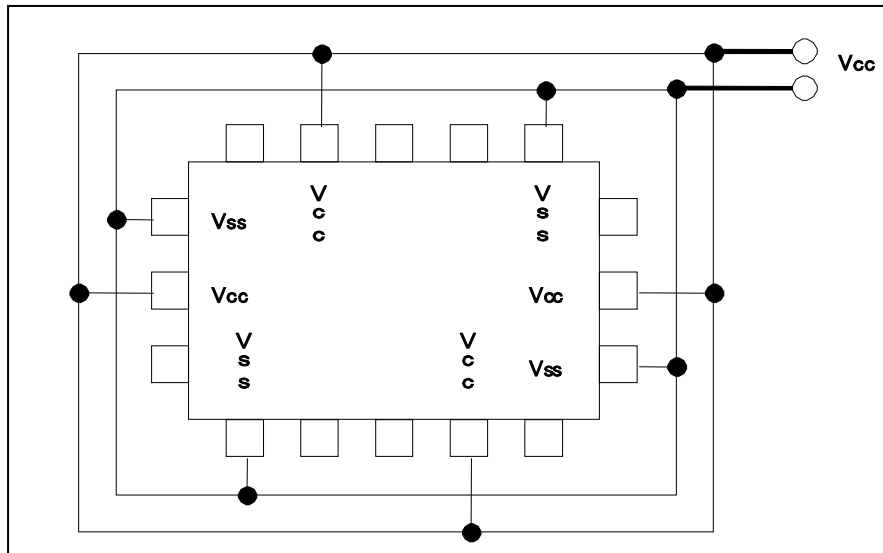
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures for unused pins, such as pulling up or pulling down the voltage with resistors of 2 kilohms or higher.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

About Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins that should be at the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also handle all the VSS power supply pins in this way as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 6-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin

About the Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

We recommend that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

About the Mode Pin (MD)

Use mode pin MD by directly connecting it to a VCC or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC or VSS pin on the printed circuit board, and connect them with low impedance.

About the Power-on Time

To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on.

Point to Note during PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that $AV_{CC}=AVRH=V_{CC}$ and $AV_{SS}/AVRL=V_{SS}$.

Points to Note About Using External Clocks

External clocks are not supported.

External direct clock input cannot be used.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC) before the application of the power supplies (AV_{CC} , AVRH, and AVRL) and analog inputs (AN0 to AN63) of an A/D converter.

At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC). Perform these power-on and power-off operations without AVRH exceeding AV_{CC} . Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AV_{CC} . (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

About C Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 154 in S6J311xJzC specifications, pin 126 in S6J311xHzC specifications) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet.

Precautions on Designing a Mounting Substrate

Measures against heat generation from the package must be taken for the mounting substrate to observe the absolute maximum rating (operating temperature). Design a mounting substrate with 4 or more layers. Connect the back of the package stage and the substrate pad with solder paste. Arrange thermal via holes on the substrate pad. For detailed information about mount conditions, contact your sales representative.

Notes on Writing to a Register Containing a Status Flag

In writing to a register containing a status flag (particularly an interrupt request flag, etc.) to control a function, it is important to take care not to accidentally clear the status flag.

Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value.

Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions have only 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into account for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

7. Block Diagram

This section provides block diagrams of the S6J3110 series.

Figure 7-1 S6J311xJAC* Block Diagram

* x: E/D

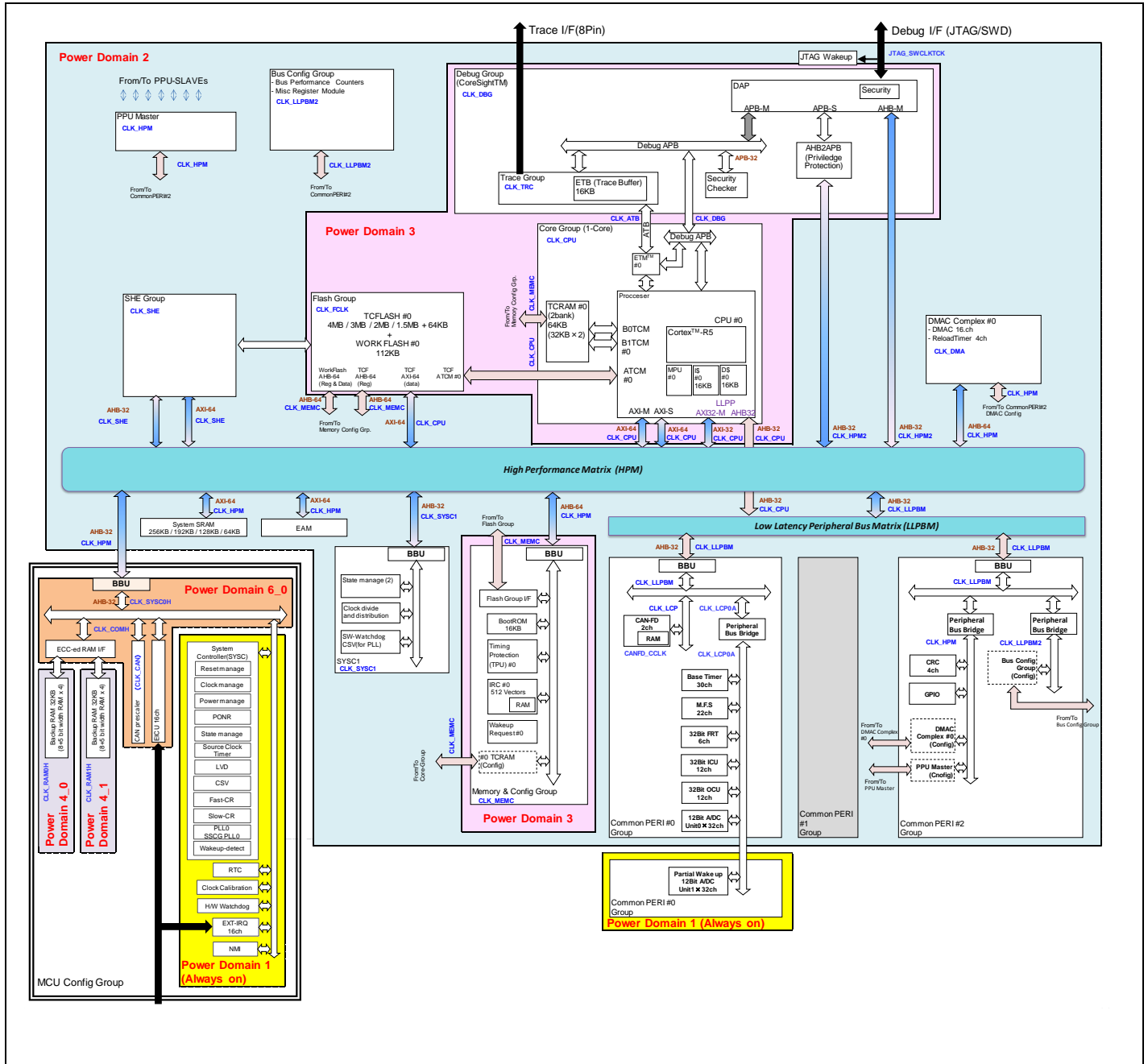
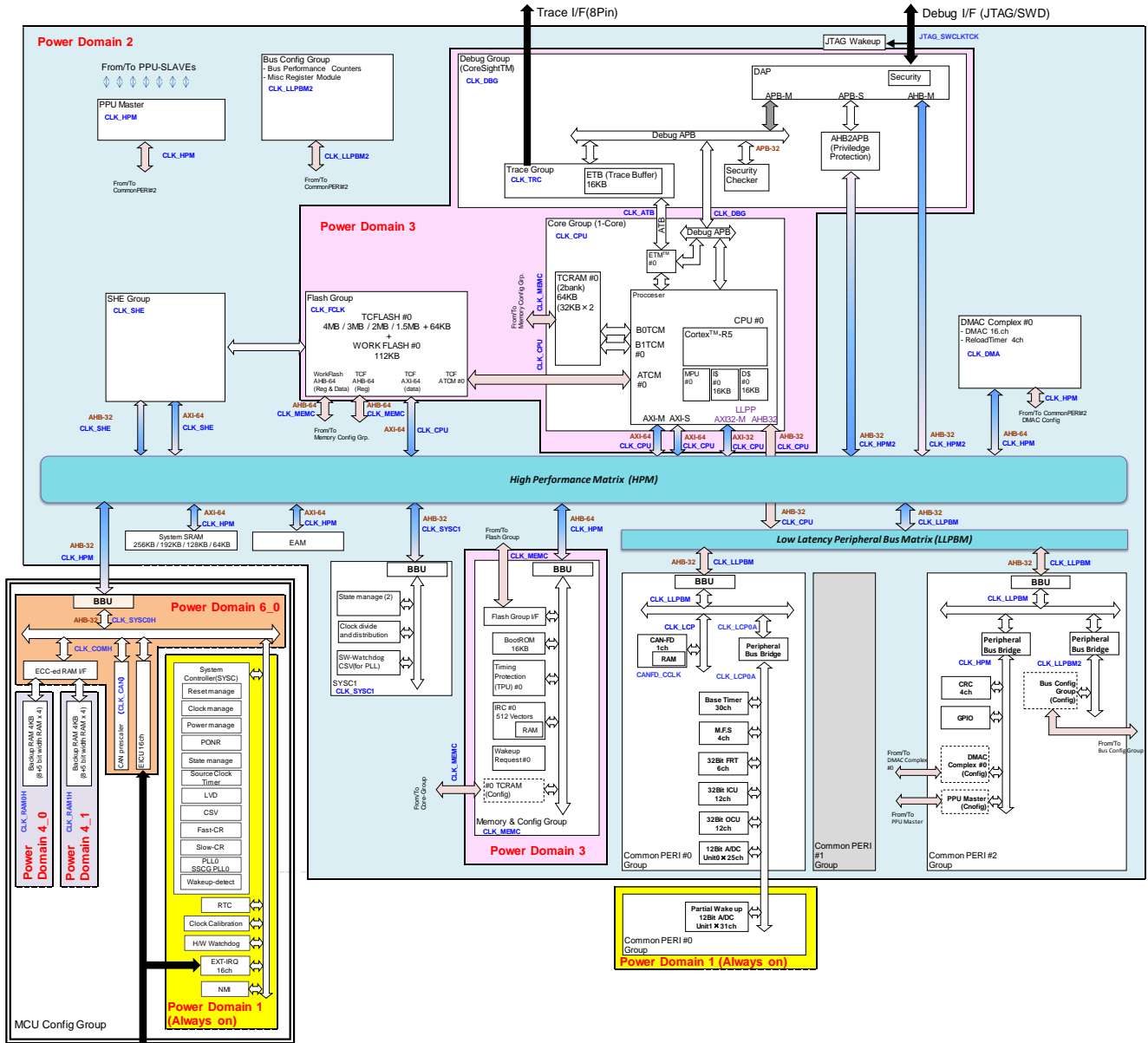


Figure 7-2 S6J311xHzC* Block Diagram

* x: E/D, z: A/B



8. Memory Map

This section explains the memory map.

Figure 8-1 Memory Map(S6J311EyzC/DyzC *)

* y: J/H, z: A/B

| ADDRESS | | group | S6J311EyzC | S6J311DyzC |
|-------------|-------------|-------------------------------|--|--|
| START | END | | part | part |
| 0x0000_0000 | 0x0000_FFFF | Internal area for CR5 Complex | TCRAM (Main 64KByte) | TCRAM (Main 64KByte) |
| 0x0001_0000 | 0x007F_FFFF | | Reserved | Reserved |
| 0x0080_0000 | 0x009E_FFFF | | Reserved | Reserved |
| 0x009F_0000 | 0x009F_FFFF | | TCM_FLASH (Small Sector 8KByte×8) | TCM_FLASH (Small Sector 8KByte×8) |
| 0x00A0_0000 | 0x00B7_FFFF | | TCM_FLASH (Code 4MByte) | TCM_FLASH (Code 3MByte) |
| 0x00B8_0000 | 0x00BF_FFFF | | | |
| 0x00C0_0000 | 0x00CF_FFFF | | Reserved | Reserved |
| 0x00D0_0000 | 0x00DF_FFFF | | Reserved | Reserved |
| 0x00E0_0000 | 0x00FF_FFFF | | AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror) | AXI_FLASH_MEMORY (Small Sector 8KByte×8 *Mirror) |
| 0x0100_0000 | 0x019E_FFFF | | AXI_FLASH_MEMORY (Code 4MByte *Mirror) | AXI_FLASH_MEMORY (Code 3MByte *Mirror) |
| 0x019F_0000 | 0x019F_FFFF | | | |
| 0x01A0_0000 | 0x01B7_FFFF | | Reserved | Reserved |
| 0x01B8_0000 | 0x01BF_FFFF | | Reserved | Reserved |
| 0x01C0_0000 | 0x01CF_FFFF | | Reserved | Reserved |
| 0x01D0_0000 | 0x01DF_FFFF | Reserved | Reserved | |
| 0x01E0_0000 | 0x01FF_FFFF | Reserved | Reserved | |
| 0x0200_0000 | 0x0200_FFFF | SYSTEM SRAM (256KByte) | SYSTEM SRAM (192KByte) | |
| 0x0201_0000 | 0x0201_FFFF | Reserved | Reserved | |
| 0x0202_0000 | 0x0202_FFFF | Reserved | Reserved | |
| 0x0203_0000 | 0x0203_FFFF | Reserved | Reserved | |
| 0x0204_0000 | 0x027F_FFFF | Exclusive Access Memory | Exclusive Access Memory | |
| 0x0280_0000 | 0x0280_002F | Reserved | Reserved | |
| 0x0280_0030 | 0x03FF_FFFF | AXI_SLAVE_CORE0 | AXI_SLAVE_CORE0 | |
| 0x0400_0000 | 0x05FF_FFFF | Reserved | Reserved | |
| 0x0600_0000 | 0x06FF_FFFF | Reserved | Reserved | |
| 0x0E00_0000 | 0x0E0F_FFFF | Shared Flash and memory area | WORK_FLASH (112KByte mirror area 1) | WORK_FLASH (112KByte mirror area 1) |
| 0x0E01_C000 | 0x0E0F_FFFF | | Reserved | Reserved |
| 0x0E10_0000 | 0x0E1F_FFFF | | Reserved | Reserved |
| 0x0E20_0000 | 0x0E21_BFFF | | WORK_FLASH (112KByte mirror area 3) | WORK_FLASH (112KByte mirror area 3) |
| 0x0E21_C000 | 0x0E2F_FFFF | | Reserved | Reserved |
| 0x0E30_0000 | 0x0E31_BFFF | | WORK_FLASH (112KByte mirror area 4) | WORK_FLASH (112KByte mirror area 4) |
| 0x0E31_C000 | 0x0E3F_FFFF | | Reserved | Reserved |
| 0x0E40_0000 | 0x0E7F_FFFF | | Reserved | Reserved |
| 0x0E80_0000 | 0x0E80_FFFF | | Backup RAM 64KByte | Backup RAM 64KByte |
| 0x0E81_0000 | 0x0E87_FFFF | | Reserved | Reserved |
| 0x0E88_0000 | 0x0FFF_FFFF | Reserved | Reserved | |
| 0x1000_0000 | 0xAFFF_FFFF | Reserved | Reserved | |
| 0xB000_0000 | 0xB483_FFFF | Peri area | Peri_area | Peri_area |
| 0xB484_0000 | 0xB484_FFFF | | APPS#5 | APPS#5 |
| 0xB485_0000 | 0xB7FF_FFFF | | Peri_area | Peri_area |
| 0xB800_0000 | 0xBFFF_DFFF | Reserved | Reserved | |
| 0xFFFE_E000 | 0xFFFF_FFFF | ERRCFG | ERRCFG | |
| 0xFFFF_0000 | 0xFFFF_3FFF | BootROM | BootRom | |
| 0xFFFF_4000 | 0xFFFF_FFFF | Reserved | Reserved | |

- Only the CPU core can access 0000_0000 ~ 01FF_FFFF. Bus masters other than the CPU core cannot access the region.
- Internal area of CR5 complex (0000_0000 ~ 01FF_FFFF) is mapped to AXI_SLAVE_CORE0. All bus masters can access to internal area of CR5 complex via AXI_SLAVE_CORE0.
- In each of the following memory area combinations, the areas are physically the same memory area.
 1. TCM FLASH (0x00A0_0000 -) and AXI FLASH MEMORY (0x01A0_0000 -)
 2. TCM FLASH Small Sector (0x009F_0000 -) and AXI FLASH MEMORY Small Sector (0x019F_0000 -)
 3. WORKFLASH (0x0E00_0000 -), WORKFLASH (0x0E20_0000 -), and WORKFLASH (0x0E30_0000 -)

The ECC movement in TCM port is based on ECC setting inside the CPU.

- The differences between the TCM FLASH and AXI FLASH include the following.

| Function | TCM FLASH | AXI FLASH |
|---------------------------------------|-------------------------------|----------------|
| High-speed Access Using Dedicated Bus | Applicable | Not applicable |
| Write and Erase | Not applicable (Read-only) | Applicable |
| Read | Applicable | Applicable |

- The differences between WORKFLASH areas include the following.

| Area | Function |
|------------------|---------------------------------------|
| WORKFLASH Area 1 | Used in write operation (with ECC) |
| WORKFLASH Area 3 | Used in write operation (without ECC) |
| WORKFLASH Area 4 | Used in read operation |

□ Terms are as follows.

| Term | Description |
|----------------|---|
| TCM RAM | Main RAM |
| TCM FLASH | Program FLASH (TCM area) |
| AXI FLASH | Program FLASH (AXI area) This is physically the same as the TCM FLASH. |
| SYSTEM RAM | System RAM |
| AXI SLAVE CORE | AXI CPU control area |
| WORKFLASH | FLASH for work |
| BACKUP RAM | Backup RAM |
| Peri area | Entire area for peripheral functions |
| APPS#5 | Part of area for peripheral functions |
| ERRCFG | Error configuration area |
| BootROM | ROM for reset boot |

Table 8-1 S6J311xJAC* Peripheral Map

* x: E/D

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------------------|---|--------|
| B000_0000 | B010_7FFF | | Reserved | - |
| B010_8000 | B010_80FF | SystemSRAM | SystemSRAM registers | - |
| B010_8100 | B02F_FFFF | | Reserved | - |
| B030_0000 | B030_7FFF | SYSC1 | System Controller #1 | - |
| B030_8000 | B03F_FFFF | SYSC1 | SWDT | - |
| B040_0000 | B040_7FFF | MEMORY_CONFIG_GROUP | IRC0 | 21 |
| B040_8000 | B040_FFFF | MEMORY_CONFIG_GROUP | TPU0 | 19 |
| B041_0000 | B041_0FFF | MEMORY_CONFIG_GROUP | TCRAM Control Status Register | 16 |
| B041_1000 | B041_1FFF | MEMORY_CONFIG_GROUP | TCFlash Control Status Register | 17 |
| B041_2000 | B041_20FF | MEMORY_CONFIG_GROUP | WFlash Control Status Register | 18 |
| B041_2100 | B04F_FFFF | | Reserved | - |
| B050_0000 | B05F_FFFF | | Reserved | - |
| B060_0000 | B060_007F | MCU_CONFIG_GROUP | Protection register area | - |
| B060_0080 | B060_00FF | MCU_CONFIG_GROUP | RUN profile register area | - |
| B060_0100 | B060_017F | MCU_CONFIG_GROUP | PSS profile register area | - |
| B060_0180 | B060_01FF | MCU_CONFIG_GROUP | APP profile register area | - |
| B060_0200 | B060_027F | MCU_CONFIG_GROUP | STS profile register area | - |
| B060_0280 | B060_02FF | MCU_CONFIG_GROUP | System register area | - |
| B060_0300 | B060_037F | MCU_CONFIG_GROUP | CSV | - |
| B060_0380 | B060_03FF | MCU_CONFIG_GROUP | RESET | - |
| B060_0400 | B060_047F | MCU_CONFIG_GROUP | SCT(Fast CR) | 34 |
| B060_0480 | B060_04FF | MCU_CONFIG_GROUP | SCT(Slow CR) | 33 |
| B060_0500 | B060_05FF | MCU_CONFIG_GROUP | SCT(Main clock) | 35 |
| B060_0600 | B060_067F | MCU_CONFIG_GROUP | Clock System | - |
| B060_0680 | B060_06FF | MCU_CONFIG_GROUP | Special register area | - |
| B060_0700 | B060_07FF | MCU_CONFIG_GROUP | Debug register area | - |
| B060_0800 | B060_BFFF | MCU_CONFIG_GROUP | Mode | - |
| B060_C000 | B060_FFFF | MCU_CONFIG_GROUP | HWDT | - |
| B061_0000 | B061_7FFF | | Reserved | - |
| B061_8000 | B061_FFFF | MCU_CONFIG_GROUP | RTC | 32 |
| B062_0000 | B063_FFFF | MCU_CONFIG_GROUP | EIC | - |
| B064_0000 | B065_FFFF | | Reserved | - |
| B066_0000 | B067_FFFF | | Reserved | - |
| B068_0000 | B068_7FFF | MCU_CONFIG_GROUP | BURAMIF | - |
| B068_8000 | B068_83FF | MCU_CONFIG_GROUP | EICU | 37 |
| B068_8400 | B068_87FF | MCU_CONFIG_GROUP | CR Calibration | 38 |
| B068_8800 | B068_8BFF | MCU_CONFIG_GROUP | IRQ ALL | 42 |
| B068_8C00 | B068_FFFF | MCU_CONFIG_GROUP | CAN Prescaler | 43 |
| B069_0000 | B06F_FFFF | | Reserved | - |
| B070_0000 | B07F_FFFF | | Reserved | - |
| B080_0000 | B0FF_FFFF | Bit RMW alias | Bit RMW alias for MCU config Gr (Covers B060_0000 -- B06F_FFFF) | - |
| B100_0000 | B10F_FFFF | Bit RMW alias | Bit RMW alias for SYSC1 (Covers B030_0000 -- B031_FFFF) | - |
| B110_0000 | B11F_FFFF | Bit RMW alias | Bit RMW alias for MEMC (Covers B040_0000 -- B041_FFFF) | - |
| B120_0000 | B1FF_FFFF | | Reserved | - |
| B200_0000 | B20F_FFFF | SHE | SHE configuration registers | 63 |
| B210_0000 | B46F_FFFF | | Reserved | - |
| B470_0000 | B470_3FFF | CommonPERI #2 | DMAC #0 registers | 64 |
| B470_4000 | B470_FFFF | | Reserved | - |
| B471_0000 | B471_0FFF | CommonPERI #2 | MPU for DMAC#0 | 66 |
| B471_1000 | B471_3FFF | | Reserved | - |
| B471_4000 | B471_4FFF | CommonPERI #2 | DMA Complex #0 registers (Additional registers, RLTs) | 68 |
| B471_5000 | B471_7FFF | | Reserved | - |
| B471_8000 | B471_83FF | CommonPERI #2 | CRC#0 | 70 |
| B471_8400 | B471_87FF | CommonPERI #2 | CRC#1 | 71 |
| B471_8800 | B471_8BFF | CommonPERI #2 | CRC#2 | 72 |
| B471_8C00 | B471_8FFF | CommonPERI #2 | CRC#3 | 73 |
| B471_9000 | B473_7FFF | | Reserved | - |
| B473_8000 | B473_FFFF | CommonPERI #2 | GPIO | 74 |
| B474_0000 | B474_7FFF | CommonPERI #2 | PPC | 75 |
| B474_8000 | B474_FFFF | CommonPERI #2 | RIC | 76 |
| B475_0000 | B475_7FFF | CommonPERI #2 | PPU | - |
| B475_8000 | B478_FBFF | | Reserved | - |
| B478_FC00 | B478_FFFF | | Reserved | - |
| B479_0000 | B47F_FFFF | | Reserved | - |

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------------|--|--------|
| B480_0000 | B480_03FF | CommonPERI #0 | M.F.Serial ch.0 | 176 |
| B480_0400 | B480_07FF | CommonPERI #0 | M.F.Serial ch.1 | 177 |
| B480_0800 | B480_0BFF | CommonPERI #0 | M.F.Serial ch.2 | 178 |
| B480_0C00 | B480_0FFF | CommonPERI #0 | M.F.Serial ch.3 | 179 |
| B480_1000 | B480_13FF | CommonPERI #0 | M.F.Serial ch.4 | 180 |
| B480_1400 | B480_17FF | CommonPERI #0 | M.F.Serial ch.5 | 181 |
| B480_1800 | B480_1BFF | CommonPERI #0 | M.F.Serial ch.6 | 182 |
| B480_1C00 | B480_1FFF | CommonPERI #0 | M.F.Serial ch.7 | 183 |
| B480_2000 | B480_7FFF | | Reserved | - |
| B480_8000 | B480_83FF | CommonPERI #0 | BaseTimer ch.0 | 88 |
| B480_8400 | B480_87FF | CommonPERI #0 | BaseTimer ch.1 | 89 |
| B480_8800 | B480_8BFF | CommonPERI #0 | BaseTimer ch.2 | 90 |
| B480_8C00 | B480_8FFF | CommonPERI #0 | BaseTimer ch.3 | 91 |
| B480_9000 | B480_93FF | CommonPERI #0 | BaseTimer ch.4 | 92 |
| B480_9400 | B480_97FF | CommonPERI #0 | BaseTimer ch.5 | 93 |
| B480_9800 | B480_9BFF | CommonPERI #0 | BaseTimer ch.6 | 94 |
| B480_9C00 | B480_9FFF | CommonPERI #0 | BaseTimer ch.7 | 95 |
| B480_A000 | B480_A3FF | CommonPERI #0 | BaseTimer ch.8 | 96 |
| B480_A400 | B480_A7FF | CommonPERI #0 | BaseTimer ch.9 | 97 |
| B480_A800 | B480_ABFF | CommonPERI #0 | BaseTimer ch.10 | 98 |
| B480_AC00 | B480_AFFF | CommonPERI #0 | BaseTimer ch.11 | 99 |
| B480_B000 | B481_FFFF | | Reserved | - |
| B482_0000 | B482_03FF | CommonPERI #0 | FRT ch.0 | 208 |
| B482_0400 | B482_07FF | CommonPERI #0 | FRT ch.1 | 209 |
| B482_0800 | B482_0BFF | CommonPERI #0 | FRT ch.2 | 210 |
| B482_0C00 | B482_0FFF | CommonPERI #0 | FRT ch.3 | 211 |
| B482_1000 | B482_13FF | CommonPERI #0 | FRT ch.4 | 212 |
| B482_1400 | B482_17FF | CommonPERI #0 | FRT ch.5 | 213 |
| B482_1800 | B482_7FFF | | Reserved | - |
| B482_8000 | B482_83FF | CommonPERI #0 | ICU ch.0 / ch1 | 224 |
| B482_8400 | B482_87FF | CommonPERI #0 | ICU ch.2 / ch3 | 225 |
| B482_8800 | B482_8BFF | CommonPERI #0 | ICU ch.4 / ch5 | 226 |
| B482_8C00 | B482_8FFF | CommonPERI #0 | ICU ch.6 / ch7 | 227 |
| B482_9000 | B482_93FF | CommonPERI #0 | ICU ch.8 / ch9 | 228 |
| B482_9400 | B482_97FF | CommonPERI #0 | ICU ch.10 / ch11 | 229 |
| B482_9800 | B482_FFFF | | Reserved | - |
| B483_0000 | B483_03FF | CommonPERI #0 | OCU ch.0 / ch1 | 240 |
| B483_0400 | B483_07FF | CommonPERI #0 | OCU ch.2 / ch3 | 241 |
| B483_0800 | B483_0BFF | CommonPERI #0 | OCU ch.4 / ch5 | 242 |
| B483_0C00 | B483_0FFF | CommonPERI #0 | OCU ch.6 / ch7 | 243 |
| B483_1000 | B483_13FF | CommonPERI #0 | OCU ch.8 / ch9 | 244 |
| B483_1400 | B483_17FF | CommonPERI #0 | OCU ch.10 / ch11 | 245 |
| B483_1800 | B483_FBFF | | Reserved | - |
| B483_FC00 | B483_FFFF | | Reserved | - |
| B484_0000 | B484_FFFF | APPS #5 | APPS#5 area | - |
| B485_0000 | B489_FFFF | | Reserved | - |
| B48A_0000 | B48B_0FFF | | Reserved | - |
| B48B_1000 | B48B_FBFF | | Reserved | - |
| B48B_FC00 | B48B_FFFF | | Reserved | - |
| B48C_0000 | B48F_FFFF | | Reserved | - |
| B490_0000 | B490_FFFF | CommonPERI #0 | CAN_FD ch0 | 256 |
| B491_0000 | B491_FFFF | CommonPERI #0 | CAN_FD ch1 | 257 |
| B492_0000 | B4BF_FFFF | | Reserved | - |
| B4C0_0000 | B4FF_FFFF | Bit RMW alias | Bit RMW alias for CPER#0(Covers B490_0000 -- B497_FFFF) | - |
| B500_0000 | B5FF_FFFF | | Reserved | - |
| B600_0000 | B6FF_FFFF | | Reserved | - |
| B700_0000 | B77F_FFFF | Bit RMW alias | Bit RMW alias for CPER#2 (Covers B470_0000 -- B47F_FFFF) | - |
| B780_0000 | B7BF_FFFF | Bit RMW alias | Bit RMW alias for CPER#0 (Covers B480_0000 -- B487_FFFF) | - |
| B7C0_0000 | B7FF_FFFF | | Reserved | - |
| B800_0000 | FFFE_DFFF | | Reserved | - |
| FFFE_E000 | FFFE_FBFC | Error Config | IRC | - |
| FFFE_FC00 | FFFE_FFFF | Error Config | BootROM I/F | 20 |

Table 8-2 S6J311xJAC APPS#5 Area

* x:E/D

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------|-----------------------------|--------|
| B484_0000 | B484_03FF | APPS #5 | M.F.Serial ch.8 | 264 |
| B484_0400 | B484_07FF | APPS #5 | M.F.Serial ch.9 | 265 |
| B484_0800 | B484_0BFF | APPS #5 | M.F.Serial ch.10 | 266 |
| B484_0C00 | B484_0FFF | APPS #5 | M.F.Serial ch.11 | 267 |
| B484_1000 | B484_13FF | APPS #5 | M.F.Serial ch.12 | 268 |
| B484_1400 | B484_17FF | APPS #5 | M.F.Serial ch.13 | 269 |
| B484_1800 | B484_1BFF | APPS #5 | M.F.Serial ch.14 | 270 |
| B484_1C00 | B484_1FFF | APPS #5 | M.F.Serial ch.15 | 271 |
| B484_2000 | B484_23FF | APPS #5 | M.F.Serial ch.16 | 272 |
| B484_2400 | B484_27FF | APPS #5 | M.F.Serial ch.17 | 273 |
| B484_2800 | B484_2BFF | APPS #5 | M.F.Serial ch.18 | 274 |
| B484_2C00 | B484_2FFF | APPS #5 | M.F.Serial ch.19 | 275 |
| B484_3000 | B484_33FF | APPS #5 | M.F.Serial ch.20 | 276 |
| B484_3400 | B484_37FF | APPS #5 | M.F.Serial ch.21 | 277 |
| B484_3800 | B484_3BFF | APPS #5 | BaseTimer ch.12 | 278 |
| B484_3C00 | B484_3FFF | APPS #5 | BaseTimer ch.13 | 279 |
| B484_4000 | B484_43FF | APPS #5 | BaseTimer ch.14 | 280 |
| B484_4400 | B484_47FF | APPS #5 | BaseTimer ch.15 | 281 |
| B484_4800 | B484_4BFF | APPS #5 | BaseTimer ch.16 | 282 |
| B484_4C00 | B484_4FFF | APPS #5 | BaseTimer ch.17 | 283 |
| B484_5000 | B484_53FF | APPS #5 | BaseTimer ch.18 | 284 |
| B484_5400 | B484_57FF | APPS #5 | BaseTimer ch.19 | 285 |
| B484_5800 | B484_5BFF | APPS #5 | BaseTimer ch.20 | 286 |
| B484_5C00 | B484_5FFF | APPS #5 | BaseTimer ch.21 | 287 |
| B484_6000 | B484_63FF | APPS #5 | BaseTimer ch.22 | 288 |
| B484_6400 | B484_67FF | APPS #5 | BaseTimer ch.23 | 289 |
| B484_6800 | B484_6BFF | APPS #5 | BaseTimer ch.24 | 290 |
| B484_6C00 | B484_6FFF | APPS #5 | BaseTimer ch.25 | 291 |
| B484_7000 | B484_73FF | APPS #5 | BaseTimer ch.26 | 292 |
| B484_7400 | B484_77FF | APPS #5 | BaseTimer ch.27 | 293 |
| B484_7800 | B484_7BFF | APPS #5 | BaseTimer ch.28 | 294 |
| B484_7C00 | B484_7FFF | APPS #5 | BaseTimer ch.29 | 295 |
| B484_8000 | B484_83FF | APPS #5 | A/D unit0 | 296 |
| B484_8400 | B484_87FF | APPS #5 | A/D unit1 , Partial Wake Up | 297 |
| B484_8800 | B484_8BFF | APPS #5 | A/D analog input control | 298 |
| B484_8C00 | B484_8FFF | | Reserved | - |
| B484_9000 | B484_93FF | APPS #5 | Global Timer | 300 |
| B484_9400 | B484_FFFF | | Reserved | - |

Table 8-3 S6J311xHzC Peripheral Map

* x:E/D, z:A/B

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------------------|---|--------|
| B000_0000 | B010_7FFF | | Reserved | - |
| B010_8000 | B010_80FF | SystemSRAM | SystemSRAM registers | - |
| B010_8100 | B02F_FFFF | | Reserved | - |
| B030_0000 | B030_7FFF | SYSC1 | System Controller #1 | - |
| B030_8000 | B03F_FFFF | SYSC1 | SWDT | - |
| B040_0000 | B040_7FFF | MEMORY_CONFIG_GROUP | IRC0 | 21 |
| B040_8000 | B040_FFFF | MEMORY_CONFIG_GROUP | TPU0 | 19 |
| B041_0000 | B041_0FFF | MEMORY_CONFIG_GROUP | TCRAM Control Status Register | 16 |
| B041_1000 | B041_1FFF | MEMORY_CONFIG_GROUP | TCFlash Control Status Register | 17 |
| B041_2000 | B041_20FF | MEMORY_CONFIG_GROUP | WFlash Control Status Register | 18 |
| B041_2100 | B04F_FFFF | | Reserved | - |
| B050_0000 | B05F_FFFF | | Reserved | - |
| B060_0000 | B060_007F | MCU_CONFIG_GROUP | Protection register area | - |
| B060_0080 | B060_00FF | MCU_CONFIG_GROUP | RUN profile register area | - |
| B060_0100 | B060_017F | MCU_CONFIG_GROUP | PSS profile register area | - |
| B060_0180 | B060_01FF | MCU_CONFIG_GROUP | APP profile register area | - |
| B060_0200 | B060_027F | MCU_CONFIG_GROUP | STS profile register area | - |
| B060_0280 | B060_02FF | MCU_CONFIG_GROUP | System register area | - |
| B060_0300 | B060_037F | MCU_CONFIG_GROUP | CSV | - |
| B060_0380 | B060_03FF | MCU_CONFIG_GROUP | RESET | - |
| B060_0400 | B060_047F | MCU_CONFIG_GROUP | SCT(Fast CR) | 34 |
| B060_0480 | B060_04FF | MCU_CONFIG_GROUP | SCT(Slow CR) | 33 |
| B060_0500 | B060_05FF | MCU_CONFIG_GROUP | SCT(Main clock) | 35 |
| B060_0600 | B060_067F | MCU_CONFIG_GROUP | Clock System | - |
| B060_0680 | B060_06FF | MCU_CONFIG_GROUP | Special register area | - |
| B060_0700 | B060_07FF | MCU_CONFIG_GROUP | Debug register area | - |
| B060_0800 | B060_BFFF | MCU_CONFIG_GROUP | Mode | - |
| B060_C000 | B060_FFFF | MCU_CONFIG_GROUP | HWDT | - |
| B061_0000 | B061_7FFF | | Reserved | - |
| B061_8000 | B061_FFFF | MCU_CONFIG_GROUP | RTC | 32 |
| B062_0000 | B063_FFFF | MCU_CONFIG_GROUP | EIC | - |
| B064_0000 | B065_FFFF | | Reserved | - |
| B066_0000 | B067_FFFF | | Reserved | - |
| B068_0000 | B068_7FFF | MCU_CONFIG_GROUP | BURAMIF | - |
| B068_8000 | B068_83FF | MCU_CONFIG_GROUP | EICU | 37 |
| B068_8400 | B068_87FF | MCU_CONFIG_GROUP | CR_Calibration | 38 |
| B068_8800 | B068_8BFF | MCU_CONFIG_GROUP | IRQ_ALL | 42 |
| B068_8C00 | B068_FFFF | MCU_CONFIG_GROUP | CAN Prescaler | 43 |
| B069_0000 | B06F_FFFF | | Reserved | - |
| B070_0000 | B07F_FFFF | | Reserved | - |
| B080_0000 | B0FF_FFFF | Bit RMW alias | Bit RMW alias for MCU config Gr (Covers B060_0000 -- B06F_FFFF) | - |
| B100_0000 | B10F_FFFF | Bit RMW alias | Bit RMW alias for SYSC1 (Covers B030_0000 -- B031_FFFF) | - |
| B110_0000 | B11F_FFFF | Bit RMW alias | Bit RMW alias for MEMC (Covers B040_0000 -- B041_FFFF) | - |
| B120_0000 | B1FF_FFFF | | Reserved | - |
| B200_0000 | B20F_FFFF | SHE | SHE configuration registers | 63 |
| B210_0000 | B46F_FFFF | | Reserved | - |
| B470_0000 | B470_3FFF | CommonPERI #2 | DMAC #0 registers | 64 |
| B470_4000 | B470_FFFF | | Reserved | - |
| B471_0000 | B471_0FFF | CommonPERI #2 | MPU for DMAC#0 | 66 |
| B471_1000 | B471_3FFF | | Reserved | - |
| B471_4000 | B471_4FFF | CommonPERI #2 | DMA Complex #0 registers (Additional registers, RLTs) | 68 |
| B471_5000 | B471_7FFF | | Reserved | - |
| B471_8000 | B471_83FF | CommonPERI #2 | CRC#0 | 70 |
| B471_8400 | B471_87FF | CommonPERI #2 | CRC#1 | 71 |
| B471_8800 | B471_8BFF | CommonPERI #2 | CRC#2 | 72 |
| B471_8C00 | B471_8FFF | CommonPERI #2 | CRC#3 | 73 |
| B471_9000 | B473_7FFF | | Reserved | - |
| B473_8000 | B473_FFFF | CommonPERI #2 | GPIO | 74 |
| B474_0000 | B474_7FFF | CommonPERI #2 | PPC | 75 |
| B474_8000 | B474_FFFF | CommonPERI #2 | RIC | 76 |
| B475_0000 | B475_7FFF | CommonPERI #2 | PPU | - |
| B475_8000 | B478_FBFF | | Reserved | - |
| B478_FC00 | B478_FFFF | | Reserved | - |
| B479_0000 | B47F_FFFF | | Reserved | - |

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------------|---|--------|
| B480_0000 | B480_03FF | CommonPERI #0 | M.F.Serial ch.0 | 176 |
| B480_0400 | B480_07FF | CommonPERI #0 | M.F.Serial ch.1 | 177 |
| B480_0800 | B480_0BFF | CommonPERI #0 | M.F.Serial ch.2 | 178 |
| B480_0C00 | B480_0FFF | CommonPERI #0 | M.F.Serial ch.3 | 179 |
| B480_1000 | B480_7FFF | | Reserved | - |
| B480_8000 | B480_83FF | CommonPERI #0 | BaseTimer ch.0 | 88 |
| B480_8400 | B480_87FF | CommonPERI #0 | BaseTimer ch.1 | 89 |
| B480_8800 | B480_8BFF | CommonPERI #0 | BaseTimer ch.2 | 90 |
| B480_8C00 | B480_8FFF | CommonPERI #0 | BaseTimer ch.3 | 91 |
| B480_9000 | B480_93FF | CommonPERI #0 | BaseTimer ch.4 | 92 |
| B480_9400 | B480_97FF | CommonPERI #0 | BaseTimer ch.5 | 93 |
| B480_9800 | B480_9BFF | CommonPERI #0 | BaseTimer ch.6 | 94 |
| B480_9C00 | B480_9FFF | CommonPERI #0 | BaseTimer ch.7 | 95 |
| B480_A000 | B480_A3FF | CommonPERI #0 | BaseTimer ch.8 | 96 |
| B480_A400 | B480_A7FF | CommonPERI #0 | BaseTimer ch.9 | 97 |
| B480_A800 | B480_ABFF | CommonPERI #0 | BaseTimer ch.10 | 98 |
| B480_AC00 | B480_AFFF | CommonPERI #0 | BaseTimer ch.11 | 99 |
| B480_B000 | B481_FFFF | | Reserved | - |
| B482_0000 | B482_03FF | CommonPERI #0 | FRT ch.0 | 208 |
| B482_0400 | B482_07FF | CommonPERI #0 | FRT ch.1 | 209 |
| B482_0800 | B482_0BFF | CommonPERI #0 | FRT ch.2 | 210 |
| B482_0C00 | B482_0FFF | CommonPERI #0 | FRT ch.3 | 211 |
| B482_1000 | B482_13FF | CommonPERI #0 | FRT ch.4 | 212 |
| B482_1400 | B482_17FF | CommonPERI #0 | FRT ch.5 | 213 |
| B482_1800 | B482_7FFF | | Reserved | - |
| B482_8000 | B482_83FF | CommonPERI #0 | ICU ch.0 / ch1 | 224 |
| B482_8400 | B482_87FF | CommonPERI #0 | ICU ch.2 / ch3 | 225 |
| B482_8800 | B482_8BFF | CommonPERI #0 | ICU ch.4 / ch5 | 226 |
| B482_8C00 | B482_8FFF | CommonPERI #0 | ICU ch.6 / ch7 | 227 |
| B482_9000 | B482_93FF | CommonPERI #0 | ICU ch.8 / ch9 | 228 |
| B482_9400 | B482_97FF | CommonPERI #0 | ICU ch.10 / ch11 | 229 |
| B482_9800 | B482_FFFF | | Reserved | - |
| B483_0000 | B483_03FF | CommonPERI #0 | OCU ch.0 / ch1 | 240 |
| B483_0400 | B483_07FF | CommonPERI #0 | OCU ch.2 / ch3 | 241 |
| B483_0800 | B483_0BFF | CommonPERI #0 | OCU ch.4 / ch5 | 242 |
| B483_0C00 | B483_0FFF | CommonPERI #0 | OCU ch.6 / ch7 | 243 |
| B483_1000 | B483_13FF | CommonPERI #0 | OCU ch.8 / ch9 | 244 |
| B483_1400 | B483_17FF | CommonPERI #0 | OCU ch.10 / ch11 | 245 |
| B483_1800 | B483_FBFF | | Reserved | - |
| B483_FC00 | B483_FFFF | | Reserved | - |
| B484_0000 | B484_FFFF | APPS #5 | APPS#5 area | - |
| B485_0000 | B489_FFFF | | Reserved | - |
| B48A_0000 | B48B_0FFF | | Reserved | - |
| B48B_1000 | B48B_FBFF | | Reserved | - |
| B48B_FC00 | B48B_FFFF | | Reserved | - |
| B48C_0000 | B48F_FFFF | | Reserved | - |
| B490_0000 | B490_FFFF | CommonPERI #0 | CAN_FD ch0 | 256 |
| B491_0000 | B4BF_FFFF | | Reserved | - |
| B4C0_0000 | B4FF_FFFF | Bit RMW alias | Bit RMW alias for CPERI#0(Covers B490_0000 -- B497_FFFF) | - |
| B500_0000 | B5FF_FFFF | | Reserved | - |
| B600_0000 | B6FF_FFFF | | Reserved | - |
| B700_0000 | B77F_FFFF | Bit RMW alias | Bit RMW alias for CPERI#2 (Covers B470_0000 -- B47F_FFFF) | - |
| B780_0000 | B7BF_FFFF | Bit RMW alias | Bit RMW alias for CPERI#0 (Covers B480_0000 -- B487_FFFF) | - |
| B7C0_0000 | B7FF_FFFF | | Reserved | - |
| B800_0000 | FFFE_DFFF | | Reserved | - |
| FFFE_E000 | FFFE_FBFC | Error Config | IRC | - |
| FFFE_FC00 | FFFE_FFFF | Error Config | BootROM I/F | 20 |

Table 8-4 S6J311xHzC APPS#5 Area

* x:E/D, z:A/B

| START Address | END Address | Group | Function | PPU No |
|---------------|-------------|---------|-----------------------------|--------|
| B484_0000 | B484_37FF | | Reserved | - |
| B484_3800 | B484_3BFF | APPS #5 | BaseTimer ch.12 | 278 |
| B484_3C00 | B484_3FFF | APPS #5 | BaseTimer ch.13 | 279 |
| B484_4000 | B484_43FF | APPS #5 | BaseTimer ch.14 | 280 |
| B484_4400 | B484_47FF | APPS #5 | BaseTimer ch.15 | 281 |
| B484_4800 | B484_4BFF | APPS #5 | BaseTimer ch.16 | 282 |
| B484_4C00 | B484_4FFF | APPS #5 | BaseTimer ch.17 | 283 |
| B484_5000 | B484_53FF | APPS #5 | BaseTimer ch.18 | 284 |
| B484_5400 | B484_57FF | APPS #5 | BaseTimer ch.19 | 285 |
| B484_5800 | B484_5BFF | APPS #5 | BaseTimer ch.20 | 286 |
| B484_5C00 | B484_5FFF | APPS #5 | BaseTimer ch.21 | 287 |
| B484_6000 | B484_63FF | APPS #5 | BaseTimer ch.22 | 288 |
| B484_6400 | B484_67FF | APPS #5 | BaseTimer ch.23 | 289 |
| B484_6800 | B484_6BFF | APPS #5 | BaseTimer ch.24 | 290 |
| B484_6C00 | B484_6FFF | APPS #5 | BaseTimer ch.25 | 291 |
| B484_7000 | B484_73FF | APPS #5 | BaseTimer ch.26 | 292 |
| B484_7400 | B484_77FF | APPS #5 | BaseTimer ch.27 | 293 |
| B484_7800 | B484_7BFF | APPS #5 | BaseTimer ch.28 | 294 |
| B484_7C00 | B484_7FFF | APPS #5 | BaseTimer ch.29 | 295 |
| B484_8000 | B484_83FF | APPS #5 | A/D unit0 | 296 |
| B484_8400 | B484_87FF | APPS #5 | A/D unit1 , Partial Wake Up | 297 |
| B484_8800 | B484_8BFF | APPS #5 | A/D analog input control | 298 |
| B484_8C00 | B484_8FFF | | Reserved | - |
| B484_9000 | B484_93FF | APPS #5 | Global Timer | 300 |
| B484_9400 | B484_FFFF | | Reserved | - |

When MPU attribute of Cortex-R5 is configured as "Normal", store buffer inside Cortex-R5 can operate and write data can be merged. To avoid influence of this data merger, MPU attribute "Device" or "Strongly Ordered" should be used.

MPU attribute "Device" or "Strongly Ordered" must be used for areas below, to avoid this influence.

- Backup RAM area (BACKUP_RAM) [0E80_0000 ~ 0E87_FFFF]
- Peripheral area (Peri area) [B000_0000 ~ B7FF_FFFF]
- Error Config area (ERRCFG) [FFFE_E000 ~ FFFE_FFFF]

MPU attribute "Device" or "Strongly Ordered" is required for accesses to areas below, in particular situation.

- FLASH Memory (when writing commands)

SHE OFF product is prohibited to access SHE area (B200_0000 to B20F_FFFF)

9. Pin Statuses In CPU Status

Table 9-1 S6J311xJAC* Pin State Table

* x: E/D

| Pin No. | Pin Name | GPORTE Control | External Reset Factor 1 | | | External Reset Factor 2 | | | External Reset Factor 3 | | Internal Reset Factor *2 | Sleep mode | Stop mode *4 | | Timer mode *4 | | | | |
|---------|--|-------------------|--|---------------------------------|----------------------------------|---------------------------------|-------------------------------------|---|--|---|-----------------------------|--------------------------|-------------------------------------|---|--------------------------|--|---|--|---|
| | | | External factor generation in progress | After external factor releasing | While Generating External Factor | After Releasing External Factor | Internal reset issuance in progress | After internal reset issuance (Before GPORTE setting) | Internal reset issuance in progress | After internal reset issuance (Before GPORTE setting) | | | Internal reset issuance in progress | After internal reset issuance (Before GPORTE setting) | CPU Sleep | High impedance disabled (SYS00_SPECIFGR_PSSPACTRL=0) | High impedance enabled (SYS00_SPECIFGR_PSSPACTRL=1) | High impedance disabled (SYS00_SPECIFGR_PSSPACTRL=0) | High impedance enabled (SYS00_SPECIFGR_PSSPACTRL=1) |
| | | | | | | | | | | | | | | | | | | | |
| 2 | P000/SOT2_1 | With control | Hi-Z/ Input blocked | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retains | Last state retained | Last state retained (*3) | Last state retained (*3) | Last state retained (*3) | Last state retained (*3) | Last state retained (*3) | Last state retained (*3) | | | |
| 3 | P001/SCS20_1 | | | | | | | | | | | | | | | | | | |
| 4 | P002/SCS21_1/TIOA0_1 | | | | | | | | | | | | | | | | | | |
| 5 | P003/SCS22_1 | | | | | | | | | | | | | | | | | | |
| 6 | P004/SCS23_1/TIOA1_1 | | | | | | | | | | | | | | | | | | |
| 7 | P005/IN6_0/SIN3_0 | | | | | | | | | | | | | | | | | | |
| 8 | P006/IN7_0/SOT3_0/SDA3_0 | | | | | | | | | | | | | | | | | | |
| 9 | P007/IN8_0/SCK18_1/SCK3_0/SCL3_0 | | | | | | | | | | | | | | | | | | |
| 10 | P008/IN9_0/SCS180_1/SCS30_0/TIOA0_0 | | | | | | | | | | | | | | | | | | |
| 11 | P009/IN10_0/SIN8_0/TIOA1_0/INT0_1 | | | | | | | | | | | | | | | | | | |
| 12 | P010/IN11_0/SOT8_0/SDA8_0/TIOA2_0 | | | | | | | | | | | | | | | | | | |
| 13 | P011/SIN18_1/TIOA2_1 | | | | | | | | | | | | | | | | | | |
| 14 | P012/OUT5_0/SCK8_0/SCL8_0/TIOA3_0 | | | | | | | | | | | | | | | | | | |
| 15 | P013/OUT6_0/SCS80_0/TIOA4_0 | | | | | | | | | | | | | | | | | | |
| 16 | P014/SOT18_1/TIOA3_1 | | | | | | | | | | | | | | | | | | |
| 17 | P015/OUT7_0/SCS81_0/TIOA5_0 | | | | | | | | | | | | | | | | | | |
| 18 | P016/OUT8_0/SCS82_0/TIOA6_0 | | | | | | | | | | | | | | | | | | |
| 19 | P017/OUT9_0/SCS83_0/TIOA7_0 | | | | | | | | | | | | | | | | | | |
| 20 | P018/OUT10_0/TIOA8_0 | | | | | | | | | | | | | | | | | | |
| 21 | P019/OUT11_0/TIOB0_0/TEXT0_0 | | | | | | | | | | | | | | | | | | |
| 22 | P020/SOT0_0/SDA0_0/TIOB1_0/TEXT1_0 | | | | | | | | | | | | | | | | | | |
| 23 | P021/SCK4_1/SCK0_0/SCL0_0/TIOB2_0 | | | | | | | | | | | | | | | | | | |
| 24 | P022/SIN0_0/TIOB3_0/INT3_0 | | | | | | | | | | | | | | | | | | |
| 25 | P023/SIN4_1/SCS0_0/TIOB4_0 | | | | | | | | | | | | | | | | | | |
| 26 | P024/SOT4_1/TIOB5_0 | | | | | | | | | | | | | | | | | | |
| 27 | P025/SCS40_1 | | | | | | | | | | | | | | | | | | |
| 28 | P026/SCS41_1 | | | | | | | | | | | | | | | | | | |
| 29 | P027/SCS42_1/TIOA4_1/TIOB6_0/INT1_1/TEXT0_1 | | | | | | | | | | | | | | | | | | |
| 30 | P028/OUT0_1/SIN1_0/TIOB7_0/INT4_0 | | | | | | | | | | | | | | | | | | |
| 31 | P029/OUT1_1/SOT1_0/SDA1_0/AN0 | | | | | | | | | | | | | | | | | | |
| 32 | P030/OUT2_1/SCS43_1 | | | | | | | | | | | | | | | | | | |
| 33 | P031/OUT3_1/SCS1_0/AN1 | | | | | | | | | | | | | | | | | | |
| 34 | P100/OUT4_1/SCK1_0/SCL1_0/AN2 | | | | | | | | | | | | | | | | | | |
| 35 | P101/OUT5_1/AN3 | | | | | | | | | | | | | | | | | | |
| 36 | P102/AN4 | | | | | | | | | | | | | | | | | | |
| 37 | P103/OUT6_1/SIN17_0/AN5 | | | | | | | | | | | | | | | | | | |
| 38 | P104/SOT17_0/SDA17_0 | | | | | | | | | | | | | | | | | | |
| 39 | P105/OUT7_1/SCK17_0/SCL17_0/TIOA9_0 | | | | | | | | | | | | | | | | | | |
| 40 | P106/OUT8_1/TX1_2/SCS170_0 | | | | | | | | | | | | | | | | | | |
| 41 | P107/OUT9_1/RX1_2/SIN19_0/TIOA10_0/INT2_1 | | | | | | | | | | | | | | | | | | |
| 42 | P108/OUT10_1/SOT19_0/SDA19_0/AN6/TIOA11_0/INT3_1 | | | | | | | | | | | | | | | | | | |
| 43 | P109/OUT11_1/SIN19_1/SCK19_0/SCL19_0/TIOA12_0 | | | | | | | | | | | | | | | | | | |
| 47 | P110/SCS190_0/AN7 | | | | | | | | | | | | | | | | | | |
| 48 | P111/SIN18_0/AN8 | | | | | | | | | | | | | | | | | | |
| 49 | P112/SOT18_0/SDA18_0/AN9/TIOA13_0 | | | | | | | | | | | | | | | | | | |
| 50 | P113/SOT19_1/SCK18_0/SCL18_0/TIOA5_1 | | | | | | | | | | | | | | | | | | |
| 51 | P114/SCS180_0/AN10/TIOA6_1 | | | | | | | | | | | | | | | | | | |
| 55 | P115 | | | | | | | | | | | | | | | | | | |
| 56 | P116/AN11 | | | | | | | | | | | | | | | | | | |
| 57 | P117/AN12/INT4_1 | | | | | | | | | | | | | | | | | | |
| 58 | P118/AN13/INT5_1 | | | | | | | | | | | | | | | | | | |
| 59 | P119/SCS60_0/AN14 | | | | | | | | | | | | | | | | | | |
| 60 | P120/SCS61_0/AN15 | | | | | | | | | | | | | | | | | | |
| 61 | P121/SCS160_0/AN16/TIOA14_0 | | | | | | | | | | | | | | | | | | |
| 62 | P122/SCS62_0/AN17/TIOA11_1 | | | | | | | | | | | | | | | | | | |
| 63 | P123/SCS63_0/AN18/TIOA12_1 | | | | | | | | | | | | | | | | | | |
| 64 | P124/SIN16_0/TIOA15_0 | | | | | | | | | | | | | | | | | | |
| 65 | P125/SOT16_0/SDA16_0/TIOA16_0 | | | | | | | | | | | | | | | | | | |
| 66 | P126/SCK16_0/SCL16_0/AN19 | | | | | | | | | | | | | | | | | | |
| 67 | P127/SCS203_0/AN20/TEXT1_1 | | | | | | | | | | | | | | | | | | |
| 68 | P128/SCS200_0/AN21/TEXT2_1 | | | | | | | | | | | | | | | | | | |
| 69 | P129/IN6_1/SCS201_0/AN22 | | | | | | | | | | | | | | | | | | |
| 70 | P130/IN7_1/SIN6_0/AN23/INT5_0 | | | | | | | | | | | | | | | | | | |
| 71 | P131/IN8_1/SOT6_0/SDA6_0/AN24 | | | | | | | | | | | | | | | | | | |
| 72 | P200/SCS202_0/AN25/TIOA17_0 | | | | | | | | | | | | | | | | | | |
| 73 | P201/SIN20_0/AN26/TIOA18_0 | | | | | | | | | | | | | | | | | | |
| 74 | P202/IN9_1/SCK6_0/SCL6_0/INT6_1 | | | | | | | | | | | | | | | | | | |
| 75 | P203/INT0_1 | | | | | | | | | | | | | | | | | | |
| 76 | P204/IN11_1/SOT20_0/SDA20_0/AN27 | | | | | | | | | | | | | | | | | | |
| 77 | P205/SCK20_0/SCL20_0/AN28/TEXT3_1 | | | | | | | | | | | | | | | | | | |
| 78 | P206/SCS43_0/AN29/TEXT4_1 | | | | | | | | | | | | | | | | | | |
| 79 | P207/SCK4_0/SCL4_0/AN30/INT7_1/TEXT5_1 | | | | | | | | | | | | | | | | | | |
| 80 | P208/SCS42_0/AN31/TIOA19_0 | | | | | | | | | | | | | | | | | | |
| 81 | P209/SOT4_0/SDA4_0/AN32/TIOA20_0 | | | | | | | | | | | | | | | | | | |
| 82 | P210/IN0_2/SIN4_0/AN33/TIOA21_0/INT6_0 | | | | | | | | | | | | | | | | | | |
| 83 | P211/IN1_2/SCS40_0/AN34/TIOA22_0 | | | | | | | | | | | | | | | | | | |
| 84 | P212/IN2_2/SCS50_1/SCS41_0/AN35/TIOA13_1 | | | | | | | | | | | | | | | | | | |
| 85 | P213/IN3_2/SIN5_1/TIOA14_1/INT8_1 | | | | | | | | | | | | | | | | | | |
| 86 | P214/IN4_2/SOT5_1/TIOA15_1 | | | | | | | | | | | | | | | | | | |
| 87 | P215/IN5_2/SCK5_1/TIOA16_1/INT9_1 | | | | | | | | | | | | | | | | | | |

| Pin No. | Pin Name | GPORTE Control | External Reset Factor 1 | | External Reset Factor 2 | | External Reset Factor 3 | | Internal Reset Factor *2 | Sleep mode | Stop mode *4 | | Timer mode *4 | |
|---------|---|----------------|--|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|---------------------|--|---------------------|--|---|--|---|
| | | | External factor generation in progress | After external factor releasing | While Generating External Factor | After Releasing External Factor | External Reset Factor 3 | CPU Sleep | | | High impedance disabled (SYSIO.SPECFGR.FSSPADCTRL=0) | High impedance enabled (SYSIO.SPECFGR.FSSPADCTRL=1) | High impedance disabled (SYSIO.SPECFGR.FSSPADCTRL=0) | High impedance enabled (SYSIO.SPECFGR.FSSPADCTRL=1) |
| | | | Internal reset issuance in progress | Internal reset issuance in progress | Internal reset issuance in progress | Internal reset issuance in progress | Internal reset issuance in progress | | | | | | | |
| 90 | P216/SIN15_0 | | | | | | | | | | | | | |
| 91 | P217/SOT15_0/SDA15_0 | | | | | | | | | | | | | |
| 92 | P218/SCK15_0/SCL15_0/AN36/TEXT2_0 | | | | | | | | | | | | | |
| 93 | P219/SCS150_0/AN37/TEXT3_0 | | | | | | | | | | | | | |
| 94 | P220/IN6_2/SCS53_0/AN38 | | | | | | | | | | | | | |
| 95 | P221/SCS52_0 | | | | | | | | | | | | | |
| 96 | P222/IN7_2/SIN5_0/AN39/INT7_0 | | | | | | | | | | | | | |
| 97 | P223/IN8_2/PWU_AN0/SCS51_0/AN40 | | | | | | | | | | | | | |
| 98 | P224/IN9_2/PWU_AN1/TX0_2/SCS50_0/AN41 | | | | | | | | | | | | | |
| 99 | P225/IN10_2/PWU_AN2/RX0_2/SOT5_0/SDA5_0/AN42/INT0_0 | With control | Hi-Z/ Input blocked | Hi-Z /Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked (*1) | Last state retained (*3) | Hi-Z/ Input blocked (*1) |
| 100 | P226/IN11_2/PWU_AN3/SCK5_0/SCL5_0/AN43/TQA17_1 | | | | | | | | | | | | | |
| 104 | P227/PWU_AN4/SCK10_0/SCL10_0/AN44/TQA23_0 | | | | | | | | | | | | | |
| 105 | P228/PWU_AN5/TX0_1/SOT10_0/SDA10_0/AN45/TQA24_0 | | | | | | | | | | | | | |
| 106 | P229/OUT0_0/PWU_AN6/RX0_1/SIN10_0/AN46/TQA25_0/INT8_0 | | | | | | | | | | | | | |
| 107 | P230/OUT1_0/PWU_AN7/SCK103_0/AN47/TQA26_0 | | | | | | | | | | | | | |
| 108 | P231/OUT2_0/SCS102_0/AN48/TQA27_0 | | | | | | | | | | | | | |
| 109 | P300/OUT3_0/SCS101_0/AN49/TQA28_0 | | | | | | | | | | | | | |
| 110 | P301/OUT4_0/SCS100_0/AN50/TQA18_1 | | | | | | | | | | | | | |
| 111 | P302/SIN14_0/AN51/TQA19_1 | | | | | | | | | | | | | |
| 112 | P303/SOT14_0/SDA14_0 | | | | | | | | | | | | | |
| 113 | P304/SCK14_0/SCL14_0/AN52/TQA20_1/TEXT4_0 | | | | | | | | | | | | | |
| 114 | P305/SCS140_0/AN53/TQA29_0/TEXT5_0 | | | | | | | | | | | | | |
| 115 | NMIK | - | Input enabled | | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| 116 | P306/TX0_0/SCS73_0/AN54 | | | | | | | | | | | | | |
| 117 | P307/RX0_0/SCS72_0/AN55/INT1_0 | | | | | | | | | | | | | |
| 118 | P308/IN0_1/SCK13_0/SCL13_0/AN56/TQA28_1 | | | | | | | | | | | | | |
| 119 | P309/IN1_1/SCS130_0/AN57/TQA29_1 | | | | | | | | | | | | | |
| 120 | P310/SIN13_0/INT15_0 | | | | | | | | | | | | | |
| 121 | P311/SOT13_0/SDA13_0 | | | | | | | | | | | | | |
| 122 | P312/IN2_1/SCS71_0/AN58 | | | | | | | | | | | | | |
| 123 | P313/IN3_1/SOT7_0/SDA7_0/AN59/INT10_1 | With control | Hi-Z/ Input blocked | Hi-Z /Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked (*1) | Last state retained (*3) | Hi-Z/ Input blocked (*1) |
| 124 | P314/IN4_1/SCK7_0/SCL7_0/AN60/TQA7_1 | | | | | | | | | | | | | |
| 125 | P315/IN5_1/SCS70_0/AN61/TQA8_1 | | | | | | | | | | | | | |
| 126 | P316/TQA21_1 | | | | | | | | | | | | | |
| 127 | P317/TX1_1/AN62/TQA9_1/INT11_1 | | | | | | | | | | | | | |
| 128 | P318/RX1_1/TQA10_1/INT9_0 | | | | | | | | | | | | | |
| 129 | P319/SIN7_0/AN63/INT12_1 | | | | | | | | | | | | | |
| 130 | P320/PWUTRG | | | | | | | | | | | | | |
| 131 | P321 | | | | | | | | | | | | | |
| 134 | TRST/P322 | | | | | | | | | | | | | |
| 135 | TDO/P323 | | | | | | | | | | | | | |
| 136 | TD/P324 | | | | | | | | | | | | | |
| 137 | TMS | | | | | | | | | | | | | |
| 138 | TCK | | | | | | | | | | | | | |
| 139 | P325/SIN21_0/INT10_0 | | | | | | | | | | | | | |
| 140 | P326/SOT21_0/SDA21_0 | | | | | | | | | | | | | |
| 141 | P327/SCK6_1/SCK21_0/SCL21_0 | With control | Hi-Z/ Input blocked | Hi-Z /Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked (*1) | Last state retained (*3) | Hi-Z/ Input blocked (*1) |
| 142 | P328/SOT6_1/SCS210_0 | | | | | | | | | | | | | |
| 143 | P329/SINE_1 | | | | | | | | | | | | | |
| 144 | P330 | | | | | | | | | | | | | |
| 145 | MD | | | | | | | | | | | | | |
| 146 | X0 | | | | | | | | | | | | | |
| 147 | X1 | | | | | | | | | | | | | |
| 149 | P331/SCS60_1 | | | | | | | | | | | | | |
| 150 | P400/SCS61_1 | With control | Hi-Z/ Input blocked | Hi-Z /Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked |
| 151 | RSTX | | | | | | | | | | | | | |
| 155 | P401/IN0_0/TX1_0/SCS62_1 | | | | | | | | | | | | | |
| 156 | P402/IN1_0/RX1_0/SCS63_1/SCS90_0/INT2_0 | | | | | | | | | | | | | |
| 157 | P403/IN2_0/TRACEDATA0 | | | | | | | | | | | | | |
| 158 | P404/IN3_0/TRACEDATA1 | | | | | | | | | | | | | |
| 159 | P405/IN4_0/SIN9_0/INT11_0/TRACEDATA2 | | | | | | | | | | | | | |
| 160 | P406/SOT9_0/SDA9_0/TRACEDATA3 | | | | | | | | | | | | | |
| 161 | P407/SCK7_1/SCS9_0/SCL9_0/TRACEDATA4 | | | | | | | | | | | | | |
| 162 | P408/SIN2_0/INT12_0/TRACEDATA5 | | | | | | | | | | | | | |
| 163 | P409/SOT2_0/SDA2_0/TQA24_1/TRACEDATA6 | | | | | | | | | | | | | |
| 164 | P410/SCS70_1 | | | | | | | | | | | | | |
| 165 | P411/SCS71_1/SCK2_0/SCL2_0/INT13_1/TRACEDATA7 | With control | Hi-Z/ Input blocked | Hi-Z /Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked (*1) | Last state retained (*3) | Hi-Z/ Input blocked (*1) |
| 166 | P412/SCS72_1/TQA25_1 | | | | | | | | | | | | | |
| 167 | P413/SCS73_1/SCS20_0/INT14_1 | | | | | | | | | | | | | |
| 168 | P414/SCS21_0/SIN11_0 | | | | | | | | | | | | | |
| 169 | P415/SOT11_0/SDA11_0/TQA26_1/INT13_0 | | | | | | | | | | | | | |
| 170 | P416/IN5_0/SIN7_1/SCK11_0/SCL11_0/TQA22_1 | | | | | | | | | | | | | |
| 171 | P417/SOT7_1/SCS110_0/TQA23_1/INT15_1 | | | | | | | | | | | | | |
| 172 | P418/SCS22_0/SIN12_0/INT14_0 | | | | | | | | | | | | | |
| 173 | P419/SCS23_0/SOT12_0/SDA12_0/TQA27_1 | | | | | | | | | | | | | |
| 174 | P420/SCK2_1/SCK12_0/SCL12_0/TRACECLK | | | | | | | | | | | | | |
| 175 | P421/SIN2_1/SCS120_0/TRACECTL | | | | | | | | | | | | | |

Table 9-2 S6J311xHzC Pin State Table

* x: E/D, z: A/B

| Pin No. | Pin Name | GPORTEN Control | External Reset Factor 1 | | External Reset Factor 2 | | External Reset Factor 3 | | Internal Reset Factor 2 | Sleep mode | Stop mode *4 | | Timer mode *4 | | | |
|---------|-------------------------------------|-----------------|--|-------------------------------------|--|---------------------------------|-------------------------------------|--|--|---------------------|--|--|--|---|--|---|
| | | | External factor generation in progress | After external factor releasing | While Generating External Factor | After Releasing External Factor | Internal reset issuance in progress | After internal reset issuance (Before GPORT setting) | | | Internal reset issuance in progress | After internal reset issuance (Before GPORT setting) | High impedance disabled (SYSIO_SPECIFGR_PSSPACTRL=0) | High impedance enabled (SYSIO_SPECIFGR_PSSPACTRL=1) | High impedance disabled (SYSIO_SPECIFGR_PSSPACTRL=0) | High impedance enabled (SYSIO_SPECIFGR_PSSPACTRL=1) |
| | | | Internal reset issuance in progress | Internal reset issuance in progress | After internal reset issuance (Before GPORT setting) | Before internal reset issuance | Internal reset issuance in progress | Internal reset issuance in progress | | | After internal reset issuance (Before GPORT setting) | Internal reset issuance in progress | After internal reset issuance (Before GPORT setting) | CPU Sleep | High impedance disabled (SYSIO_SPECIFGR_PSSPACTRL=0) | High impedance enabled (SYSIO_SPECIFGR_PSSPACTRL=1) |
| 2 | P000/SOT2_1 | | | | | | | | | | | | | | | |
| 3 | P001/SCS20_1 | | | | | | | | | | | | | | | |
| 4 | P003/SCS22_1 | | | | | | | | | | | | | | | |
| 5 | P005/IN6_0/SIN3_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 6 | P006/SOT3_0/SDA3_0/INT7_0 | | | | | | | | | | | | | | | |
| 7 | P007/SCK3_0/SCL3_0/IN8_0 | | | | | | | | | | | | | | | |
| 8 | P008/IN9_0/SCS30_0/TIOA0_0 | | | | | | | | | | | | | | | |
| 9 | P009/INT10_0/TIOA1_0/INT0_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 10 | P010/INT11_0/TIOA2_0 | | | | | | | | | | | | | | | |
| 11 | P012/OUT5_0/TIOA3_0 | | | | | | | | | | | | | | | |
| 12 | P013/OUT8_0/TIOA4_0 | | | | | | | | | | | | | | | |
| 13 | P015/OUT7_0/TIOA5_0 | | | | | | | | | | | | | | | |
| 14 | P016/OUT8_0/TIOA6_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 15 | P017/OUT9_0/TIOA7_0 | | | | | | | | | | | | | | | |
| 16 | P018/OUT10_0/TIOA8_0 | | | | | | | | | | | | | | | |
| 17 | P019/OUT11_0/TIOB0_0/TEXT0_0 | | | | | | | | | | | | | | | |
| 18 | P020/SOT0_0/SDA0_0/TEXT1_0/TIOB1_0 | | | | | | | | | | | | | | | |
| 19 | P021/SCK0_0/SCL0_0/TIOB2_0 | | | | | | | | | | | | | | | |
| 20 | P022/SIN0_0/TIOB3_0/INT3_0 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 21 | P023/SCS0_0/TIOB4_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 22 | P024/TIOB5_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 23 | P027/TIOA4_1/TIOB6_0/INT1_1/TEXT0_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 24 | P028/OUT0_1/SIN1_0/TIOB7_0/INT4_0 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 25 | P029/AN0/SOT1_0/SDA1_0/OUT1_1 | | | | | | | | | | | | | | | |
| 26 | P030/OUT2_1 | | | | | | | | | | | | | | | |
| 27 | P031/OUT3_1/SCS1_0/AN1 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 28 | P100/AN2/SCK1_0/SCL1_0/OUT4_1 | | | | | | | | | | | | | | | |
| 29 | P101/OUT5_1/AN3 | | | | | | | | | | | | | | | |
| 30 | P103/OUT6_1/AN5 | | | | | | | | | | | | | | | |
| 31 | P105/OUT7_1/TIOA9_0 | | | | | | | | | | | | | | | |
| 32 | P106/OUT8_1 | | | | | | | | | | | | | | | |
| 33 | P107/OUT9_1/TIOA10_0/INT2_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 34 | P108/OUT10_1/AN6/TIOA11_0/INT3_1 | | | | | | | | | | | | | | | |
| 35 | P109/OUT11_1/TIOA12_0 | | | | | | | | | | | | | | | |
| 36 | P112/AN9/TIOA13_0 | With control | Hi-Z/ Input blocked | | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retains | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | |
| 40 | P113/TIOA5_1 | | | | | | | | | | | | | | | |
| 41 | P114/AN10/TIOA6_1 | | | | | | | | | | | | | | | |
| 45 | P115 | | | | | | | | | | | | | | | |
| 46 | P117/AN12/INT4_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 47 | P118/AN13/INT5_1 | | | | | | | | | | | | | | | |
| 48 | P119/AN14 | | | | | | | | | | | | | | | |
| 49 | P120/AN15 | | | | | | | | | | | | | | | |
| 50 | P122/AN17/TIOA11_1 | | | | | | | | | | | | | | | |
| 51 | P123/AN18/TIOA12_1 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 52 | P126/AN19 | | | | | | | | | | | | | | | |
| 53 | P127/AN20/TEXT1_1 | | | | | | | | | | | | | | | |
| 54 | P128/AN21/TEXT2_1 | | | | | | | | | | | | | | | |
| 55 | P129/IN6_1/AN22 | | | | | | | | | | | | | | | |
| 56 | P130/IN7_1/AN23/INT5_0 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 57 | P131/IN8_1/AN24 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 58 | P202/IN9_1/INT6_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 59 | P203/INT0_1 | | | | | | | | | | | | | | | |
| 60 | P204/INT1_1/AN27 | | | | | | | | | | | | | | | |
| 61 | P205/AN28/TEXT3_1 | | | | | | | | | | | | | | | |
| 62 | P206/AN29/TEXT4_1 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 63 | P207/AN30/INT7_1/TEXT5_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 64 | P208/AN31/TIOA19_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 65 | P209/AN32/TIOA20_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 66 | P210/IN0_2/AN33/TIOA21_0/INT6_0 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 67 | P211/IN1_2/AN34/TIOA22_0 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 68 | P212/IN2_2/AN35/TIOA13_1 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 69 | P213/IN3_2/TIOA14_1/INT8_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |
| 70 | P214/IN4_2/TIOA15_1 | | | | | | | | | | | Hi-Z/ Input blocked | | Hi-Z/ Input blocked | | |
| 71 | P215/IN5_2/TIOA16_1/INT9_1 | | | | | | | | | | | Hi-Z/ Input blocked (*) | | Hi-Z/ Input blocked (*) | | |

| Pin No. | Pin Name | GPORTEN Control | External Reset Factor 1 | | | External Reset Factor 2 | | | External Reset Factor 3 | | Internal Reset Factor ² | Sleep mode | Stop mode ⁴ | | Timer mode ⁴ | | | | |
|---------|--|-----------------|-------------------------------------|---------------------------------|---|----------------------------------|---------------------------------|---|---|---|---|--|---|---|---|---|--|---|--|
| | | | Internal reset issuance in progress | After external factor releasing | | While Generating External Factor | After Releasing External Factor | | Internal reset issuance in progress | After internal reset issuance (Below GPORT setting) | | | Internal reset issuance in progress | After internal reset issuance (Below GPORT setting) | CPU Sleep | High impedance disabled (SYSIO_SPECIFGR, PSSIPADCTRL=0) | High impedance enabled (SYSIO_SPECIFGR, PSSIPADCTRL=1) | High impedance disabled (SYSIO_SPECIFGR, PSSIPADCTRL=0) | High impedance enabled (SYSIO_SPECIFGR, PSSIPADCTRL=1) |
| | | | | Internal reset in progress | After internal reset issuance (Below GPORT setting) | | Before internal reset issuance | After internal reset issuance (Below GPORT setting) | | | | | | | | | | | |
| 74 | P218/AN36/TEXT2_0 | With control | Hi-Z/ Input blocked | | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | | |
| 75 | P219/AN37/TEXT3_0 | | | | | | | | | | | | | | | | | | |
| 76 | P220/IN6_2/AN38 | | | | | | | | | | | | | | | | | | |
| 77 | P222/INT_2/AN39/INT1_0 | | | | | | | | | | | | | | | | | | |
| 78 | P223/IN8_2/AN40 | | | | | | | | | | | | | | | | | | |
| 79 | P224/IN9_2/TXD_2/AN41 | | | | | | | | | | | | | | | | | | |
| 80 | P225/INT0_2/RXD_2/AN42/INT0_0 | | | | | | | | | | | | | | | | | | |
| 81 | P226/IN11_2/AN43/TIOA17_1 | | | | | | | | | | | | | | | | | | |
| 86 | P227/AN44/TIOA23_0 | | | | | | | | | | | | | | | | | | |
| 86 | P228/TXD_1/AN45/TIOA24_0 | | | | | | | | | | | | | | | | | | |
| 87 | P229/OUT0_0/RXD_1/AN46/TIOA25_0/INT8_0 | | | | | | | | | | | | | | | | | | |
| 88 | P230/OUT1_0/AN47/TIOA26_0 | | | | | | | | | | | | | | | | | | |
| 89 | P231/OUT2_0/AN48/TIOA27_0 | | | | | | | | | | | | | | | | | | |
| 90 | P300/OUT3_0/AN49/TIOA28_0 | | | | | | | | | | | | | | | | | | |
| 91 | P301/OUT4_0/AN50/TIOA19_1 | | | | | | | | | | | | | | | | | | |
| 92 | P302/AN51/TIOA19_1 | | | | | | | | | | | | | | | | | | |
| 93 | P304/AN52/TIOA20_1/TEXT4_0 | | | | | | | | | | | | | | | | | | |
| 94 | P305/AN53/TIOA29_0/TEXT5_0 | | | | | | | | | | | | | | | | | | |
| 95 | NMX | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | | |
| 96 | P306/TXD_0/AN54 | With control | Hi-Z/ Input blocked | | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | | |
| 97 | P307/RXD_0/AN55/INT1_0 | | | | | | | | | | | | | | | | | | |
| 98 | P308/IN0_1/AN56/TIOA28_1 | | | | | | | | | | | | | | | | | | |
| 99 | P309/INT_1/AN57/TIOA29_1 | | | | | | | | | | | | | | | | | | |
| 100 | P312/IN2_1/AN58 | | | | | | | | | | | | | | | | | | |
| 101 | P313/IN3_1/AN59/INT10_1 | | | | | | | | | | | | | | | | | | |
| 102 | P314/IN4_1/AN60/TIOA7_1 | | | | | | | | | | | | | | | | | | |
| 103 | P315/IN5_1/AN61/TIOA8_1 | | | | | | | | | | | | | | | | | | |
| 104 | P317/AN62/TIOA9_1/INT11_1 | | | | | | | | | | | | | | | | | | |
| 107 | P321/PWUTRG | | | | | | | | | | | | | | | | - | Hi-Z/ Input blocked | Hi-Z/ Input blocked |
| 110 | TRST/P322 | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 111 | TD0/P323 | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled (Status immediately before the shutdown retaine) *6 | Input enabled (Last state retained) *6 | Input enabled (Last state retained) (*3) *6 | Input enabled (Hi-Z/ Input blocked) (*6) | Input enabled (Last state retained) (*3) *6 | Input enabled (Hi-Z/ Input blocked) (*6) | Input enabled (Last state retained) (*3) *6 | Input enabled (Hi-Z/ Input blocked) (*6) | | | |
| 112 | TD1/P324 | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 113 | TMS | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 114 | TCR | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 115 | P327 | With control | Hi-Z/ Input blocked | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | | |
| 116 | P330 | | | | | | | | | | | | | | | | | | |
| 117 | MD | | | | | | | | | | | | | | | | | | |
| 118 | X0 | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 119 | X1 | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 121 | P331 | With control | Hi-Z/ Input blocked | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | | |
| 122 | P400 | | | | | | | | | | | | | | | | | | |
| 123 | RSTX | - | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | | | |
| 127 | P401/IN0_0 | With control | Hi-Z/ Input blocked | | Hi-Z/ Last status retained | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Status immediately before the shutdown retaine | Last state retained | Last state retained (*3) | Hi-Z/ Input blocked | Hi-Z/ Input blocked | Last state retained (*3) | Hi-Z/ Input blocked | | | |
| 128 | P402/IN1_0/INT2_0 | | | | | | | | | | | | | | | | | | |
| 129 | P403/IN2_0/TRACEDATA0 | | | | | | | | | | | | | | | | | | |
| 130 | P404/IN3_0/TRACEDATA1 | | | | | | | | | | | | | | | | | | |
| 131 | P405/IN4_0/INT11_0/TRACEDATA2 | | | | | | | | | | | | | | | | | | |
| 132 | P406/TRACEDATA3 | | | | | | | | | | | | | | | | | | |
| 133 | P407/TRACEDATA4 | | | | | | | | | | | | | | | | | | |
| 134 | P408/IN2_0/INT12_0/TRACEDATA5 | | | | | | | | | | | | | | | | | | |
| 135 | P409/SOT2_0/SDA2_0/TIOA24_1/TRACEDATA6 | | | | | | | | | | | | | | | | | | |
| 136 | P411/INT13_1/SCK2_0/SCL2_0/TRACEDATA7 | | | | | | | | | | | | | | | | | | |
| 137 | P413/SCS20_0/INT14_1 | | | | | | | | | | | | | | | | | | |
| 138 | P414/SCS21_0 | | | | | | | | | | | | | | | | | | |
| 139 | P416/IN5_0/TIOA22_1 | | | | | | | | | | | | | | | | | | |
| 140 | P417/TIOA23_1/INT15_1 | | | | | | | | | | | | | | | | | | |
| 141 | P418/SCS22_0/INT14_0 | | | | | | | | | | | | | | | | | | |
| 142 | P420/SCK2_1/TRACECLK | | | | | | | | | | | | | | | | | | |
| 143 | P421/IN2_1/TRACECTL | | | | | | | | | | | | | | | | | | |

*1: Input disable is not valid when external interrupts are enabled.

*2: Recovery from standby (power off) becomes a factor.

*3: The pin state from the time that HOLDIO_PD2 was set (SYSC_SSPECFGR.HOLDIO_PD2=1) is retained. If power-off has not occurred and HOLDIO_PD2 has not been set (SYSC_SSPECFGR.HOLDIO_PD2=0), the last state is retained.

*4: To power off power domains 2 and 3, be sure to set HOLDIO_PD2 (SYSC_SSPECFGR.HOLDIO_PD2=1).

*5: When the PWU function is enabled, a change to output occurs.

*6: The pin state when the PORT function is enabled is shown.

*7: When PPC_PCFGrijj:POF[2:0] is set to initial value.

-External Reset Factor 1

Power-on reset (PONR)

RAM retention low-voltage detection reset (RVD)

Internal power supply low-voltage detection reset (LVDL1R)

RSTX pin + MD pin simultaneous assert reset (INITX)

-External Reset Factor 2

RSTX pin input reset (RSTX)

-External Reset Factor 3

Hardware watchdog reset (HWDR)

Software watchdog reset (SWDR)

PLL clock supervisor reset (CSVPRn)

SSCG clock supervisor reset (CSVSRn)

Profile error reset (PRFERR)

Software trigger hard reset (SHRST)

Software reset (SRST)

-Internal Reset Factor

Standby transition reset/ Power domain reset

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|----------------------|----------------------|----------------------|------|------------------------------------|
| | | Min | Max | | |
| Power supply voltage ^{*1, *2} | V _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | |
| Analog supply voltage ^{*1, *2} | AV _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | V _{CC} =AV _{CC} |
| Analog reference voltage ^{*1} | AVRH | V _{SS} -0.3 | V _{SS} +6.0 | V | AVRH ≤ AV _{CC} |
| Input voltage ^{*1} | V _I | V _{SS} -0.3 | V _{CC} +0.3 | V | |
| Analog pin input voltage ^{*1} | V _{IA} | V _{SS} -0.3 | V _{CC} +0.3 | V | |
| Output voltage ^{*1} | V _O | V _{SS} -0.3 | V _{CC} +0.3 | V | |
| Maximum clamp current | I _{CLAMP} | - | 4 | mA | *7 |
| Total maximum clamp current | Σ I _{CLAMP} | - | 20 | mA | *7 |
| "L"-level maximum output current ^{*3} | I _{OL1} | - | 3.5 | mA | When setting is 1 mA ^{*6} |
| | I _{OL2} | - | 7 | mA | When setting is 2 mA |
| "L"-level average output current ^{*4} | I _{OLAV1} | - | 1 | mA | When setting is 1 mA ^{*6} |
| | I _{OLAV2} | - | 2 | mA | When setting is 2 mA |
| "L"-level total output current ^{*5} | ΣI _{OL} | - | 40 | mA | *6 |
| "H"-level maximum output current ^{*3} | I _{OH1} | - | -3.5 | mA | When setting is 1 mA ^{*6} |
| | I _{OH2} | - | -7 | mA | When setting is 2 mA |
| "H"-level average output current ^{*4} | I _{OHAV1} | - | -1 | mA | When setting is 1 mA ^{*6} |
| | I _{OHAV2} | - | -2 | mA | When setting is 2 mA |
| "H"-level total output current ^{*5} | ΣI _{OH} | - | -40 | mA | *6 |
| Power consumption | P _D | - | 2000 | mW | *8 |
| Operating temperature | T _A | -40 | +105 | °C | |
| Storage temperature | T _{stg} | -55 | +150 | °C | |

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V.

*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current X the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

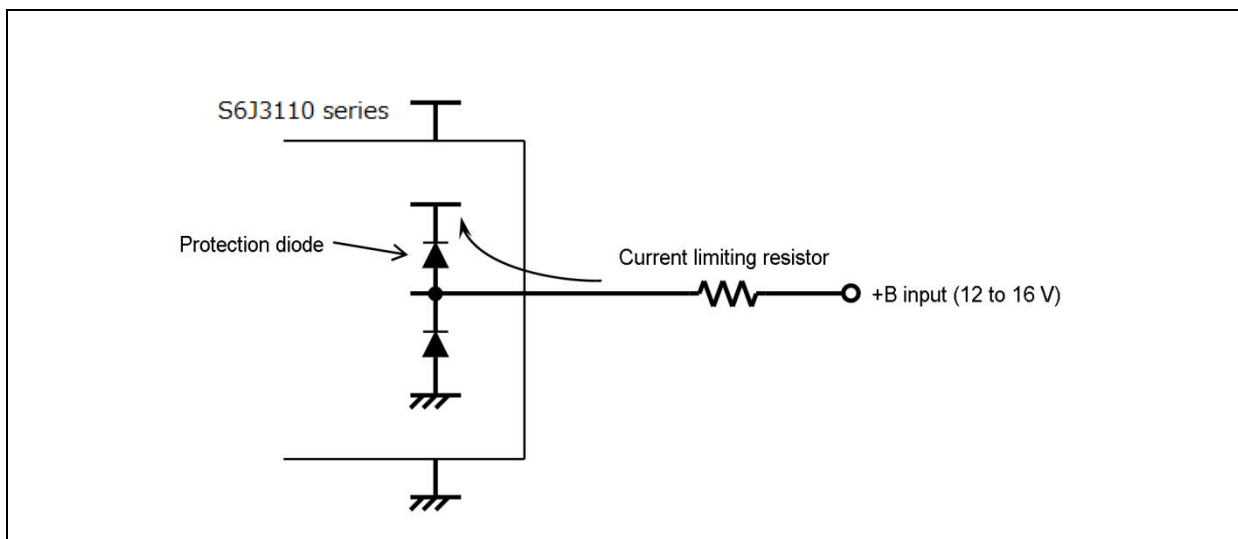
*6: Corresponding pins: general-purpose ports

*7: Corresponding pins: All general-purpose ports and analog input pins

- Use the device within the recommended operating conditions.
- Use the device with direct voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

*8: It is standard when four-layer substrate is used.

Example of a recommended circuit



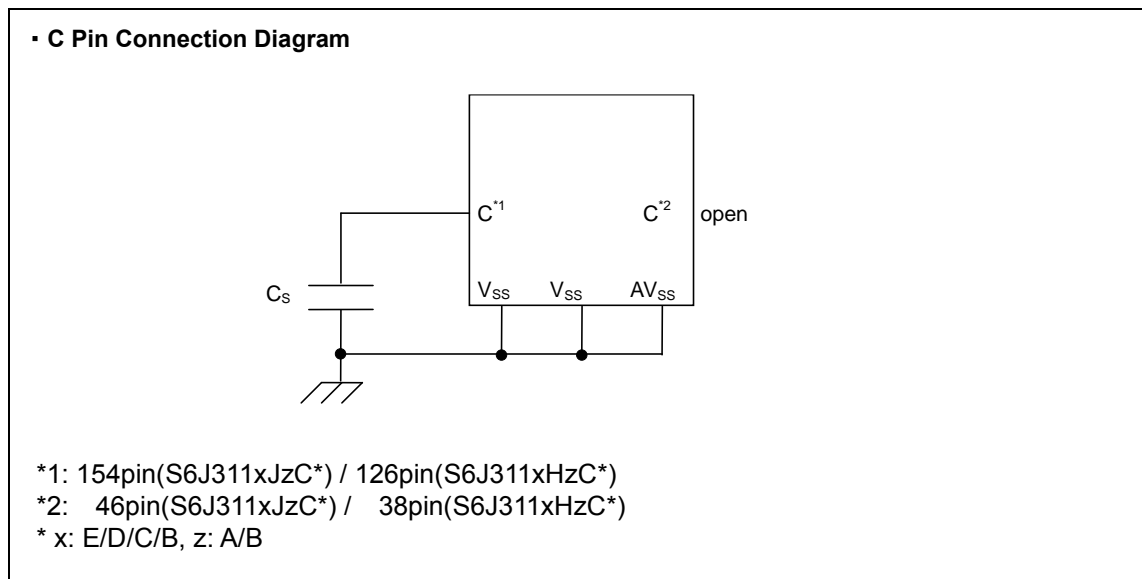
WARNING:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

10.2 Recommended Operating Conditions

 (V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Rating | | Unit | Remarks |
|-----------------------|------------------|--------|------|------|---|
| | | Min | Max | | |
| Supply voltage | V _{CC} | 4.5 | 5.25 | V | Recommended operation assurance range |
| | AV _{CC} | 4.5 | 5.25 | V | |
| | V _{CC} | 3.5 | 5.25 | V | Operation assurance range |
| | AV _{CC} | 3.5 | 5.25 | V | |
| Smoothing capacitor* | C _S | 4.7 | | μF | Tolerance of up to ±40% 154pin(LEP176) / 126pin(LES144) Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C _S as the smoothing capacitor on the VCC pin. |
| Operating temperature | T _A | -40 | +105 | °C | See the notes below. |

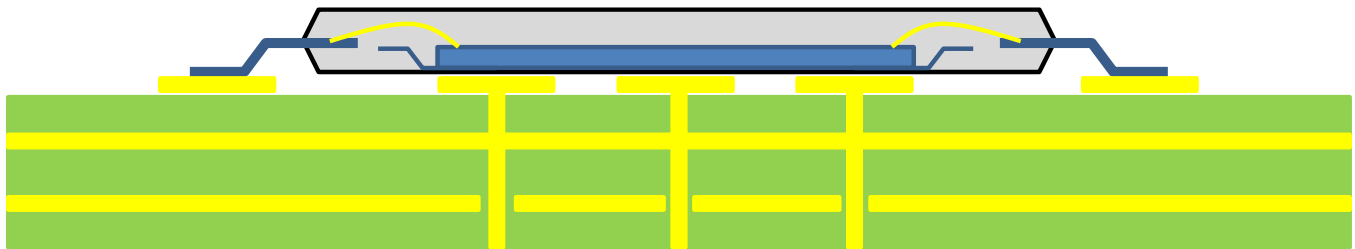
 *: For the connections of smoothing capacitor C_S, see the following diagram.

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Note:

- The following condition should be satisfied in order to facilitate heat dissipation.
 1. 4 or more layers PCB should be used.
 2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)
 3. 1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.
 4. 35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.
 5. The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.

Figure 10.2-1: Example thermal via holes on PCB.



Notes:

- Figure 10.2-1 is a schematic diagram showing PCB in section.
- Figure 10.2-2, Figure 10.2-3 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.
- If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Figure 10.2-2: Land Pattern and Thermal Via LEP176

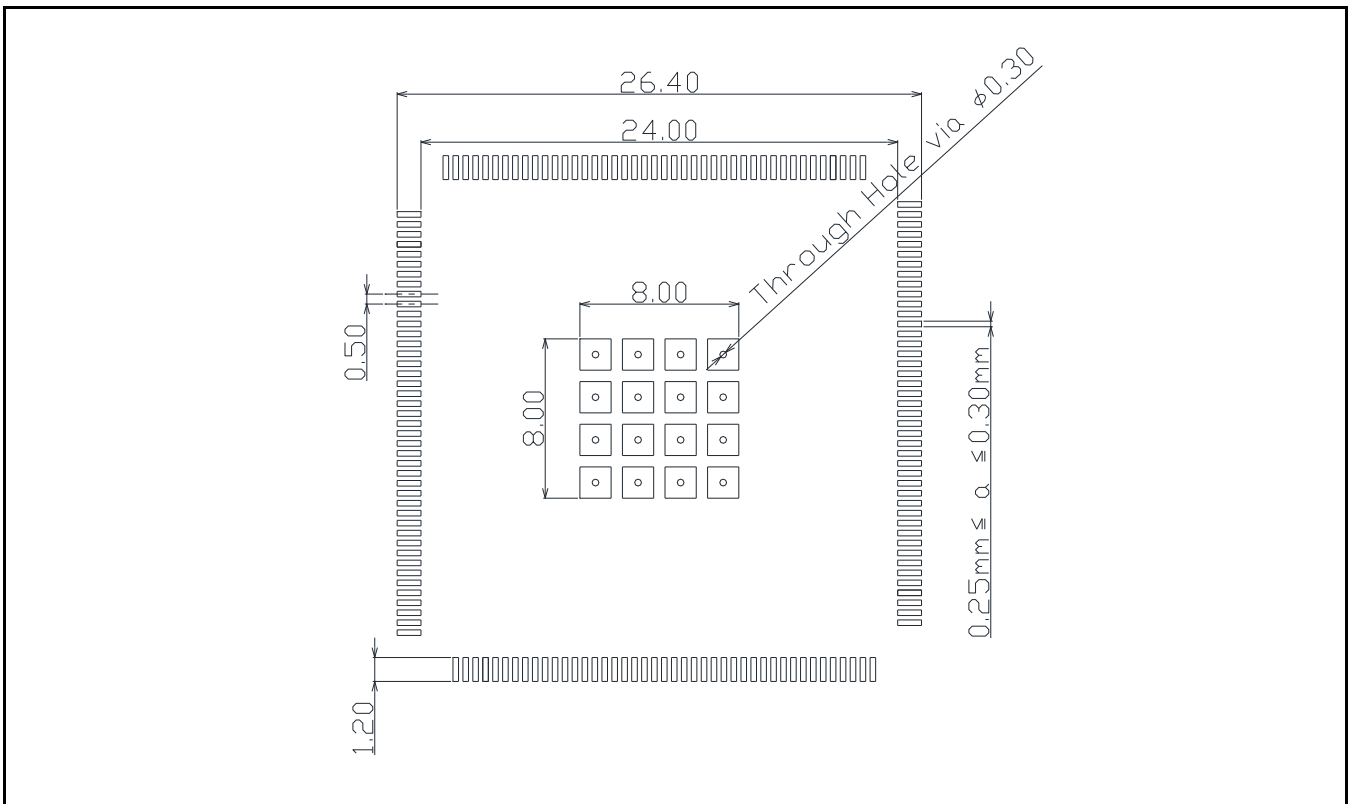
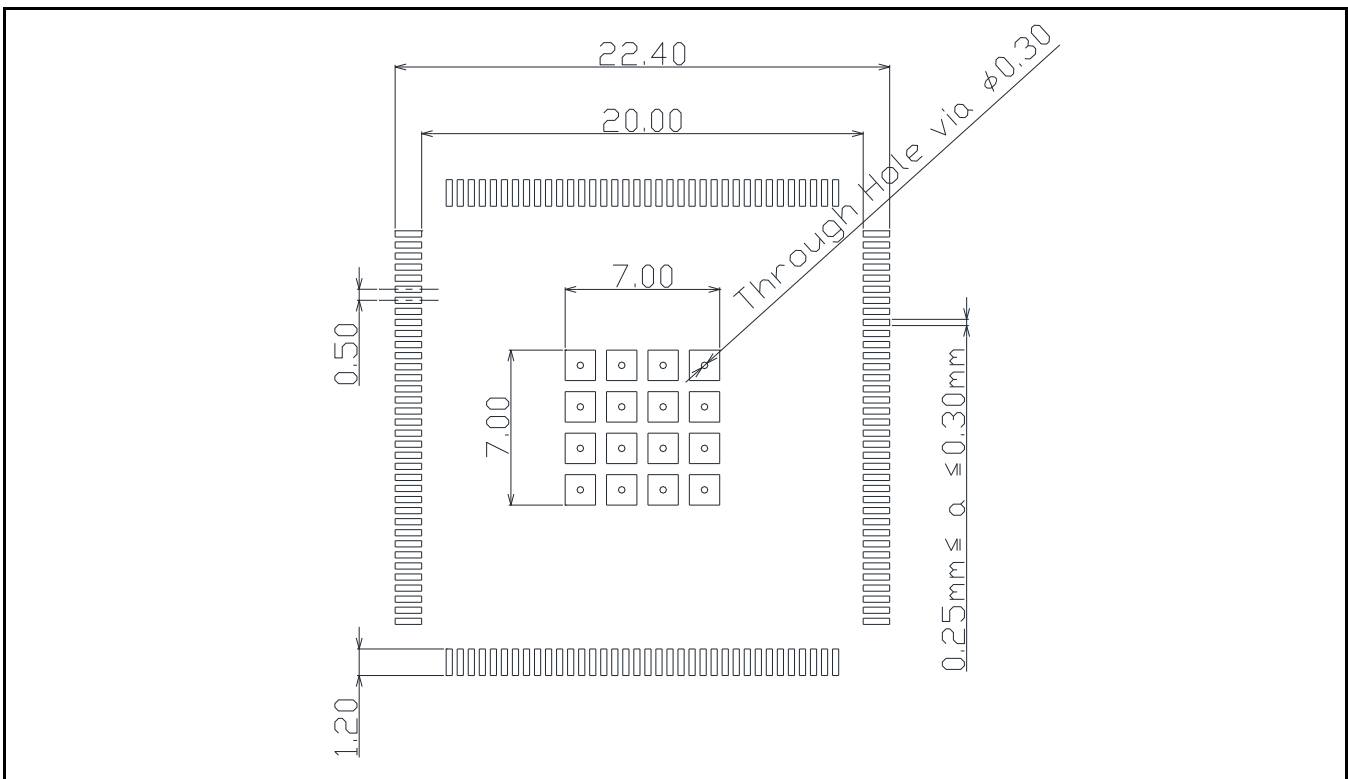


Figure 10.2-3: Land Pattern and Thermal Via LES144



10.3 DC Characteristics

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|-------------------------|------------------|--|-----------------------------------|----------------------|-----|----------------------|------|---------|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V _{IH1} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | CMOS Schmitt input level selected | 0.7×V _{CC} | - | V _{CC} +0.3 | V | |
| | V _{IH2} | P401 to P421 | Automotive input level selected | 0.8×V _{CC} | - | V _{CC} +0.3 | V | |
| | V _{IH4} | RSTX, NMIX | - | 0.7×V _{CC} | - | V _{CC} +0.3 | V | |
| | V _{IH5} | MD | - | 0.7×V _{CC} | - | V _{CC} +0.3 | V | |
| | V _{IH6} | TRST, TCK, TDI, TMS | TTL | 2.3 | - | V _{CC} +0.3 | V | |
| "L" level input voltage | V _{IL1} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | CMOS Schmitt input level selected | V _{SS} -0.3 | - | 0.3×V _{CC} | V | |
| | V _{IL2} | P401 to P421 | Automotive input level selected | V _{SS} -0.3 | - | 0.5×V _{CC} | V | |
| | V _{IL4} | RSTX, NMIX | - | V _{SS} -0.3 | - | 0.3×V _{CC} | V | |
| | V _{IL5} | MD | - | V _{SS} -0.3 | - | 0.3×V _{CC} | V | |
| | V _{IL6} | TRST, TCK, TDI, TMS | TTL | V _{SS} -0.3 | - | 0.8 | V | |

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|--------------------------|------------------|---|--|----------------------|-----|-----------------|------|---------|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | V _{OH1} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P321 to P324 P325 to P331, P400 to P421 | V _{CC} =4.5 V I _{OH} =-2.0 mA | V _{CC} -0.5 | - | V _{CC} | V | |
| "H" level output voltage | V _{OH2} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | V _{CC} =4.5 V I _{OH} =-1.0 mA | V _{CC} -0.5 | - | V _{CC} | V | |
| "L" level output voltage | V _{OL1} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P321 to P324 P325 to P331, P400 to P421 | V _{CC} =4.5 V I _{OL} =2.0 mA | 0 | - | 0.4 | V | |
| "L" level output voltage | V _{OL2} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | V _{CC} =4.5 V I _{OL} =1.0 mA | 0 | - | 0.4 | V | |

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|-----------------------|--------------------|--|---|-------|-----|-----|------|---------|
| | | | | Min | Typ | Max | | |
| Input leakage current | I _{IL} | All input pins | V _{CC} =AV _{CC} =5.25 V V _{SS} < V _I < V _{CC} | -5 | - | +5 | μA | |
| Pull-up resistor | R _{UP1} | RSTX, NMIX | - | 25 | - | 100 | kΩ | |
| | R _{UP2} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | Pull-up resistor selected | 25 | - | 100 | kΩ | |
| | R _{UP3} | TDI(P324),TMS, TCK | - | 25 | - | 100 | kΩ | |
| Pull-down resistor | R _{down1} | P000 to P031, P100 to P131, P200 to P231, P300 to P320, P325 to P331, P400 to P421 | Pull-down resistor selected | 25 | - | 100 | kΩ | |
| | R _{down2} | TRST(P322) | - | 25 | - | 100 | kΩ | |
| Input capacitance | C _{IN} | Pins other than V _{CC} , V _{SS} , AV _{CC0} ,AV _{CC1} , AV _{SS0} ,AV _{SS1} | - | - | 5 | 15 | pF | |

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|----------------------|----------------------|----------|-----------------------|-------|-------|----------------------|------|--|
| | | | | Min | Typ | Max | | |
| Power supply current | I _{CC5} | VCC | Normal operation | - | 140 | 320 | mA | Operating at 144 MHz |
| | | | Flash write/erase | - | 160 | 343 | mA | Operating at 144 MHz |
| | I _{CCS5} | | CPU Sleep | - | 82 | 265 | mA | Operating at 144 MHz |
| | I _{CC75} | | Timer mode | - | 946.0 | 2967.9 | μA | T _A =25°C Slow-CR source Oscillation |
| | I _{CH5} | | Stop mode | - | 945.1 | 2966.2 | μA | T _A =25°C |
| | I _{CCP} | | PWU mode (Shutdown) | - | 53.4 | 130.6 | μA | T _A =25°C (PWU operation cycle 16ms) |
| | | | | - | 47.1 | 116.4 | μA | T _A =25°C (PWU operation cycle 32ms) |
| | I _{CC752} | | Timer mode (Shutdown) | - | 40.9 | 102.3 | μA | T _A =25°C Slow-CR source Oscillation |
| I _{CH52} | Stop mode (Shutdown) | - | 40.1 | 101.4 | μA | T _A =25°C | | |

Refer to Hardware manual "APPENDIX State transition" for Internal clock frequency setting / Setting of the power domain / Regulator setting.

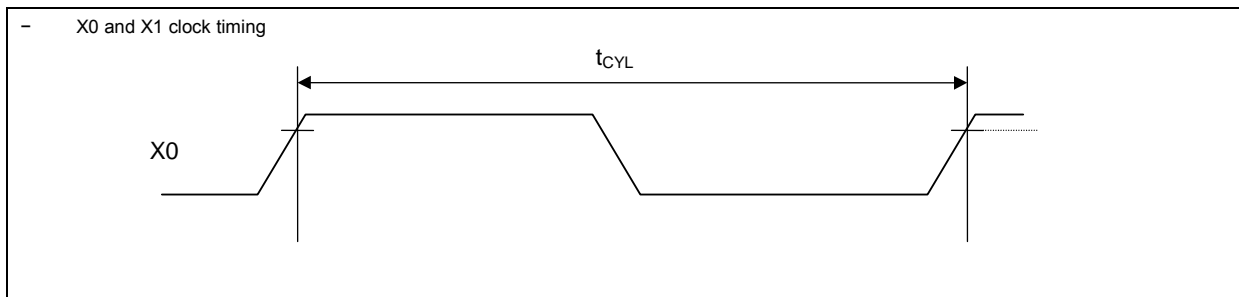
10.4 AC Characteristics

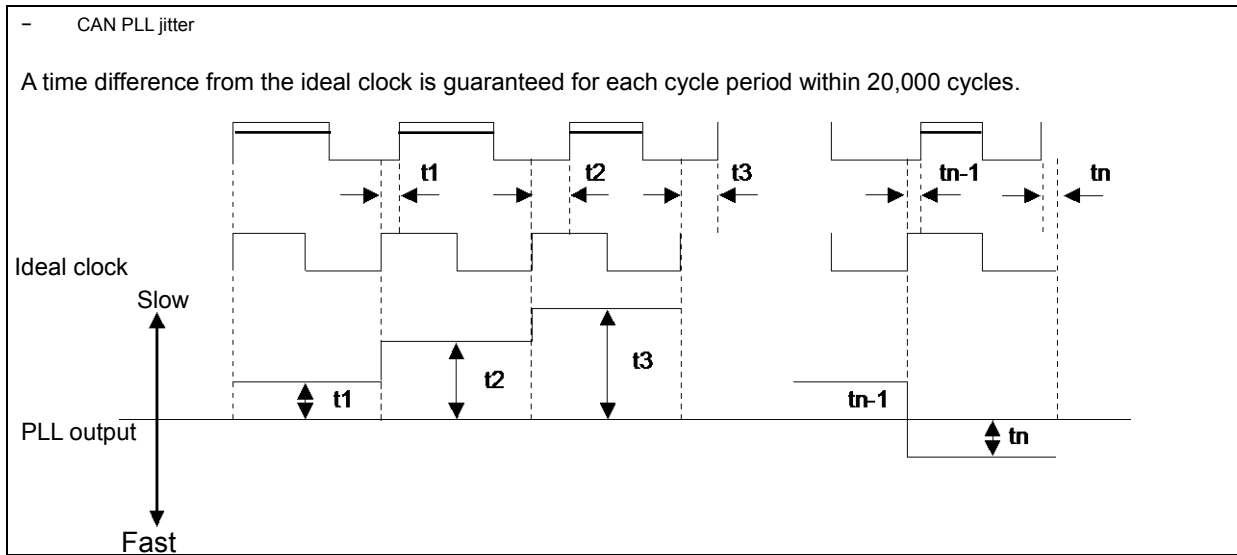
10.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|--|-----------------------|----------|------------|-------|-----|-----|------|---------|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | F _C | X0, X1 | - | - | 4 | - | MHz | |
| Source oscillation clock cycle time | t _{CYL} | X0, X1 | - | - | 250 | - | ns | |
| CAN PLL jitter (during lock) | t _{PJ} | - | - | -10 | - | +10 | ns | * |
| Built-in slow-CR oscillation frequency | F _{CRS} | - | - | 50 | 100 | 150 | kHz | |
| Built-in fast-CR oscillation frequency | F _{CRF} | - | - | 2.4 | 4 | 6.0 | MHz | |
| PLL input clock frequency | F _{PLLI} | - | - | - | 4 | - | MHz | |
| PLL macro oscillation clock frequency | F _{PLLO} | - | - | 400 | - | 576 | MHz | |
| SSCG-PLL input clock frequency | F _{SSCGPLLI} | - | - | - | 4 | - | MHz | |
| SSCG-PLL macro oscillation clock frequency | F _{SSCGPLLO} | - | - | 400 | - | 576 | MHz | |

*: The maximum/minimum values have been standardized with the main clock and PLL clock in use.



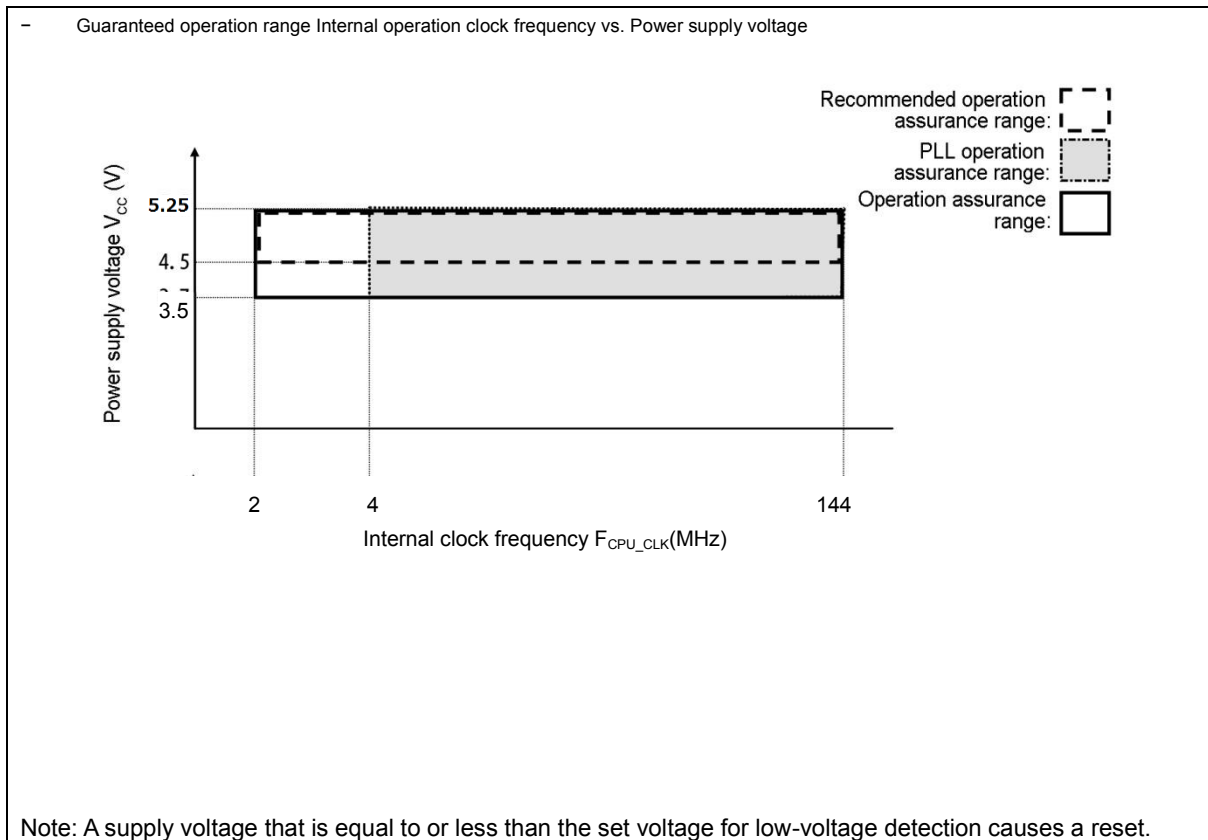


10.4.2 Internal Clock Timing

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|--------------------------|--------------|----------|------------|-------|-----|-----|------------|-------------|
| | | | | Min | Typ | Max | | |
| Internal clock frequency | FCLK_CPU | - | - | - | - | 144 | MHz | CLK_CPU |
| | FCLK_FCLK | - | - | - | - | 72 | MHz | CLK_FCLK |
| | FCLK_ATB | - | - | - | - | 72 | MHz | CLK_ATB |
| | FCLK_DBG | - | - | - | - | 72 | MHz | CLK_DBG |
| | FCLK_HPM | - | - | - | - | 36 | MHz | CLK_HPM |
| | FCLK_HPM2 | - | - | - | - | 18 | MHz | CLK_HPM2 |
| | FCLK_DMA | - | - | - | - | 36 | MHz | CLK_DMA |
| | FCLK_MEMC | - | - | - | - | 36 | MHz | CLK_MEMC |
| | FCLK_SYSC1 | - | - | - | - | 36 | MHz | CLK_SYSC1 |
| | FCLK_HAPP0A0 | - | - | - | - | 36 | MHz | CLK_HAPP0A0 |
| | FCLK_HAPP0A1 | - | - | - | - | 36 | MHz | CLK_HAPP0A1 |
| | FCLK_HAPP1B0 | - | - | - | - | 36 | MHz | CLK_HAPP1B0 |
| | FCLK_HAPP1B1 | - | - | - | - | 36 | MHz | CLK_HAPP1B1 |
| | FCLK_LLPBM | - | - | - | - | 144 | MHz | CLK_LLPBM |
| | FCLK_LLPBM2 | - | - | - | - | 72 | MHz | CLK_LLPBM2 |
| | FCLK_LCP | - | - | - | - | 72 | MHz | CLK_LCP |
| | FCLK_LCP0 | - | - | - | - | 36 | MHz | CLK_LCP0 |
| | FCLK_LCP0A | - | - | - | - | 36 | MHz | CLK_LCP0A |
| | FCLK_LAPPA0 | - | - | - | - | 36 | MHz | CLK_LAPPA0 |
| | FCLK_LAPPA0A | - | - | - | - | 36 | MHz | CLK_LAPPA0A |
| | FCLK_LAPP1 | - | - | - | - | 36 | MHz | CLK_LAPP1 |
| | FCLK_LAPP1A | - | - | - | - | 36 | MHz | CLK_LAPP1A |
| | FCLK_TRC | - | - | - | - | 36 | MHz | CLK_TRC |
| | FCLK_SYSC0H | - | - | - | - | 36 | MHz | CLK_SYSC0H |
| | FCLK_COMH | - | - | - | - | 36 | MHz | CLK_COMH |
| | FCLK_RAM0H | - | - | - | - | 36 | MHz | CLK_RAM0H |
| | FCLK_RAM1H | - | - | - | - | 36 | MHz | CLK_RAM1H |
| | FCLK_SYSC0P | - | - | - | - | 36 | MHz | CLK_SYSCP0 |
| FCLK_COMP | - | - | - | - | 36 | MHz | CLK_COMP | |
| FCLK_CANFD | - | - | - | - | 40 | MHz | CANFD_CCLK | |

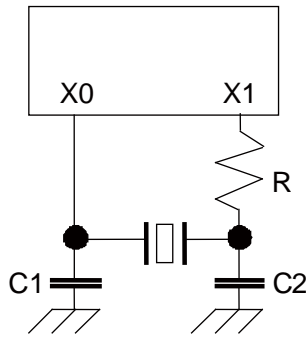
| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---------------------------|--------------|----------|------------|-------|-----|-----|----------|-------------|
| | | | | Min | Typ | Max | | |
| Internal clock cycle time | tCLK_CPU | - | - | 6.9 | - | - | ns | CLK_CPU |
| | tCLK_FCLK | - | - | 13.8 | - | - | ns | CLK_FCLK |
| | tCLK_ATB | - | - | 13.8 | - | - | ns | CLK_ATB |
| | tCLK_DBG | - | - | 13.8 | - | - | ns | CLK_DBG |
| | tCLK_HPM | - | - | 27.7 | - | - | ns | CLK_HPM |
| | tCLK_HPM2 | - | - | 55.5 | - | - | ns | CLK_HPM2 |
| | tCLK_DMA | - | - | 27.7 | - | - | ns | CLK_DMA |
| | tCLK_MEMC | - | - | 27.7 | - | - | ns | CLK_MEMC |
| | tCLK_SYSC1 | - | - | 27.7 | - | - | ns | CLK_SYSC1 |
| | tCLK_HAPP0A0 | - | - | 27.7 | - | - | ns | CLK_HAPP0A0 |
| | tCLK_HAPP0A1 | - | - | 27.7 | - | - | ns | CLK_HAPP0A1 |
| | tCLK_HAPP1B0 | - | - | 27.7 | - | - | ns | CLK_HAPP1B0 |
| | tCLK_HAPP1B1 | - | - | 27.7 | - | - | ns | CLK_HAPP1B1 |
| | tCLK_LLPBM | - | - | 6.9 | - | - | ns | CLK_LLPBM |
| | tCLK_LLPBM2 | - | - | 13.8 | - | - | ns | CLK_LLPBM2 |
| | tCLK_LCP | - | - | 13.8 | - | - | ns | CLK_LCP |
| | tCLK_LCP0 | - | - | 27.7 | - | - | ns | CLK_LCP0 |
| | tCLK_LCP0A | - | - | 27.7 | - | - | ns | CLK_LCP0A |
| | tCLK_LAPP0 | - | - | 27.7 | - | - | ns | CLK_LAPP0 |
| | tCLK_LAPP0A | - | - | 27.7 | - | - | ns | CLK_LAPP0A |
| | tCLK_LAPP1 | - | - | 27.7 | - | - | ns | CLK_LAPP1 |
| | tCLK_LAPP1A | - | - | 27.7 | - | - | ns | CLK_LAPP1A |
| | tCLK_TRC | - | - | 27.7 | - | - | ns | CLK_TRC |
| | tCLK_SYSC0H | - | - | 27.7 | - | - | ns | CLK_SYSC0H |
| | tCLK_COMH | - | - | 27.7 | - | - | ns | CLK_COMH |
| | tCLK_RAM0H | - | - | 27.7 | - | - | ns | CLK_RAM0H |
| | tCLK_RAM1H | - | - | 27.7 | - | - | ns | CLK_RAM1H |
| | tCLK_SYSC0P | - | - | 27.7 | - | - | ns | CLK_SYSC0P |
| tCLK_COMP | - | - | 27.7 | - | - | ns | CLK_COMP | |
| tCLK_CANFD | | | | 25.0 | - | - | ns | CANFD_CCLK |



Relationship between the oscillation clock frequency and internal clock frequency

| Oscillation Clock Frequency | Main Clock | PLL Multiplier Setting | PLL Output Division Setting | PLL Clock |
|-----------------------------|------------|------------------------|-----------------------------|-----------|
| 4 MHz | 4 MHz | 144 | 4 | 144 MHz |
| 4 MHz | 4 MHz | 144 | 6 | 96 MHz |

- Oscillation circuit example



Note:

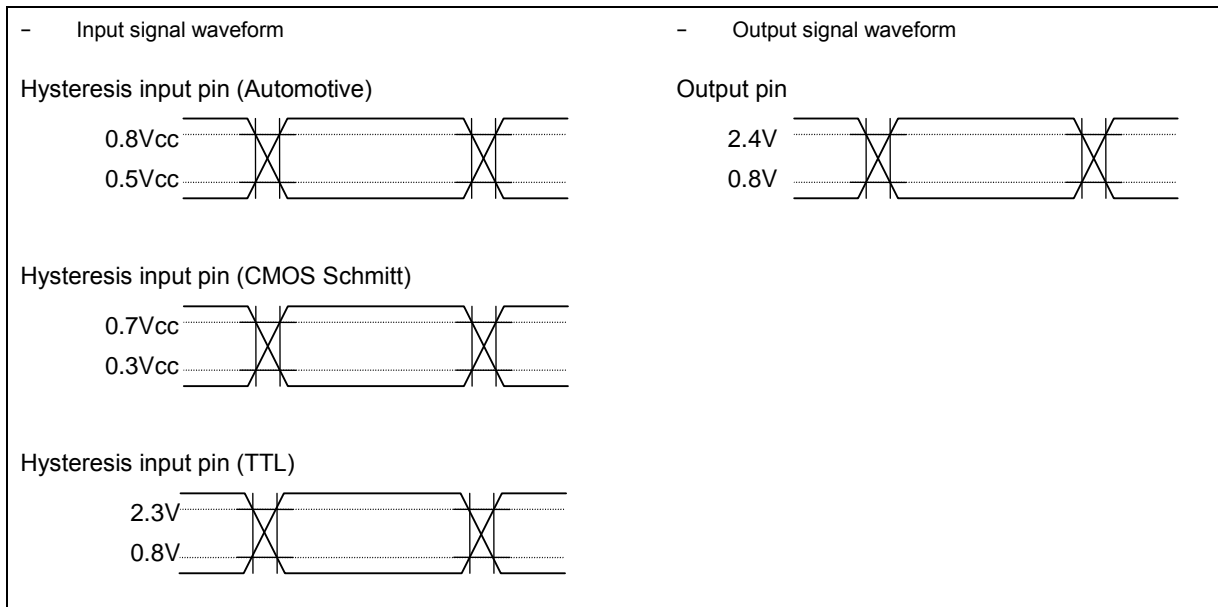
- When configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.
- The maximum PLL clock frequency must be 144MHz.

Output division configuration can be set by the following.

- PLLDIVM bit in SYSC0_RUNPLL0CNTR register
- PLLDIVM bit in SYSC0_PSSPLL0CNTR register
- SSCGDIVM bit in SYSC0_RUNSSCG0CNTR0 register
- SSCGDIVM bit in SYSC0_PSSSSCG0CNTR0 register

(e.g. If PLLout is 576MHz, these settings must be configured as "multiply by 4" and over multiplication setting)

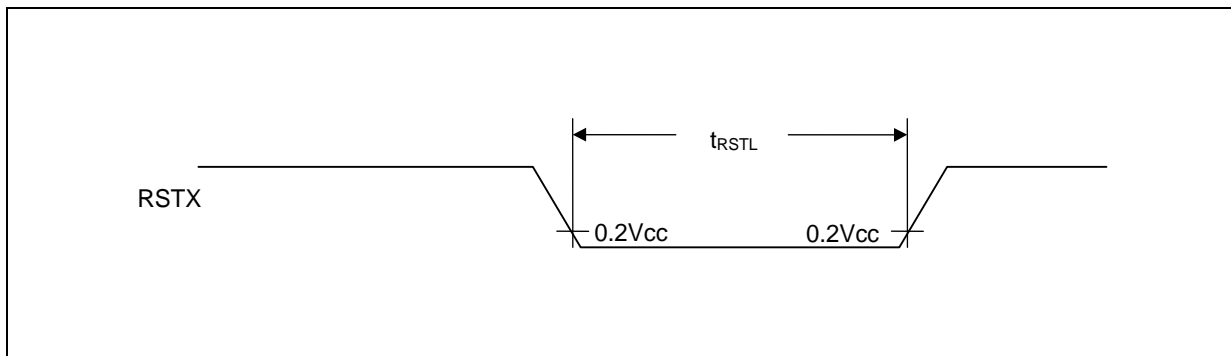
AC characteristics are specified by the following measurement reference voltage values



10.4.3 Reset Input

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------------------|-------------------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Reset input time | t _{RSTL} | RSTX | - | 10 | - | μs | |
| Width for reset input removal | | | | 1 | - | μs | |



10.4.4 Power-on Conditions

(TA: Recommended operating conditions, V_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|------------------|----------|-------------------------------------|-------|------|------|-------|---------|
| | | | | Min | Typ | Max | | |
| Level detection voltage | - | VCC | - | 2.15 | 2.35 | 2.55 | V | |
| Level release voltage | - | VCC | - | 2.25 | 2.45 | 2.65 | V | |
| Level detection hysteresis width | - | VCC | - | - | 100 | - | mV | |
| Level detection time | - | - | - | - | - | 540 | μs | *1 |
| Power off time | t _{OFF} | VCC | - | 1 | - | - | ms | *2 |
| Power ramp rate | dV/dt | VCC | VCC: 0.2V to 2.55V | - | - | 6 | mV/μs | *3 |
| Maximum ramp rate guaranteed to not generate power-on reset | dV/dt | VCC | VCC: Between 2.6V and 4.5V | - | - | 50 | mV/μs | *4 |

*1: If a power fluctuation precedes the low-voltage detection time, the detection may occur or be canceled after the supply voltage passes the detection voltage range.

*2: If V_{CC} is held below 0.2V for a minimum period of t_{OFF}, power-on reset will occur. If t_{OFF} is not satisfied, power-on reset will still occur if the power ramp rate is kept below 6mV/μs.

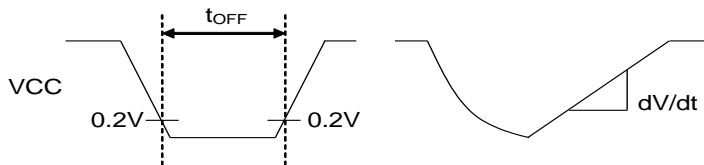
*3: This is the power ramp rate with which power-on reset will always occur regardless of power-off time, as mentioned in *2.

*4: When V_{CC} is within 2.6V - 4.5V, and V_{CC} fluctuation is below 50mV/us, the power-on reset is suppressed. Between 4.5V - 5.5V, the power-on reset does not occur with any V_{CC} fluctuation.

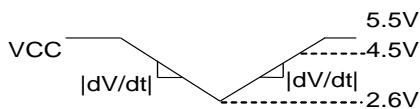
Note:

- When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and at any brownout event.

• Power off time, Power ramp rate at Power-on



• Maximum ramp rate guaranteed to not generate power-on reset



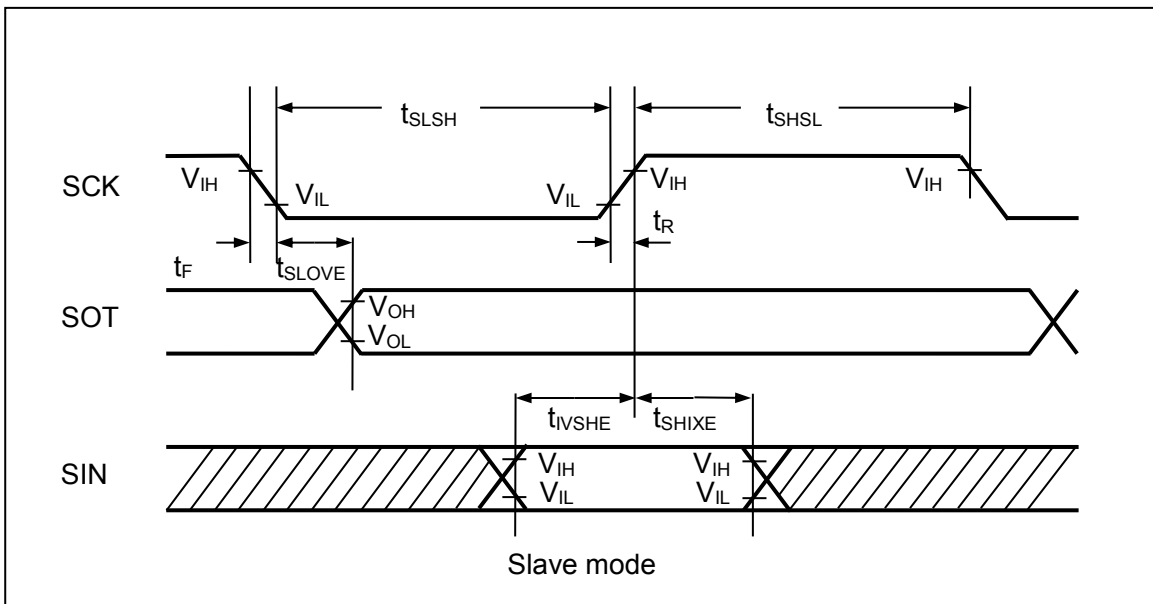
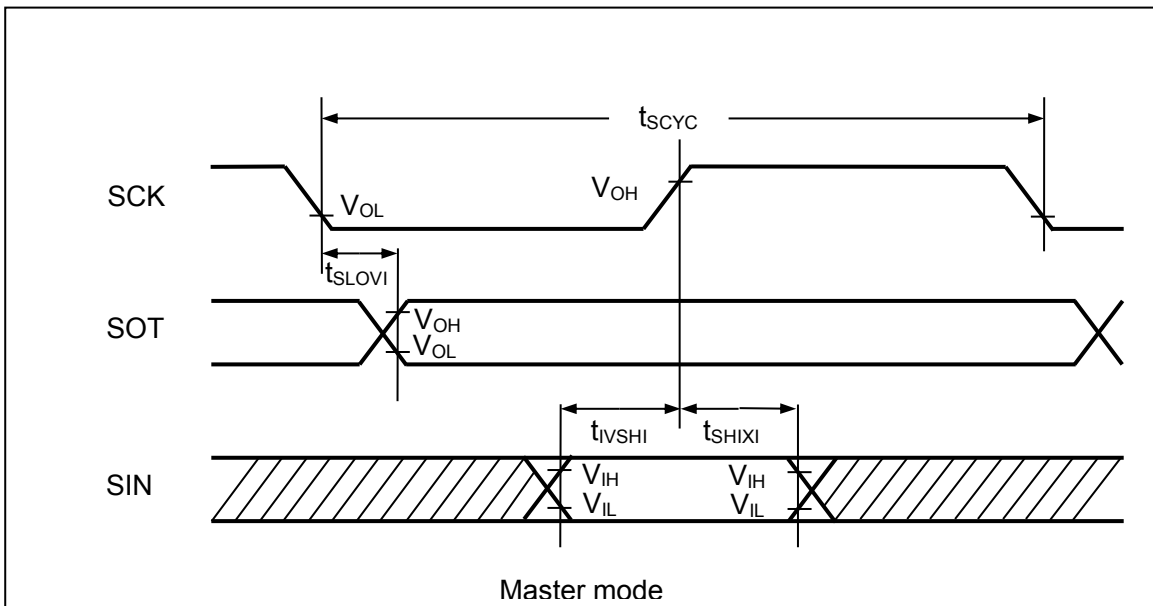
10.4.5 Multi-Function Serial
10.4.5.1 CSIO timing (SMR:MD2-0=010B)
(5-1-1) Normal Synchronous Transfer (SCR:SPI=0) and Serial Clock Output Signal Detect Level "H" (SMR:SCINV=0)

 (T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|--------------------|---------------------------------|---|-----------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t _{SCYC} | SCK0 to SCK21 | Master mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 4t _{CLK_LCP0A} | - | ns | |
| SCK ↓ → SOT delay time | t _{SLOVI} | SCK0 to SCK21 SOT0 to SOT21 | | -30 | +30 | ns | |
| Valid SIN → SCK ↑ setup time | t _{IVSHI} | SCK0 to SCK21, SIN0 to SIN21 | | 30 | - | ns | |
| SCK ↑ → Valid SIN hold time | t _{SHIXI} | | | 0 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | SCK0 to SCK21 | Slave mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CLK_LCP0A} +10 | - | ns | |
| Serial clock "L" pulse width | t _{SLSH} | | | 2t _{CLK_LCP0A} -10 | - | ns | |
| SCK ↓ → SOT delay time | t _{SLOVE} | SCK0 to SCK21, SOT0 to SOT21 | | - | 45 | ns | |
| Valid SIN → SCK ↑ setup time | t _{IVSHE} | SCK0 to SCK21, SIN0 to SIN21 | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | t _{SHIXE} | | | 20 | - | ns | |
| SCK falling time | t _F | SCK0 to SCK21 | | - | 5 | ns | |
| SCK rising time | t _R | SCK0 to SCK21 | | - | 5 | ns | |

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



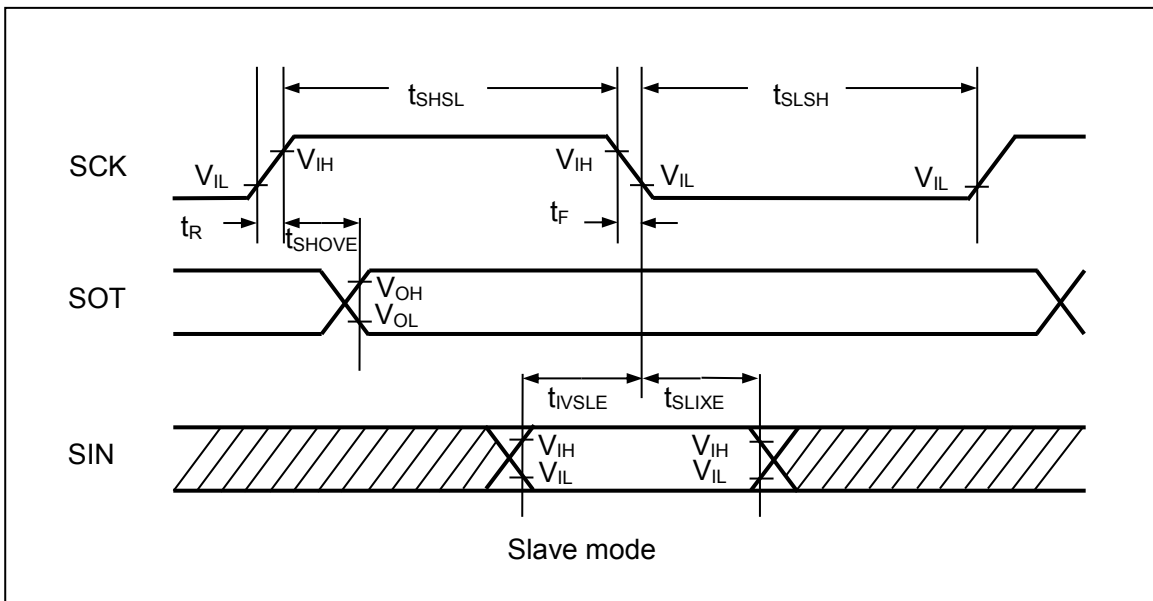
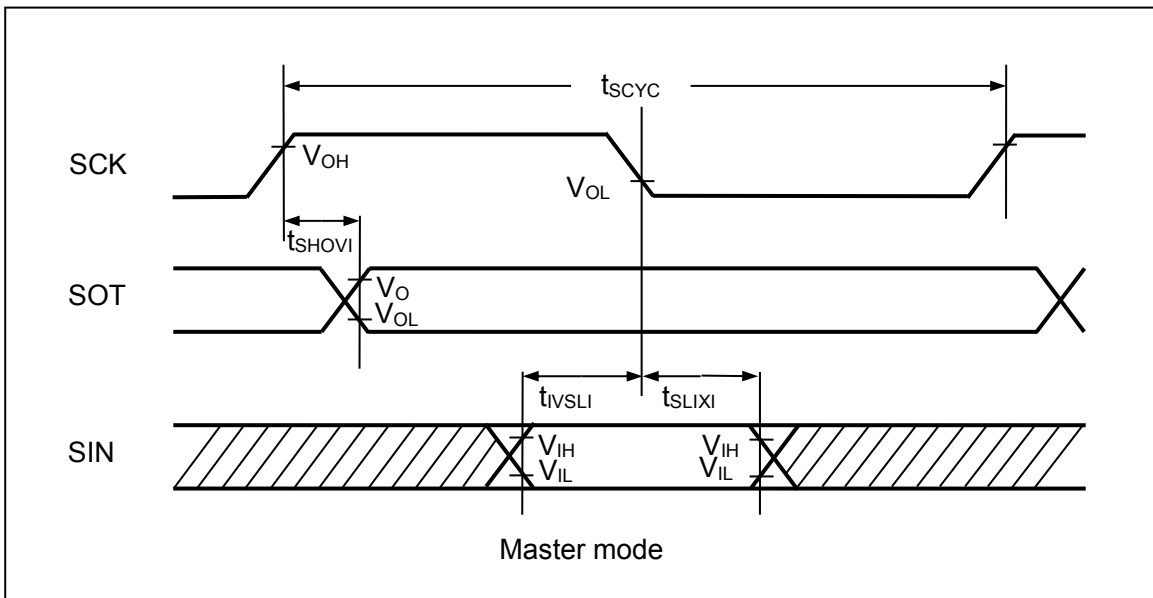
**(5-1-2) Normal Synchronous Transfer (SCR:SPI=0) and Serial Clock Output Signal Detect Level "L"
(SMR:SCINV=1)**

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|-------------|---------------------------------|--|------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK21 | Master mode ($C_L=50pF$, $I_{OL}=-2mA$, $I_{OH}=2mA$), ($C_L=20pF$, $I_{OL}=-1mA$, $I_{OH}=1mA$) | $4t_{CLK_LCP0A}$ | - | ns | |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVI} | SCK0 to SCK21, SOT0 to SOT21 | | -30 | +30 | ns | |
| Valid SIN \rightarrow SCK \downarrow setup time | t_{IVSLI} | SCK0 to SCK21, SIN0 to SIN21 | | 30 | - | ns | |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXI} | | | 0 | - | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK0 to SCK21 | Slave mode ($C_L=50pF$, $I_{OL}=-2mA$, $I_{OH}=2mA$), ($C_L=20pF$, $I_{OL}=-1mA$, $I_{OH}=1mA$) | $t_{CLK_LCP0A} + 10$ | - | ns | |
| Serial clock "L" pulse width | t_{SLSH} | | | $2t_{CLK_LCP0A} - 10$ | - | ns | |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVE} | SCK0 to SCK21, SOT0 to SOT21 | | - | 45 | ns | |
| Valid SIN \rightarrow SCK \downarrow setup time | t_{IVSLE} | SCK0 to SCK21, SIN0 to SIN21 | | 10 | - | ns | |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXE} | | | 20 | - | ns | |
| SCK falling time | t_F | SCK0 to SCK21 | | - | 5 | ns | |
| SCK rising time | t_R | SCK0 to SCK21 | | - | 5 | ns | |

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



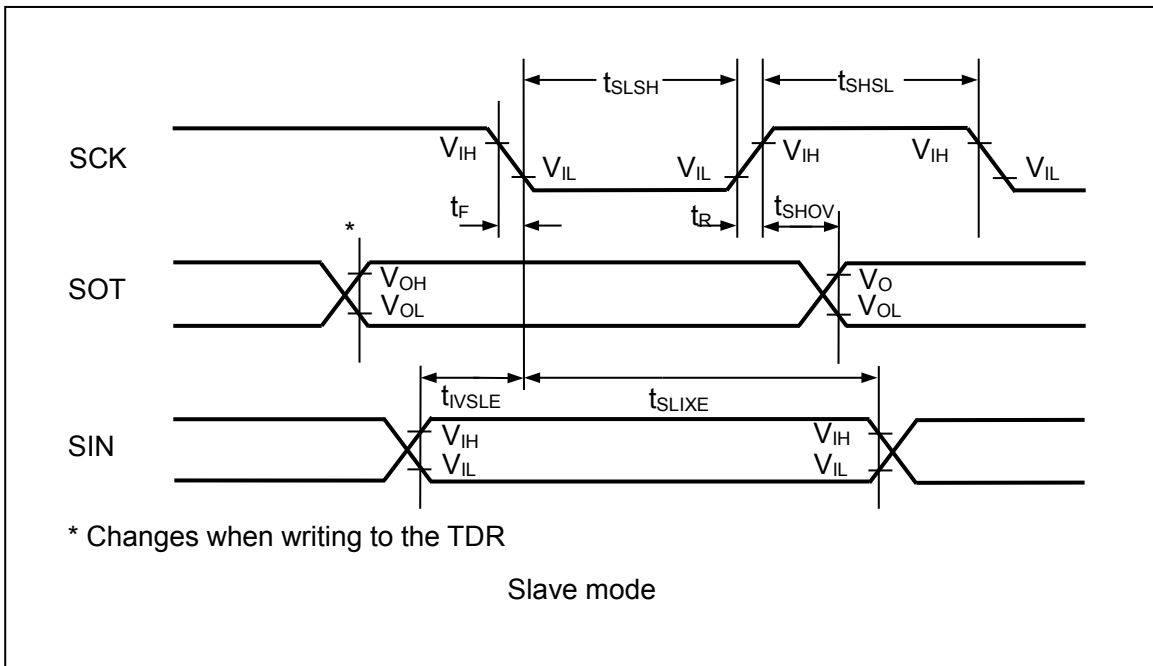
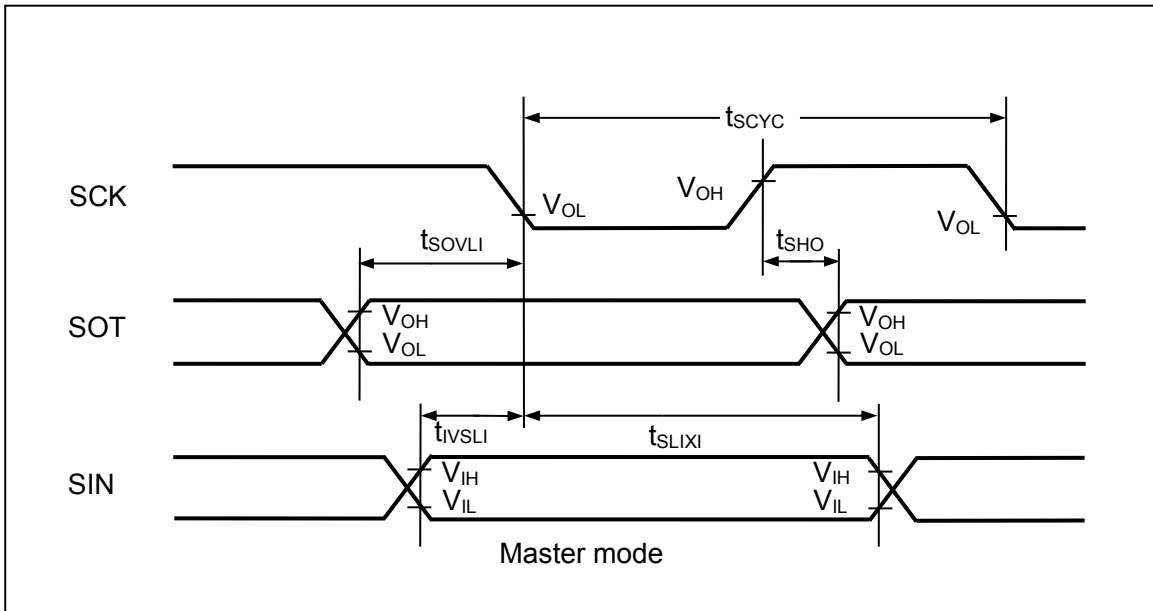
(5-1-3) SPI Compatible (SCR:SPI=1) and Serial Clock Output Signal Detect Level "H" (SMR:SCINV=0)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---|-------------|---------------------------------|--|------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK21 | Master mode ($C_L=50\text{pF}$, $I_{OL}=-2\text{mA}$, $I_{OH}=2\text{mA}$), ($C_L=20\text{pF}$, $I_{OL}=-1\text{mA}$, $I_{OH}=1\text{mA}$) | $4t_{CLK_LCP0A}$ | - | ns | |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVI} | SCK0 to SCK21, SOT0 to SOT21 | | -30 | +30 | ns | |
| Valid SIN \rightarrow SCK \downarrow setup time | t_{IVSLI} | SCK0 to SCK21, SIN0 to SIN21 | | 30 | - | ns | |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXI} | | | 0 | - | ns | |
| SOT \rightarrow SCK \downarrow delay time | t_{SOVLI} | SCK0 to SCK21, SOT0 to SOT21 | | $2t_{CLK_LCP0A} - 30$ | - | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK0 to SCK21 | Slave mode ($C_L=50\text{pF}$, $I_{OL}=-2\text{mA}$, $I_{OH}=2\text{mA}$), ($C_L=20\text{pF}$, $I_{OL}=-1\text{mA}$, $I_{OH}=1\text{mA}$) | $t_{CLK_LCP0A} + 10$ | - | ns | |
| Serial clock "L" pulse width | t_{SLSH} | | | $2t_{CLK_LCP0A} - 10$ | - | ns | |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVE} | SCK0 to SCK21, SOT0 to SOT21 | | - | 45 | ns | |
| Valid SIN \rightarrow SCK \downarrow setup time | t_{IVSLE} | SCK0 to SCK21, SIN0 to SIN21 | | 10 | - | ns | |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXE} | | | 20 | - | ns | |
| SCK falling time | t_F | SCK0 to SCK21 | | - | 5 | ns | |
| SCK rising time | t_R | SCK0 to SCK21 | | - | 5 | ns | |

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



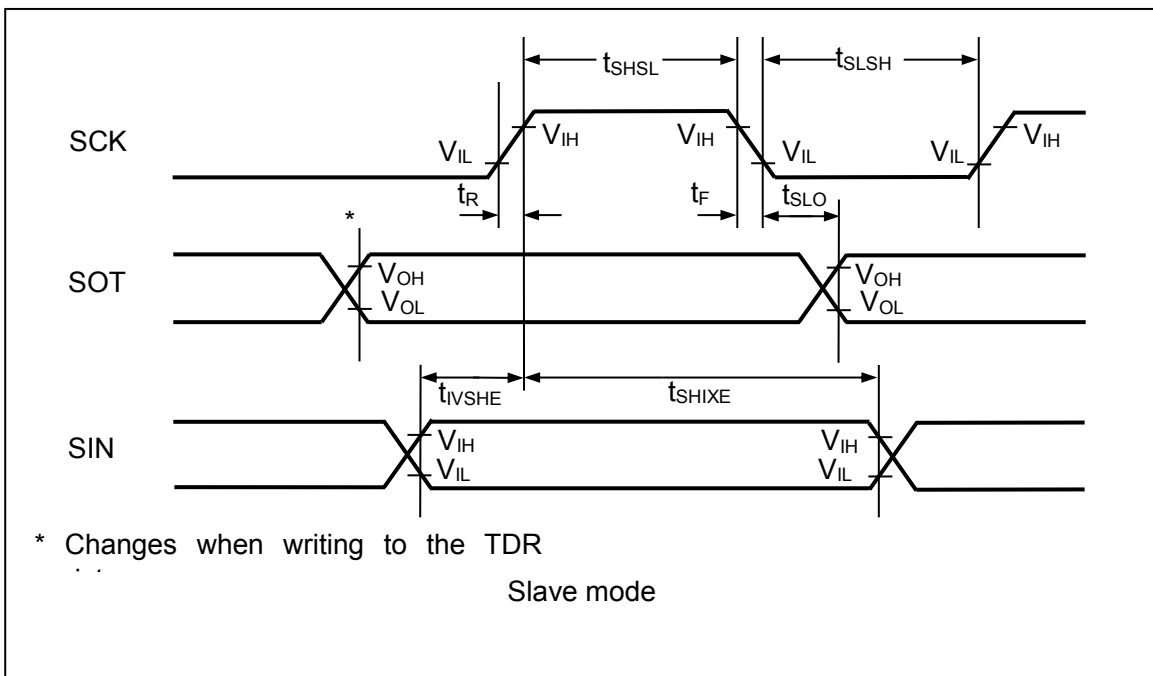
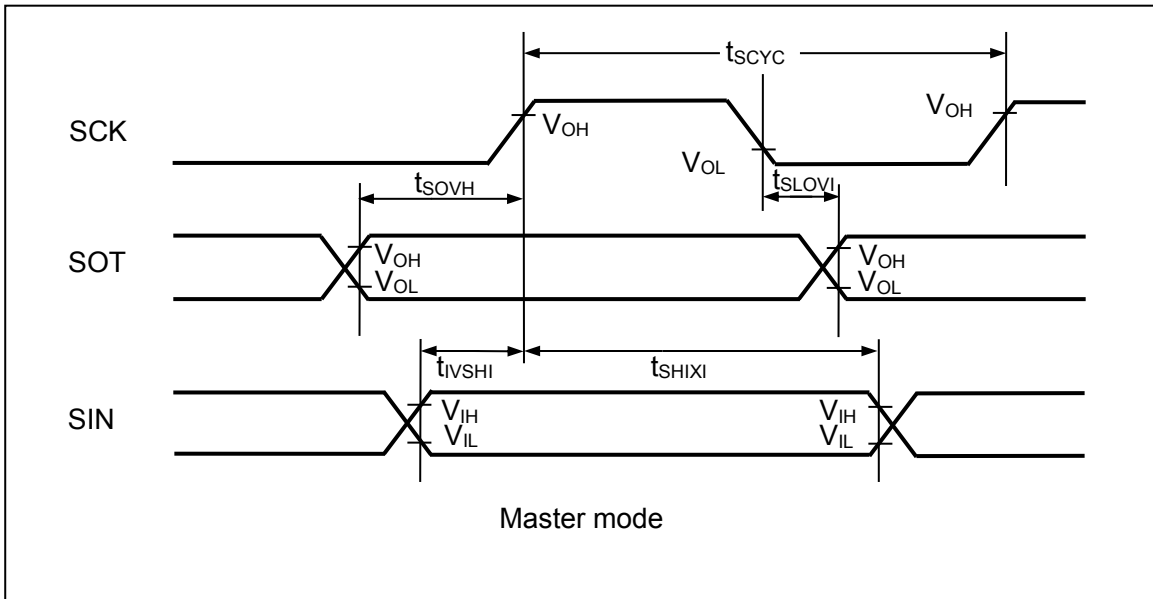
(5-1-4) SPI Compatible (SCR:SPI=1) and Serial Clock Output Signal Detect Level "L" (SMR:SCINV=1)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|-------------|----------------------------------|--|-----------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK21 | Master mode ($C_L=50\text{pF}$, $I_{OL}=-2\text{mA}$, $I_{OH}=2\text{mA}$), ($C_L=20\text{pF}$, $I_{OL}=-1\text{mA}$, $I_{OH}=1\text{mA}$) | $4t_{CLK_LCP0A}$ | - | ns | |
| SCK ↓ →SOT delay time | t_{SLOVI} | SCK0 to SCK21, SOT0 to SOT21 | | -30 | +30 | ns | |
| Valid SIN→SCK ↑ setup time | t_{IVSHI} | SCK0 to SCK21, SIN0 to SIN21 | | 30 | - | ns | |
| SCK ↑ →valid SIN hold time | t_{SHIXI} | | | 0 | - | ns | |
| SOT→SCK ↑ Delay time | t_{SOVHI} | SCK0 to SCK21, SOT0 to SOT21 | | $2t_{CLK_LCP0A} -30$ | - | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK0 to SCK21, SOT0 to SOT21 | Slave mode ($C_L=50\text{pF}$, $I_{OL}=-2\text{mA}$, $I_{OH}=2\text{mA}$), ($C_L=20\text{pF}$, $I_{OL}=-1\text{mA}$, $I_{OH}=1\text{mA}$) | $t_{CLK_LCP0A} +10$ | - | ns | |
| Serial clock "L" pulse width | t_{SLSH} | | | $2t_{CLK_LCP0A} -10$ | - | ns | |
| SCK ↓ →SOT delay time | t_{SLOVE} | SCK0 to SCK21, SOT0 to SOT21 | | - | 45 | ns | |
| Valid SIN→SCK ↑ setup time | t_{IVSHE} | SCK0 to SCK21, SSIN0 to SIN21 | | 10 | - | ns | |
| SCK ↑ →valid SIN hold time | t_{SHIXE} | | | 20 | - | ns | |
| SCK falling time | t_F | SCK0 to SCK21, SCK0 to SCK21 | | - | 5 | ns | |
| SCK rising time | t_R | | | - | 5 | ns | |

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5-1-5) Serial Chip Select Used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR, SCSFR:SCINV=0)
- Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL=1)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------------|-------------------|----------------------------------|--|---|-----------------------------|------|---------|
| | | | | Min | Max | | |
| SCS ↓ → SCK ↓ setup time | t _{CSSU} | SCK0 to SCK21 | Master mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CSSU} *1-50 | - | ns | |
| SCK ↑ → SCS ↑ hold time | t _{CSDH} | SCS0x to SCS21x | | t _{CSDH} *2+0 | - | ns | |
| SCS deselect time | t _{CSDI} | SCS0x to SCS21x | | t _{CSDS} *3-50 +5t _{CLK_LCP0A} | - | ns | |
| SCS ↓ → SCK ↓ setup time | t _{CSSE} | SCK0 to SCK21 | Slave mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCK ↑ → SCS ↑ hold time | t _{CSHE} | SCS0x to SCS21x | | 0 | - | ns | |
| SCS deselect time | t _{CSDE} | SCS0x to SCS21x | | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCS ↓ → SOT delay time | t _{DSE} | SCS0x to SCS21x | | - | 50 | ns | |
| SCS ↑ → SOT delay time | t _{DEE} | SOT0 to SOT21 | | 0 | - | ns | |
| SCK ↓ → SCS ↓ clock switch time | t _{SCC} | SCK0 to SCK21 SCS0x to SCS21x | Master mode round operation (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +0 | 3t _{CLK_LCP0A} +50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operation clock

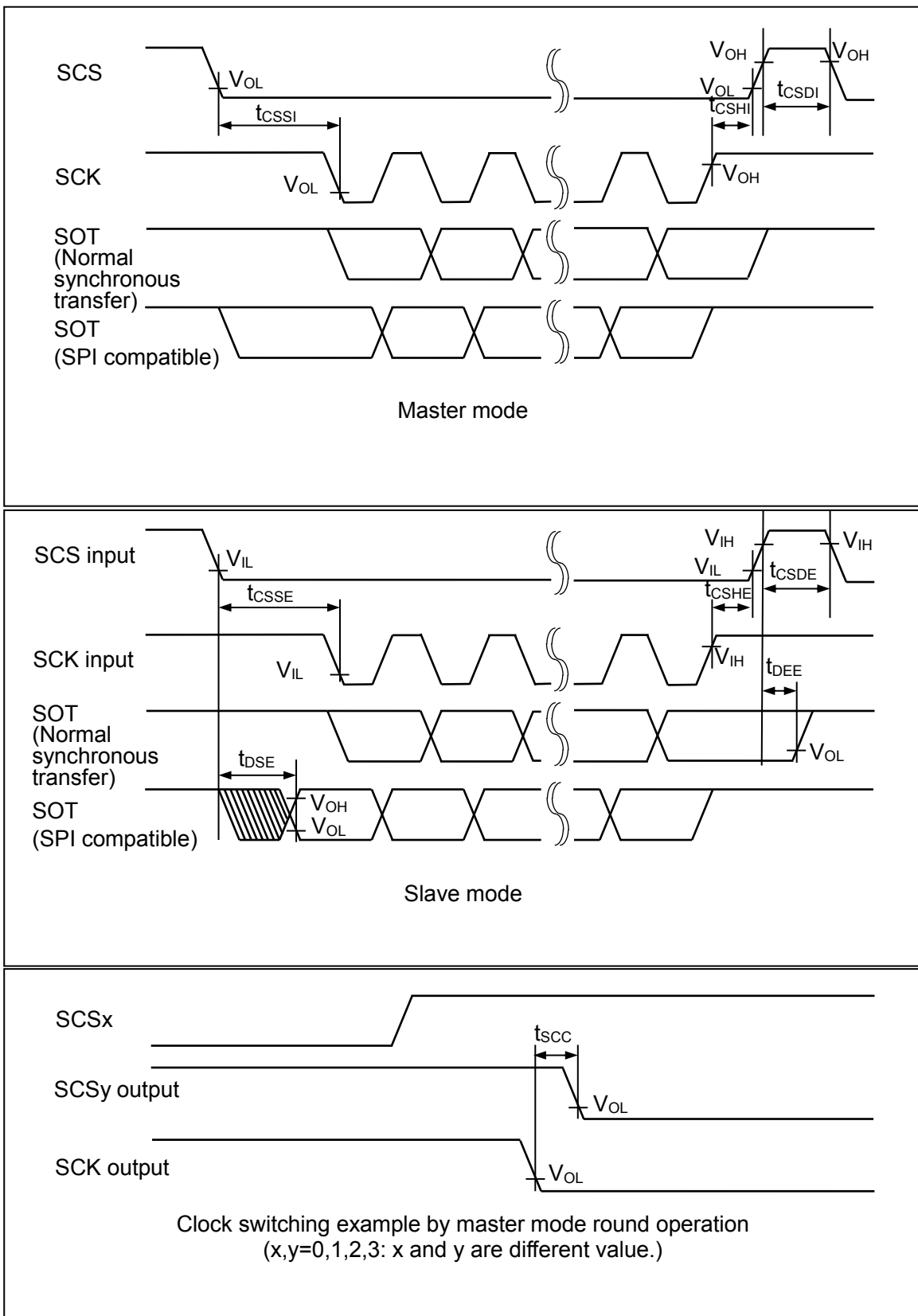
*2: t_{CSDH} = SCSTR:CSHD[7:0] x serial chip select timing operation clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operation clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

- *This is the AC characteristic in CLK synchronized mode.*
- *C_L is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*



(5-1-6) Serial Chip Select Used (SCSCR:CSSEN=1)

- Serial clock output signal detect level "L"(SMR, SCSFR:SCINV=1)
- Serial chip select inactive level "H"(SCSCR, SCSFR:CSLVL=1)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------------|-------------------|----------------------------------|--|--|----------------------------|-----------------------------|---------|
| | | | | Min | Max | | |
| SCS ↓ → SCK ↑ setup time | t _{CSSU} | SCK0 to SCK21 | Master mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CSSU} ^{*1} -50 | - | ns | |
| SCK ↓ → SCS ↑ hold time | t _{CSDH} | SCS0x to SCS21x | | t _{CSDH} ^{*2} +0 | - | ns | |
| SCS deselect time | t _{CSDI} | SCK0 to SCK21 SCS0x to SCS21x | | t _{CSDS} ^{*3} -50+5 t _{CLK_LCP0A} | - | ns | |
| SCS ↓ → SCK ↑ setup time | t _{CSSE} | SCK0 to SCK21 SCS0x to SCS21x | Slave mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCK ↓ → SCS ↑ hold time | t _{CSHE} | | | 0 | - | ns | |
| SCS deselect time | t _{CSDE} | SCS0x to SCS21x | | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCS ↓ → SOT delay time | t _{DSE} | SCS0x to SCS21x SOT0 to SOT21 | | - | 50 | ns | |
| SCS ↑ → SOT delay time | t _{DEE} | | | 0 | - | ns | |
| SCK ↑ → SCS ↓ clock switch time | t _{SCC} | SCK0 to SCK21 SCS0x to SCS21x | | Master mode round operation (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +0 | 3t _{CLK_LCP0A} +50 | ns |

 *1: t_{CSSU} = SCSTR:CSSU[7:0] x serial Chip select timing operation clock

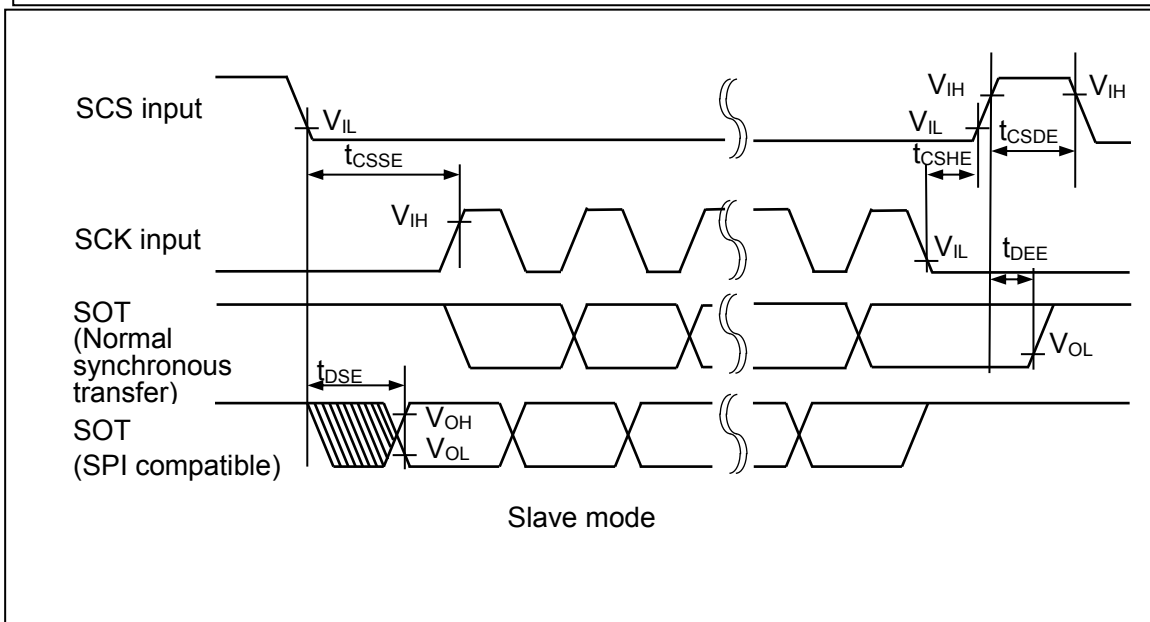
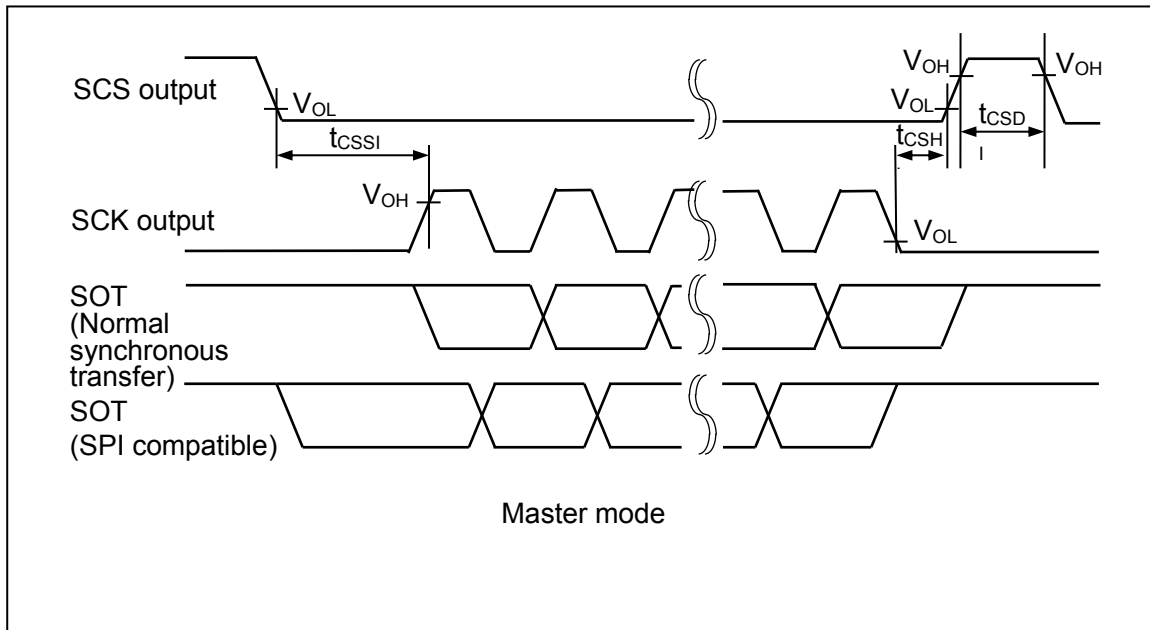
 *2: t_{CSDH} = SCSTR:CSHD[7:0] x serial Chip select timing operation clock

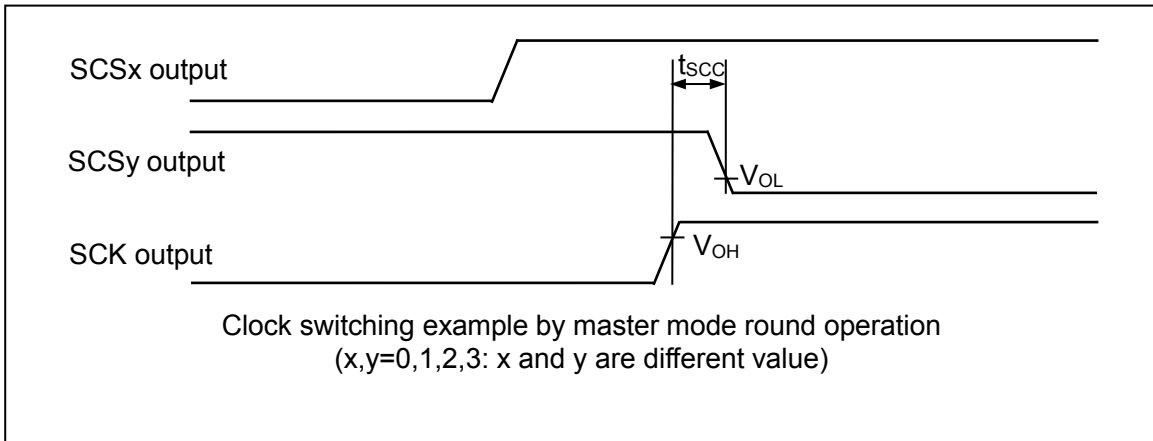
 *3: t_{CSDS} = SCSTR:CSDS[15:0] x serial Chip select timing operation clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.





(5-1-7) Serial Chip Select Used (SCSCR:CSSEN=1)

- Serial clock output signal detect level "H"(SMR, SCSFR:SCINV=0)
- Serial Chip select inactive level "L"(SCSCR, SCSFR:CSLVL=0)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------------|--------------------|----------------------------------|--|---|-----------------------------|------|---------|
| | | | | Min | Max | | |
| SCS ↑ → SCK ↓ setup time | t _{CSSI} | SCK0 to SCK21 | Master mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CSSU} ^{*1} -50 | - | ns | |
| SCK ↑ → SCS ↓ hold time | t _{CSDI} | SCS0x to SCS21x | | t _{CSDI} ^{*2} +0 | - | ns | |
| SCS deselect time | t _{CSDI} | SCS0x to SCS21x | | t _{CSDS} ^{*3} -50+5 t _{CLK_LCP0A} | - | ns | |
| SCS ↑ → SCK ↓ setup time | t _{CSSSE} | SCK0 to SCK21 | Slave mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCK ↑ → SCS ↓ hold time | t _{CSDSE} | SCS0x to SCS21x | | 0 | - | ns | |
| SCS deselect time | t _{CSDSE} | SCS0x to SCS21x | | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCS ↑ → SOT delay time | t _{DSE} | SCS0x to SCS21x | | - | 50 | ns | |
| SCS ↓ → SOT delay time | t _{DSE} | SOT0 to SOT21 | | 0 | - | ns | |
| SCK ↓ → SCS ↑ clock switch time | t _{SCC} | SCK0 to SCK21 SCS0x to SCS21x | Master mode round operation (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +0 | 3t _{CLK_LCP0A} +50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operation clock

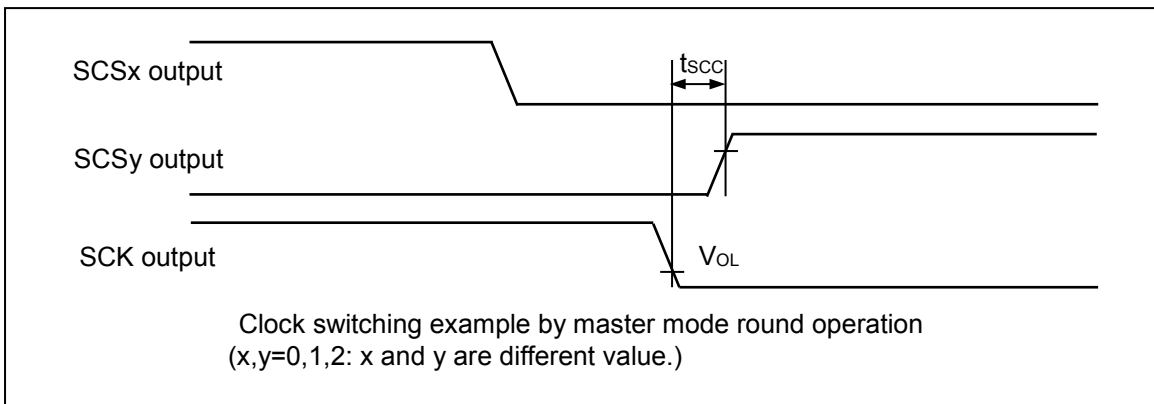
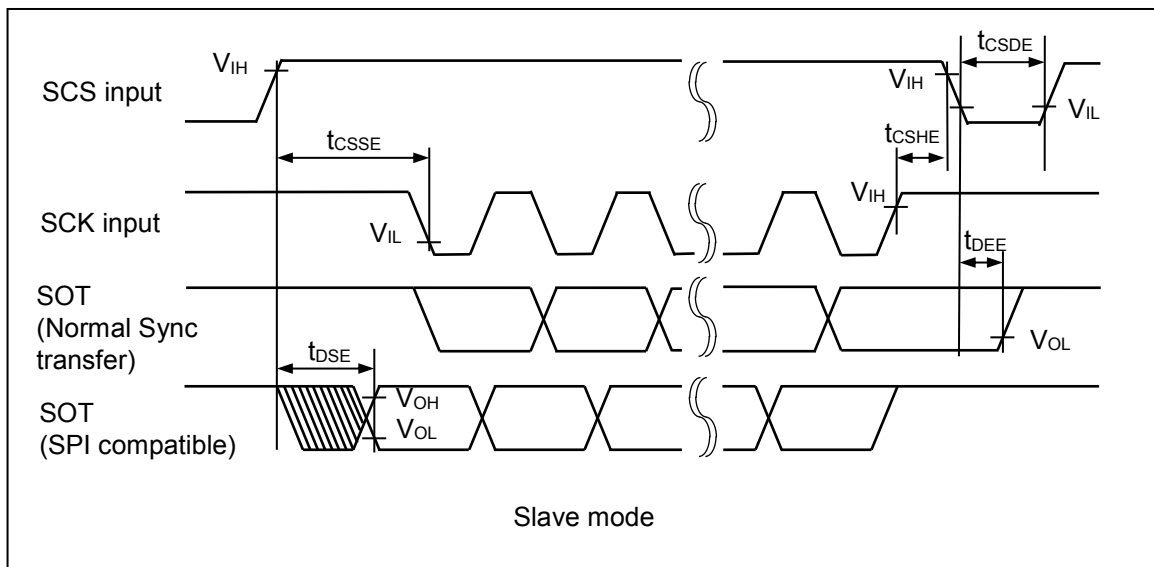
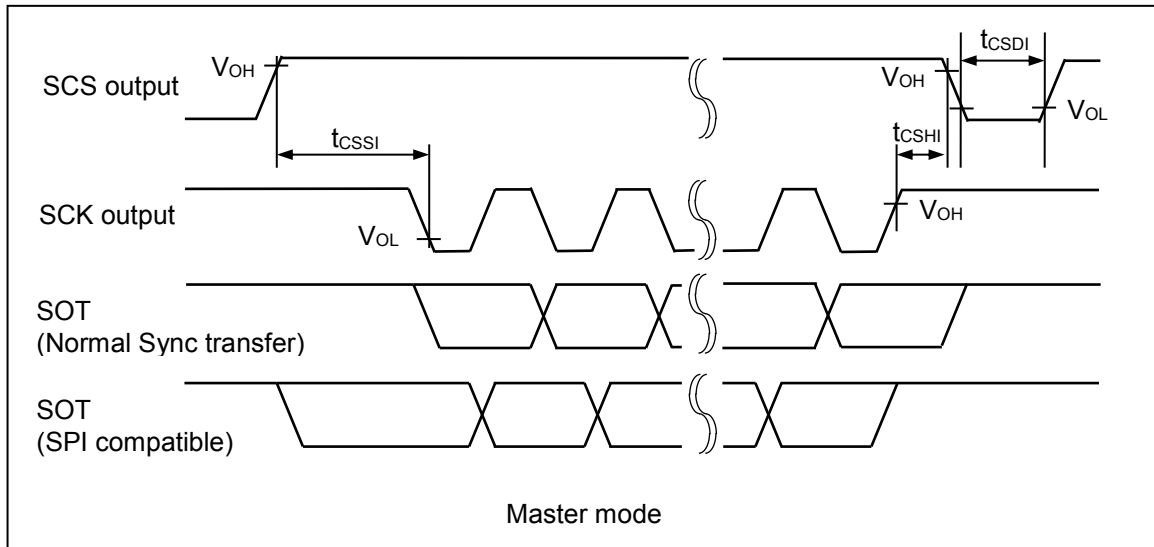
*2: t_{CSDI} = SCSTR:CSHD[7:0] x serial chip select timing operation clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operation clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

- *This is the AC characteristic in CLK synchronized mode.*
- *C_L is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual*



(5-1-8) Serial Chip Select Used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L"(SMR, SCSFR:SCINV=1)
- Serial Chip select inactive level "L"(SCSCR, SCSFR:CSLVL=0)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------------|-------------------|----------------------------------|--|---|-----------------------------|------|---------|
| | | | | Min | Max | | |
| SCS ↑ → SCK ↑ setup time | t _{CSSU} | SCK0 to SCK21 | Master mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CSSU} ^{*1} -50 | - | ns | |
| SCK ↓ → SCS ↓ hold time | t _{CSDH} | SCS0x to SCS21x | | t _{CSDH} ^{*2} +0 | - | ns | |
| SCS deselect time | t _{CSDI} | SCS0x to SCS21x | | t _{CSDS} ^{*3} -50+5 t _{CLK_LCP0A} | - | ns | |
| SCS ↑ → SCK ↑ setup time | t _{CSSE} | SCK0 to SCK21 | Slave mode (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCK ↓ → SCS ↓ hold time | t _{CSHE} | SCS0x to SCS21x | | 0 | - | ns | |
| SCS deselect time | t _{CSDE} | SCS0x to SCS21x | | 3t _{CLK_LCP0A} +30 | - | ns | |
| SCS ↑ → SOT delay time | t _{DSE} | SCS0x to SCS21x | | - | 50 | ns | |
| SCS ↓ → SOT delay time | t _{DEE} | SOT0 to SOT21 | | 0 | - | ns | |
| SCK ↑ → SCS ↑ clock switch time | t _{SCC} | SCK0 to SCK21 SCS0x to SCS21x | Master mode round operation (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | 3t _{CLK_LCP0A} +0 | 3t _{CLK_LCP0A} +50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operation clock

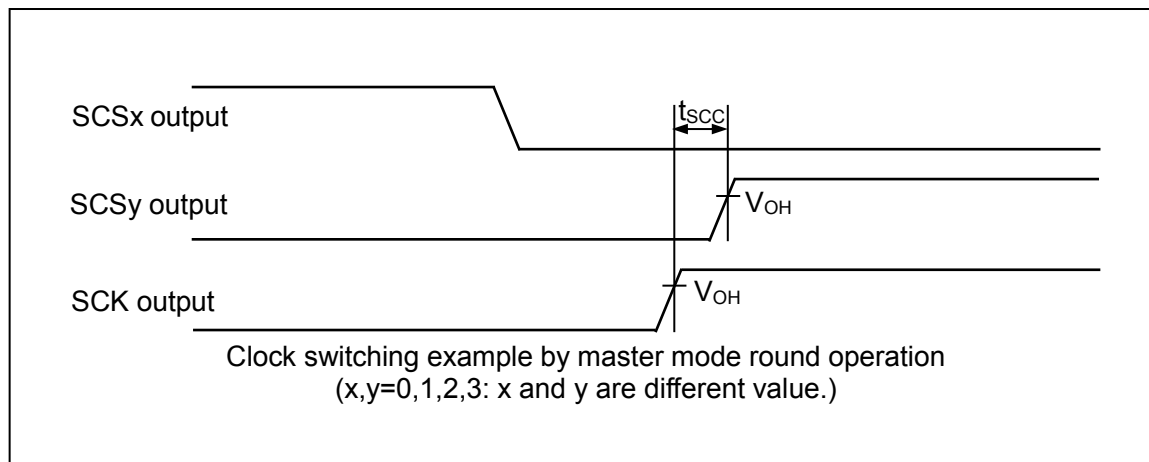
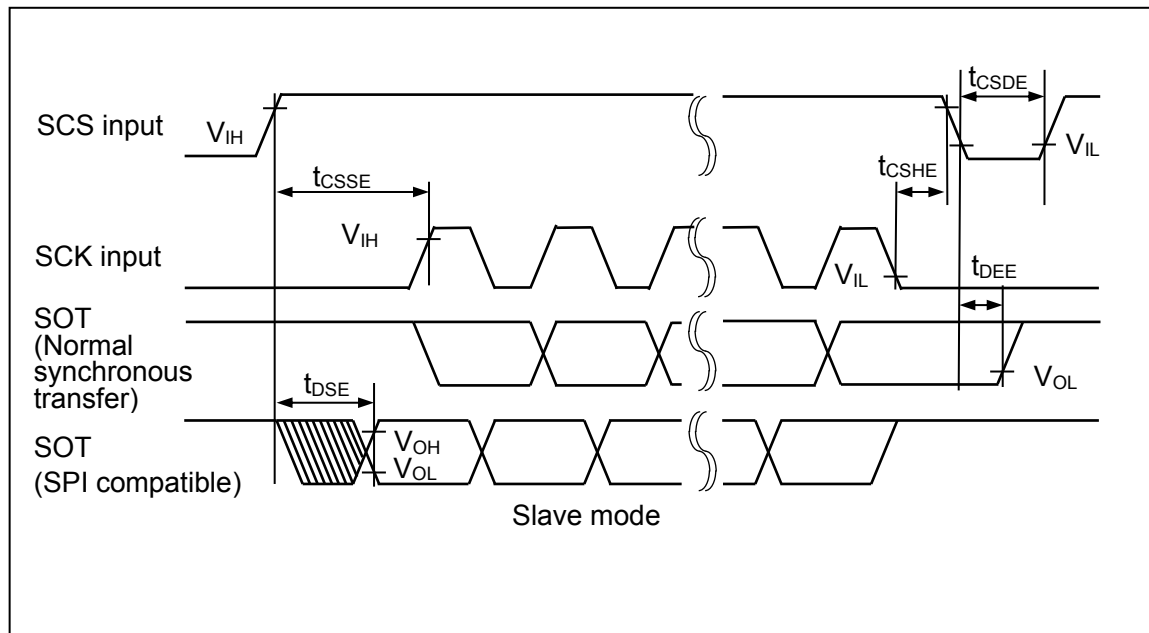
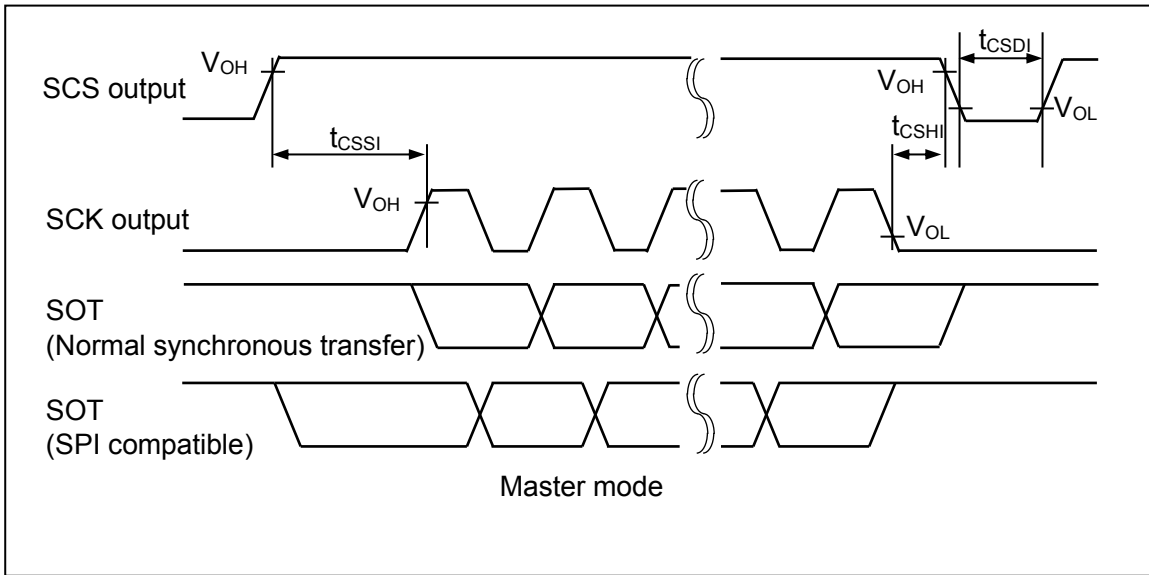
*2: t_{CSDH} = SCSTR:CSHD[7:0] x serial chip select timing operation clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operation clock

For details on *1, *2, and *3 above, see the hardware manual.

Notes:

- *This is the AC characteristic in CLK synchronized mode.*
- *C_L is the load capacitance applied to pins during testing.*
- *The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.*

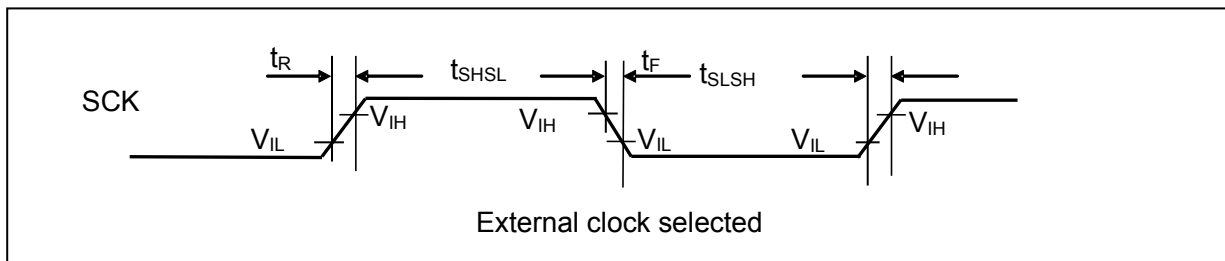


10.4.5.2 UART (Async Serial Interface) timing
(SMR:MD[2:0]=000_B, 001_B)

(5-2-1) External Clock Selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|-------------------|---------------|--|----------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | t _{SLSH} | SCK0 to SCK21 | (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CLK_LCP0A} +10 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | | | t _{CLK_LCP0A} +10 | - | ns | |
| SCK fall time | t _F | | | - | 5 | ns | |
| SCK rise time | t _R | | | - | 5 | ns | |

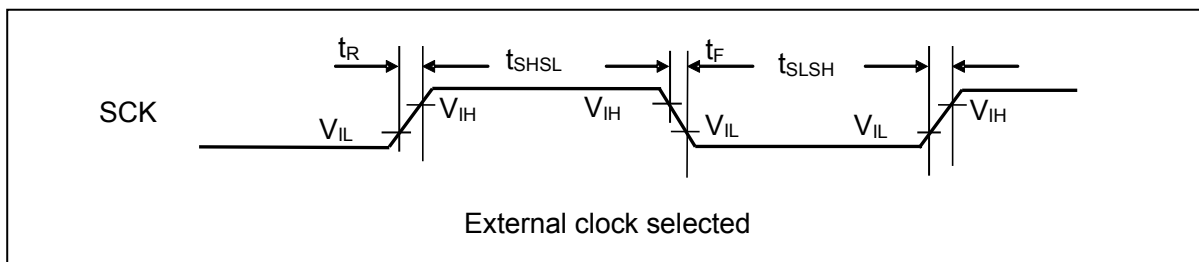


10.4.5.3 LIN interface (v2.1) (LIN Communication Control Interface (v2.1)) timing (SMR:MD[2:0]= 011B)

(5-3-1) External Clock Selected (BGR:EXT=1)

 (T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|-------------------|---------------|--|----------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | t _{SLSH} | SCK0 to SCK21 | (C _L =50pF, I _{OL} =-2mA, I _{OH} =2mA), (C _L =20pF, I _{OL} =-1mA, I _{OH} =1mA) | t _{CLK_LCP0A} +10 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | | | t _{CLK_LCP0A} +10 | - | ns | |
| SCK fall time | t _F | | | - | 5 | ns | |
| SCK rise time | t _R | | | - | 5 | ns | |



10.4.5.4 I2C timing (SMR:MD[2:0]=100B)

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Standard Mode | | Unit | Remarks |
|--|--------------------|--------------------------------|---|--------------------------------|--------------------|------|---------|
| | | | | Min | Max | | |
| SCL clock frequency | f _{SCL} | SCL0 to SCL21 | C _L =50pF, R=(V _p /I _{OL}) ⁻¹ | 0 | 100 | kHz | |
| Repeat "start" condition hold time SDA ↓ → SCL ↓ | t _{HDSTA} | SDA0 to SDA21 SCL0 to SCL21 | | 4.0 | - | μs | |
| Period of "L" for SCL clock | t _{LOW} | SCL0 to SCL21 | | 4.7 | - | μs | |
| Period of "H" for SCL clock | t _{HIGH} | | | 4.0 | - | μs | |
| Repeat "start" condition setup time SCL ↑ → SDA ↓ | t _{SUSTA} | SDA0 to SDA21 SCL0 to SCL21 | | 4.7 | - | μs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | t _{HDDAT} | | | 0 | 3.45 ^{*2} | μs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | t _{SUDAT} | | | 250 | - | ns | |
| "Stop" condition setup time SCL ↑ → SDA ↑ | t _{SUSTO} | | | 4.0 | - | μs | |
| Bus-free time between "stop" condition and "start" condition | t _{BUF} | - | | 4.7 | - | μs | |
| Noise filter | t _{SP} | - | | t _{NFT} ^{*3} | - | ns | |

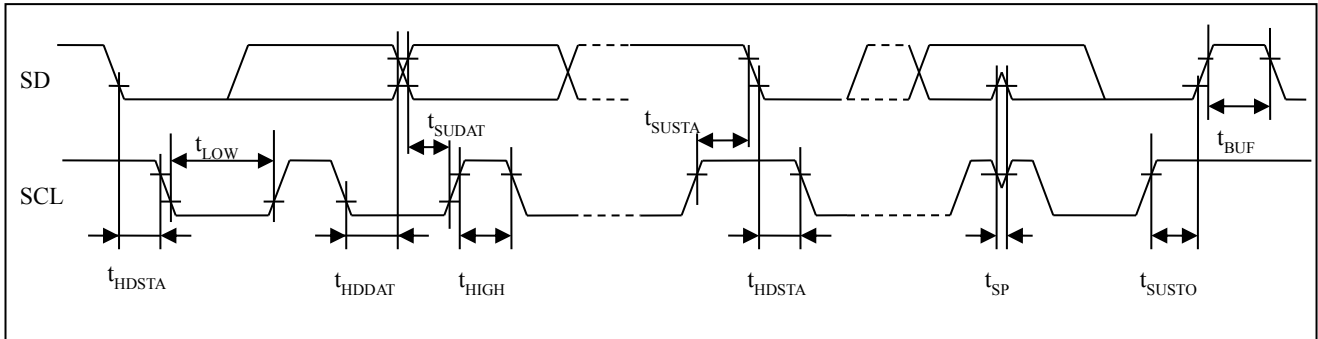
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively V_p shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the VOL guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: t_{NFT}=(NFCR:NFT[4:0]+1) x 2 x tCLK_LCP0A

Notes:

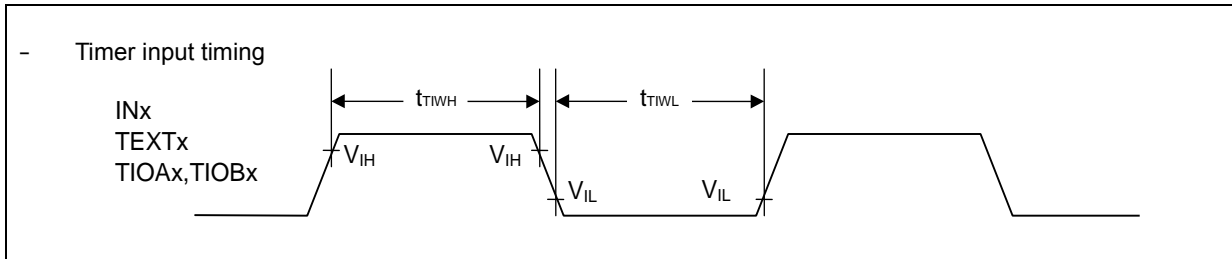
- In this device, Standard mode (Max. 100 kbps) is supported only.
- This model does not support high-speed mode. (Max. 400 kbps).
- This model does not support Min. I_{OL} = 3 mA with V_{OL} = 0.4 V.



10.5 Timer Input Timing

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

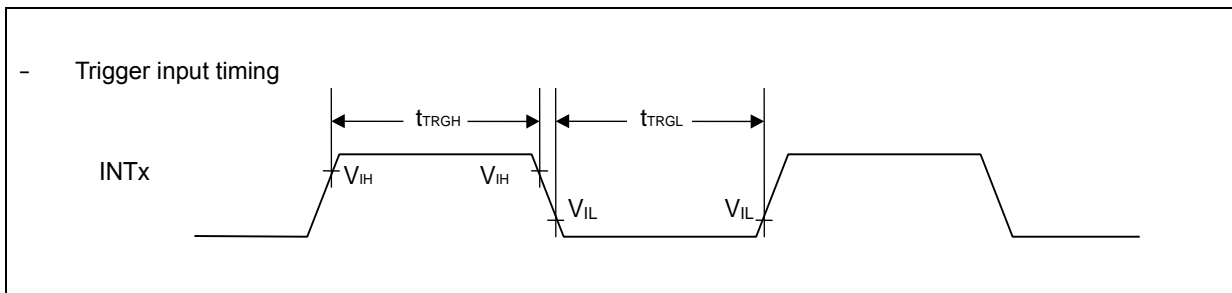
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|--------------------------|-----------------------------------|------------|-------------------|-----|------|-------------------------------|
| | | | | Min | Max | | |
| Input pulse width | t_{TWH} , t_{TWL} | IN0 to IN11 | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | | $4t_{CLK_LCP0A} < 100$ ns |
| | | TEXT0 to 5 | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | | $4t_{CLK_LCP0A} < 100$ ns |
| | | TIOA0 to TIOA29 TIOB0 to TIOB7 | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | | $4t_{CLK_LCP0A} < 100$ ns |



10.6 Trigger Input Timing

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

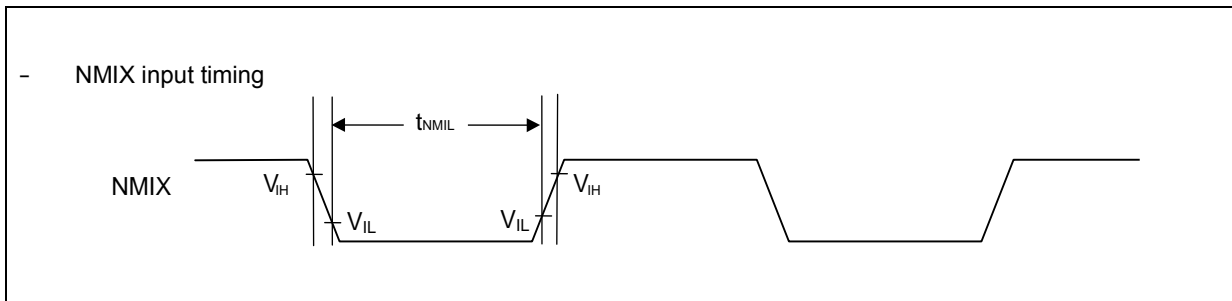
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|------------|---------------|------------|-------|-----|---------|-----------|
| | | | | Min | Max | | |
| Input pulse width | t_{TRGH} | INT0 to INT15 | - | 100 | - | ns | |
| | t_{TRGL} | INT0 to INT15 | - | 1 | - | μ s | Stop mode |



10.7 NMI Input Timing

(TA: Recommended operating conditions, Vcc=5.0 V +5%/-10%, Vss=AVss=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|------------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse width | t_{NMIL} | NMIX | - | 300 | - | ns | |



10.8 Low-Voltage Detection (External Low-Voltage Detection)

 (TA: Recommended operating conditions, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---------------------------------|------------------|----------|------------|-------|-----|------|------|--|
| | | | | Min | Typ | Max | | |
| Power supply voltage range | V _{DP5} | VCC | - | 3.5 | - | 5.25 | V | |
| Detection voltage | V _{DL0} | VCC | *1, *3 | 3.6 | 3.8 | 4.0 | V | When power-supply voltage falls and detection level is set initially |
| | V _{DL1} | VCC | *1, *4 | 3.8 | 4.0 | 4.2 | | |
| | V _{DL2} | VCC | *1, *5 | 4.0 | 4.2 | 4.4 | | |
| Hysteresis width | V _{HYS} | VCC | - | - | 100 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | T _d | - | - | - | - | 30 | μs | |
| Power supply voltage regulation | - | VCC | - | -2 | - | 2 | V/ms | *2 |

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_d), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Please suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage (V_{DL})

*3: SYSC0_RUNLVDCFGR.LVDH1V = 0100_B or SYSC0_PSSLVDCFGR.LVDH1V = 0100_B

*4: SYSC0_RUNLVDCFGR.LVDH1V = 0101_B or SYSC0_PSSLVDCFGR.LVDH1V = 0101_B

*5: SYSC0_RUNLVDCFGR.LVDH1V = 0110_B or SYSC0_PSSLVDCFGR.LVDH1V = 0110_B

10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection)

 (TA: Recommended operating conditions, $V_{SS}=AV_{SS}=0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|----------------------------|------------|----------|------------|-------|------|-----|---------------|---------------------------------|
| | | | | Min | Typ | Max | | |
| Power supply voltage range | V_{RDPS} | - | - | 0.6 | - | 1.4 | V | |
| Detection voltage* | V_{RDL} | - | *1 | 0.9 | 0.95 | 1.0 | V | When power-supply voltage falls |
| Hysteresis width | V_{RHYS} | - | - | - | 75 | - | mV | When power-supply voltage rises |
| Low-voltage detection time | T_{Rd} | - | - | - | - | 30 | μs | |

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection)

 (TA: Recommended operating conditions, $V_{SS}=AV_{SS}=0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks | Guaranteed MCU operation range |
|----------------------------|------------|----------|------------|-------|------|------|---------------|---------------------------------|--------------------------------|
| | | | | Min | Typ | Max | | | |
| Power supply voltage range | V_{RDPS} | - | - | 0.6 | - | 1.4 | V | | No |
| Detection voltage* | V_{RDL0} | - | *1, *2, *4 | 0.92 | 0.97 | 1.02 | V | When power-supply voltage falls | |
| | V_{RDL1} | - | *1, *3, *4 | 1.02 | 1.07 | 1.12 | V | | |
| Hysteresis width | V_{RHYS} | - | - | - | 75 | - | mV | When power-supply voltage rises | |
| Low-voltage detection time | T_{Rd} | - | - | - | - | 30 | μs | | |

*: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_{Rd}), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: SYSC0_RUNLVDCFGR.LVDL1V = 10_B or SYSC0_PSSLVDCFGR.LVDL1V = 10_B

*3: SYSC0_RUNLVDCFGR.LVDL1V = 11_B or SYSC0_PSSLVDCFGR.LVDL1V = 11_B

*4: These detection voltage level settings are below the minimum operation voltage.

Between these detection voltages and the minimum operation voltage, MCU functions are not guaranteed except for the low voltage detector.

Note that although the detection level is below the minimum operation voltage, the LVD reset factor flag is set as the voltage drops below the detection level.

10.11 A/D Converter

10.11.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC}=5.0 V +5%/-10%, V_{SS}=AV_{SS}=0.0 V)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|-------------------------------|------------------|-------------------------|------------------|-----|------------------|------|--|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Total Error | - | - | - | - | ±12 | LSB | *3 |
| Integral Nonlinearity | - | - | - | - | ±4.0 | LSB | *4 |
| Differential Nonlinearity | - | - | - | - | ±1.9 | LSB | *4 |
| Zero transition voltage | V _{ZT} | AN0 to AN63 | AVRL -11.5LSB | - | AVRL +12.5LSB | V | *5 |
| Full-scale transition voltage | V _{FST} | AN0 to AN63 | AVRH -13.5LSB | - | AVRH +10.5LSB | V | |
| Sampling time | t _{SMP} | - | 0.3 | - | 12 | µs | *1 |
| Compare time | t _{CMP} | - | 0.7 | - | 28 | µs | *1 |
| A/D conversion time | t _{CNV} | - | 1.0 | - | 40 | µs | *1 |
| Analog port input current | I _{AIN} | AN0 to AN63 | -1.0 | - | 1.0 | µA | V _{AVSS} ≤ V _{AIN} ≤ V _{AVCC} |
| Analog input voltage | V _{AIN} | AN0 to AN63 | AVSS | - | AVRH | V | |
| Reference voltage | AVRH | AVRH0,AVRH1 | 4.5 | - | 5.25 | V | AV _{CC} ≥ AVRH |
| | AVRL | AVRL0/AVSS0,AVRL1/AVSS1 | - | 0.0 | - | V | |
| Power supply current | I _A | AVCC | - | 500 | 900 | µA | per one unit |
| | I _{AH} | | - | 1.0 | 100 | µA | *2 |
| | I _R | AVRH | - | 1 | 2 | mA | per one unit |
| | I _{RH} | | - | - | 5.0 | µA | *2 |
| Variation between channels | - | AN0 to AN31 | - | - | 4 | LSB | |
| | | AN32 to AN63 | - | - | 4 | LSB | |

*1: Time for each channel

*2: The power supply current (V_{CC}=AV_{CC}=5.0V) is specified if the A/D converter is not operating and CPU is stopped.

*3: Total Error is a comprehensive static error that includes the linearity. 1LSB=(AVRH-AVRL)/4096

*4: 1LSB=(V_{FST}-V_{ZT})/4094

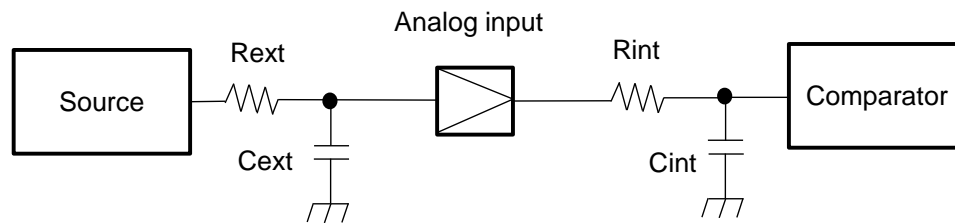
*5: 1LSB=(AVRH-AVRL)/4096

10.11.2 Notes on Using A/D Converter

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 μF) to an analog input pin.

Analog input circuit model



- R_{int} : Analog input impedance
3.9 kilohms (max) ($4.5\text{ V} \leq AV_{CC} \leq 5.25\text{ V}$)
- C_{int} : Capacitance of MCU input pin
11.0pF (max) ($4.5\text{ V} \leq AV_{CC} \leq 5.25\text{ V}$)
- R_{ext} : External driving impedance
- C_{ext} : Capacitance of PCB at A/D converter input

The following approximation formula for the replacement model above can be used:
 sampling time (minimum) = $9 \times (R_{in} + R_{ext}) \times C_{in} + R_{ext} \times C_{ext}$

Note: Listed values must be considered as reference values.

10.11.3 Definition of Terms

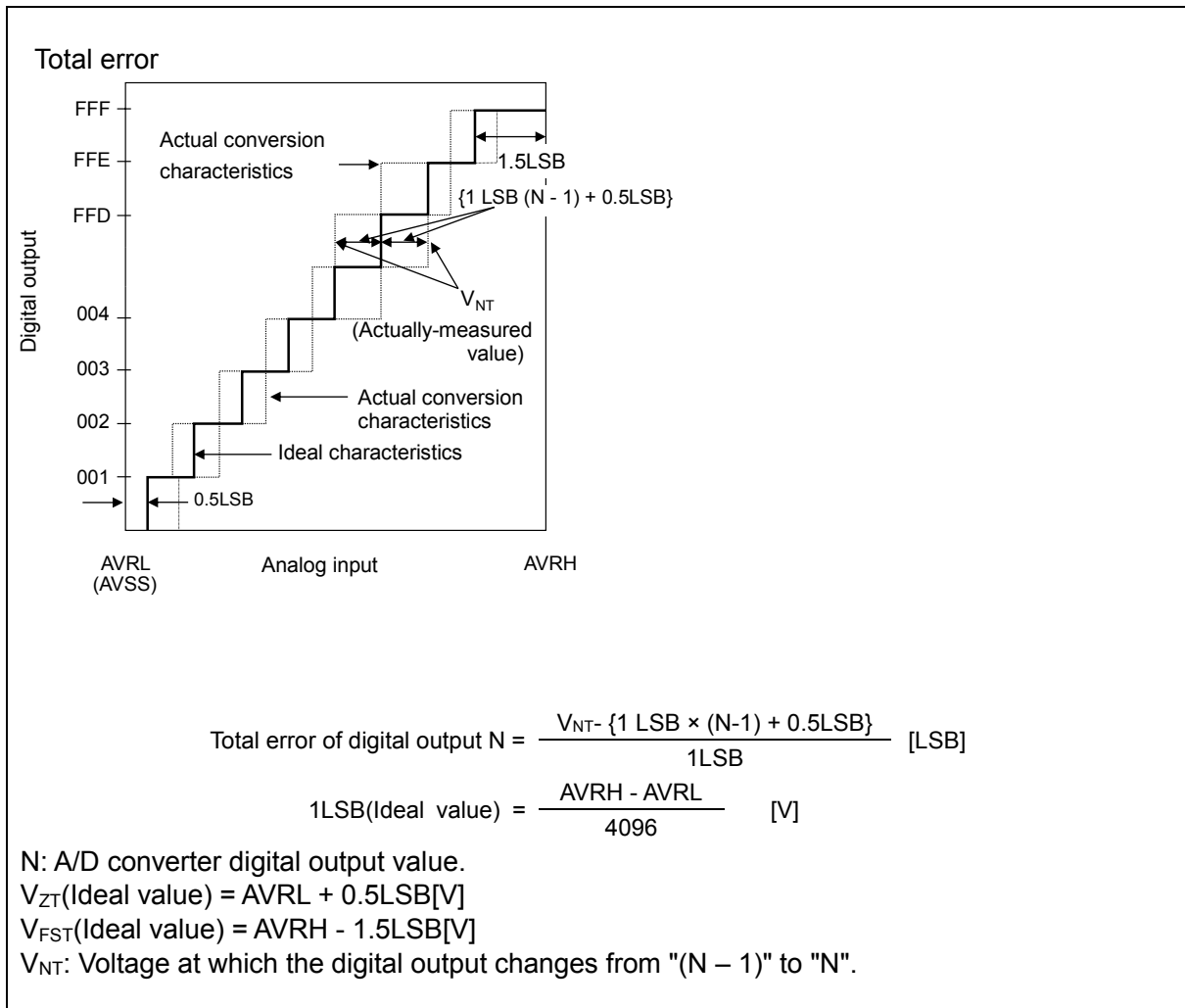
Resolution: Analog variation that is recognized by an A/D converter

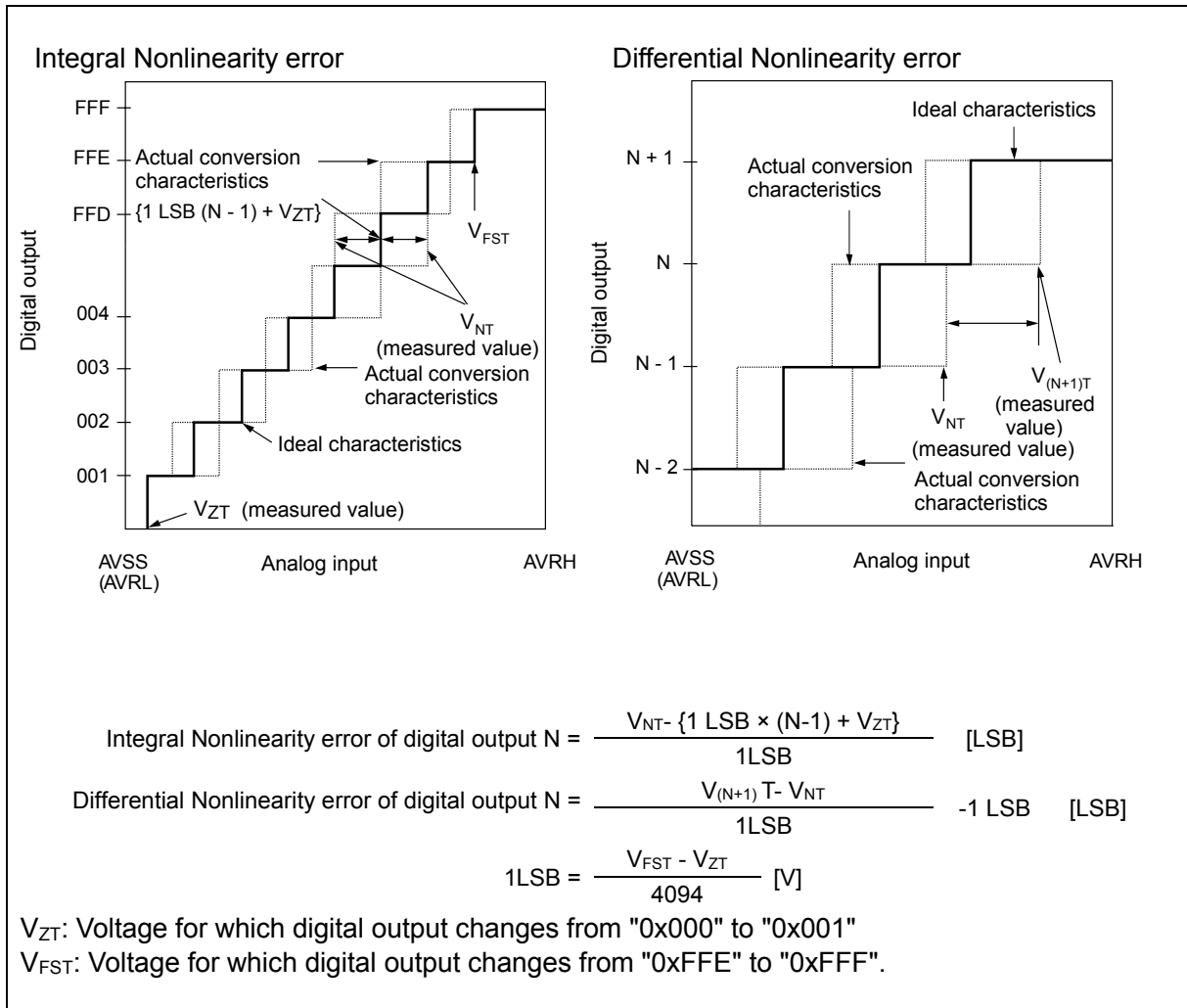
Integral Nonlinearity error ^{*1}: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non-linearity error.

Differential Nonlinearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB

Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.

*1: Represented as "Linearity error" in the former product series.





10.12 Flash Memory

| Parameter | Rating | | | Unit | Remarks |
|--|--|-----|------|------|--|
| | Min | Typ | Max | | |
| Sector erase time | - | 300 | 1100 | ms | 8-KB sector ^{*1} Internal preprogramming time included |
| | - | 800 | 3700 | ms | 64-KB sector ^{*1} Internal preprogramming time included |
| 8-bit write time | - | 15 | 288 | μs | System-level overhead time excluded ^{*1} |
| 16-bit write time | - | 19 | 384 | μs | System-level overhead time excluded ^{*1} |
| 32-bit write time | - | 27 | 567 | μs | System-level overhead time excluded ^{*1} |
| 64-bit write time | - | 45 | 945 | μs | System-level overhead time excluded ^{*1} |
| 8-bit (with ECC) write time | - | 19 | 384 | μs | System-level overhead time excluded ^{*1} |
| 16-bit (with ECC) write time | - | 23 | 483 | μs | System-level overhead time excluded ^{*1} |
| 32-bit (with ECC) write time | - | 31 | 651 | μs | System-level overhead time excluded ^{*1} |
| 64-bit (with ECC) write time | - | 49 | 1029 | μs | System-level overhead time excluded ^{*1} |
| Erase count ^{*2} / Data retention time | 1,000/20 years, 10,000/10 years, 100,000/5 years | - | - | - | Temperature at write/erase time Average temperature T _A =+85 degrees Celsius |

*1: Guaranteed value for up to 100,000 erases

*2: Number of erases for each sector

Notes:

- While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.
- In the application system where V_{CC} might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.
- To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC} at 2.7 V or more within the duration calculated by the following expression:

$$Td^{*1} [\mu s] + (1 / F_{CRF}^{*2} [MHz]) \times 1029 + 25 [\mu s]$$

*1: See "12.8 Low-voltage detection (external low-voltage detection) "

*2: See "12.4.1 Source clock timing"

11. Ordering Information

| Part Number | Package |
|-------------------|-----------------|
| S6J311EJACSE20000 | Plastic, LEP176 |
| S6J311DJACSE20000 | |
| S6J311EHACSE20000 | Plastic, LES144 |
| S6J311EHBCSE20000 | |
| S6J311DHACSE20000 | |

Note:

– S6J311xJzCSEy0000*, S6J311xHzCSEy0000*

"x"/"y" is an part number option. For the part number option, see the following table.
 For details on each package, see "PACKAGE DIMENSIONS."

* z: A/B

12. Part Number Option

| Part Number Option "x" | FLASH |
|---------------------------|---------|
| E | 4M Byte |
| D | 3M Byte |

| Part Number Option "y" | |
|---------------------------|-----------------------|
| 2 | PureSn & Halogen Free |

| Part Number Option "z" | SHE |
|---------------------------|---------|
| A | SHE ON |
| B | SHE OFF |

13. Package Dimensions

Figure 13-1 LEP176 Package Dimension

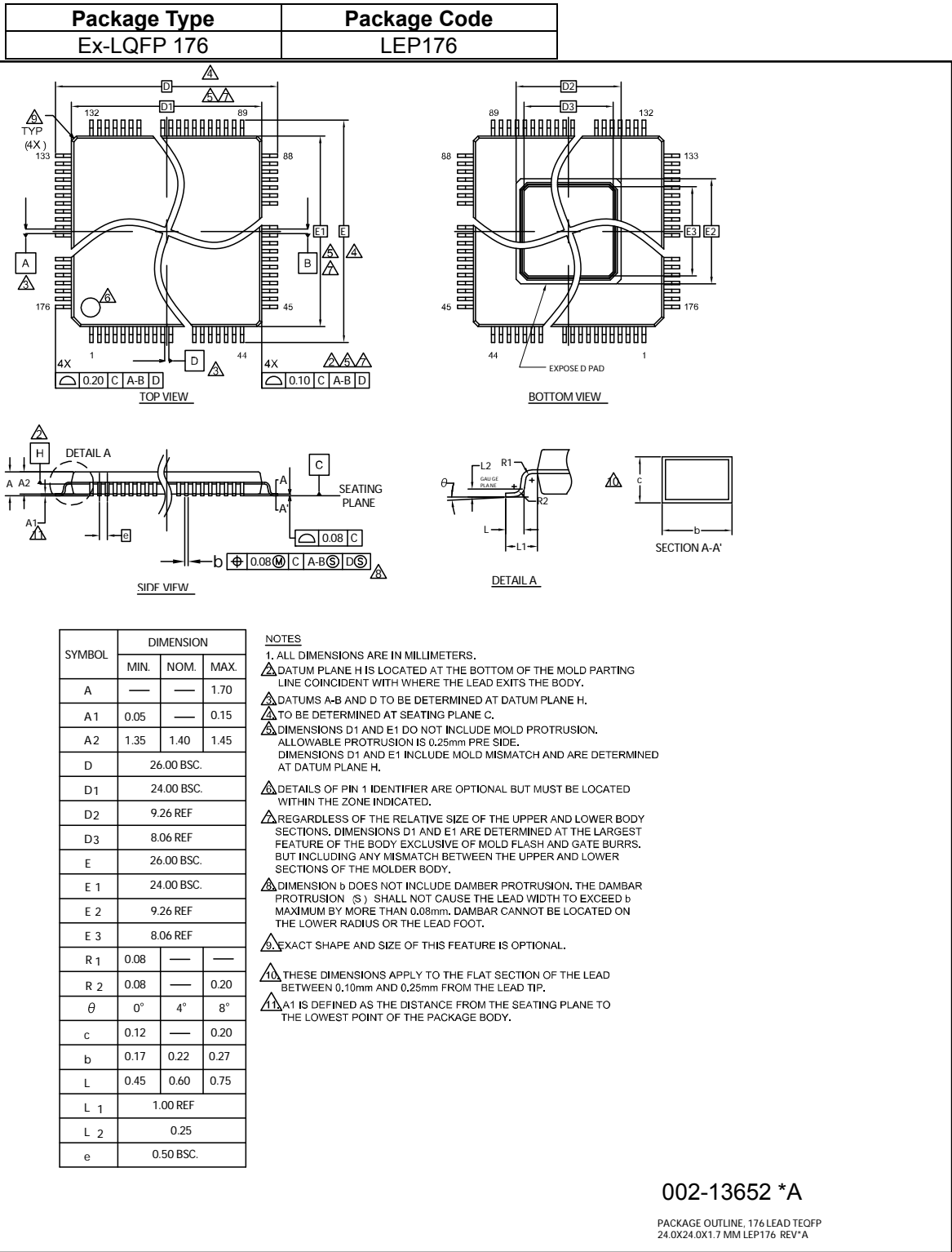
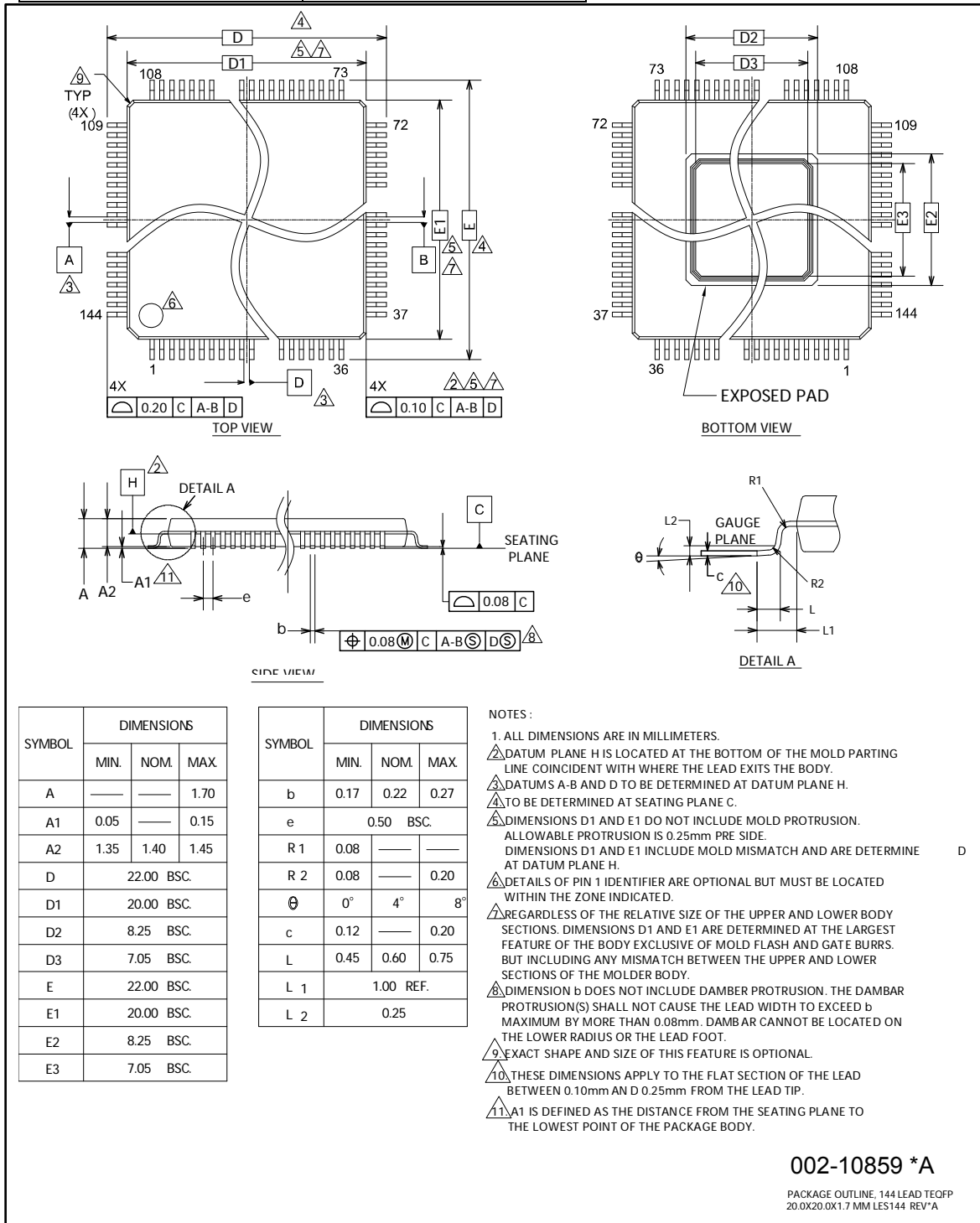


Figure 13-2 LES144 Package Dimension

| | |
|---------------------|---------------------|
| Package Type | Package Code |
| Ex-LQFP 144 | LES144 |



14. Errata

This section describes the errata for the S6J3110 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number |
|-------------------|
| S6J311EJACSE20000 |
| S6J311DJACSE20000 |
| S6J311EHACSE20000 |
| S6J311EHBCSE20000 |
| S6J311DHACSE20000 |

S6J3110 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3110 Series devices.

| Items | Part Number | Fix Status |
|---------------------------------|---|-----------------|
| MCAN wrong message transmission | S6J311EJACSE20000 S6J311DJACSE20000 S6J311EHACSE20000 S6J311EHBCSE20000 S6J311DHACSE20000 | Not be planned. |

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 Section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.
- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Request a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control field information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Define a low priority message with DLC = 0 that can be sent without harm. E.g. loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configure sufficient Tx buffers – at least two - for this message type thus that there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

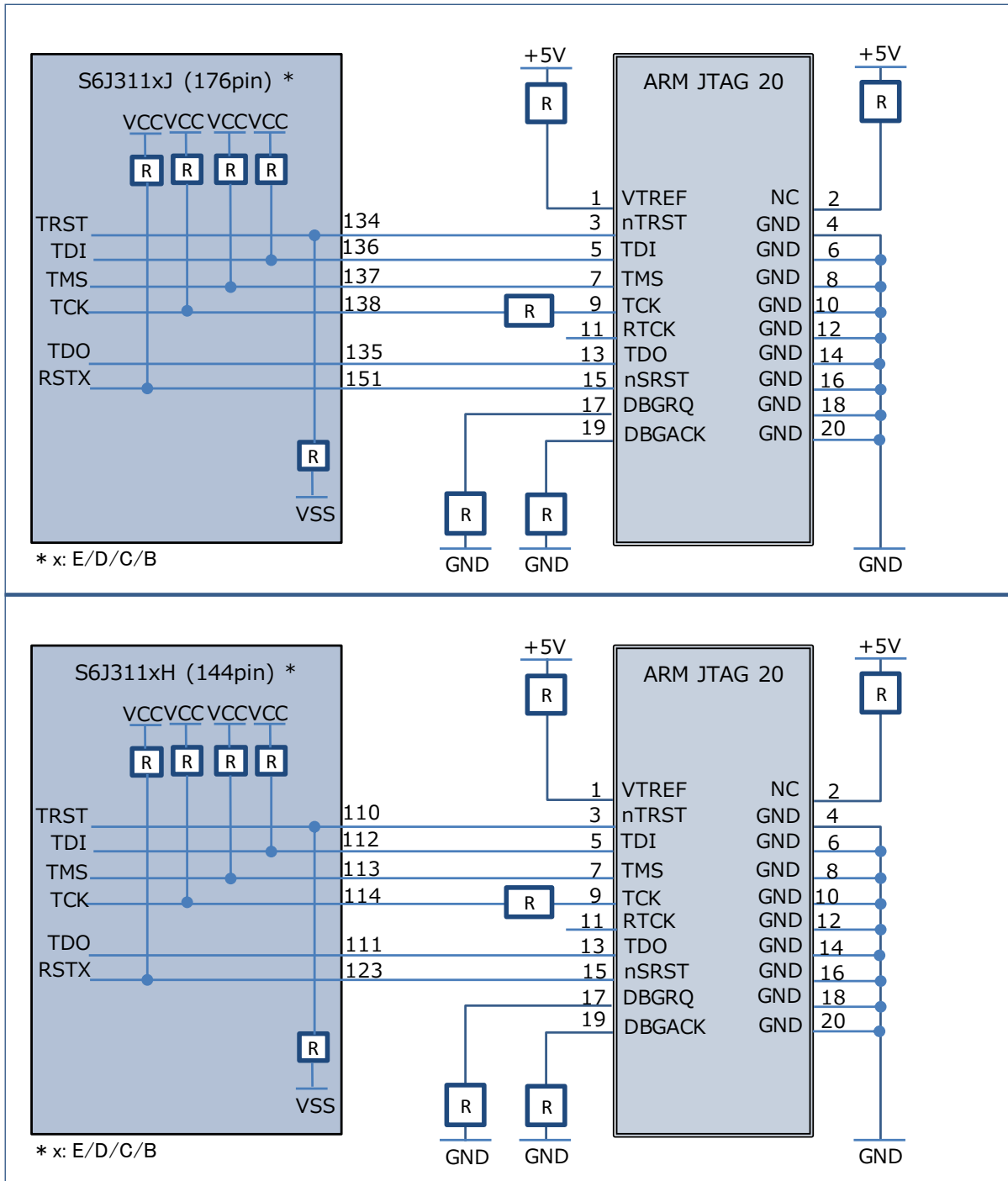
■ Fix Status

Not be planned

15. Appendix

15.1 Application 1: JTAG tool connection

This is an application example of JTAG tool connection. See the relevant application note AN203911 in detail.



16. Major Changes

| Page | Section | Change Results |
|-------------|--|--|
| Revision *A | | |
| 1 | Cover | Added the family product names |
| 1 | Cover | Revised the designation and notes |
| 1 | Cover | Revised the title as follow (error) S6J3110 Series 32-bit Microcontroller Spansion® Traveo™ Family (correct) S6J311E, S6J311D, S6J311C, S6J311B 32-Bit Traveo™ Family S6J3110 Series Microcontroller Datasheet |
| 1 | Features Cortex-R5 Core | Revised the following note (Error) -ECC support for the TCM ports (Correct) -ECC support for the TCM ports for RAM |
| 1 | Features Peripheral Functions | Added the specifications as full production |
| 1 | Features Peripheral Functions | Added I ² C function of MFS |
| 1,2 | Features Peripheral Functions | Added SHE option to the product name |
| 2 | Features Peripheral Functions | Added the following comment to 192 message buffer for CAN-FD “(reception message buffer size)” |
| 2 | Features Peripheral Functions CAN controller: CAN-FD Max 2 channel | Added -32 message buffer/channel (transmission message buffer size) |
| 2 | Features Peripheral Functions | Added “CAN-FD (V3.2.0)” under “CAN controller: CAN-FD Max 2 channel”. |
| 4 | 1. Product Lineup | Added the specifications as full production |
| 4,5 | 1. Product Lineup | Added SHE option to lineup (Table 1-1, 1-2, 1-3) |
| 6,7 | 2. Pin Assignment | Added SHE option to the product name |
| 7 | 2. Pin Assignment | Added the pin assignment figure for S6J311xHAC |
| 7 | 2. Pin Assignment | Revised the pin function name of 107pin to P321/PWUTRG |
| 8,20 | 3. Pin Description | Added SHE option to the product name |
| 8 - 27 | 3. Pin Description | Separated non-analog input IO type from Type A/B to Type P/Q |
| 8-27 | 3. Pin Description | Added I ² C bus pins |
| 25 | 3. Pin Description | Added the pin name PWUTRG to 107pin Revised the IO Circuit Type of 107pin |
| 28 | 4. I/O Circuit Types | Revised the circuit of type C |
| 30 | 4. I/O Circuit Types | Added the IO Circuit Type R |
| 37 | 6. Handling Devices About power supply pins | The explanation should be corrected as indicated by the shading below. (Error) We recommend connecting a ceramic capacitor as a bypass capacitor between VCC and VSS, near this device. (Correct) In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin. |

| Page | Section | Change Results |
|----------------|--|---|
| 37 | 6.Handling Devices | Revised the following notice. (Error) About the Power-on Time To prevent the internal built-in voltage step-down circuit from malfunctioning, secure a voltage rising time of 50 μ s (between 0.2 V and 2.7 V) or longer at the power-on time. (Correct) About the Power-on Time To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic during power-on. |
| 38 | 6.Handling Devices About C pin processing | The pins should be deleted as indicated by the shading below. (Error) This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 46 and pin 154 in S6J311xJAA specifications, pin 38 and pin 126 in S6J311xHAA specifications) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet. (Correct) This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (pin 154 in S6J311xJzC specifications, pin 126 in S6J311xHzC specifications) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest data sheet. |
| 39, 40 | 7. Block Diagram | Added SHE option to the product name |
| 39, 40 | 7. Block Diagram | Revised the block diagram of S6J311xJAC and S6J311xHAC |
| 40 | 7. Block Diagram | Added Partial Wake up in the diagram of Power Domain 1(Always on) |
| 41 | 8. Memory Map | Revised the memory map of S6J311ExAC / S6J311DxAC / S6J311CxAC / S6J311BxAC |
| 41,44,46,47,49 | 8. Memory Map | Added SHE option to the product name |
| 42 | 8. Memory Map | Added the following notes The ECC movement in TCM port is based on ECC setting inside the CPU. |
| 44 - 49 | 8. Memory Map | Revised the peripheral map of S6J311xJAC and S6J311xHAC |
| 46,49 | 8. Memory Map | Added Global Timer to Table 8-2 and Table 8-4 |
| 49 | 8. Memory Map | Added about the setting of MPU attribute for memory area |
| 49 | 8. Memory Map | Added the the following restriction about SHE OFF product |
| 50,52 | 9. Pin Statuses In CPU Status | Added SHE option to the product name |
| 50 - 53 | 9. Pin Statuses In CPU Status | Revised the pin status table of S6J311xJAC and S6J311xHAC |
| 50 - 53 | 9. Pin Statuses In CPU Status | Corrected the state name from "Watch mode" to "Timer mode" |
| 51 | 9. Pin Statuses In CPU Status | Revised the Pin name of 130pin as follows (Error) P320/PWUTRG/WOT (Correct) P320/PWUTRG |
| 53 | 9. Pin Statuses In CPU Status | Revised the pin status table for P321 |
| 53 | 9. Pin Statuses In CPU Status | Added the pin name PWUTRG to 107pin |
| 54 | 9. Pin Statuses In CPU Status | Added the following note *7: When PPC_PCFGrijj:POF[2:0] is set to initial value. |

| Page | Section | Change Results | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|--|----------------------|--------|------------------------------------|---------|------|---------|-----|-----|--|-----------------|----------------------|----------------------|---|--|---|------------------|----------------------|----------------------|---|----------|-----------|--------|--------|--|------|---------|-----|-----|--|-----------------|----------------------|----------------------|---|--|---|------------------|----------------------|----------------------|---|------------------------------------|
| 55 | 10. Electrical Characteristics 10.1 Absolute Maximum Ratings | <p>The notes should be corrected as indicated by the shading below. (Error)</p> <table border="1"> <thead> <tr> <th rowspan="2">Parameter</th> <th rowspan="2">Symbol</th> <th colspan="2">Rating</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>Power supply voltage^{*1, *2}</td> <td>V_{CC}</td> <td>V_{SS}-0.3</td> <td>V_{SS}+6.0</td> <td>V</td> <td></td> </tr> <tr> <td>Analog supply voltage^{*1, *2}</td> <td>AV_{CC}</td> <td>V_{SS}-0.3</td> <td>V_{SS}+6.0</td> <td>V</td> <td>AvccsVcc</td> </tr> </tbody> </table> <p>(Correct)</p> <table border="1"> <thead> <tr> <th rowspan="2">Parameter</th> <th rowspan="2">Symbol</th> <th colspan="2">Rating</th> <th rowspan="2">Unit</th> <th rowspan="2">Remarks</th> </tr> <tr> <th>Min</th> <th>Max</th> </tr> </thead> <tbody> <tr> <td>Power supply voltage^{*1, *2}</td> <td>V_{CC}</td> <td>V_{SS}-0.3</td> <td>V_{SS}+6.0</td> <td>V</td> <td></td> </tr> <tr> <td>Analog supply voltage^{*1, *2}</td> <td>AV_{CC}</td> <td>V_{SS}-0.3</td> <td>V_{SS}+6.0</td> <td>V</td> <td>V_{CC} = AV_{CC}</td> </tr> </tbody> </table> | Parameter | Symbol | Rating | | Unit | Remarks | Min | Max | Power supply voltage ^{*1, *2} | V _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | | Analog supply voltage ^{*1, *2} | AV _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | AvccsVcc | Parameter | Symbol | Rating | | Unit | Remarks | Min | Max | Power supply voltage ^{*1, *2} | V _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | | Analog supply voltage ^{*1, *2} | AV _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | V _{CC} = AV _{CC} |
| Parameter | Symbol | Rating | | | Unit | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Min | Max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power supply voltage ^{*1, *2} | V _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Analog supply voltage ^{*1, *2} | AV _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | AvccsVcc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Parameter | Symbol | Rating | | Unit | Remarks | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Min | Max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Power supply voltage ^{*1, *2} | V _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Analog supply voltage ^{*1, *2} | AV _{CC} | V _{SS} -0.3 | V _{SS} +6.0 | V | V _{CC} = AV _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 55 | 10. Electrical Characteristics 10.1 Absolute Maximum Ratings | <p>Revised the following note</p> <p>*2: AVCC and VCC must be set to the same voltage. It is required that AVCC does not exceed VCC and that the voltage at the analog inputs does not exceed AVCC when the power is switched on.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 57 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Separated the specification of smoothing capacitor from C_{S1}, C_{S2} to C_S Revised the figure and table</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 57 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Added the following remarks to “Smoothing capacitor”</p> <p>Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 57 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Revised the notes of “C pin connection diagram” as follow: *1: 154pin(S6J311xJzC*) / 126pin(S6J311xHzC*) *2: 46pin(S6J311xJzC*) / 38pin(S6J311xHzC*) * x: E/D/C/B, z: A/B</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 57 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Revised the connection of C pin in “C pin connection diagram”</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 58 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Added the following notes</p> <p>-The following condition should be satisfied in order to facilitate heat dissipation. 1.4 or more layers PCB should be used. 2.The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard) 3.1 layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground. 4.35~50% of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer. 5.The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 58 | 10. Electrical Characteristics 10.2 Recommended operating conditions | <p>Added the following notes</p> <p>-Figure 2-1 is a schematic diagram showing PCB in section. -Figure 2-2, Figure 2-3 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands. -If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Page | Section | Change Results |
|--------|--|---|
| 58,59 | 10. Electrical Characteristics 10.2 Recommended operating conditions | Added the following figures Figure 10.2-1: Example thermal via holes on PCB. Figure 10.2-2: Land Pattern and Thermal Via LEP176 Figure 10.2-3: Land Pattern and Thermal Via LES144 |
| 60 | 10. Electrical Characteristics 10.3 DC characteristics | Revised the minimum value of V_{IH6} 2.0 -> 2.3 |
| 64 | 10. Electrical Characteristics 10.4.1 Source clock timing | Added the following characteristics - PLL input clock frequency (F_{PLLI}) - PLL macro oscillation clock frequency (F_{PLLO}) - SSCG-PLL input clock frequency ($F_{SSCGPLLI}$) - SSCG-PLL macro oscillation clock frequency ($F_{SSCGPLLO}$) |
| 66, 67 | 10. Electrical Characteristics 10.4.2 Internal clock timing | Added the following characteristics - F_{CLK_CANFD} , t_{CLK_CANFD} (CANFD_CCLK) |
| 67 | 10. Electrical Characteristics 10.4.2 Internal Clock Timing | Revised the following Symbol. (Error) t_{CLK_FMA} (Correct) t_{CLK_DMA} |
| 67 | 10. Electrical Characteristics 10.4.2 Internal Clock Timing | Revised the following Values (Error) t_{CLK_LAPP1} min:41.6 / t_{CLK_LAPP1A} min:41.6 (Correct) t_{CLK_LAPP1} min:27.7 / t_{CLK_LAPP1A} min:27.7 |
| 68 | 10. Electrical Characteristics 10.4.2 Internal clock timing | Rivised the internal clock definition in the following figure. "Guaranteed operation range Internal operation clock frequency vs. Power supply voltage" F_{CD0_CLK} -> F_{CPU_CLK} |
| 69 | 10. Electrical Characteristics 10.4.2 Internal clock timing | Added the note of maximum PLL clock frequency setting "PLLDIVM" and "SSCGDIVM" |
| 70 | 10. Electrical Characteristics 10.4.2 Internal clock timing | Revised the voltage value of Hysteresis input pin (TTL). 2.0V -> 2.3V |
| 72 | 10. Electrical Characteristics 10.4.4 Power-on conditions | Revised the note"*1" for "Level detection time" |
| 72 | 10. Electrical Characteristics 10.4.4 Power-on Conditions | Revised the value of level detection voltage (Error) min 2.25 / typ 2.45 / max 2.65 (Correct) min 2.15 / typ 2.35 / max 2.55 |
| 72 | 10. Electrical Characteristics 10.4.4 Power-on Conditions | Deleted the Slope detection undetected specification. Added the Power ramp rate and Maximum ramp rate guaranteed to not generate power-on reset. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, Maximum ramp rate guaranteed to not generate power-on reset. |
| 87 | 10. Electrical Characteristics 10.4.5 Multi-function serial 10.4.5.1 CSIO timing (SMR:MD2-0=010B) (5-1-7) Serial chip select used (SCSCR:CSEN=1) | Added figures for the characteristic |
| 95,96 | 10. Electrical Characteristics 10.4.5.4 I2C timing (SMR:MD[2:0]=100B) | Added the AC characteristic for I2C |
| 98 | 10. Electrical Characteristics 10.6 Trigger input timing | Deleted the following pin names in the table of Input pulse width and figure of Trigger input timing "RX0 to RX1", "RXx" |
| 100 | 10. Electrical Characteristics 10.8 Low-voltage detection(external low-voltage detection) | Revised the following characteristics V_{DL} -> V_{DL0} , V_{DL1} , V_{DL2} |
| 100 | 10. Electrical Characteristics 10.8 Low-voltage detection(external low-voltage detection) | Added the register setting for the following characteristics V_{DL0} , V_{DL1} , V_{DL2} |
| 101 | 10. Electrical Characteristics 10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection) | Revised the title in 10.9 "Internal Low-Voltage Detection" to "RAM Retention Low-Voltage Detection". |

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| 101 | 10. Electrical Characteristics 10.10 Low-voltage detection(1.2V power supply low-voltage detection) | Revised the following characteristics V _{RDL} -> V _{RDL0} , V _{RDL1} |
| 101 | 10. Electrical Characteristics 10.10 Low-voltage detection(1.2V power supply low-voltage detection) | Added the register setting for the following characteristics V _{RDL0} , V _{RDL1} |
| 101 | 10. Electrical Characteristics 10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection) | Added the notice *4 |
| 103 | 10.11 A/D converter 10.11.2 Notes on Using A/D converter | Revised the figure "Analog input circuit model" |
| 104 | 10. Electrical Characteristics 10.11.3 Definition of terms | Revised the following notes (error) Total error : Difference between the actual value and the theoretical value. The total error (correct) Total error: Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error. |
| 104 | 10.11 A/D converter 10.11.3 Definition of terms | Revised the title as follows "12.11.3 Glossary" -> "12.11.3 Definition of terms" |
| 104 - 105 | 10.11 A/D converter 10.11.3 Definition of terms | Revised the following names (meaning is same) - Integral linearity error -> Integral Nonlinearity error - Differential linearity error -> Differential Nonlinearity error |
| 106 | 10.12 Flash memory | Revised the items of sector erase time and write time Filled maximum values in the Rating table |
| 106 | 10.12 Flash memory | Added the notes of power management for Flash memory |
| 107 | 11. Ordering Information | Revised the Part Number as full production |
| 107 | 11. Ordering Information | Added SHE option to the part number |
| 107 | 12. Part Number Option | Added the part number options as full production |
| 107 | 12. Part Number Option | Added Part Number Option "z" as SHE option |
| 109 | 13. Package Dimensions | Added the package dimension of LES144 |
| 1,2,4 to 27, 38 to41,44, 46,47,49,50, 52,57,72, 107, | - | Revised part number from S6J311xxxA to S6J311xxxC. |

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: S6J311E, S6J311D 32-Bit Traveo™ Family S6J3110 Series Microcontroller Datasheet

Document Number: 002-05681

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|----------|---------|-----------------|-----------------|--|
| ** | - | MXNI | 06/25/2014 | Migrated to Cypress and assigned document number 002-05681. No change to document contents or format. |
| *A | 5311068 | WECU | 06/20/2016 | Updated to Cypress format. Revised the title. Revised part number from S6J311xxxA to S6J311xxxC. For detail, see "Major Changes". |
| *B | 5375454 | WECU | 07/27/2016 | Page 72, 10.4.4 Power-on Conditions Revised Level detection time from 30 to 540, Revised *1 to *4 and Note. Page 101, 10.9 Low-Voltage Detection (RAM Retention Low-Voltage Detection) Added * and Note to Detection voltage. Page 101, 10.10 Low-Voltage Detection (1.2 V Power Supply Low-Voltage Detection) Added * and Note to Detection voltage. |
| *C | 5554875 | WECU | 12/15/2016 | Page 108 to 109, Replaced 13. Package Dimensions Page 110, Added 14.Appendix |
| *D | 5782404 | YOST | 06/22/2017 | Updated Cypress logo. Updated Copyright. |
| *E | 6275935 | MXNI | 08/15/2018 | Part Number Option is updated. Page 24, Revised 3. Pin Description Page 108,109 Updated 13. Package Dimensions Changed A1 MAX. of LEP176 and LES144 Page 110, Added 14. Errata |

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