16-Bit, Single-Ended Analog Input/Output Stereo Audio Codec

FEATURES

- **Monolithic 16-Bit ΔΣ ADC and DAC**
- **Stereo ADC:**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter**
  - **64× Oversampling**
  - **High Performance**
    - **THD+N: –84 dB**
    - **SNR: 89 dB**
    - **Dynamic Range: 89 dB**
  - **Digital High-Pass Filter**
- **Stereo DAC:**
  - **Single-Ended Voltage Output**
  - **Analog Low-Pass Filter**
  - **8× Oversampling Digital Filter**
  - **High Performance**
    - **THD+N: –84 dB**
    - **SNR: 93 dB**
    - **Dynamic Range: 93 dB**
- **Special Features**
  - **Digital De-Emphasis**
  - **Power Down: ADC/DAC Independent**
- **Sampling Rate: 4 kHz to 48 kHz**
- **System Clock: 256 f_S, 384 f_S, 512 f_S**
- **Single 3-V Power Supply**
- **Small Package: 24-Lead TSSOP**

APPLICATIONS

- **Sampling Keyboards**
- **Digital Mixers**
- **Effects Processors**
- **Hard-Disk Recorders**
- **Data Recorders**
- **Digital Video Cameras**

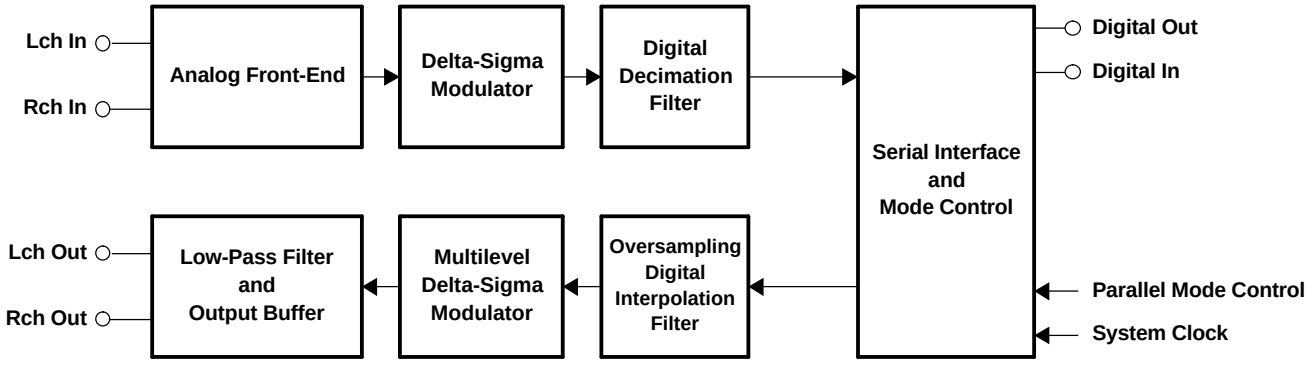
DESCRIPTION

The PCM3006 is a low-cost, single-chip stereo audio codec (analog-to-digital and digital-to-analog converters) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64-times oversampling. The ADCs include a digital decimation filter, and the DACs include an 8-times oversampling digital interpolation filter. The DACs also include a digital de-emphasis function. The PCM3006 operates with 16-bit, left-justified for ADC, right-justified for DAC data formats.

The PCM3006 provides a power-down mode that operates on the ADCs and DACs independently.

The PCM3006 is fabricated using a highly advanced CMOS process, and is available in a small 24-pin TSSOP package. The PCM3006 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required.



B0006-02

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER		CONDITIONS	PCM3006T			UNITS
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT						
Input Logic						
V_{IH} (1)	Input logic level		0.7 V_{DD}			VDC
V_{IL} (1)					0.3 V_{DD}	
I_{IN} (2)	Input logic current				±1	μA
I_{IN} (3)					100	
Output Logic						
V_{OH} (4)	Output logic level	I_{OUT} = –1 mA	V_{DD} – 0.3			VDC
V_{OL} (4)		I_{OUT} = 1 mA			0.3	
CLOCK FREQUENCY						
f_S	Sampling frequency		4	44.1	48	kHz
	System clock frequency	256 f_S	1.024	11.2896	12.288	MHz
		384 f_S	1.536	16.9344	18.432	
		512 f_S	2.048	22.5792	24.576	
ADC CHARACTERISTICS						
Resolution				16		Bits
DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±2	±5	% of FSR
	Gain drift			±20		ppm of FSR/°C
Dynamic Performance (5)						
	THD+N	V_{IN} = –0.5 dB		–84	–77	dB
		V_{IN}= –60 dB		–26		
	Dynamic range	A-weighted	84	89		dB
	Signal-to-noise ratio	A-weighted	84	89		dB
	Channel separation		82	86		dB
Digital Filter Performance						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
	Delay time			17.4/f_S		s

(1) Pins 7, 8, 9, 10, 11, 15, 17, 18: $\overline{\text{PDAD}}$, $\overline{\text{PDDA}}$, SYSCLK, LRCIN, BCKIN, DIN, DEM1, DEM0 (Schmitt-trigger input with 100-kΩ typical internal pulldown resistor)
(2) Pins 9, 10, 11, 15: SYSCLK, LRCIN, BCKIN, DIN (Schmitt-trigger input)
(3) Pins 7, 8, 17, 18: $\overline{\text{PDAD}}$, $\overline{\text{PDDA}}$, DEM1, DEM0 (Schmitt-trigger input, 100-kΩ typical internal pulldown resistor)
(4) Pin 12: DOUT
(5) f_{IN} = 1 kHz, using System Two™ audio measurement system by Audio Precision™, rms mode with 20-kHz LPF, 400-Hz HPF used for performance calculation.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER	CONDITIONS	PCM3006T			UNITS
		MIN	TYP	MAX	
HPF frequency response	–3 dB		0.019 f_S		mHz
Analog Input					
Voltage range			0.6 V_{CC}		Vp-p
Center voltage			0.5 V_{CC}		VDC
Input impedance			30		kΩ
Antialiasing filter frequency response	–3 dB		150		kHz
DAC CHARACTERISTICS					
Resolution			16		Bits
DC Accuracy					
Gain mismatch, channel-to-channel			±1	3	% of FSR
Gain error			±1	5	% of FSR
Gain drift			±20		ppm of FSR/°C
Bipolar zero error			±2.5		% of FSR
Bipolar zero drift			±20		ppm of FSR/°C
Dynamic Performance(6)					
THD+N	V_{OUT} = 0 dB (full scale)		–84	–77	dB
	V_{OUT} = –60 dB		–30		
Dynamic range	EIAJ, A-weighted	86	93		dB
Signal-to-noise ratio	EIAJ, A-weighted	86	93		dB
Channel separation		84	90		dB
Digital Filter Performance					
Pass band				0.445 f_S	Hz
Stop band		0.555 f_S			Hz
Pass-band ripple				±0.17	dB
Stop-band attenuation		–35			dB
Delay time			11.1/f_S		s
Analog Output					
Voltage range			0.6 V_{CC}		Vp-p
Center voltage			0.5 V_{CC}		VDC
Load impedance	AC coupling	10			kΩ
LPF frequency response	f = 20 kHz		–0.16		dB

(6) f_{OUT} = 1 kHz, using System Two audio measurement system by Audio Precision, rms mode with 20-kHz LPF, 400-Hz HPF used for performance calculation.

ELECTRICAL CHARACTERISTICS (continued)

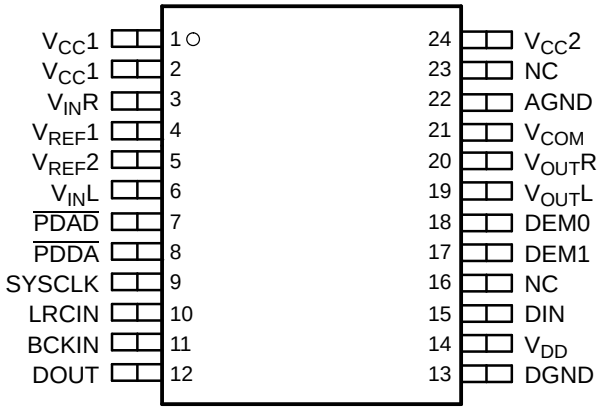
All specifications at T_A = 25°C, V_{DD} = V_{CC} = 3 V, f_S = 44.1 kHz, SYSCLK = 384 f_S, and 16-bit data, unless otherwise noted

PARAMETER		CONDITIONS	PCM3006T			UNITS
			MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS						
V_{CC}, V_{DD}	Voltage range	–25°C to 85°C	2.7	3	3.6	VDC
		0°C to 70°C(7)	2.4	3	3.6	
	Supply current	ADC/DAC operation, V_{CC} = V_{DD} = 3 V		18	24	mA
		ADC operation, V_{CC} = V_{DD} = 3 V		12	16	
		DAC operation, V_{CC} = V_{DD} = 3 V		7	10	
		ADC/DAC power down(8), V_{CC} = V_{DD} = 3 V		50		μA
	Power dissipation	ADC/DAC operation, V_{CC} = V_{DD} = 3 V		54	72	mW
		ADC operation, V_{CC} = V_{DD} = 3 V		36	48	
		DAC operation, V_{CC} = V_{DD} = 3 V		21	30	
		ADC/DAC power down(8), V_{CC} = V_{DD} = 3 V		150		μW
TEMPERATURE RANGE						
T_A	Operation		–25		85	°C
T_{stg}	Storage		–55		125	
θ_{JA}	Thermal resistance			100		°C/W

(7) Applies for voltages between 2.4 V and 2.7 V, for 0°C to 70°C, and 256-f_S/512-f_S operation (384-f_S not available)
(8) SYSCLK, BCKIN, and LRCIN are stopped.

PIN CONFIGURATION

PCM3006
(TOP VIEW)



NC = No Connection

P0006-01

PIN ASSIGNMENTS

NAME	PIN	I/O	DESCRIPTION
AGND	22	–	Analog ground
BCKIN	11	I	Bit clock input(1)
DEM0	18	I	De-emphasis control 0(1)(2)
DEM1	17	I	De-emphasis control 1(1)(2)
DGND	13	–	Digital ground
DIN	15	I	Data input(1)
DOUT	12	O	Data output
LRCIN	10	I	Sample rate clock input (f_S)(1)
NC	16, 23	–	No connection
$\overline{\text{PDAD}}$	7	I	ADC power down, active LOW(1)(2)
$\overline{\text{PDDA}}$	8	I	DAC power down, active LOW(1)(2)
SYSCLK	9	I	System clock input(1)
$V_{CC}1$	1, 2	–	ADC analog power supply
$V_{CC}2$	24	–	DAC analog power supply
V_{COM}	21	–	ADC/DAC common
V_{DD}	14	–	Digital power supply
$V_{IN}L$	6	I	ADC analog input, Lch
$V_{IN}R$	3	I	ADC analog input, Rch
$V_{OUT}L$	19	O	DAC analog output, Lch
$V_{OUT}R$	20	O	DAC analog output, Rch
$V_{REF}1$	4	–	ADC reference, 1
$V_{REF}2$	5	–	ADC reference, 2

(1) Schmitt-trigger input
(2) With 100-kΩ typical internal pulldown resistor

ABSOLUTE MAXIMUM RATINGS

Supply voltage: V_{DD}, $V_{CC}1$, $V_{CC}2$	–0.3 V to 6.5 V
Supply voltage differences	±0.1 V
GND voltage differences	±0.1 V
Digital input voltage	–0.3 V to V_{DD} + 0.3 V, < 6.5 V
Analog input voltage	–0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3 V, < 6.5 V
Power dissipation	300 mW
Input current (any pins except supplies)	±10 mA
Operating temperature	–25°C to 85°C
Storage temperature	–55°C to 125°C
Lead temperature, soldering	260°C, 5 s
Package temperature (IR reflow, peak)	235°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage , $V_{CC}1$, $V_{CC}2$		2.7	3	3.6	V
Digital supply voltage , V_{DD}		2.7	3	3.6	V
Analog input voltage, full scale (–0 db)	V_{CC} = 3 V		1.8		Vp-p
Digital input logic family			CMOS		
Digital input clock frequency	System clock	8.192		24.576	MHz
	Sampling clock	32		48	kHz
Analog output load resistance		10			kΩ
Analog output load capacitance			30		pF
Digital output load capacitance			10		pF
Operating free-air temperature, T_A		–25		85	°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA	QUANTITY
PCM3006T	24-pin TSSOP	DCV	PCM3006T	PCM3006T	Rails	128
				PCM3006T/2K	Tape and reel	2000

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

ADC SECTION

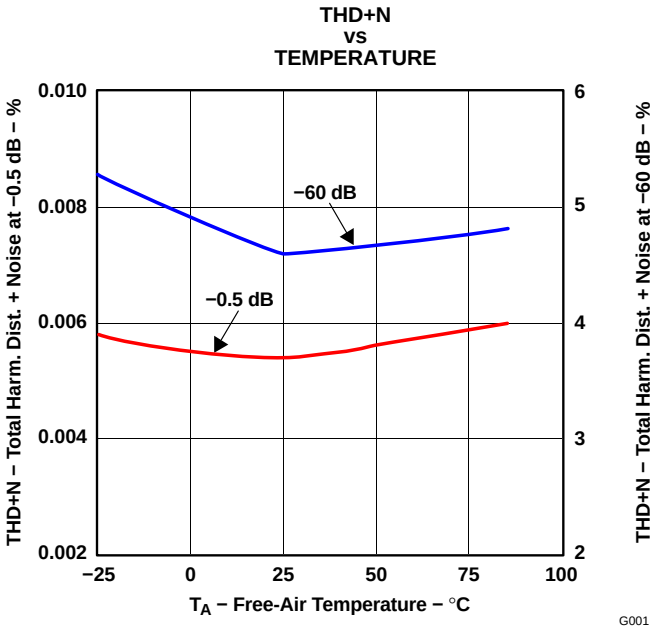


Figure 1.

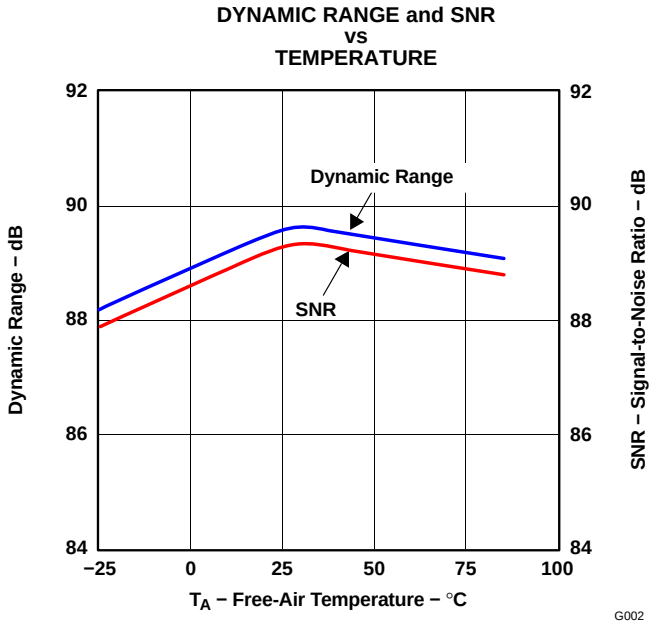


Figure 2.

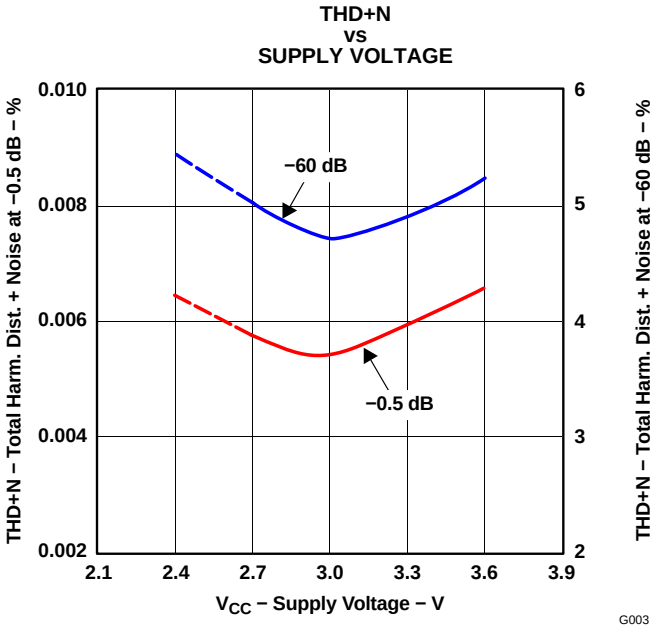


Figure 3.

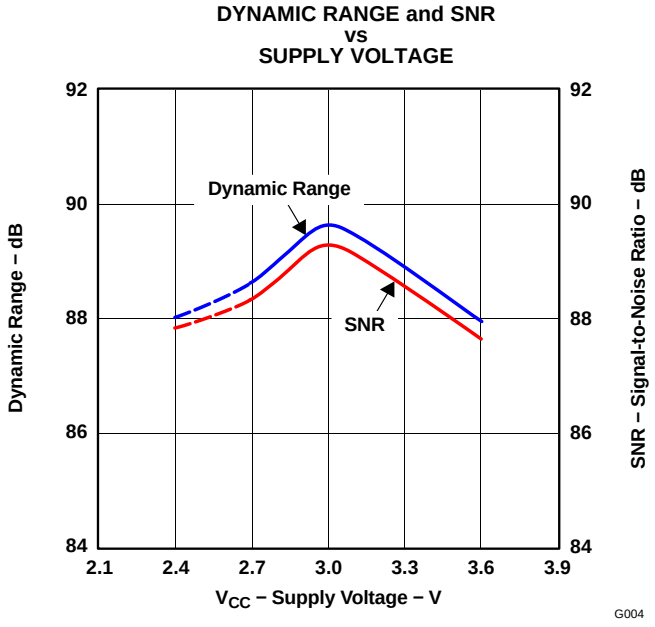


Figure 4.

NOTE: All characteristics at supply voltages from 2.4 V to 2.7 V are measured at SYSCLK = 256 f_S.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

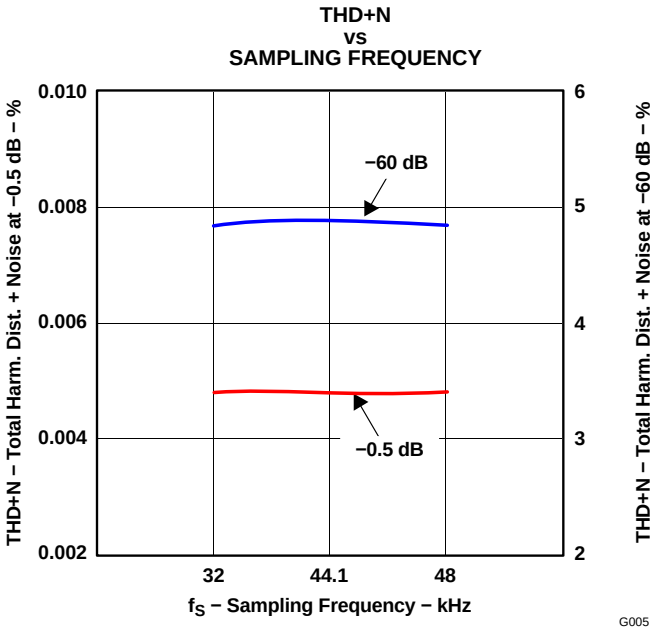


Figure 5.

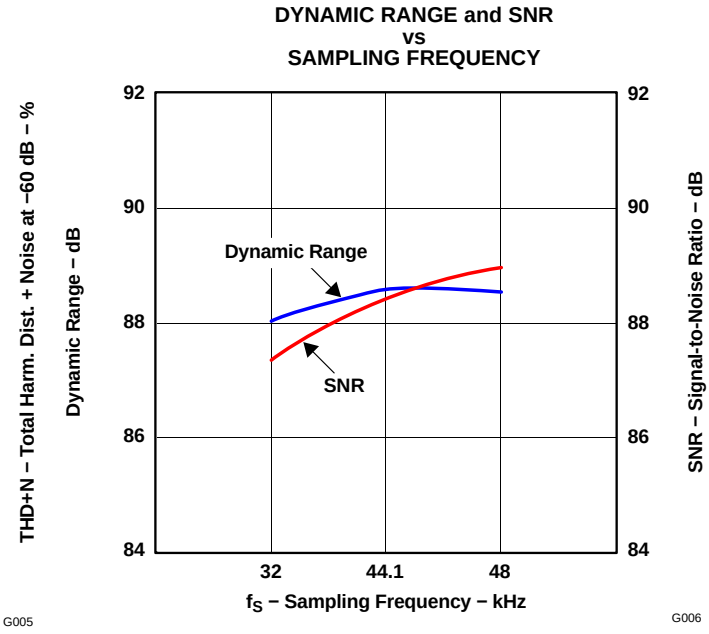


Figure 6.

DAC SECTION

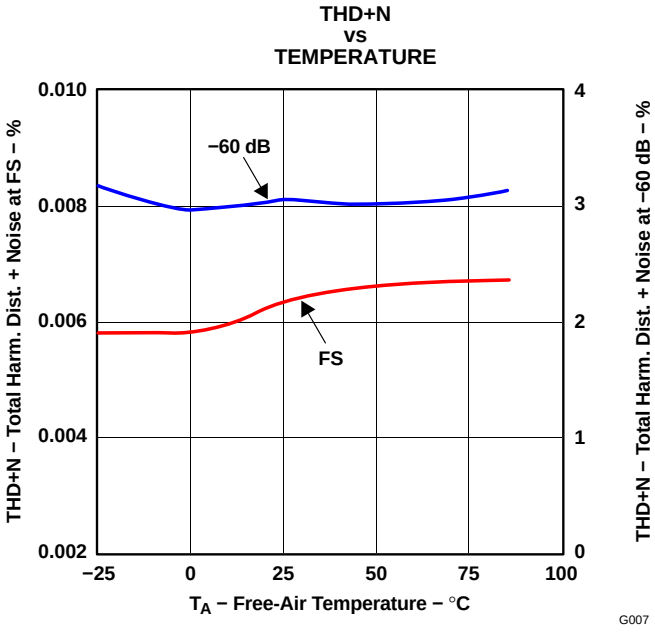


Figure 7.

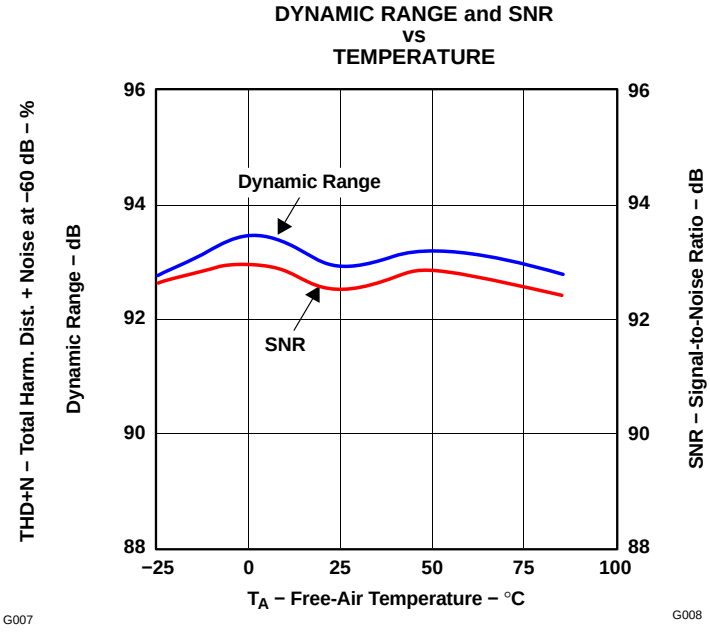


Figure 8.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, f_{SYSCLK} = 384 f_S, and f_{SIGNAL} = 1 kHz, unless otherwise noted

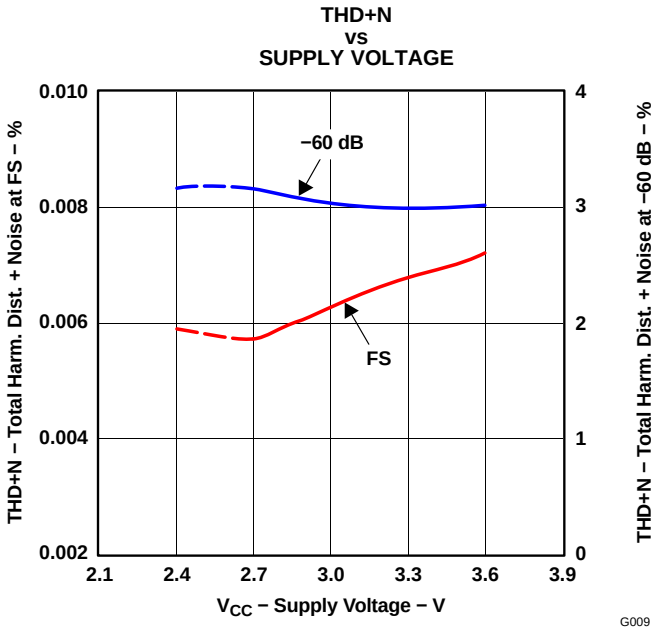


Figure 9.

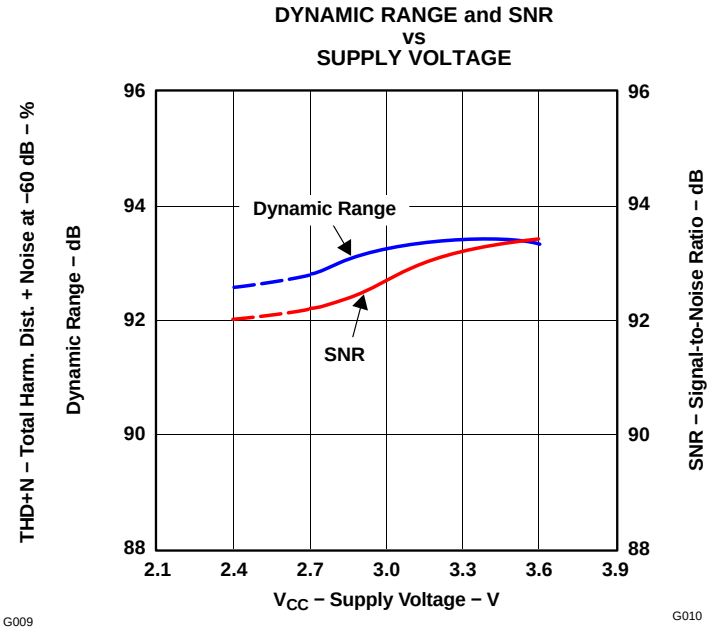


Figure 10.

NOTE: All characteristics at supply voltages from 2.4 V to 2.7 V are measured at SYSCLK = 256 f_S.

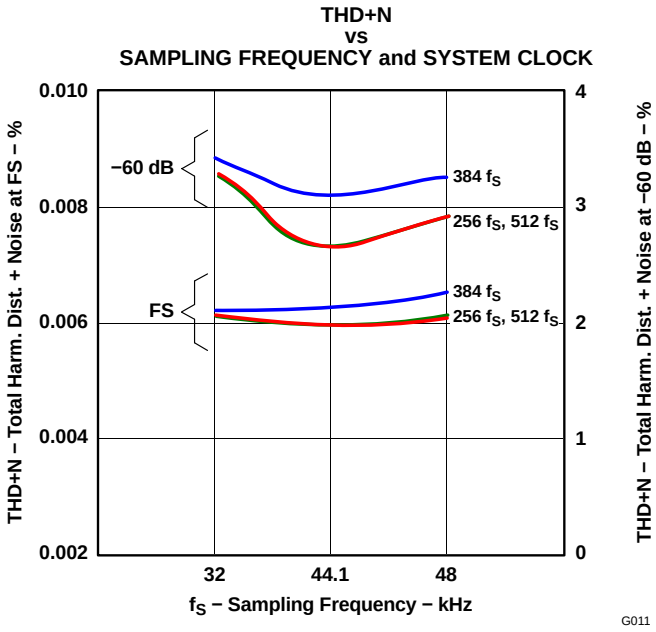


Figure 11.

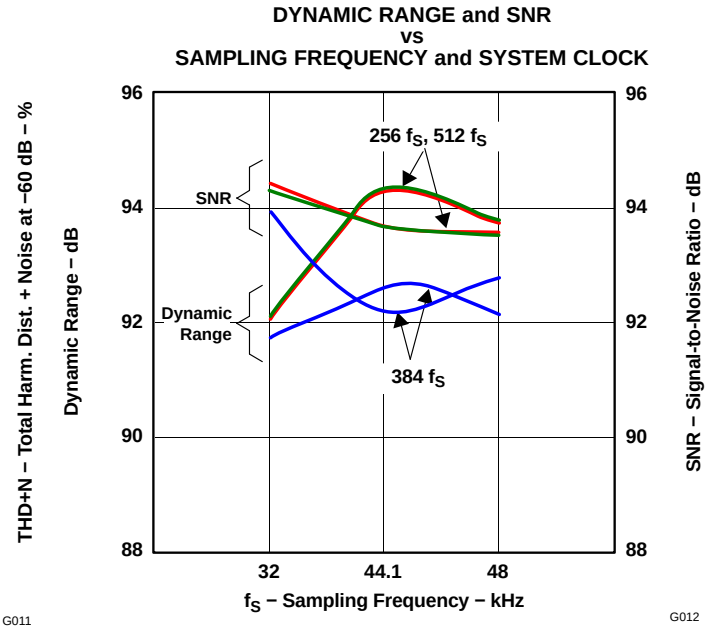


Figure 12.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

DECIMATION FILTER

OVERALL CHARACTERISTICS

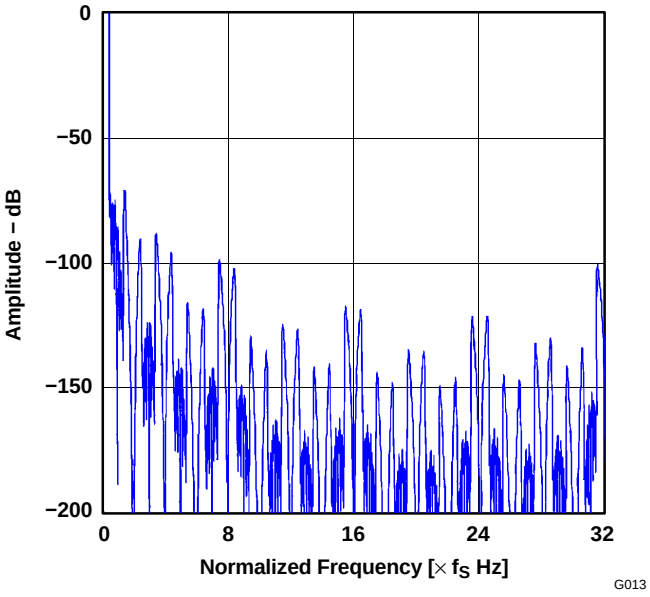


Figure 13.

STOP-BAND ATTENUATION CHARACTERISTICS

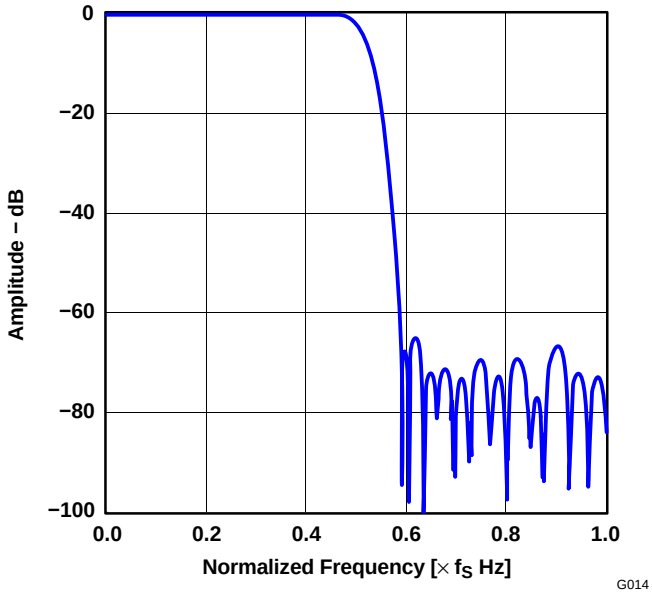


Figure 14.

PASS-BAND RIPPLE CHARACTERISTICS

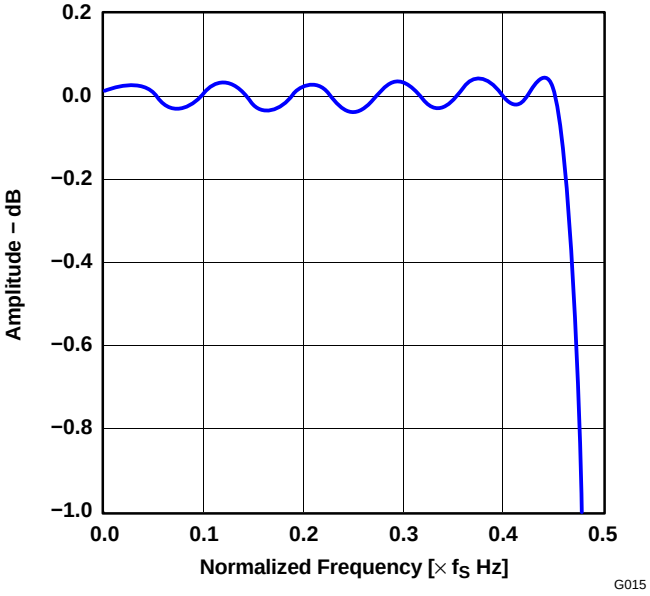


Figure 15.

TRANSITION BAND CHARACTERISTICS

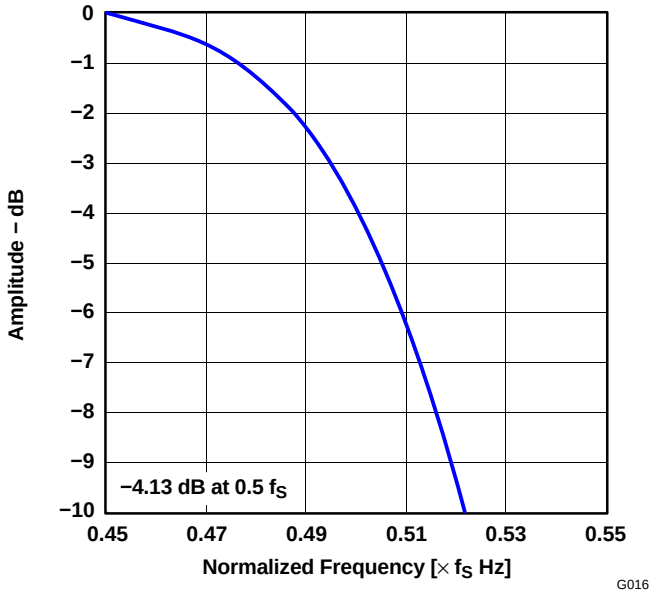


Figure 16.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

HIGH-PASS FILTER

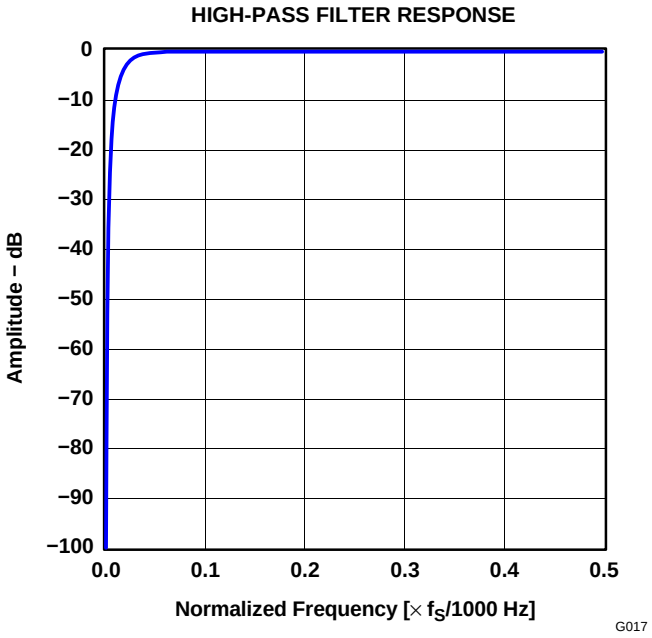


Figure 17.

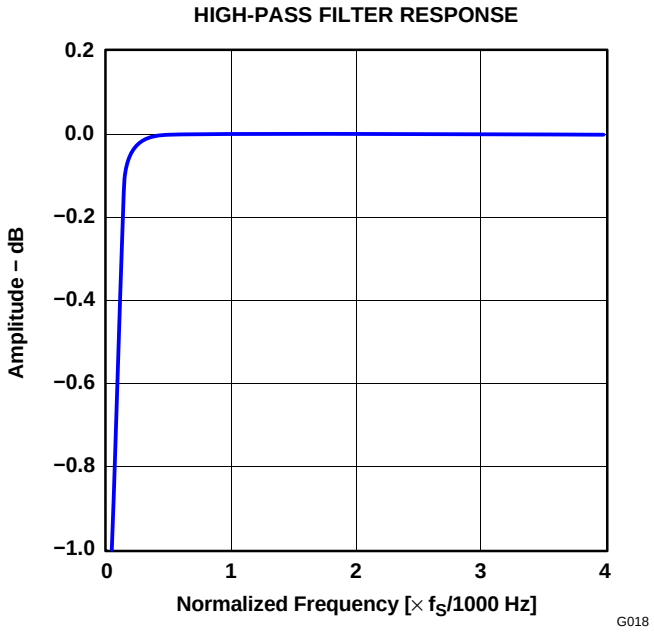


Figure 18.

ANTIALIASING FILTER

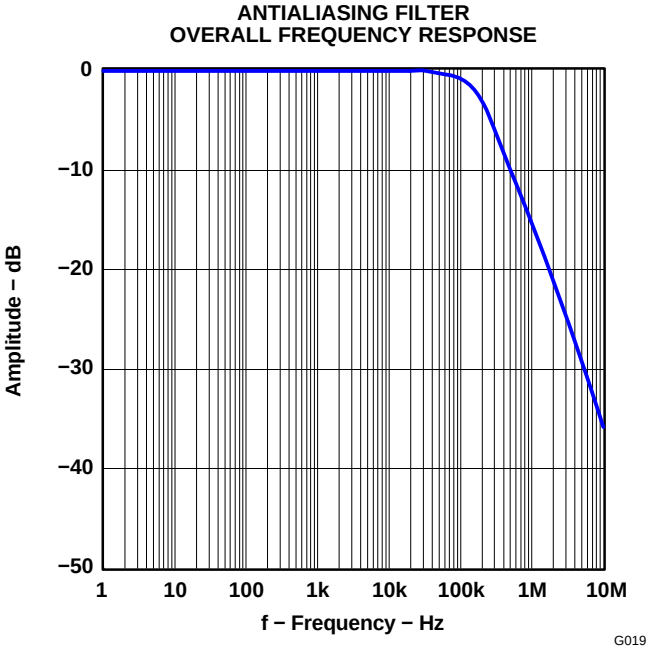


Figure 19.

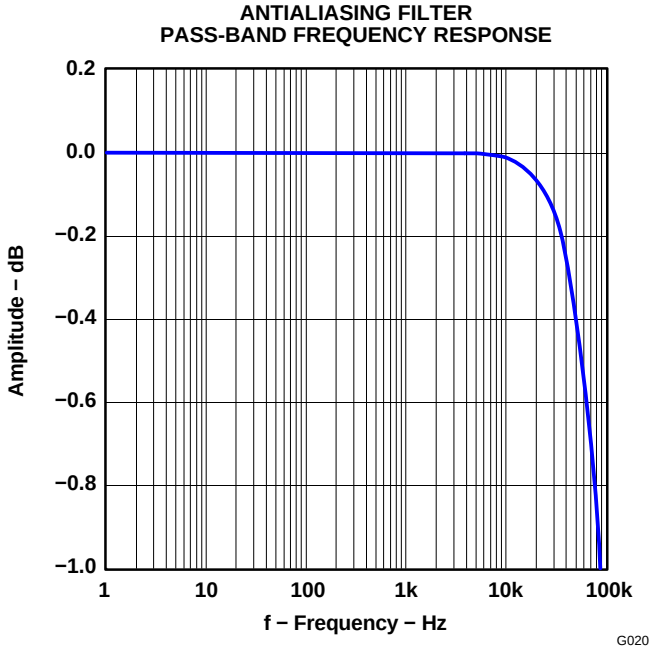


Figure 20.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

DIGITAL FILTER

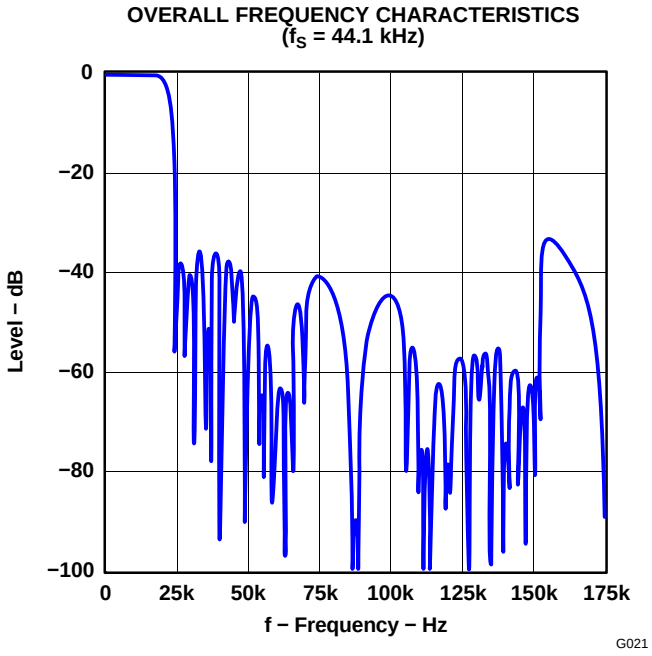


Figure 21.

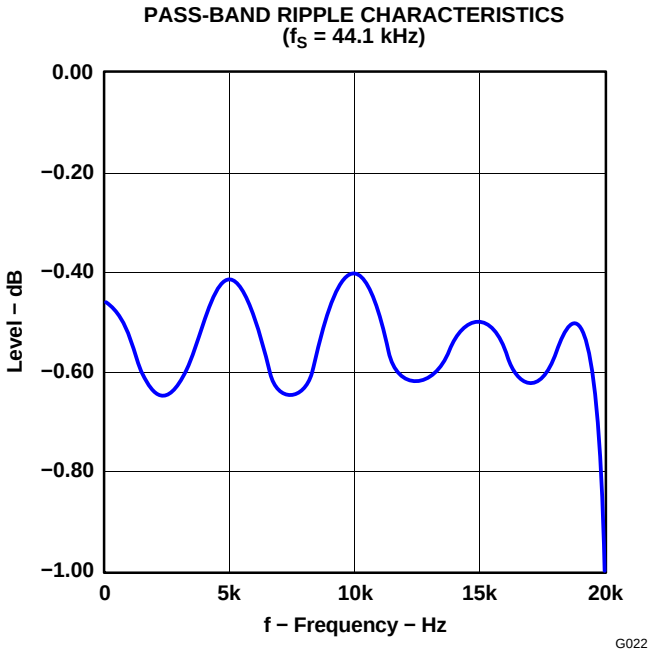


Figure 22.

DE-EMPHASIS FILTER

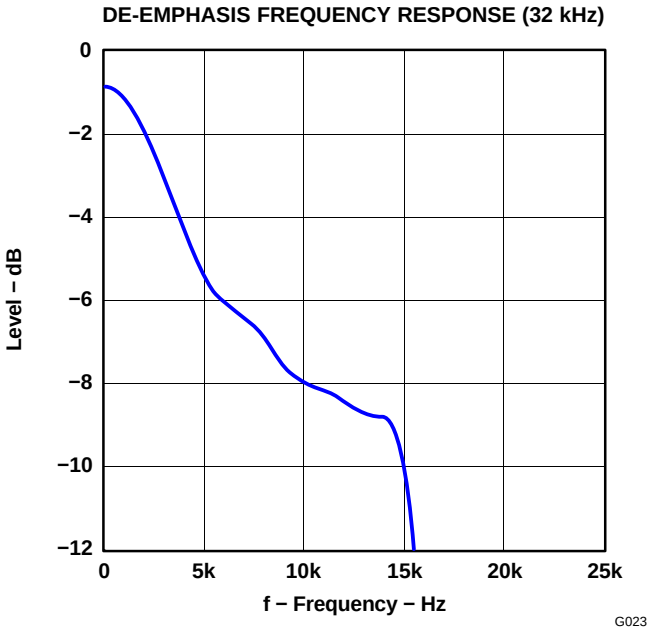


Figure 23.

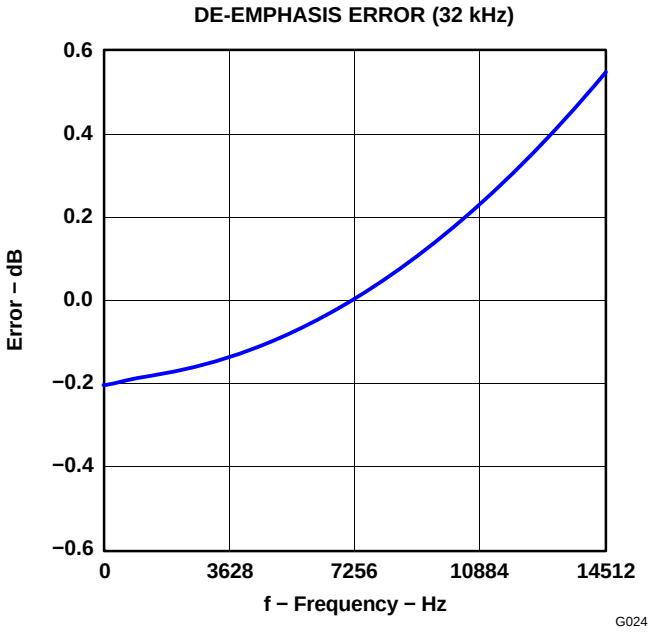


Figure 24.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

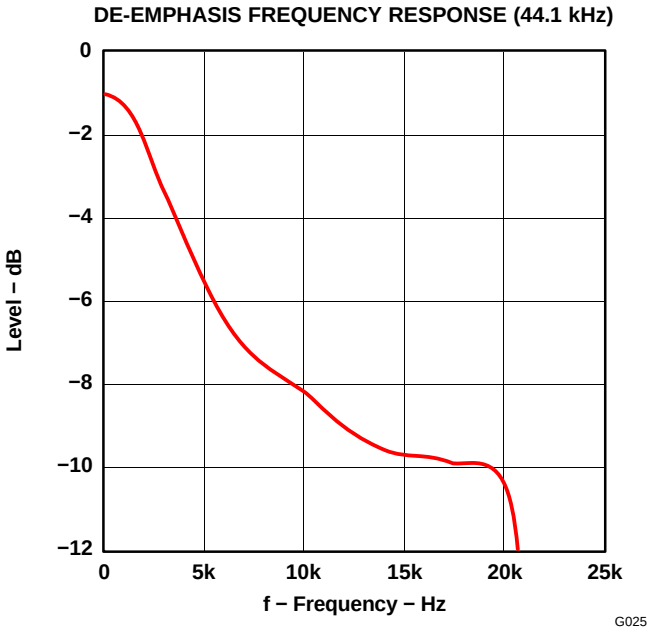


Figure 25.

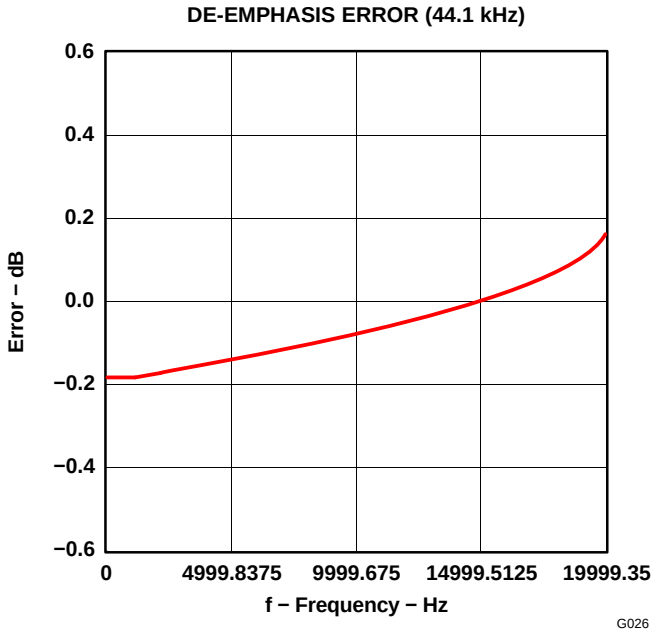


Figure 26.

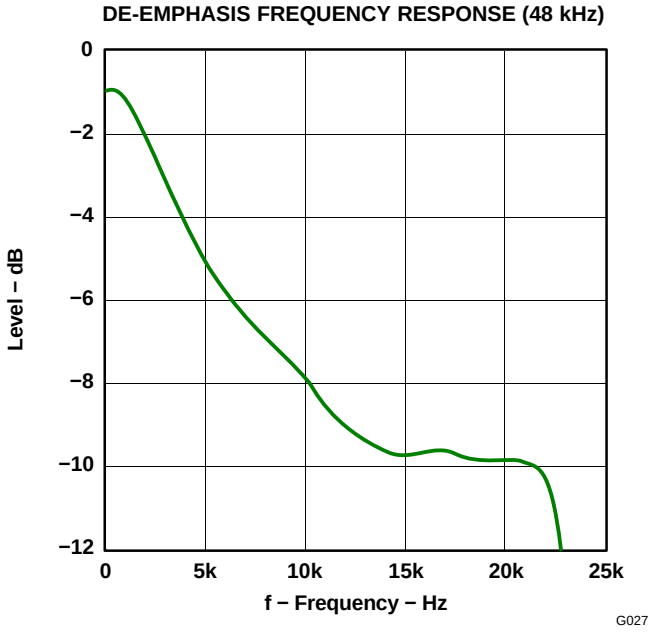


Figure 27.

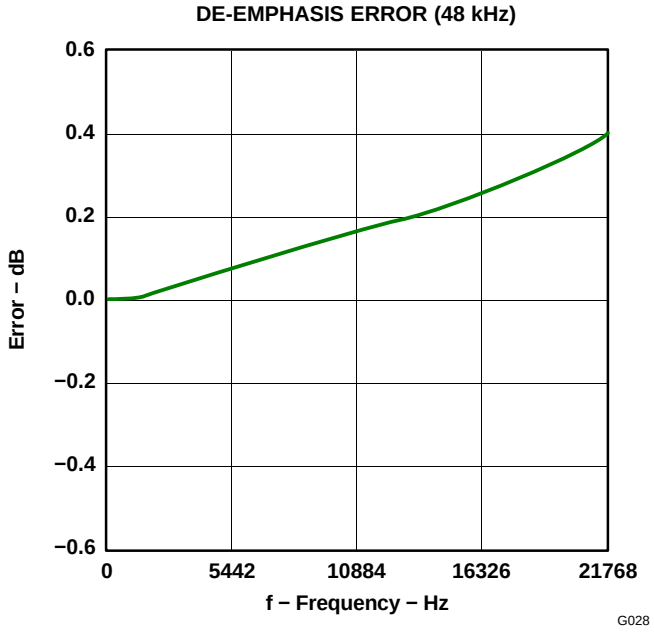


Figure 28.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

All specifications at T_A = 25°C, V_{CC} = V_{DD} = 3 V, f_S = 44.1 kHz, and f_{SYSCLK} = 384 f_S, unless otherwise noted

ANALOG LOW-PASS FILTER

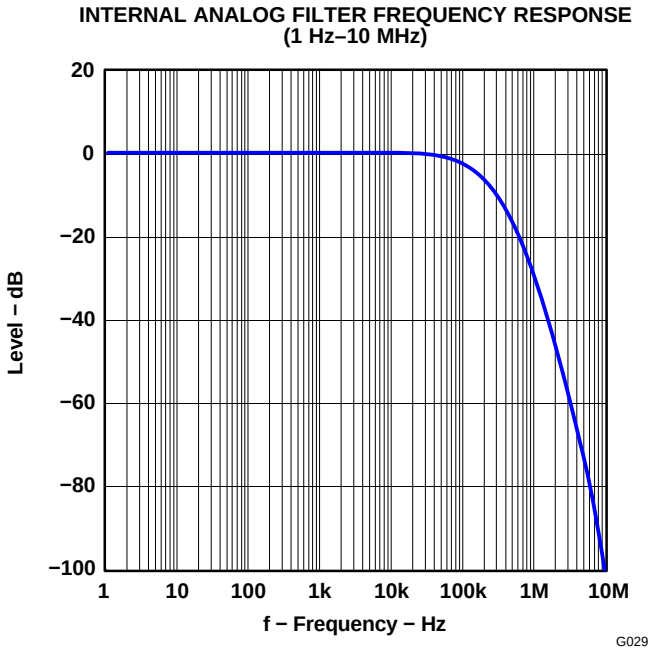


Figure 29.

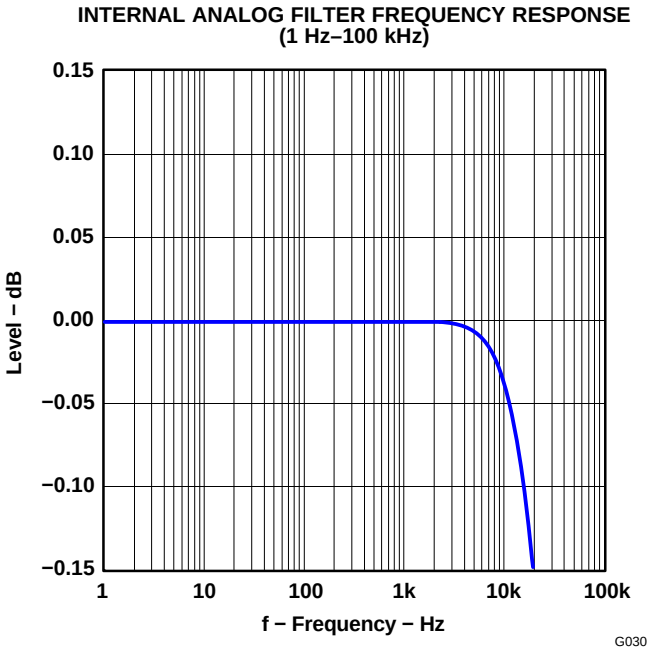
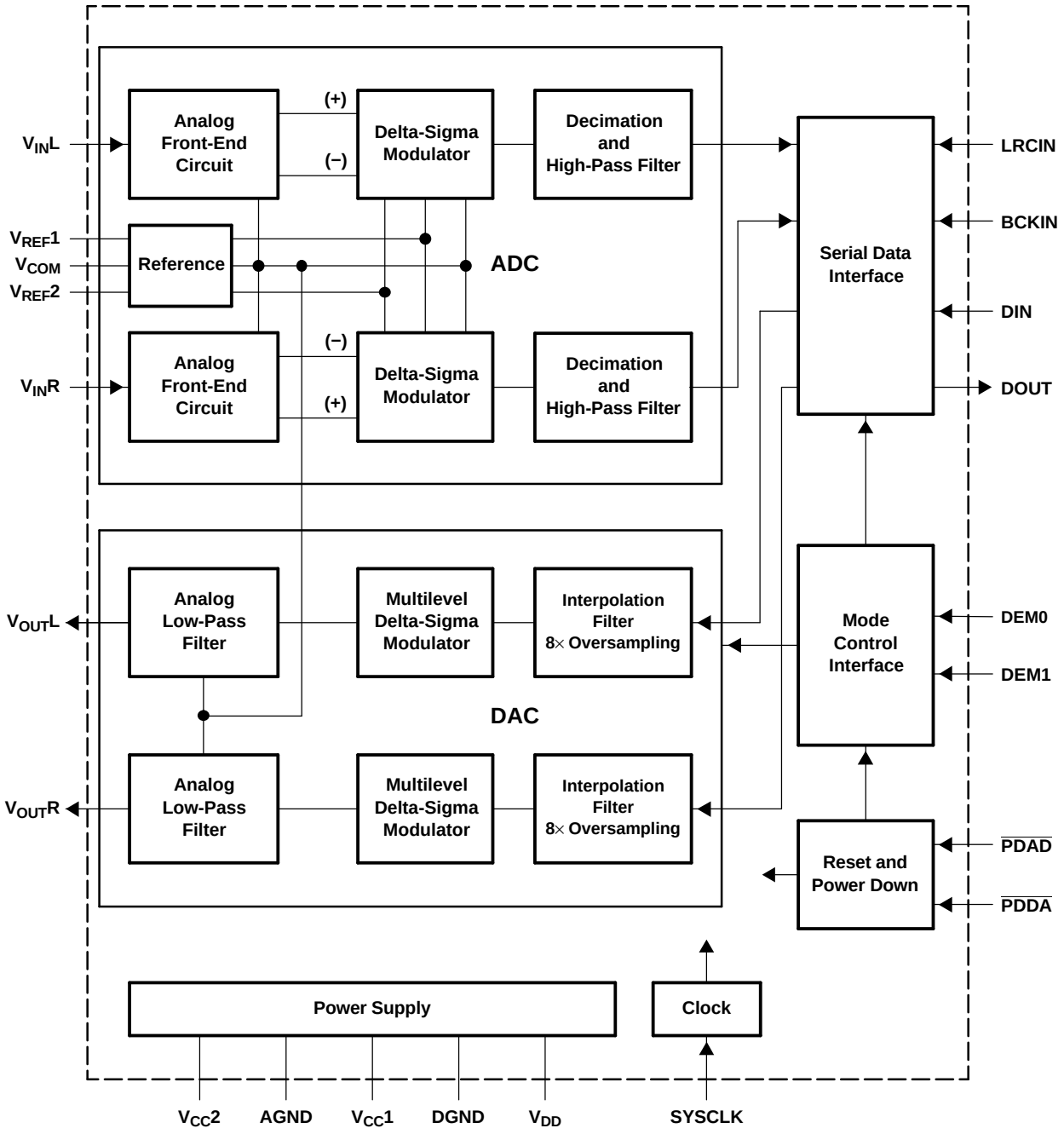


Figure 30.

BLOCK DIAGRAM



B0004-04

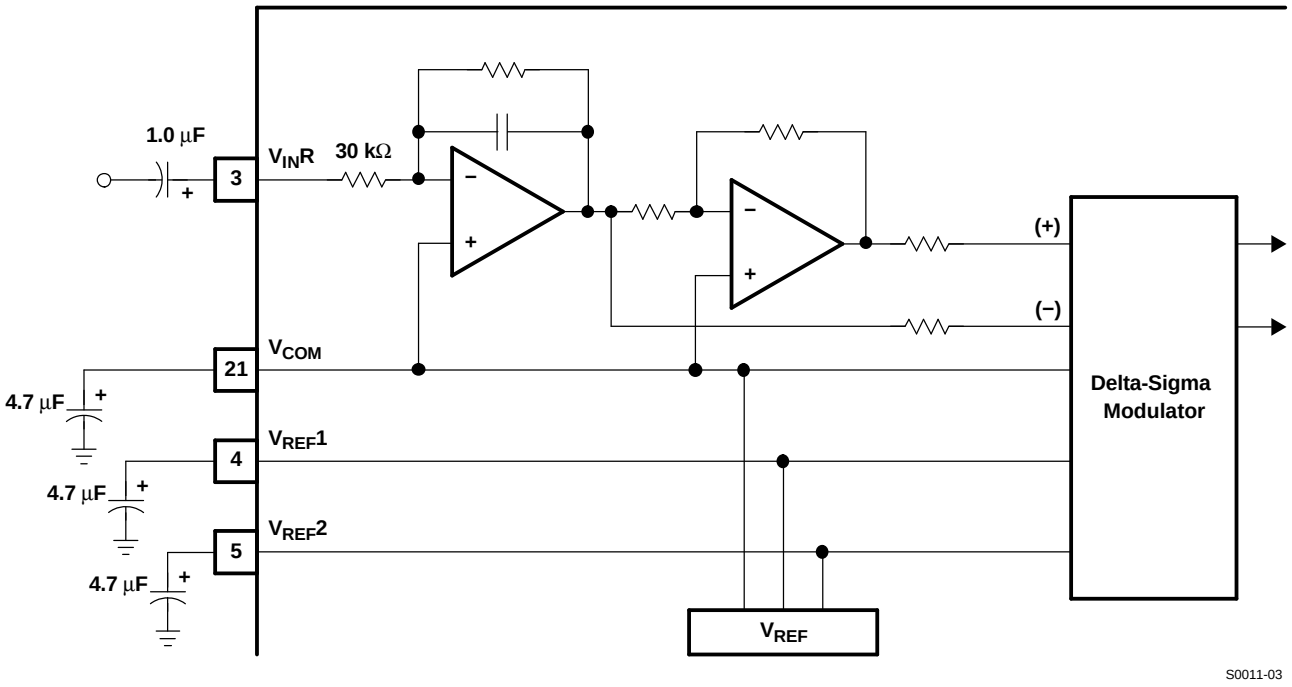


Figure 31. Analog Front End (Single-Channel)

APPLICATION INFORMATION

PCM AUDIO INTERFACE

The four-wire digital audio interface for the PCM3006 comprises LRCIN (pin 10), BCKIN (pin 11), DIN (pin 15), and DOUT (pin 12). The PCM3006 accepts 16-bit MSB-first, right-justified format for the DAC and 16-bit MSB-first, left-justified format for the ADC. The PCM3006 can accept 32, 48, or 64 bit clocks (BCKIN) in one clock of LRCIN. Figure 32 and Figure 33 illustrate audio data input/output format and timing.

FORMAT 0: PCM3006

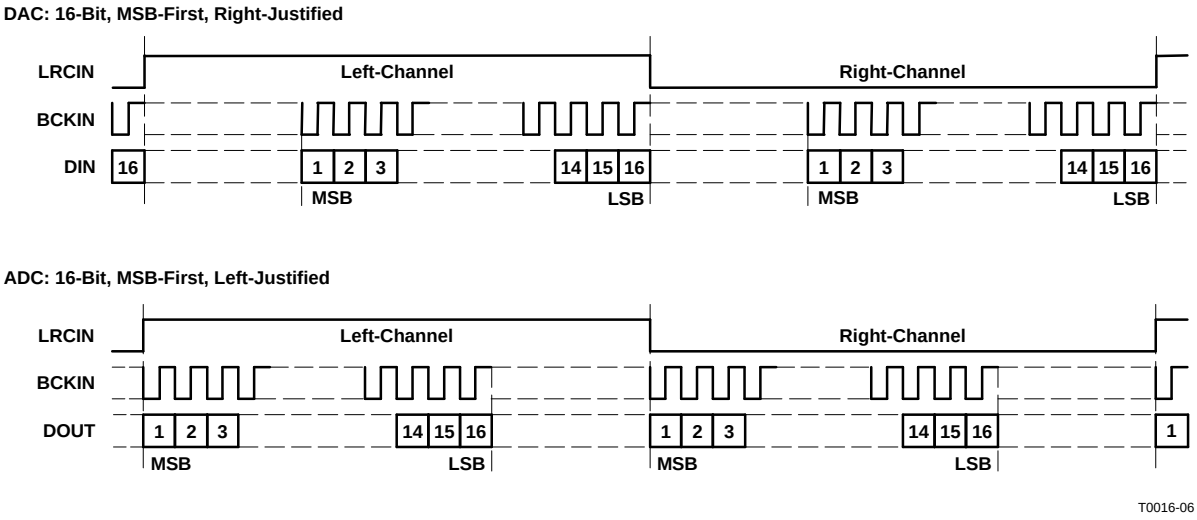
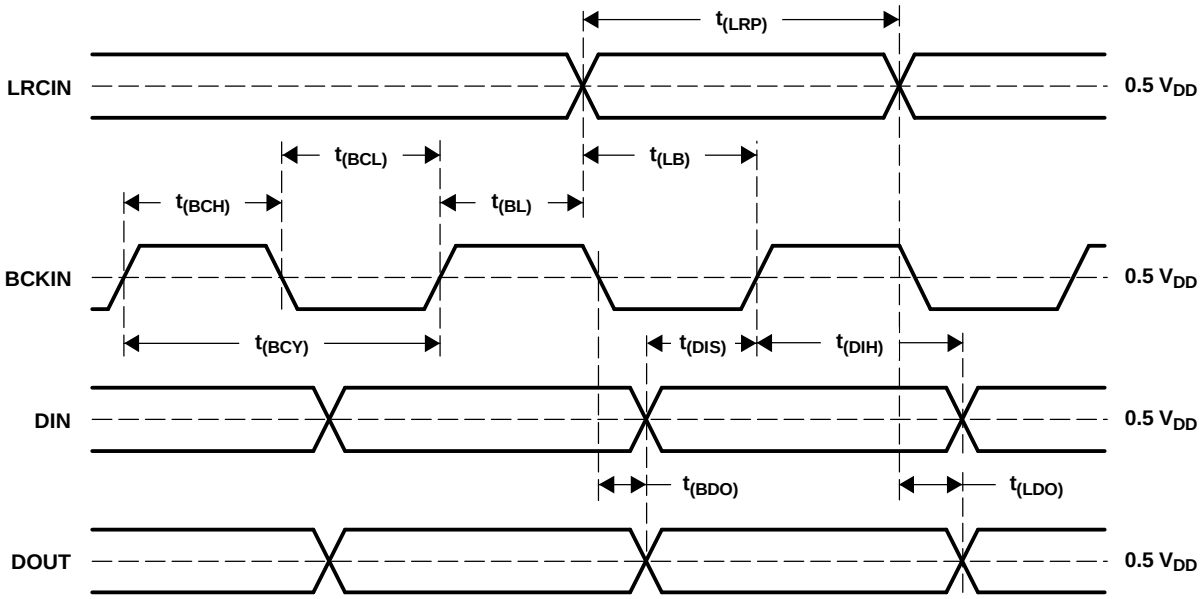


Figure 32. Audio Data Input/Output Format



BCKIN pulse cycle time	$t_{(BCY)}$	300 ns (min)
BCKIN pulse duration, HIGH	$t_{(BCH)}$	120 ns (min)
BCKIN pulse duration, LOW	$t_{(BCL)}$	120 ns (min)
BCKIN rising edge to LRCIN edge	$t_{(BL)}$	40 ns (min)
LRCIN edge to BCKIN rising edge	$t_{(LB)}$	40 ns (min)
LRCIN pulse duration	$t_{(LRP)}$	$t_{(BCY)}$ (min)
DIN setup time	$t_{(DIS)}$	40 ns (min)
DIN hold time	$t_{(DIH)}$	40 ns (min)
DOUT delay time to BCKIN falling edge	$t_{(BDO)}$	40 ns (max)
DOUT delay time to LRCIN edge	$t_{(LDO)}$	40 ns (max)
Rising time of all signals	$t_{(RISE)}$	20 ns (max)
Falling time of all signals	$t_{(FALL)}$	20 ns (max)

Figure 33. Audio Data Input/Output Timing

SYSTEM CLOCK

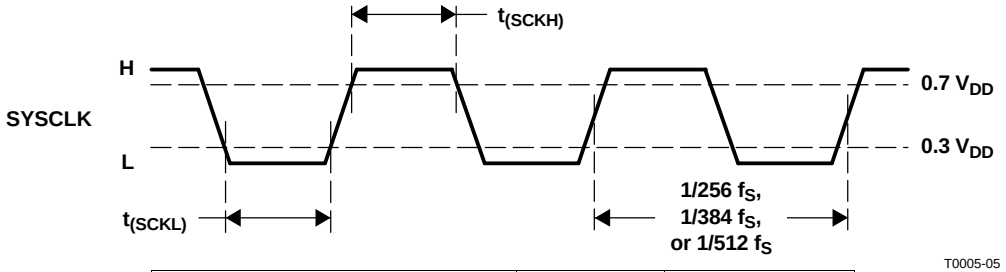
The system clock for the PCM3006 must be either 256 f_S, 384 f_S or 512 f_S, where f_S is the audio sampling frequency. The system clock should be provided to SYSCLK (pin 9).

The PCM3006 also has a system clock detection circuit that automatically senses if the system clock is operating at 256 f_S, 384 f_S, or 512 f_S. When a 384-f_S or 512-f_S system clock is used, the clock is divded into 256 f_S automatically. The 256-f_S clock is used to operate the digital filter and the delta-sigma modulator.

Table 1 lists the relationship of typical sampling frequencies and system clock frequencies, and Figure 34 illustrates the system clock timing.

Table 1. System Clock Frequencies

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY MHz		
	256 f_s	**384 f_s**	**512 f_s**
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760



System clock duration, HIGH	$t_{(SCKH)}$	12 ns (min)
System clock duration, LOW	$t_{(SCKL)}$	12 ns (min)

Figure 34. System Clock Timing

RESET

The PCM3006 has an internal power-on reset circuit, as well as an external forced reset. The internal power-on reset initializes (resets) when the supply voltage V_{DD} > 2.2 V (typ). External forced reset occurs when $\overline{PDAD}$ = LOW and $\overline{PDDA}$ = LOW. Figure 35 shows the internal power-on reset timing and Figure 36 shows the external forced reset timing by $\overline{PDAD}$ and $\overline{PDDA}$. During external forced reset, the outputs of the DAC are forced to GND (see Figure 37). The analog outputs are then forced to 0.5 V_{CC} during $t_{(DACDLY1)}$ (16384/f_S) after reset removal. The outputs of ADC are also invalid; digital outputs are forced to all zero during $t_{(ADCDLY1)}$ (18432/f_S) after reset removal.

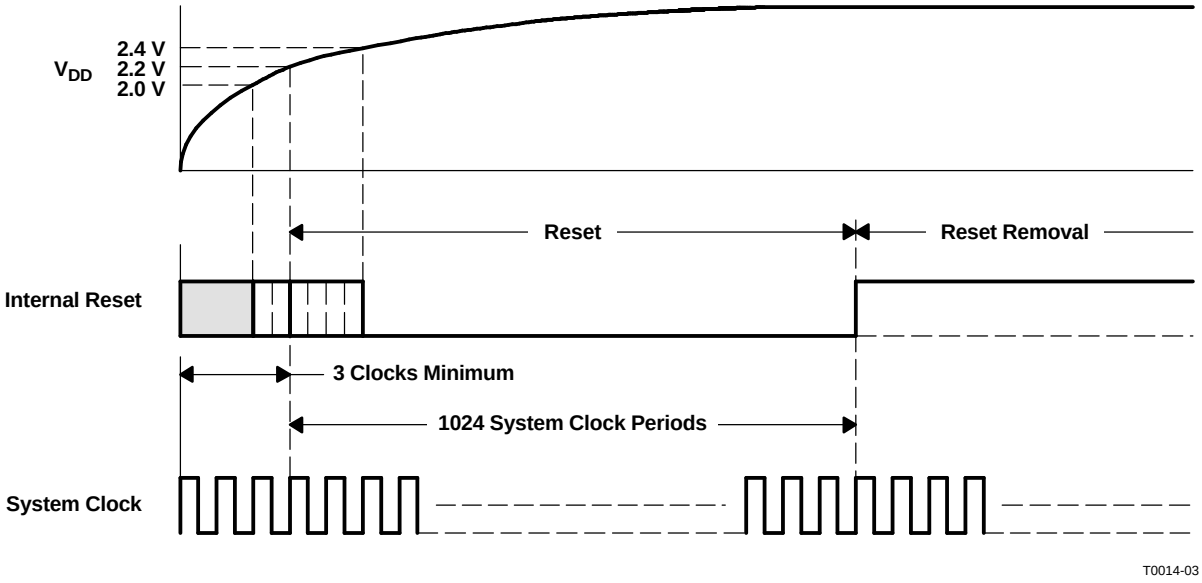


Figure 35. Internal Power-On Reset Timing

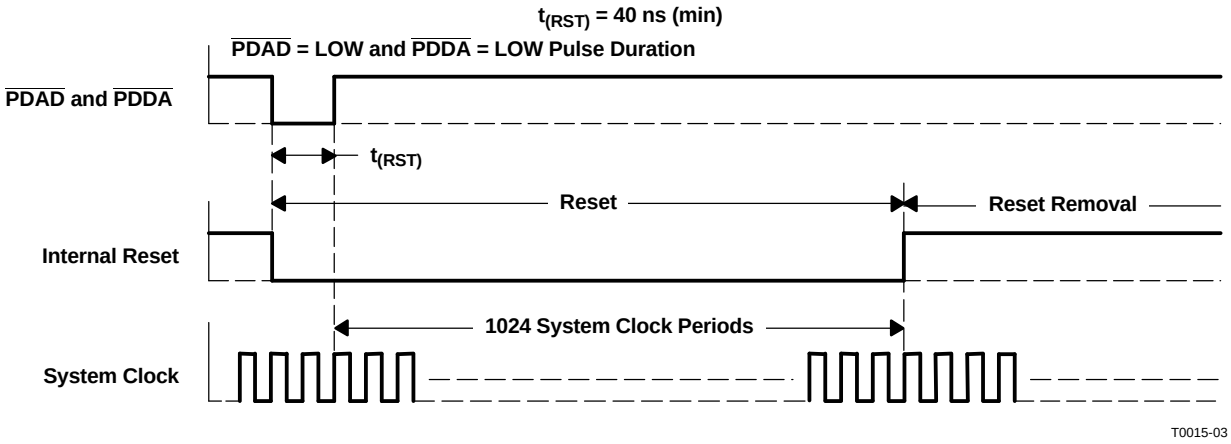
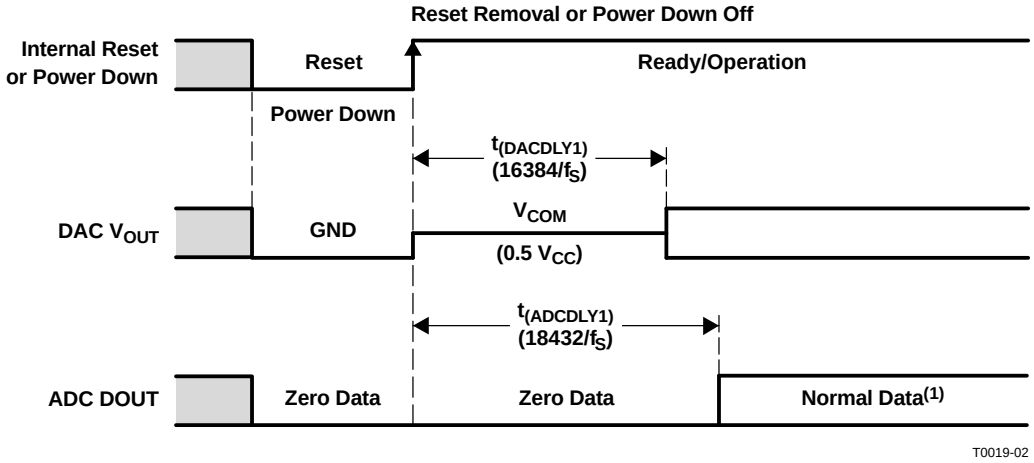


Figure 36. External Forced-Reset Timing

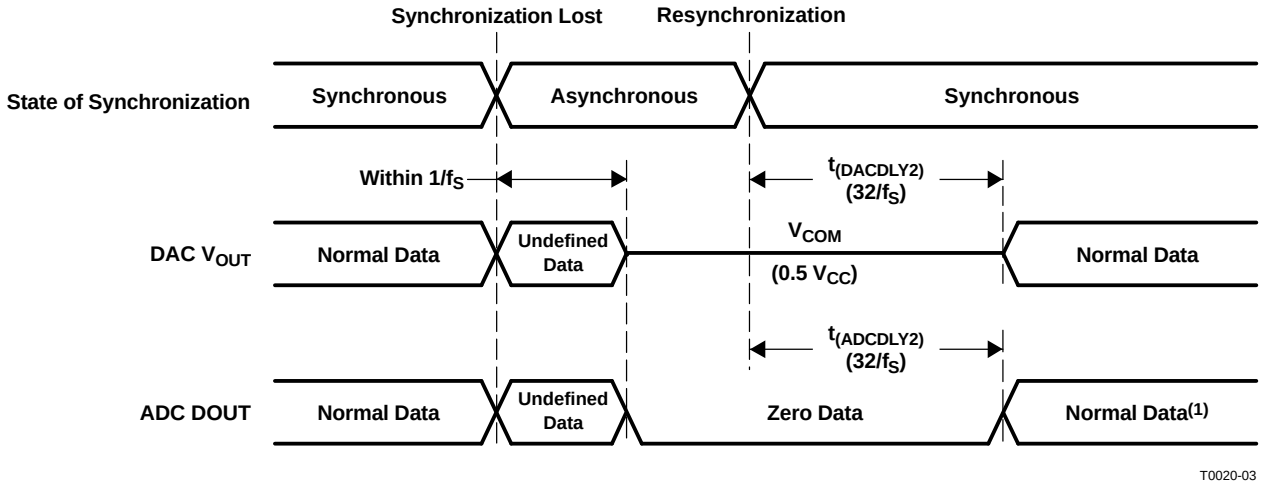


(1) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 37. DAC Output and ADC Output for Reset and Power Down

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM3006 operates with LRCIN synchronized to the system clock. The PCM3006 does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization of LRCIN and the system clock. If the relationship between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC stops within $1/f_S$, and the analog output is forced to bipolar zero (0.5 V_{CC}) until $t_{(DACDLY2)}$ delay time after the system clock is resynchronized to LRCIN. Internal operation of the ADC also stops within $1/f_S$, and the digital output codes are set to bipolar zero until $t_{(DACDLY2)}$ delay time after resynchronization occurs. If LRCIN remains synchronized to the system clock within 5 or fewer bit clocks, operation is normal. Figure 38 illustrates the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($<1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which cause output noise.



(1) The HPF transient response (exponentially attenuated signal from ±0.2% dc of FSR with 200-ms time constant) appears initially.

Figure 38. DAC Output and ADC Output for Loss of Synchronization

OPERATIONAL CONTROL

The PCM3006 has hardwire functional control using $\overline{\text{PDAD}}$ (pin 7) and $\overline{\text{PDDA}}$ (pin 8) for power-down control and DEM0 (pin 18) and DEM1 (pin 17) for de-emphasis.

$\overline{\text{PDAD}}$: ADC Power-Down Control (Pin 7)

This pin places the ADC section in the lowest power-consumption mode. The ADC operation is stopped by cutting the supply current to the ADC section, and DOUT is fixed to zero during ADC power-down-mode enable. Figure 37 illustrates the ADC DOUT response for ADC power-down ON/OFF. This does not affect the DAC operation.

$\overline{\text{PDAD}}$	POWER DOWN
Low	ADC power-down mode enabled
High	ADC power-down mode disabled

$\overline{\text{PDDA}}$: DAC Power-Down Control (Pin 8)

This pin places the DAC section in the lowest power-consumption mode. The DAC operation is stopped by cutting the supply current to the DAC section and VOUT is fixed to GND during DAC power-down-mode enable. Figure 37 illustrates the DAC VOUT response for DAC power-down ON/OFF. This does not affect the ADC operation.

$\overline{\text{PDDA}}$	POWER DOWN
Low	DAC power-down mode enabled
High	DAC power-down mode disabled

DEM [1:0]: DAC De-Emphasis Control (Pin 17 and Pin 18)

These pins select the de-emphasis mode as shown below:

DEM1	DEM0	DE-EMPHASIS
Low	Low	De-emphasis 44.1 kHz ON
Low	High	De-emphasis OFF
High	Low	De-emphasis 48 kHz ON
High	High	De-emphasis 32 kHz ON

APPLICATION AND LAYOUT CONSIDERATIONS

POWER-SUPPLY BYPASSING

The digital and analog power supply lines to the PCM3006 should be bypassed to the corresponding ground pins with both 0.1-μF ceramic and 10-μF tantalum capacitors as close to the device pins as possible. Although the PCM3006 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power-supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize the dynamic performance of the PCM3006, the analog and digital grounds are not connected internally. The PCM3006 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3006 ground pins to the analog ground plane using low-impedance connections. The PCM3006 should reside entirely over this plane to avoid coupling high-frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT

A tantalum capacitor, between 1 μF and 10 μF, is recommended as an ac-coupling capacitor at the inputs. Combined with the 30-kΩ characteristic input impedance, a 1-μF coupling capacitor establishes a 5.3-Hz cutoff frequency for blocking dc. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 30-kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7-μF to 10-μF tantalum capacitor is recommended between $V_{REF}1$, $V_{REF}2$, and AGND to ensure low source impedance for the ADC references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

V_{COM} INPUT

A 4.7-μF to 10-μF tantalum capacitor is recommended between V_{COM} and AGND to ensure low source impedance of the ADC and DAC common voltage. This capacitor should be located as close as possible to the V_{COM} pin to reduce dynamic errors on the ADC and DAC common voltage.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3006. The duty cycle and jitter at the system clock input pin should be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN), and word clock (LCRIN) must also be supplied simultaneously. Failure to supply the audio clocks results in a power dissipation increase of up to three times normal dissipation and can degrade long-term reliability if the maximum power-dissipation limit is exceeded.

RST CONTROL

If capacitors larger than 22 μF are used between V_{REF} and V_{COM}, external reset control by $\overline{\text{PDAD}}$ = LOW and $\overline{\text{PDDA}}$ = LOW is required after the V_{REF}, V_{COM} transient response has settled.

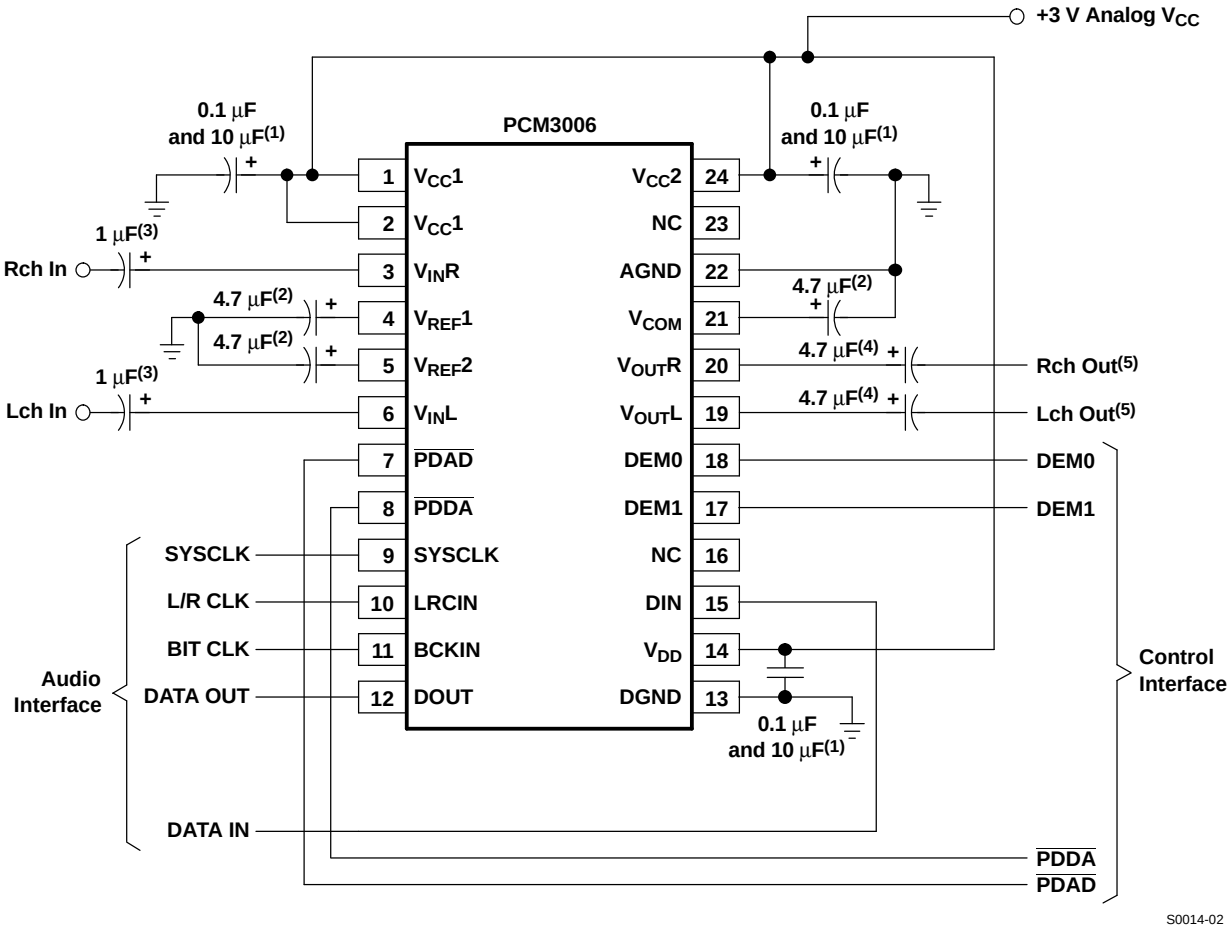
EXTERNAL MUTE CONTROL

Click noises are caused by dc level changes at the DAC output. To avoid any click noises going in and out of power-down mode, an external mute control is generally required. The recommended control sequence is as follows: external mute ON, codec power-down OFF, and then external mute OFF.

NOTE: If SYSCLK is stopped when the PCM3006 is in power-down mode, the device is internally reset.

TYPICAL CONNECTION DIAGRAM

Figure 39 is a schematic diagram showing typical connections for the PCM3006.



(1) 0.1-µF ceramic and 10-µF tantalum, typical, depending on power supply quality and pattern layout

(2) 4.7-µF, typical, gives settling time with a 30-ms (4.7 µF × 6.4 kΩ) time constant in the power ON and power-down OFF periods.

(3) 1-µF, typical, gives a 5.3-Hz cutoff frequency for the input HPF in normal operation, and gives a settling time with a 30-ms (1 µF × 30 kΩ) time constant in the power ON and power-down OFF periods.

(4) 4.7-µF, typical, gives a 3.4-Hz cutoff frequency for the output HPF in normal operation, and gives a settling time with a 47-ms (4.7 µF × 10 kΩ) time constant in the power ON and power-down OFF periods.

(5) Post low-pass filter with RIN > 10 kΩ, depending on the system performance requirements

Figure 39. Typical Connection Diagram for PCM3006

THEORY OF OPERATION

ADC SECTION

The PCM3006 ADC consists of two reference circuits, a stereo single-to-differential converter, a fully differential 5-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram in this data sheet illustrates the architecture of the ADC section, Figure 31 shows the single-to-differential converter, and Figure 40 illustrates the architecture of the 5-order delta-sigma modulator and transfer functions.

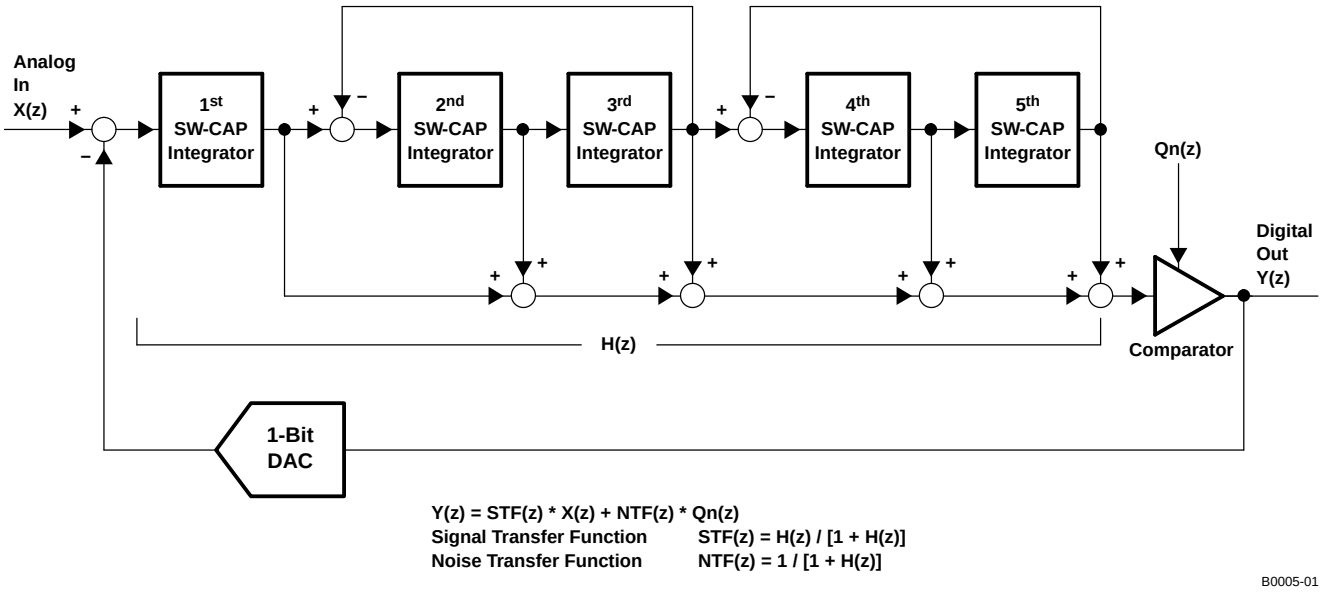


Figure 40. Simplified 5-Order Delta-Sigma Modulator

An internal reference circuit with three external capacitors provides all reference voltages that are required by the ADC, which defines the full-scale range for the converter. The internal single-to-differential voltage converter saves the design, space, and extra parts needed for the external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides wide dynamic range and excellent power-supply rejection performance. The input signal is sampled at 64× the oversampling rate, eliminating the need for a sample-and-hold circuit and simplifying antialias filtering requirements. The 5-order delta-sigma noise shaper consists of five integrators using switched-capacitor topology, a comparator, and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The 64-f_S one-bit data stream from the modulator is converted to 1-f_S 16-bit data words by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a high-pass filter function contained within the decimation filter.

DAC SECTION

The delta-sigma DAC section of the PCM3006 is based on a 5-level amplitude quantizer and a third-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 41. This 5-level delta-sigma modulator has the advantage of stability and clock-jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8× interpolation filter is 64 f_S for a 256-f_S system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator shown in Figure 42.

THEORY OF OPERATION (continued)

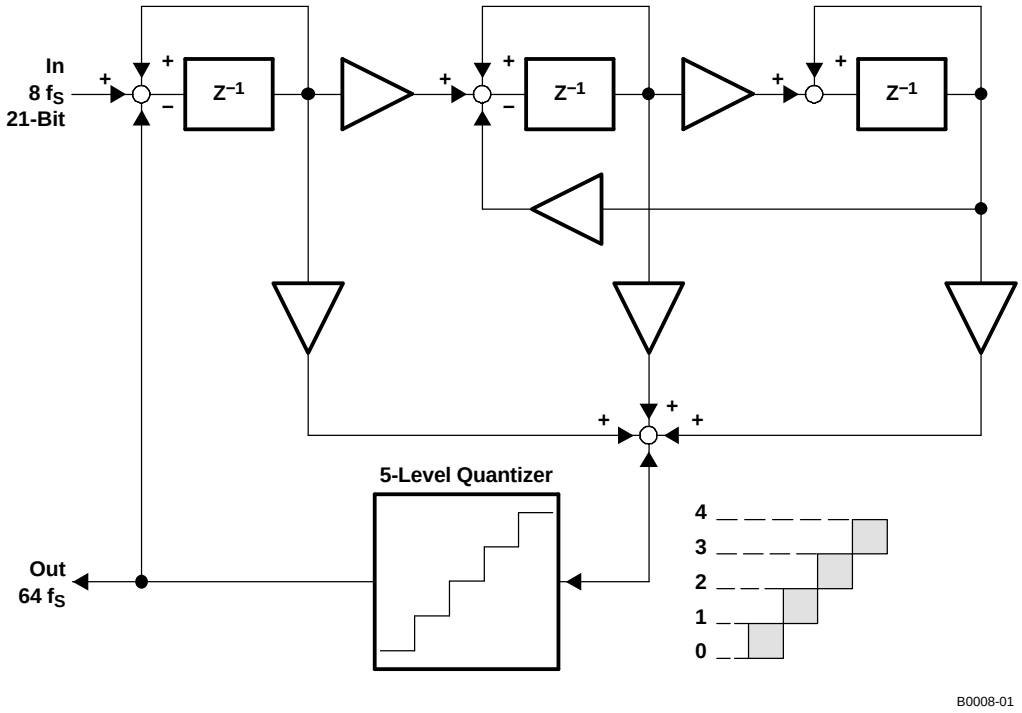


Figure 41. 5-Level ΔΣ Modulator Block Diagram

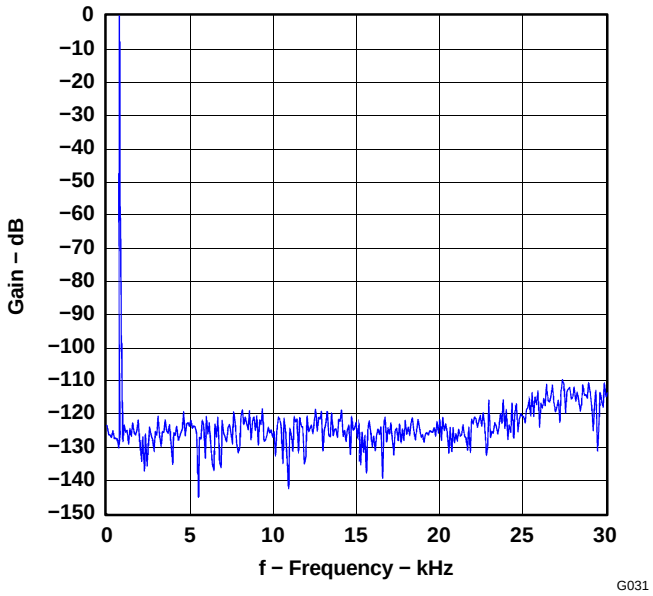


Figure 42. Quantization Noise Spectrum

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCM3006T	ACTIVE	SSOP	DCV	24	128	Green (RoHS & no Sb/Br)	CU SNBI	Level-1-260C-UNLIM
PCM3006T/2K	ACTIVE	SSOP	DCV	24	2000	Green (RoHS & no Sb/Br)	CU SNBI	Level-1-260C-UNLIM
PCM3006T/2KG6	ACTIVE	SSOP	DCV	24	2000	Green (RoHS & no Sb/Br)	CU SNBI	Level-1-260C-UNLIM
PCM3006TG6	ACTIVE	SSOP	DCV	24	128	Green (RoHS & no Sb/Br)	CU SNBI	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

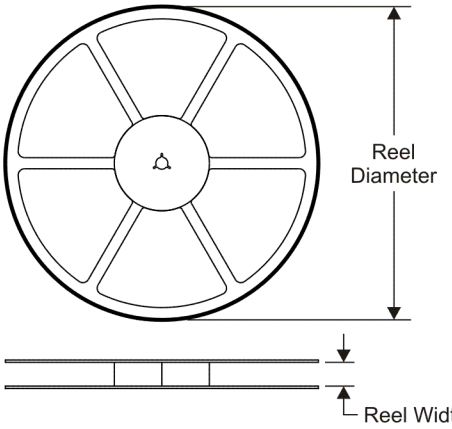
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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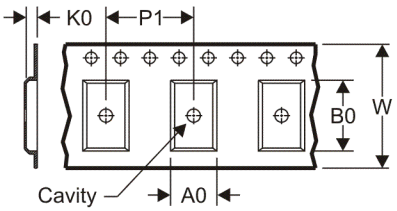
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

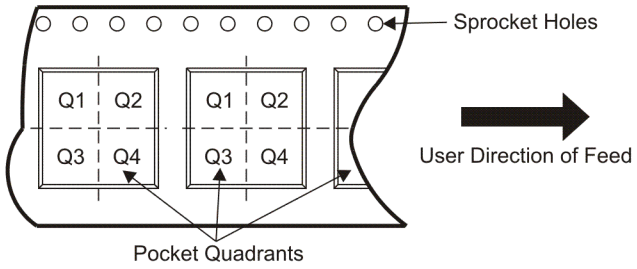


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

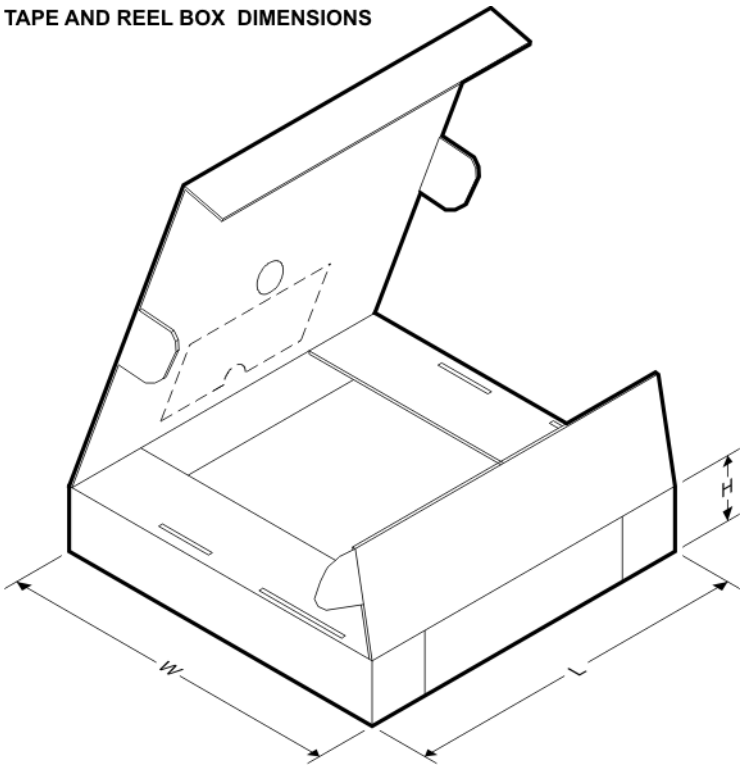
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM3006T/2K	SSOP	DCV	24	2000	330.0	17.4	8.1	8.5	1.75	12.0	16.0	Q1

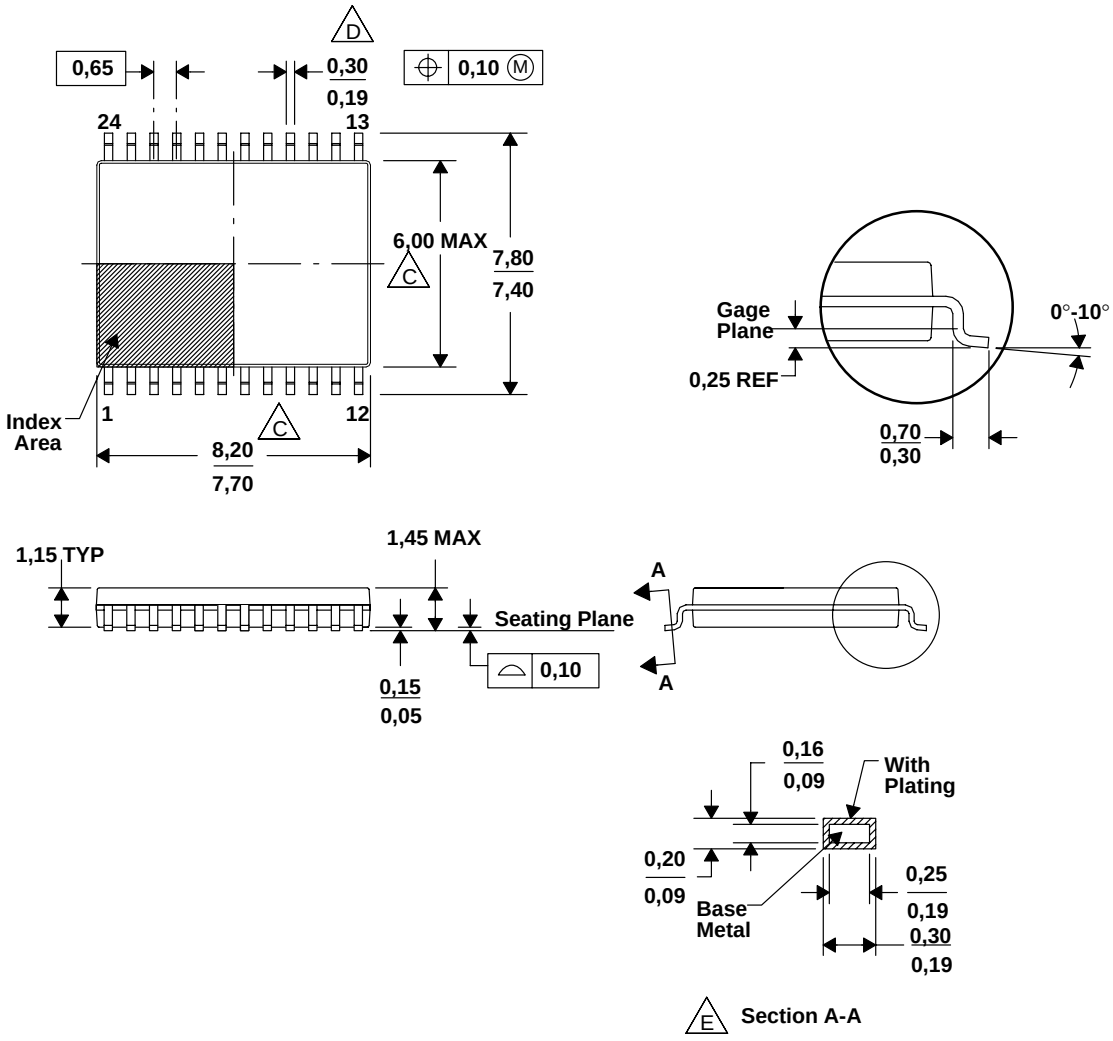
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM3006T/2K	SSOP	DCV	24	2000	346.0	346.0	33.0

DCV (R-PSOP-G24) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions, but do include mold mismatch and are measured at datum plane, mold parting line. Mold flash or protrusion shall not exceed 0,20mm per side.
D. Lead width dimension does not include dambar protrusion/ intrusion. Allowable dambar protrusion shall be 0,13mm total in excess of width dimension at maximum material condition. Dambar intrusion shall not reduce width dimension by more than 0,07mm at least material condition.
E. All dimensions in Section A-A apply to the flat section of the lead between 0,10mm and 0,25mm from the lead tips.
F. A visual index feature must be located within the cross-hatched area.

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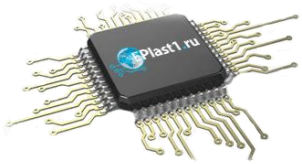
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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.