# USB2640i/USB2641i

# Industrial Temperature USB 2.0 Flash Media Controller and USB Hub Combo

## PRODUCT FEATURES

**Datasheet**

### General Description

The SMSC USB2640i/USB2641i is a USB 2.0 compliant, Hi-Speed hub for USB port expansion with an attached mass storage class peripheral controller. The controller allows read/write capability to popular flash media from the following families:

- Secure Digital™ (SD)
- MultiMediaCard™ (MMC)
- xD-Picture Card™ (xD)[1]
- Memory Stick®(MS)

The USB2640i/USB2641i is a fully integrated, single chip solution providing USB expansion and integrated flash card media reader/writer capability of ultra high performance operation. Average sustained transfer rates exceeding 35 MB/s are possible[2].

### Highlights

- Hub controller with internally connected ultra fast flash media reader/writer and 2 exposed downstream ports for external peripheral expansion
- Flash media reader/writer employs multiplexed card interfaces which are optimized for use with single card insertion combo sockets
- Hardware-controlled data flow architecture for all self-mapped media
- Optional support for external firmware access via SPI interface
- **PortMap**
  - — Flexible port mapping and port disable sequencing supports multiple platform designs
- **PortSwap**
  - — Programmable USB differential-pair pin locations eases PCB design by aligning USB signal traces directly to connectors
- **PHYBoost**
  - — Programmable USB transceiver drive strength recovers signal integrity

1.Support and capabilities for xD-Picture Card are not applicable for the USB2641i. Please obtain a user license from the xD-Picture Card License Office to support this flash media format.
2.Host and media dependent.

### Features

- Compliant with the following flash media card specifications: SD 2.0 / MMC 4.2 / MS 1.43 / MS-Pro 1.02 / MS-PRO-HG 1.01 / MS-Duo 1.10 / xD 1.2
- Supports a single external 3.3 V supply source; internal regulators provide 1.8 V internal core voltage for additional bill of materials and power savings
- The transaction translator (TT) in the hub supports operation of Full-Speed and Low-Speed peripherals
- 9 K RAM | 64 K on-chip ROM
- Enhanced EMI rejection and ESD protection performance
- Onboard 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
- Up to 9 GPIOs for special functions
- 8051 8-bit microprocessor
- Hub and flash media reader/writer configuration from a single source: External $I^2C$ ROM or external SPI ROM
  - — Configures internal code using an external $I^2C$ EEPROM
  - — Supports external code using a SPI Flash EEPROM
  - — Customizable vendor ID, product ID, language ID
- EEPROM update via USB
- 48-pin QFN lead-free, RoHS compliant package (7x7 mm)
- The SMSC USB2640i/USB2641i supports the industrial temperature range of -40°C to 85°C

### Applications

- Desktop and mobile PCs
- Personal mobile devices
- Printers
- GPS navigation systems
- Media Players/Viewers
- Consumer A/V
- Set-top boxes
- Industrial products

## ORDER NUMBERS:

**USB2640i/USB2641i-HZH-XX for 48-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE**

"XX" in the order number indicates the internal ROM firmware revision level.

Please contact your SMSC representative for more information.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

# Table of Contents

# List of Tables

# List of Figures

# Chapter 1 Overview

The SMSC USB2640i/USB2641i is an integrated USB 2.0 compliant, Hi-Speed hub for USB port expansion with an attached bulk only mass storage class peripheral controller. This multi-format flash media controller and USB Hub Combo features three downstream ports: one port is dedicated to an internally connected ultra fast flash media reader/writer and two exposed downstream ports are available for external peripheral expansion.

The SMSC USB2640i/USB2641i is an ultra fast, OEM-configurable, hub controller IC with three downstream ports for embedded USB solutions. The USB2640i/USB2641i will attach to an upstream port as a Full-Speed Hub or as a Full-/Hi-Speed Hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed Hub) downstream devices on all of the enabled downstream ports.

All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down and pull-up resistors on D+ and D– pins. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

The USB2640i/USB2641i includes programmable features such as:

**PortMap** which provides flexible port mapping and disable sequences. The downstream ports of a USB2640i/USB2641i hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB2640i/USB2641i automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

**PortSwap** which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.

**PHYBoost** which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity that has been compromised by system level variables such as poor PCB layout, long cables, etc.

## 1.1 Device Features

### Hardware Features

- Single chip flash media controller
- The SMSC USB2640i/USB2641i supports the industrial temperature range of -40°C to 85°C
- Transaction translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

**Compliant with the following flash media card specifications:**

- Secure Digital 2.0 / MultiMediaCard 4.2
  - SD 2.0, HS-SD, HC-SD
  - TransFlash™ and reduced form factor media
  - 1/4/8 bit MMC 4.2
- SDIO and MMC streaming mode support
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2 (USB2640i only)
- On board 24 MHz crystal driver circuit
- Optional external 24 MHz clock input
  - Must be used with an external resistor divider to provide a 1.8 V signal
- Up to 9 GPIOs: Configuration and polarity for special function use such as LED indicators, button inputs, and power control to memory devices
  - The number of actual GPIOs depends on the implementation configuration used
  - One GPIO available with up to 200 mA drive and protected “fold-back” short circuit current
- 8051 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 KB ROM; 9 KB RAM
- Internal regulator for 1.8 V core operation
- Optimized pinout improves signal flow, easing implementation and allowing for improved signal integrity treatment

### Software Features

- Optimized for low latency interrupt handling
- Hub and flash media reader/writer configuration from a single source: External $I^2C$ ROM or external SPI ROM
- EEPROM update via USB
- Please see the USB2640i/USB2641i Software Release Notes for additional software features

## 1.2 OEM Selectable Features

### Hub

A default configuration is available in USB2640i/USB2641i following a reset. The USB2640i/USB2641i may also be configured by an external $I^2C$ EEPROM or via external SPI ROM flash.

The USB2640i/USB2641i supports several OEM selectable features:

- Compound Device support (port is permanently hardwired to a downstream USB peripheral device), on a port-by-port basis.
- Select over-current sensing and port power control on an individual (port-by-port) or ganged (all ports together) basis to match the OEM's choice of circuit board component selection.
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs.
- Configure the delay time for turning on downstream port power.
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequence. Ports can be disabled/reordered in any sequence to support multiple platforms with a single design. The hub will automatically reorder the remaining ports to match the host controller's numbering scheme.
- Programmable USB differential-pair pin location.
  - Eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength. Recover USB signal integrity due to compromised system environments using four levels of signal drive strength.
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port.
- Indicate the maximum current required for the hub controller.

### Flash Media Controller

- Customize vendor ID, product ID, and device ID.
- 12-hex digit (max) serial number string
- Customizable vendor specific data by optional use of external serial EEPROM
- 28-character manufacturer ID and product string for flash media reader/writer
- LED blink interval or duration

# Chapter 2 Acronyms

**FM:** Flash Media

**FMC:** Flash Media Controller

**FS:** Full-speed Device

**LS:** Low-speed Device

**HS:** Hi-speed Device

**I²C®:** Inter-Integrated Circuit[1]

**MMC:** MultiMediaCard

**MS:** Memory Stick

**MSC:** Memory Stick Controller

**OCS:** Over-current Sense

**RXD:** Received eXchange Data

**SD:** Secure Digital

**SDC:** Secure Digital Controller

**TXD:** Transmit eXchange Data

**UART:** Universal Asynchronous Receiver-Transmitter

**UCHAR:** Unsigned Character

**UINT:** Unsigned Integer

**xD:** xD-Picture Card



1.I²C is a registered trademark of Philips Corporation.

# Chapter 3 Pin Configurations

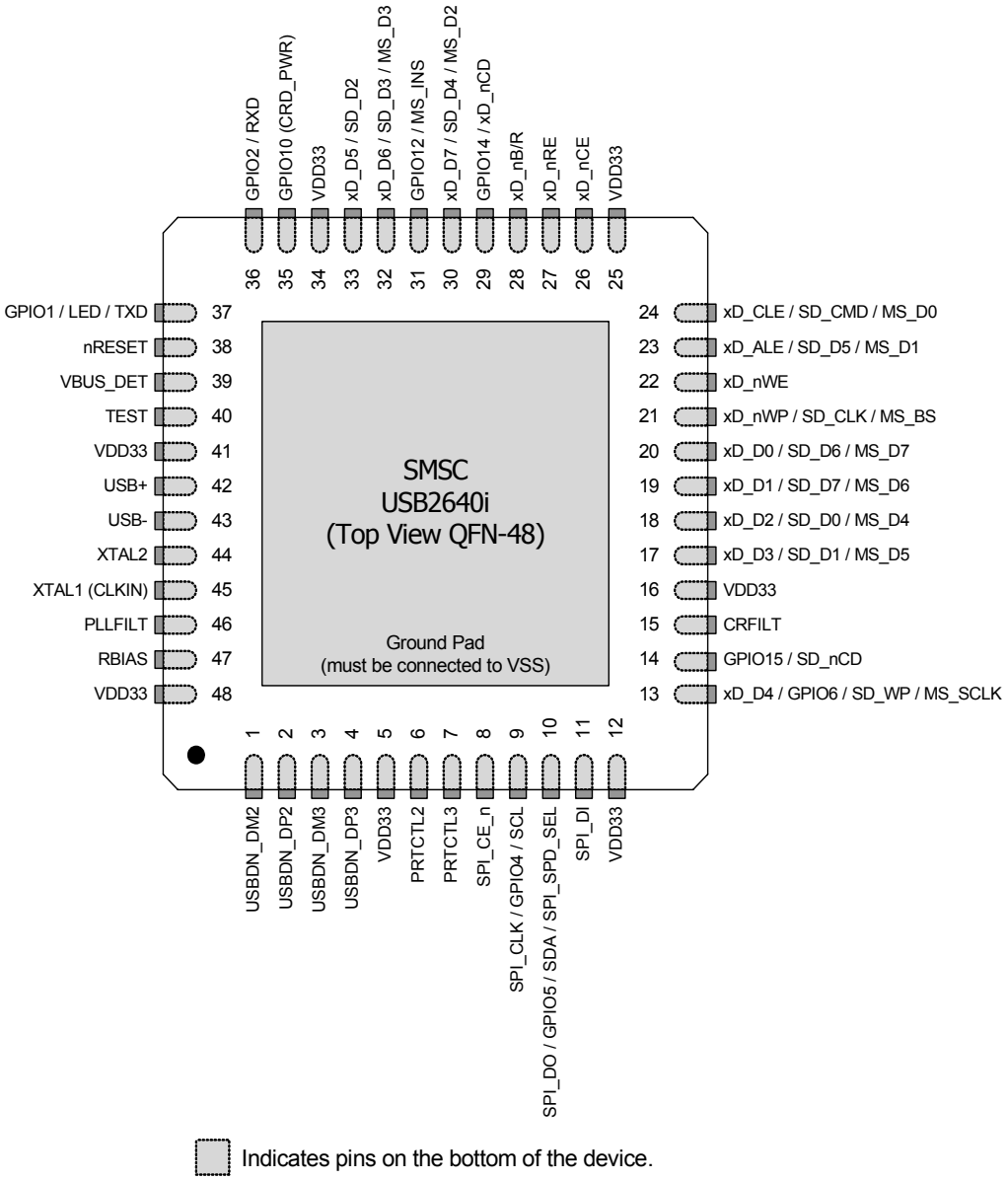



**Figure 3.1 USB2640i 48-Pin QFN**

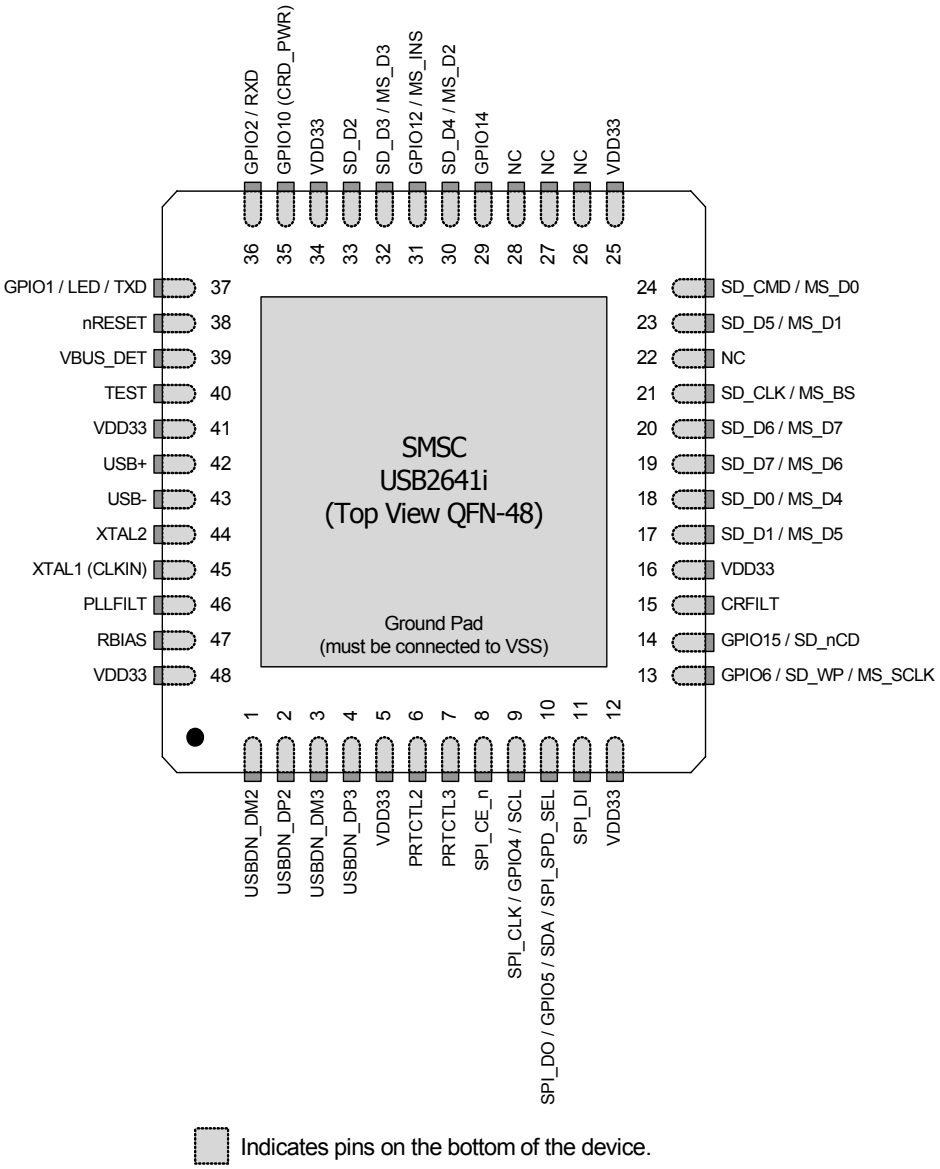



**Figure 3.2 USB2641i 48-Pin QFN**

# Chapter 4 Block Diagrams

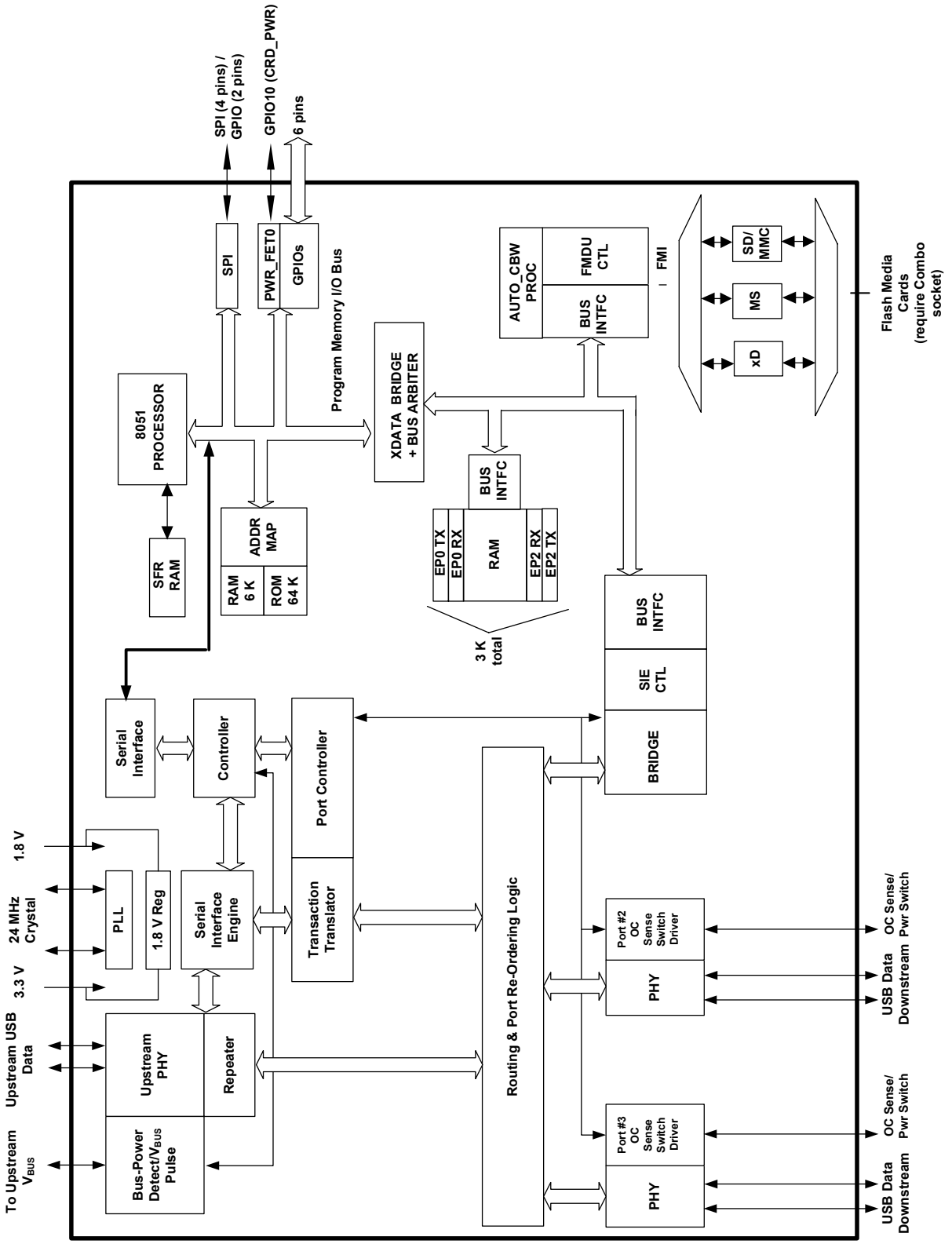



**Figure 4.1 USB2640i Block Diagram**

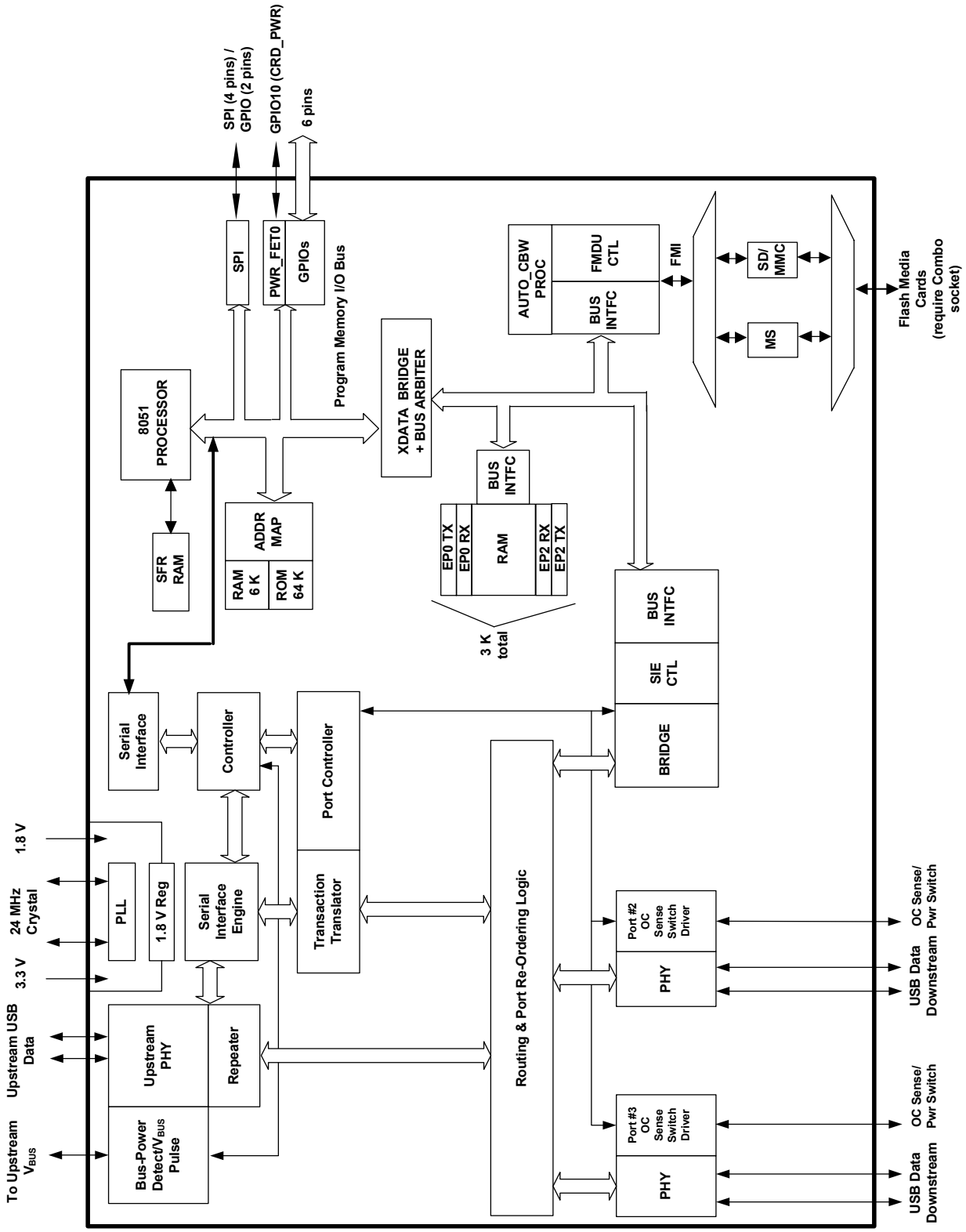



**Figure 4.2 USB2641i Block Diagram**

# Chapter 5 Pin Tables

## 5.1 48-Pin Tables

**Table 5.1 USB2640i 48-Pin Table**

| | | | |
|---|---|---|---|
| **xD-PICTURE CARD (Only in USB2640i) / SECURE DIGITAL / MEMORY STICK INTERFACE (18 PINS)** | | | |
| xD_D3 / SD_D1 / MS_D5 | xD_D2 / SD_D0 / MS_D4 | xD_D1 / SD_D7 / MS_D6 | xD_D0 / SD_D6 / MS_D7 |
| xD_nWP / SD_CLK / MS_BS | xD_ALE / SD_D5 / MS_D1 | xD_CLE / SD_CMD / MS_D0 | xD_D7 / SD_D4 / MS_D2 |
| xD_D6 / SD_D3 / MS_D3 | xD_D5 / SD_D2 | xD_nRE | xD_nWE |
| xD_D4 / GPIO6 / SD_WP / MS_SCLK | xD_nB/R | xD_nCE | GPIO12 / MS_INS |
| GPIO14 / xD_nCD | GPIO15 / SD_nCD | | |
| **USB INTERFACE (5 PINS)** | | | |
| USB+ | USB- | XTAL1 (CLKIN) | XTAL2 |
| RBIAS | | | |
| **2-PORT USB INTERFACE (7 PINS)** | | | |
| USBDN_DP2 | USBDN_DM2 | PRTCTL2 | PRTCTL3 |
| USBDN_DP3 | USBDN_DM3 | VBUS_DET | |

**Table 5.1 USB2640i 48-Pin Table (continued)**

| | | | |
|---|---|---|---|
| **SPI INTERFACE (4 PINS)** | | | |
| SPI_CE_n | SPI_CLK / GPIO4 / SCL | SPI_DO / GPIO5 / SDA / SPI_SPD_SEL | SPI_DI |
| **MISC (5 PINS)** | | | |
| nRESET | TEST | GPIO1 / LED / TXD | GPIO2 / RXD |
| GPIO10 (CRD_PWR) | | | |
| **POWER AND GROUND (9 PINS)** | | | |
| (7) VDD33 | CRFILT | PLLFILT | |
| **TOTAL 48** | | | |

**Table 5.2 USB2641i 48-Pin Table**

| | | | |
|---|---|---|---|
| **SECURE DIGITAL / MEMORY STICK INTERFACE (14 PINS)** | | | |
| SD_D1 / MS_D5 | SD_D0 / MS_D4 | SD_D7 / MS_D6 | SD_D6 / MS_D7 |
| SD_CLK / MS_BS | SD_D5 / MS_D1 | SD_CMD / MS_D0 | SD_D4 / MS_D2 |
| SD_D3 / MS_D3 | SD_D2 | GPIO12 / MS_INS | GPIO14 |
| GPIO6 / SD_WP / MS_SCLK | GPIO15 / SD_nCD | | |
| **USB INTERFACE (5 PINS)** | | | |
| USB+ | USB- | XTAL1 (CLKIN) | XTAL2 |

**Table 5.2 USB2641i 48-Pin Table (continued)**

| | | | |
|---|---|---|---|
| RBIAS | | | |
| **2-PORT USB INTERFACE (7 PINS)** | | | |
| USBDN_DP2 | USBDN_DM2 | PRTCTL2 | PRTCTL3 |
| USBDN_DP3 | USBDN_DM3 | VBUS_DET | |
| **SPI INTERFACE (4 PINS)** | | | |
| SPI_CE_n | SPI_CLK / GPIO4 / SCL | SPI_DO / GPIO5 / SDA / SPI_SPD_SEL | SPI_DI |
| **MISC (5 PINS)** | | | |
| nRESET | TEST | GPIO1 / LED / TXD | GPIO2 / RXD |
| GPIO10 (CRD_PWR) | | | |
| **POWER AND GROUND (13 PINS)** | | | |
| (7) VDD33 | CRFILT | PLLFILT | PLLFILT |
| (4) NC | | | |
| **TOTAL 48** | | | |

# Chapter 6 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 7, "Configuration Options," on page 28. Please reference Chapter 2, Acronyms for a list of the acronyms used.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present in the signal name, the signal is asserted at a high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

## 6.1 USB2640i/USB2641i Pin Descriptions

**Table 6.1 USB2640i/USB2641i Pin Descriptions**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| **xD-PICTURE CARD INTERFACE (APPLIES ONLY TO USB2640i)** | | | |
| xD_D[7:0] | 30<br>32<br>33<br>13<br>17<br>18<br>19<br>20 | I/O12PU | xD-Picture Card Data 7-0<br><br>These pins are the bi-directional data signal xD_D7 - xD_D0 and have weak internal pull-up resistors. |
| xD_ALE | 23 | O12PD | xD-Picture Card Address Strobe<br><br>This pin is an active high Address Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled. |
| xD_nB/R | 28 | IPU | xD-Picture Card Busy or Data Ready<br><br>This pin is connected to the BSY/RDY pin of the xD-Picture Card device.<br><br>When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET.<br><br>If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required). |

**Table 6.1 USB2640i/USB2641i Pin Descriptions (continued)**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| xD_nCE | 26 | O12PU | xD-Picture Card Chip Enable<br><br>This pin is an active low chip enable signal for the xD-Picture Card device.<br><br>When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET.<br><br>If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required). |
| xD_CLE | 24 | O12PD | xD-Picture Card Command Strobe<br><br>This pin is an active high Command Latch Enable signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled. |
| GPIO14 / | 29 | I/O12 | This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| xD_nCD | | | xD-Picture Card Detection GPIO<br><br>This is a GPIO designated by the default firmware as the xD-Picture Card detection pin. |
| xD_nRE | 27 | O12PU | xD-Picture Read Enable<br><br>This pin is an active low read strobe signal for the xD-Picture Card device.<br><br>When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET.<br><br>If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required). |
| xD_nWE | 22 | O12PU | xD-Picture Card Write Enable<br><br>This pin is an active low write strobe signal for the xD-Picture Card device.<br><br>When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal power FET.<br><br>If an external FET is used (the internal FET is disabled), then the internal pull-up is not available (an external pull-up is required). |
| xD_nWP | 21 | O12PD | xD-Picture Card Write Protect<br><br>This pin is an active low write protect signal for the xD-Picture Card device. This pin has a weak pull-down resistor that is permanently enabled. |
| **MEMORY STICK INTERFACE** | | | |
| MS_BS | 21 | O12 | Memory Stick Bus State<br><br>This pin is connected to the bus state pin of the MS device. It is used to control the Bus States 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device. |

**Table 6.1 USB2640i/USB2641i Pin Descriptions (continued)**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| GPIO12 / | 31 | I/O12 | This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| MS_INS | | IPU | Memory Stick Card Insertion GPIO<br><br>This is a GPIO designated by the default firmware as the Memory Stick card detection pin and has an internal weak pull-up resistor. |
| MS_SCLK | 13 | O12 | Memory Stick System Clock<br><br>This pin is an output clock signal to the MS device. |
| MS_D[7:0] | 20<br>19<br>17<br>18<br>32<br>30<br>23<br>24 | I/O12PD | Memory Stick System Data In/Out<br><br>These pins are the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on MS_D0.<br><br>MS_D0, MS_D2, and MS_D3 have weak pull-down resistors. MS_D1 has a pull down resistor if in parallel mode, otherwise it is disabled. In 4- or 8-bit parallel modes, all MS_D7 - MS_D0 signals have weak pull-down resistors. |
| **SECURE DIGITAL / MULTIMEDIACARD INTERFACE** | | | |
| SD_D[7:0] | 19<br>20<br>23<br>30<br>32<br>33<br>17<br>18 | I/O12PU | Secure Digital Data 7-0<br><br>These are the bi-directional data signals SD_D0-SD_D7 and have weak pull-up resistors. |
| SD_CLK | 21 | O12 | Secure Digital Clock<br><br>This is an output clock signal to the SD/MMC device. |
| SD_CMD | 24 | I/O12PU | Secure Digital Command<br><br>This is a bi-directional signal that connects to the CMD signal of the SD/MMC device and has an internal weak pull-up resistor. |
| GPIO6 / | 13 | I/O12 | This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| SD_WP | | | Secure Digital Write Protected GPIO<br><br>This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect detect pin. |
| GPIO15 / | 14 | I/O12 | This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| SD_nCD | | | Secure Digital Card Detect GPIO<br><br>This is a GPIO designated by the default firmware as the Secure Digital card detection pin. |

**Table 6.1 USB2640i/USB2641i Pin Descriptions (continued)**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| **USB INTERFACE** | | | |
| USB-<br>USB+ | 43<br>42 | I/O-U | USB Bus Data<br><br>These pins connect to the upstream USB bus data signals. USB+ and USB- can be swapped using the PortSwap feature (See Section 7.3.5.20, "F1h: Port Swap," on page 46). |
| USBDN_DM [3:2]<br>USBDN_DP [3:2] | 3<br>1<br>4<br>2 | I/O-U | USB Bus Data<br><br>These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature (See Section 7.3.5.20, "F1h: Port Swap," on page 46). |
| PRTCTL[3:2] | 7<br>6 | I/OD12PU | USB Power Enable<br><br>As an output, these pins enable power to downstream USB peripheral devices and have weak internal pull-up resistors. See Section 6.3, "Port Power Control" for diagram and usage instructions.<br><br>As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, the pins turn the power off. |
| VBUS_DET | 39 | I | Detect Upstream VBUS Power<br><br>Detects the state of upstream VBUS power. The Hub monitors VBUS_DET to determine when to assert the internal D+ pull-up resistor (signaling a connect event).<br><br>When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the Hub.<br><br>For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33.<br><br>VBUS is a 3.3 volt input. A resistor divider must be used if connecting to 5 volts of USB power. |
| RBIAS | 47 | I-R | USB Transceiver Bias<br><br>A 12.0 kΩ ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents. |
| XTAL1 (CLKIN) | 45 | ICLKx | 24 MHz Crystal Input or External clock Input<br><br>This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz 1.8 V clock when a crystal is not used. |
| XTAL2 | 44 | OCLKx | 24 MHz Crystal Output<br><br>This is the other terminal of the crystal, or it is left open when an external clock source is used to drive XTAL1(CLKIN). |

**Table 6.1 USB2640i/USB2641i Pin Descriptions (continued)**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| **SPI INTERFACE** | | | |
| SPI_CE_n | 8 | O12 | SPI Chip Enable<br><br>This is the active low chip enable output.<br><br>When the SPI interface is enabled, drive this pin high in power down states. |
| SPI_CLK / | 9 | I/O12 | SPI Clock<br><br>This is the SPI clock out to the serial ROM. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, drive this pin low. |
| GPIO4 / | | | This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| SCL | | | When configured, this is the $I^2C$ EEPROM clock pin. |
| SPI_DO / | 10 | I/O12 | SPI Data Out<br><br>This is the data out for the SPI port. See Section 6.4, "ROM BOOT Sequence" for diagram and usage instructions. |
| GPIO5 / | | | This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| SDA / | | | This pin is the data pin when the device is connected to the optional $I^2C$ EEPROM. |
| SPI_SPD_SEL | | | This pin is used to select the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled.<br><br>‘0’ = 30 MHz (No external resistor should be applied)<br>‘1’ = 60 MHz (A 10 K external pull-up resistor must be applied)<br><br>If the latched value is '1', then the pin is tri-stated when the chip is in the suspend state.<br><br>If the latched value is '0', then the pin is driven low during a suspend state. |
| SPI_DI | 11 | I/O12PD | SPI Data In<br><br>This is the data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating. |
| **MISC** | | | |
| GPIO1 / | 37 | I/O12 | This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| LED / | | | GPIO1 can be used as an LED output. |
| TXD | | | The signal can be used as input to the TxD of UART in the device. Custom firmware is required to activate this function. |

**Table 6.1 USB2640i/USB2641i Pin Descriptions (continued)**

| SYMBOL | 48-PIN QFN | BUFFER TYPE (Table 6.2) | DESCRIPTION |
|---|---|---|---|
| GPIO2 / | 36 | I/O12 | This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this function. |
| RXD | | | This signal can used as input to the RXD of the internal UART. Custom firmware is required to activate this function. |
| GPIO10 (CRD_PWR) | 35 | I/O200 | Card power drive: 3.3 V (100 mA or 200 mA)<br><br>This pin powers the multiplexed flash media interface (slot) for xD, MS, and SD/MMC. If card power is not being used to power the multiplexed flash media interface, this pin may be used as a GPIO.<br><br>It is a requirement for this to be the only FET used to power xD-Picture Card devices. Failure to do this will violate xD voltage specification on xD-Picture Card device pins.<br><br>Bits 0, 1, 2, and 3 control FET 2 of Register A5h. Please reference Section 7.3.4.5, "A8h: LED Blink Interval (1 byte)," on page 38. |
| nRESET | 38 | IS | RESET Input<br><br>The system uses this active low signal to reset the chip. The active low pulse should be at least 1 µs wide. |
| TEST | 40 | I | TEST Input<br><br>Tie this pin to ground for normal operation. |
| NC | 22<br>26<br>27<br>28 | | No Connects<br><br>No connect pins only apply to the USB2641i. No trace or signal should be routed or attached to these pins. |
| **DIGITAL / POWER / GROUND** | | | |
| CRFILT | 15 | | VDD Core Regulator Filter Capacitor<br><br>This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS. |
| VDD33 | 5<br>12<br>16<br>25<br>34<br>41<br>48 | | 3.3 V Power and Voltage Regulator Inputs<br><br>Please refer to Chapter 10, "DC Parameters," on page 58 for more information.<br><br>Pins 16 and 48 each require an external bypass capacitor of 4.7 µF minimum. |
| PLLFILT | 46 | | PLL Regulator Filter Capacitor<br><br>This pin must have a 1.0 µF (or greater) ±20% (ESR <0.1 Ω) capacitor to VSS. |
| VSS | ePad | | The ground pad / ePad is the only VSS for the device and must be tied to ground with multiple vias. |

## 6.2 Buffer Type Descriptions

**Table 6.2 USB2640i/USB2641i Buffer Type Descriptions**

| BUFFER | DESCRIPTION |
|---|---|
| I | Input. |
| IPU | Input, weak internal pull-up. |
| IS | Input with Schmitt trigger. |
| I/O12 | Input/output buffer with 12 mA sink and 12 mA source. |
| I/O200 | Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled. |
| I/O12PD | Input/output buffer with 12 mA sink and 12 mA source, with an internal weak pull-down resistor. |
| I/O12PU | Open drain, 12 mA sink with pull-up. Input with Schmitt trigger. |
| I/OD12PU | Input/open drain output buffer with a 12 mA sink. |
| O12 | Output buffer with a 12 mA sink and a 12 mA source. |
| O12PD | Output buffer with 12 mA sink and 12 mA source, with a pull-down resistor. |
| O12PU | Output buffer with 12 mA sink and 12 mA source, with a pull-up resistor. |
| ICLKx | XTAL clock input. |
| OCLKx | XTAL clock output. |
| I/O-U | Analog input/output as defined in the USB 2.0 Specification. |
| I-R | RBIAS. |

## 6.3 Port Power Control

### Port Power Control Using USB Power Switch

The USB2640i/USB2641i has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The internal over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

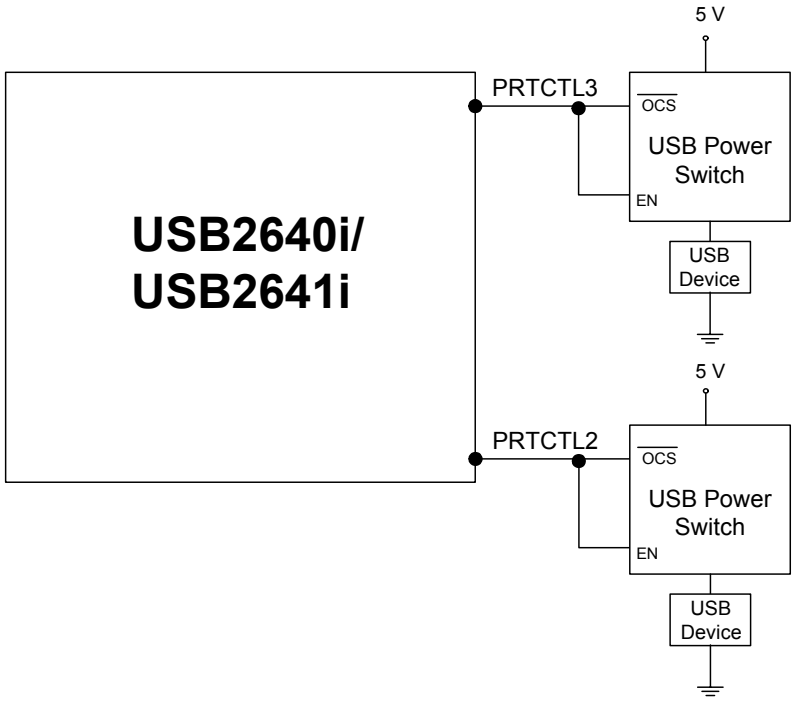



**Figure 6.1 Port Power Control with USB Power Switch**

### Port Power Control Using a Poly Fuse

When using the USB2640i/USB2641i with a poly fuse, an external diode must be used (See Figure 6.2). When disabling port power, the USB2640i/USB2641i will drive a '0'. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB2640i/USB2641i output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. The open drain output condition means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open causing the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volt, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

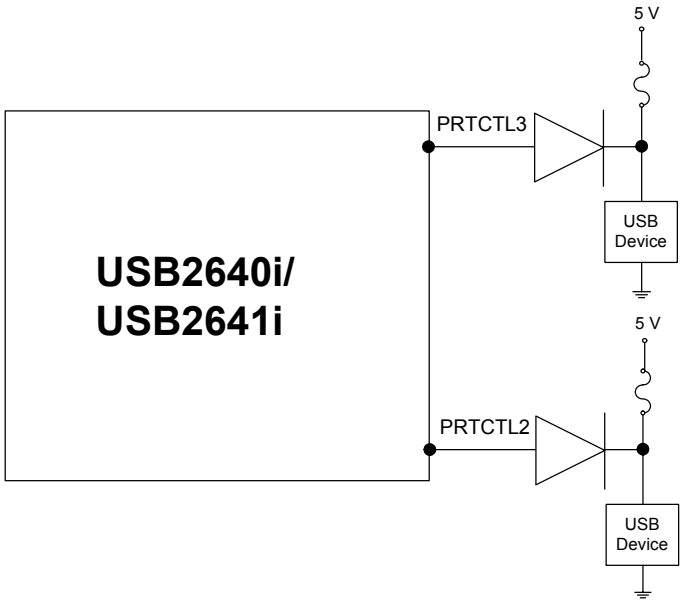



**Figure 6.2 Port Power control with Poly Fuse**

When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

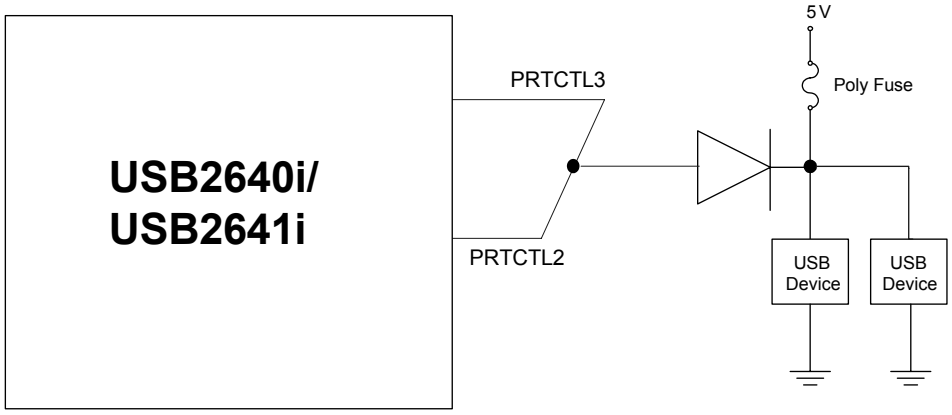



**Figure 6.3 Port Power with Ganged Control with Poly Fuse**

## 6.4 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of "2DFU" (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an $I^2C$ ROM. The firmware looks for the signature 'ATA2' at the offset of 0xFC-0xFF in the $I^2C$ ROM. The firmware reads in the $I^2C$ ROM to configure the hardware and software internally. Please refer to section 7.3.2 EEPROM Data Descriptor on page 29 for the details of the configuration options.

The SPI ROM required for the USB2640i/USB2641i must be 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the SPI_SPD_SEL. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor. SPI_SPD_SEL: This pin is used to choose the speed of the SPI interface. During nRESET assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When nRESET is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled.

The firmware can determine the speed of operation on the SPI port by checking the SPI_SPEED in the SPI_CTL register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

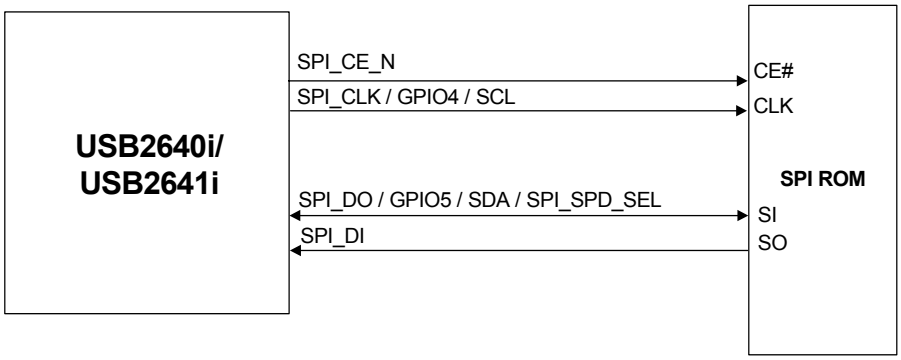



**Figure 6.4 USB2640i/USB2641i SPI ROM Connection**

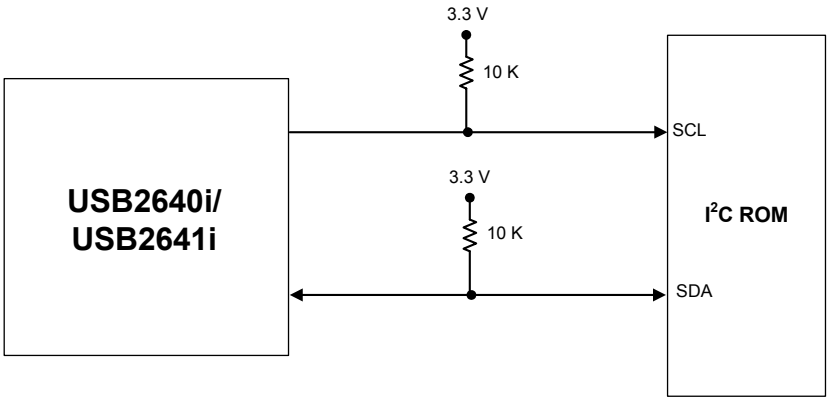



**Figure 6.5 USB2640i/USB2641i $I^2C$ Connection**

# Chapter 7 Configuration Options

## 7.1 Hub

SMSC's USB 2.0 hub is fully compliant to the Universal Serial Bus Specification available from the USB Implementer's Forum found at http://www.usb.org (Revision 2.0 April 27, 2000 and the 12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides 1 transaction translator (TT) that is shared by both downstream ports (defined as a single-TT configuration). The TT contains 4 non-periodic buffers.

### 7.1.1 Hub Configuration Options

The SMSC hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub:

- via the internal default settings or
- by settings stored in an external EEPROM or SPI Flash device.

#### 7.1.1.1 Power Switching Polarity

The hub only supports active high port power controllers.

### 7.1.2 VBus Detect

According to Section 7.2.1 of the USB 2.0 Specification, a downstream port cannot provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The VBUS_DET pin on the hub monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

## 7.2 Card Reader

The SMSC USB2640i/USB2641i is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0 / MultiMediaCard 4.2
  -SD 2.0, HS-SD, HC-SD
  -TransFlash™ and reduced form factor media
  -1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  -Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro
- Memory Stick Duo 1.10
- xD-Picture Card 1.2 compliant

## 7.3 System Configurations

### 7.3.1 EEPROM/SPI Interface

The USB2640i/USB2641i can be configured via a 2-wire ($I^2C$) EEPROM (256x8 or a recommended 512x8 for internal ROM support) or an external SPI ROM flash device containing the firmware for the USB2640i/USB2641i. If an external configuration device does not exist, the internal default values will be used. If one of the external devices is used for configuration, the OEM can update the values through the USB interface. The hub will then “attach” to the upstream USB host.

When using an external SPI Flash, the register addresses in the following three tables (Table 7.1, Table 7.2, ) refer to offsets from the starting location ‘FE80h’.

The USBDM tool set is available in the USB264x Hub Card reader combo software release package. To download the software package from SMSC’s website, please visit:

https://www2.smsc.com/mkt/CW_SFT_PUB.nsf/Agreements/OBJ+Hub+Card+Reader

to go to the OBJ Hub Card Reader Software Download Agreement. Review the license, and if you agree, check the “I agree” box and then select “Confirm”. You will then be able to download the USB264x Hub Card reader combo release package zip file containing the USBDM tool set.

Please note that the following applies to the system values and descriptions when used:

- N/A = Not applicable to this part
- Reserved = For internal use

### 7.3.2 EEPROM Data Descriptor

**Table 7.1 Internal Flash Media Controller Configurations**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| 00h | USB_SER_LEN | USB Serial String Descriptor Length | 1Ah |
| 01h | USB_SER_TYP | USB Serial String Descriptor Type | 03h |
| 02h-19h | USB_SER_NUM | USB Serial Number | "000000264001" (See Note 7.1) |
| 1Ah-1Bh | USB_VID | USB Vendor Identifier | 0424 |
| 1Ch-1Dh | USB_PID | USB Product Identifier | 4050 |
| 1Eh | USB_LANG_LEN | USB Language String Descriptor Length | 04h |
| 1Fh | USB_LANG_TYP | USB Language String Descriptor Type | 03h |
| 20h | USB_LANG_ID_LSB | USB Language Identifier Least Significant Byte | 09h (See Note 7.3) |
| 21h | USB_LANG_ID_MSB | USB Language Identifier Most Significant Byte | 04h (See Note 7.3) |
| 22h | USB_MFR_STR_LEN | USB Manufacturer String Descriptor Length | 10h |
| 23h | USB_MFR_STR_TYP | USB Manufacturer String Descriptor Type | 03h |
| 24h-31h | USB_MFR_STR | USB Manufacturer String | “Generic” (See Note 7.1) |

**Table 7.1 Internal Flash Media Controller Configurations (continued)**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| 32h-5Dh | Reserved | - | 00h |
| 5Eh | USB_PRD_STR_LEN | USB Product String Descriptor Length | 30h |
| 5Fh | USB_PRD_STR_TYP | USB Product String Descriptor Type | 03h |
| 60h-99h | USB_PRD_STR | USB Product String | "Ultra Fast Media Reader" (See Note 7.1) |
| 9Ah | USB_BM_ATT | USB BmAttribute | 80h |
| 9Bh | USB_MAX_PWR | USB Max Power | 30h (96 mA) |
| 9Ch | ATT_LB | Attribute Lo byte | 40h (Reverse SD_WP only) |
| 9Dh | ATT_HLB | Attribute Hi Lo byte | 00h |
| 9Eh | ATT_LHB | Attribute Lo Hi byte | 00h |
| 9Fh | ATT_HB | Attribute Hi byte | 00h |
| A0h | MS_PWR_LB | Memory Stick Device Power Lo byte | 08h |
| A1h | MS_PWR_HB | Memory Stick Device Power Hi byte | 00h |
| A2h | Not Applicable | - | 80h |
| A3h | Not Applicable | - | 00h |
| A4h | SM_PWR_LB | Smart Media Device Power Lo byte | 00h (See Note 7.2) |
| A5h | SM_PWR_HB | Smart Media Device Power Hi byte | 08h (See Note 7.2) |
| A6h | SD_PWR_LB | Secure Digital Device Power Lo byte | 00h |
| A7h | SD_PWR_HB | Secure Digital Device Power Hi byte | 80h |
| A8h | LED_BLK_INT | LED Blink Interval | 02h |
| A9h | LED_BLK_DUR | LED Blink After Access | 28h |
| AAh - B0h | DEV0_ID_STR | Device 0 Identifier String | “COMBO” |
| B1h - B7h | DEV1_ID_STR | Device 1 Identifier String | N/A |
| B8h - BEh | DEV2_ID_STR | Device 2 Identifier String | N/A |
| BFh - C5h | DEV3_ID_STR | Device 3 Identifier String | N/A |
| C6h - CDh | INQ_VEN_STR | Inquiry Vendor String | “Generic” |
| CEh - D2h | INQ_PRD_STR | Inquiry Product String | 2640 |
| D3h | DYN_NUM_LUN | Dynamic Number of LUNs | FFh |
| D4h - D7h | LUN_DEV_MAP | Device to LUN Mapping | FFh, FFh, FFh, FFh |

**Table 7.1 Internal Flash Media Controller Configurations (continued)**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| D8h - DAh | Reserved | - | 00h, 04h, 09h |
| DBh - DDh | Reserved | - | 5Ch, 59h, 9Ah |

**Table 7.2 Hub Controller Configurations**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| DEh | VID_LSB | Vendor ID Least Significant Byte | 24h |
| DFh | VID_MSB | Vendor ID Most Significant Byte | 04h |
| E0h | PID_LSB | Product ID Least Significant Byte | 40h |
| E1h | PID_MSB | Product ID Most Significant Byte | 26h |
| E2h | DID_LSB | Device ID Least Significant Byte | 00h |
| E3h | DID_MSB | Device ID Most Significant Byte | 00h |
| E4h | CFG_DAT_BYT1 | Configuration Data Byte 1 | 8Bh |
| E5h | CFG_DAT_BYT2 | Configuration Data Byte 2 | 28h |
| E6h | CFG_DAT_BYT3 | Configuration Data Byte 3 | 00h |
| E7h | NR_DEVICE | Non-Removable Devices | 02h |
| E8h | PORT_DIS_SP | Port Disable (Self) | 00h |
| E9h | PORT_DIS_BP | Port Disable (Bus) | 00h |
| EAh | MAX_PWR_SP | Max Power (Self) | 01h |
| EBh | MAX_PWR_BP | Max Power (Bus) | 32h |
| ECh | HC_MAX_C_SP | Hub Controller Max Current (Self) | 01h |
| EDh | HC_MAX_C_BP | Hub Controller Max Current (Bus) | 32h |
| EEh | PWR_ON_TIME | Power-on Time | 32h |
| EFh | BOOST_UP | Boost_Up | 00h |
| F0h | BOOST_3:0 | Boost_3:0 | 00h |
| F1h | PRT_SWP | Port Swap | 00h |
| F2h | PRTM12 | Port Map 12 | 00h |
| F3h | PRTM3 | Port Map 3 | 00h |

**Table 7.3 Other Internal Configurations**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| F4h | Reserved | - | 00h |
| F5h | Reserved | - | 66h |
| F6-FBh | Reserved | - | 00h |

**Table 7.3 Other Internal Configurations**

| ADDRESS | REGISTER NAME | DESCRIPTION | DEFAULT VALUE |
|---|---|---|---|
| FCh-FFh | NVSTORE_SIG | Non-volatile storage signature (“ATA2”) | “ATA2” |

**Note 7.1** This value is a UNICODE UTF-16LE encoded string value that meets the USB 2.0 Specification (Revision 2.0, 2000). Values in double quotations without this note are ASCII values.

**Note 7.2** A value of “SM” will be overridden with “xD” once an xD-Picture Card has been identified.

**Note 7.3** For a list of the most current 16-bit language ID’s defined by the USB-IF, please visit http://www.unicode.org or consult *The Unicode Standard, Worldwide Character Encoding,* (Version 4.0), The Unicode Consortium, Addison-Wesley Publishing Company, Reading, Massachusetts.

## 7.3.3 EEPROM Data Descriptor Register Descriptions

### 7.3.3.1 00h: USB Serial String Descriptor Length

\

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 0 | USB_SER_LEN | USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes). |

### 7.3.3.2 01h: USB Serial String Descriptor Type

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1 | USB_SER_TYP | USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type. |

### 7.3.3.3 02h-19h: USB Serial Number Option

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 25:2 | USB_SER_NUM | Maximum string length is 12 hex digits. Must be unique to each device. |

### 7.3.3.4 1Ah-1Bh: USB Vendor Identifier Option

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1:0 | USB_VID | This ID is unique for every vendor. The vendor ID is assigned by the USB Implementer’s Forum. |

### 7.3.3.5 1Ch-1Dh: USB Product Identifier Option

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1:0 | USB_PID | This ID is unique for every product. The product ID is assigned by the vendor. |

#### 7.3.3.6 1Eh: USB Language String Descriptor Length

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 0 | USB_LANG_LEN | USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes). |

#### 7.3.3.7 1Fh: USB Language String Descriptor Type

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1 | USB_LANG_TYP | USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type. |

#### 7.3.3.8 20h: USB Language Identifier Least Significant Byte

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 2 | USB_LANG_ID _LSB | English Language Code = ‘0409’. See Note 7.3 to reference additional language ID’s defined by the USB-IF. |

#### 7.3.3.9 21h: USB Language Identifier Most Significant Byte

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 3 | USB_LANG_ID _MSB | English Language Code = ‘0409’. See Note 7.3 to reference additional language ID’s defined by the USB-IF. |

#### 7.3.3.10 22h: USB Manufacturer String Descriptor Length

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 0 | USB_MFR_STR _LEN | USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes). |

#### 7.3.3.11 23h: USB Manufacturer String Descriptor Type

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1 | USB_MFR_STR _TYP | USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type. |

#### 7.3.3.12 24h-31h: USB Manufacturer String

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 15:2 | USB_MFR_STR | Maximum string length is 28 characters. (See Note 7.4) |

#### 7.3.3.13 32h-5Dh: Reserved

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 59:16 | Reserved | Reserved. |

#### 7.3.3.14 5Eh: USB Product String Descriptor Length

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 0 | USB_PRD_STR | USB serial string descriptor length as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bLength” which describes the size of the string descriptor (in bytes). |

#### 7.3.3.15 5Fh: USB Product String Descriptor Type

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1 | USB_PRD_STR | USB serial string descriptor type as defined by Section 9.6.7 “String” of the USB 2.0 Specification (Revision 2.0, 2000). This field is the “bDescriptorType” which is a constant value associated with a string descriptor type. |

#### 7.3.3.16 60h-99h: USB Product String

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 59:2 | USB_PRD_STR | This string will be used during the USB enumeration process in the Windows operating system. Maximum string length is 28 characters. (See Note 7.4) |

**Note 7.4** While the full strings are reported during USB enumeration, Windows XP/Vista reads concatenated version of the strings from the standard SCSI inquiry response when storing the values for display in the Windows registry and device manager.

#### 7.3.3.17 9Ah: USB BmAttribute (1 byte)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | USB_BM_ATT | Self- or Bus-Power: Selects between self- and bus-powered operation.<br><br>The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).<br><br>When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a Compound Device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 Specification is not violated.<br><br>When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current.<br><br>**80 = Bus-powered operation (default)**<br>C0 = Self-powered operation<br>A0 = Bus-powered operation with remote wake-up<br>E0 = Self-powered operation with remote wake-up |

#### 7.3.3.18 9Bh: USB MaxPower (1 byte)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | USB_MAX_PWR | USB Max Power per the USB 2.0 Specification. Do NOT set this value greater than 100 mA. |

#### 7.3.3.19 9Ch-9Fh: Attribute Byte Descriptions

| BYTE | BYTE NAME | BIT | DESCRIPTION |
|---|---|---|---|
| 0 | ATT_LB | 3:0 | Always reads ‘0’. |
| | | 4 | Inquire Manufacturer and Product ID Strings<br><br>‘1’ - Use the Inquiry Manufacturer and Product ID Strings.<br><br>‘0’ (default) - Use the USB Descriptor Manufacturer and Product ID Strings. |
| | | 5 | Always reads ‘0’. |
| | | 6 | Reverse SD Card Write Protect Sense<br><br>‘1’ (default) - SD cards will be write protected when SW_nWP is high, and writable when SW_nWP is low.<br><br>‘0’ - SD cards will be write protected when SW_nWP is low, and writable when SW_nWP is high. |
| | | 7 | Reserved |

| BYTE | BYTE NAME | BIT | DESCRIPTION |
|---|---|---|---|
| 1 | ATT_HLB | 3:0 | Always reads ‘0’. |
| | | 4 | Activity LED True polarity<br>‘1’ - Activity LED to Low True.<br>‘0’ (default) - Activity LED polarity to High True. |
| | | 5 | Common Media Insert / Media Activity LED<br>‘1’ - The activity LED will function as a common media inserted/media access LED.<br>‘0’ (default) - The activity LED will remain in its idle state until media is accessed. |
| | | 7:6 | Always reads ‘0’. |
| 2 | ATT_LHB | 0 | Attach on Card Insert / Detach on Card Removal<br>‘1’ - Attach on Insert is enabled.<br>‘0’ (default) - Attach on Insert is disabled. |
| | | 1 | Always reads ‘0’. |
| | | 2 | Enable Device Power Configuration<br>‘1’ - Custom Device Power Configuration stored in the NVSTORE is used.<br>‘0’ (default) - Default Device Power Configuration is used. |
| | | 7:3 | Always reads ‘0’. |
| 3 | ATT_HB | 6:0 | Always reads ‘0’. |
| | | 7 | xD Player Mode |

### 7.3.4 A0h-A7h: Device Power Configuration

The USB4640/USB4640i has one internal FET which can be utilized for card power. This section describes the internal default configuration. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit can be set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its device power configuration. Bit 3 selects between internal or external card power FET options. For internal FET card power control, bits 0 through 2 are used to set the power limit. The “Device Power Configuration” bits are ignored unless the “Enable Device Power Configuration” bit is set. See Section 7.3.3.19, "9Ch-9Fh: Attribute Byte Descriptions," on page 35.

#### 7.3.4.1 A0h-A1h: Memory Stick Device Power

| FET | TYPE | BITS | BIT TYPE | DESCRIPTION |
|---|---|---|---|---|
| 0 | FET Lo Byte MS_PWR_LB | 3:0 | Low Nibble | 0000b Disabled |
| 1 | | 7:4 | High Nibble | |
| **2** | **FET Hi Byte** MS_PWR_HB | **3:0** | **Low Nibble** | 0000b Disabled<br>0001b External FET enabled<br>1000b Internal FET with 100 mA power limit<br>**1010b Internal FET with 200 mA power limit** |
| 3 | | 7:4 | High Nibble | 0000b Disabled |

#### 7.3.4.2 A2h-A3h: Not Applicable

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1:0 | Not Applicable | Not applicable to USB2640i/USB2641i. |

#### 7.3.4.3 A4h-A5h: Smart Media Device Power

| FET | TYPE | BITS | BIT TYPE | DESCRIPTION |
|---|---|---|---|---|
| 0 | FET Lo Byte SM_PWR_LB | 3:0 | Low Nibble | 0000b Disabled |
| 1 | | 7:4 | High Nibble | |
| **2** | **FET Hi Byte** SM_PWR_HB | **3:0** | **Low Nibble** | 0000b Disabled<br>0001b External FET enabled<br>1000b Internal FET with 100 mA power limit<br>**1010b Internal FET with 200 mA power limit** |
| 3 | | 7:4 | High Nibble | 0000b Disabled |

#### 7.3.4.4 A6h-A7h: Secure Digital/MultiMediaCard Device Power

| FET | TYPE | BITS | BIT TYPE | DESCRIPTION |
|---|---|---|---|---|
| 0 | FET Lo Byte SD_PWR_LB | 3:0 | Low Nibble | 0000b Disabled |
| 1 | | 7:4 | High Nibble | |
| **2** | **FET Hi Byte** SD_PWR_HB | **3:0** | **Low Nibble** | 0000b Disabled<br>0001b External FET enabled<br>1000b Internal FET with 100 mA power limit<br>**1010b Internal FET with 200 mA power limit** |
| 3 | | 7:4 | High Nibble | 0000b Disabled |

#### 7.3.4.5 A8h: LED Blink Interval (1 byte)

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 0 | LED_BLK_INT | The blink rate is programmable in 50 ms intervals. Bit 7 indicates an idle state:<br><br>‘0’ - Off<br>’1’ - On<br><br>Bits 0-6 are used to determine the blink interval up to a max of 128 x 50 ms. |

#### 7.3.4.6 A9h: LED Blink Duration (1 byte)

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 1 | LED_BLK_DUR | LED blink After Access. This byte is used to designate the number of seconds that the GPIO 1 LED will continue to blink after a drive access. Setting this byte to "05" will cause the GPIO 1 LED to blink for 5 seconds after a drive access. |

#### 7.3.4.7 AAh-B0h: Device 0 Identifier String

| BYTE | NAME | STRING | DESCRIPTION |
|---|---|---|---|
| 6:0 | DEV0_ID_STR | “COMBO” | MS, SM, and SD/MMC are mapped to device 0 identifier string because USB2640i/USB2641i only supports one LUN. When applicable, the "SM" value will be overridden with xD once an xD-Picture Card has been identified. |

#### 7.3.4.8 B1h-C5h: Not Applicable

| BYTE | NAME | DESCRIPTION |
|---|---|---|
| 20:0 | Not Applicable | Not applicable to USB2640i/USB2641i. |

#### 7.3.4.9 C6h-CDh: Inquiry Vendor String

| BYTE | NAME | STRING | DESCRIPTION |
|---|---|---|---|
| 7:0 | INQ_VEN_STR | “Generic” | If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB Descriptor Manufacturer and Product ID Strings. |

#### 7.3.4.10 CEh-D2h: Inquiry Product String

| BYTE | NAME | UINT | DESCRIPTION |
|---|---|---|---|
| 4:0 | INQ_PRD_STR | 2640 | If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB Descriptor Manufacturer and Product ID Strings. |

#### 7.3.4.11 D3h: Dynamic Number of LUNs

| BIT | BYTE NAME | UCHAR | DESCRIPTION |
|---|---|---|---|
| 7:0 | DYN_NUM_LUN | FFh | These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces.<br><br>USB2640i/USB2641i supports one LUN. MS, SM, and SD/MMC are mapped to that LUN.<br><br>If this field is set to "FF", the program assumes that you are using the default value of "04" and will display icons for xD, MS, and SD/MMC. If this field is any other value besides "FF", you must specify the LUN# assignments in the boxes starting with LUN 00 and going to (# of Icons to Display -1).<br><br>These bytes are reserved for internal use only. |

#### 7.3.4.12 D4h-D7h: Device to LUN Mapping

| BYTE | NAME | UCHARS | DESCRIPTION |
|---|---|---|---|
| 3:0 | DEV_LUN_MAP | FFh, FFh, FFh, FFh | These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces.<br><br>USB2640i/USB2641i supports one LUN. MS, SM, and SD/MMC are mapped to that LUN.<br><br>If this field is set to "FF", the program assumes that you are using the default value of "04" and will display icons for xD, MS, and SD/MMC. If this field is any other value besides "FF", you must specify the LUN# assignments in the boxes starting with LUN 00 and going to (# of Icons to Display -1).<br><br>These bytes are reserved for internal use only. |

#### 7.3.4.13 D8h-DDh: Reserved

| BYTE | BYTE NAME | DESCRIPTION |
|---|---|---|
| 5:0 | Reserved | For internal use only. |

## 7.3.5 Hub Controller Configurations

### 7.3.5.1 DEh: Vendor ID (LSB)

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | VID_LSB | Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Implementer's Forum). |

### 7.3.5.2 DFh: Vendor ID (MSB)

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | VID_MSB | Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the Vendor of the user device (assigned by USB Implementer's Forum). |

### 7.3.5.3 E0h: Product ID (LSB)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PID_LSB | Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product. |

### 7.3.5.4 E1h: Product ID (MSB)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PID_MSB | Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product. |

### 7.3.5.5 E2h: Device ID (LSB)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | DID_LSB | Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD (binary coded decimal) format. |

### 7.3.5.6 E3h: Device ID (MSB)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:0 | DID_MSB | Most Significant Byte of the Device ID. This is a 16-bit device release number in binary coded decimal (BCD) format. |

### 7.3.5.7 E4h: Configuration Data Byte 1 (CFG_DAT_BYT1)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7 | SELF_BUS_PWR | Self- or Bus-Power: Selects between self- and bus-powered operation.<br><br>The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller).<br><br>When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a Compound Device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 Specification is not violated.<br><br>When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current.<br><br>‘0’ = Bus-powered operation<br>‘1’ = Self-powered operation |
| 6 | Reserved | Always reads ‘0’. |
| 5 | HS_DISABLE | Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-Speed device, and forces attachment as Full-Speed only (i.e. no Hi-Speed support).<br><br>‘0’ = Hi-/Full-Speed<br>‘1’ = Full-Speed-Only (Hi-Speed disabled!) |
| 4 | Reserved | Always reads ‘0’. |
| 3 | EOP_DISABLE | EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the USB 2.0 Specification for additional details. Note: generation of an EOP at the EOF1 point may prevent a Host Controller (operating in FS mode) from placing the USB bus in suspend.<br><br>‘0’ = An EOP is generated at the EOF1 point if no traffic is detected.<br>‘1’ = EOP generation at EOF1 is disabled (Note: This is normal USB operation).<br><br>**Note:** This is a rarely used feature in the PC environment, existing drivers may not have been thoroughly debugged with this feature enabled. It is included because it is a permitted feature in Chapter 11 of the USB 2.0 Specification. |
| 2:1 | CURRENT_SNS | Over-Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is dependent upon the hardware implementation.<br><br>‘00’ = Ganged sensing (all ports together)<br>‘01’ = Individual port-by-port<br>‘1x’ = Over-current sensing not supported (must only be used with bus-powered configurations!) |
| 0 | PORT_PWR | Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port- by-port basis (individual). The ability to support power enabling on a port or ganged basis is dependent upon the hardware implementation.<br><br>‘0’ = Ganged switching (all ports together)<br>‘1’ = Individual port-by-port switching |

#### 7.3.5.8 E5h: Configuration Data Byte 2 (CFG_DAT_BYT2)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:6 | Reserved | Always reads ‘0’. |
| 5:4 | OC_TIMER | OverCurrent Timer: Over-current Timer delay.<br><br>00 = 50 ns<br>01 = 100 ns<br>10 = 200 ns<br>11 = 400 ns |
| 3 | COMPOUND | Compound Device: Allows OEM to indicate that the hub is part of a compound (see the USB 2.0 Specification for definition) device. The applicable port(s) must also be defined as having a "non-removable device".<br><br>When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a Compound Device.<br><br>‘0’ = No<br>‘1’ = Yes, the hub is part of a Compound Device |
| 2:0 | Always reads ‘0’. | Always reads ‘0’. |

#### 7.3.5.9 E6h: Configuration Data Byte 3 (CFG_DAT_BYT3)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:4 | Reserved | Always reads ‘0’. |
| 3 | PRTMAP_EN | Port mapping enable: Selects the method used by the hub to assign port numbers and disable ports.<br><br>‘0’ = Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as Port ‘n’ on the hub is reported as Port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host.<br><br>Register 300Ah: Port Disable For Self-Powered Operation (Reset = 0x00).<br>Register 300Bh: Port Disable For Bus-Powered Operation (Reset = 0x00).<br><br>‘1’ = Port map mode. The mode enables remapping via the registers defined below.<br><br>Register 30FBh: Port Map 12 (Reset = 0x00)<br>Register 30FCh: Port Map 3 (Reset = 0x00) |
| 2:0 | Reserved | Always reads ‘0’. |

#### 7.3.5.10 E7h: Non-Removable Device

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | NR_DEVICE | Indicates which port(s) include non-removable devices.<br><br>'0' = Port is removable<br>'1' = Port is non-removable<br><br>Informs the host if one of the active ports has a permanent device that is undetachable from the hub. (Note: The device must provide its own descriptor data.)<br><br>When using the internal default option, the NON_REM[1:0] pins will designate the appropriate ports as being non-removable.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved<br>Bit 3= Controls physical port 3<br>Bit 2= Controls physical port 2<br>Bit 1= Controls physical port 1<br>Bit 0= Reserved, always = '0'<br><br>**Note:** Bit 1 must be set to a '1' by the firmware for proper identification of the card reader as a non-removable device. |

#### 7.3.5.11 E8h: Port Disable For Self-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_SP | Disables 1 or more ports.<br><br>'0' = Port is available<br>'1' = Port is disabled<br><br>During self-powered operation this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a Host Controller. The ports can be disabled in any order since the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved<br>Bit 3= Controls physical port 3<br>Bit 2= Controls physical port 2<br>Bit 1= Controls physical port 1<br>Bit 0= Reserved, always = '0' |

#### 7.3.5.12 E9h: Port Disable For Bus-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PORT_DIS_BP | Disables 1 or more ports.<br><br>'0' = Port is available<br>'1' = Port is disabled<br><br>During self-powered operation, this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a Host Controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function.<br><br>When using the internal default option, the PRT_DIS[1:0] pins will disable the appropriate ports.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved<br>Bit 3= Controls physical port 3<br>Bit 2= Controls physical port 2<br>Bit 1= Controls physical port 1<br>Bit 0 is Reserved, always = '0' |

#### 7.3.5.13 EAh: Max Power For Self-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | MAX_PWR_SP | Max Power Self_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a Compound Device, and the embedded peripheral reports 0 mA in its descriptors.<br><br>**Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA. |

#### 7.3.5.14 EBh: Max Power For Bus-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | MAX_PWR_BP | Max Power Bus_Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a Compound Device, and the embedded peripheral reports 0 mA in its descriptors. |

#### 7.3.5.15 ECh: Hub Controller Max Current For Self-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_SP | Hub Controller Max Current Self-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a Compound Device.<br>**Note:** The USB 2.0 Specification does not permit this value to exceed 100 mA.<br><br>A value of 50 (decimal) indicates 100 mA, which is the default value. |

#### 7.3.5.16 EDh: Hub Controller Max Current For Bus-Powered Operation

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | HC_MAX_C_BP | Hub Controller Max Current Bus-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a Compound Device.<br><br>A value of 50 (decimal) would indicate 100 mA, which is the default value. |

#### 7.3.5.17 EEh: Power-On Time

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PWR_ON_TIME | Power-On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is adequate on that port. System software uses this value to determine how long to wait before accessing a powered-on port. |

#### 7.3.5.18 EFh: Boost_Up

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:2 | Reserved | Reserved |
| 1:0 | BOOST_IOUT | USB electrical signaling drive strength Boost Bit for the Upstream Port ‘A’.<br><br>‘00’ = Normal electrical drive strength = No boost<br>‘01’ = Elevated electrical drive strength = Low (approximately 4% boost)<br>‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost)<br>‘11’ = Elevated electrical drive strength = High (approximately 12% boost)<br><br>**Note:** “Boost” could result in non-USB Compliant parameters. OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels. |

#### 7.3.5.19 F0h: Boost_3:0

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7:6 | Reserved | Always reads ‘0’. |
| 5:4 | BOOST_IOUT_3 | Upstream USB electrical signaling drive strength Boost Bit for Downstream Port ‘3’.<br><br>‘00’ = Normal electrical drive strength = No boost<br>‘01’ = Elevated electrical drive strength = Low (approximately 4% boost)<br>‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost)<br>‘11’ = Elevated electrical drive strength = High (approximately 12% boost) |
| 3:2 | BOOST_IOUT_2 | Upstream USB electrical signaling drive strength Boost Bit for Downstream Port ‘2’.<br><br>‘00’ = Normal electrical drive strength = No boost<br>‘01’ = Elevated electrical drive strength = Low (approximately 4% boost)<br>‘10’ = Elevated electrical drive strength = Medium (approximately 8% boost)<br>‘11’ = Elevated electrical drive strength = High (approximately 12% boost)<br><br>**Note:** “Boost” could result in non-USB Compliant parameters. OEM should use a ‘00’ value unless specific implementation issues require additional signal boosting to correct for degraded USB signalling levels. |
| 1:0 | Reserved | Always reads ‘0’. |

#### 7.3.5.20 F1h: Port Swap

| BIT | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | PRT_SWP | Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors.<br><br>‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin.<br><br>‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin.<br><br>Bit 7= Reserved<br>Bit 6= Reserved<br>Bit 5= Reserved<br>Bit 4= Reserved<br>Bit 3= Controls physical port 3<br>Bit 2= Controls physical port 2<br>Bit 1= Reserved<br>Bit 0= Controls physical port 0 |

#### 7.3.5.21 F2h: Port Map 12

<table>
<tr><th>BIT</th><th>BYTE NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTM12</td><td>Port map register for ports 1 & 2.<br><br>When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub reported having.<br><br>The host's port number is referred to as "logical port number" and the physical port on the hub is the “physical port number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).<br><br>Note: OEM must ensure that contiguous logical port numbers are used, starting from number ‘1’ up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.<br><br>Table 7.4 Port Map Register for Ports 1 & 2
<table>
<tr><td>Bit [7:4]</td><td>‘0000’</td><td>Physical Port 2 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 2 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 2 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 2 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’ to ‘1111’</td><td>Illegal; Do Not Use</td></tr>
<tr><td>Bit [3:0]</td><td>‘0000’</td><td>Physical Port 1 is Disabled</td></tr>
<tr><td></td><td>‘0001’</td><td>Physical Port 1 is mapped to Logical Port 1</td></tr>
<tr><td></td><td>‘0010’</td><td>Physical Port 1 is mapped to Logical Port 2</td></tr>
<tr><td></td><td>‘0011’</td><td>Physical Port 1 is mapped to Logical Port 3</td></tr>
<tr><td></td><td>‘0100’ to ‘1111’</td><td>Illegal; Do Not Use</td></tr>
</table>
</td></tr>
</table>

### 7.3.5.22 F3h: Port Map 3

<table>
<tr><th>BIT</th><th>BYTE NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTM3</td><td>Port map register for port 3.<br><br>When a hub is enumerated by a USB Host Controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The Host Controller will number the downstream ports of the hub starting with the number '1', up to the number of ports that the hub reported having.<br><br>The host's port number is referred to as "logical port number" and the physical port on the hub is the “physical port number". When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).<br><br>Note: OEM must ensure that contiguous logical port numbers are used, starting from number ‘1’ up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</td></tr>
</table>

**Table 7.5 Port Map Register for Port 3**

| | | |
|---|---|---|
| Bit [7:4] | ‘0000’ | Reserved |
| | ‘0001’ | Reserved |
| | ‘0010’ | Reserved |
| | ‘0011’ | Reserved |
| | ‘0100’ to ‘1111’ | Illegal; Do Not Use |
| Bit [3:0] | ‘0000’ | Physical Port 3 is Disabled |
| | ‘0001’ | Physical Port 3 is mapped to Logical Port 1 |
| | ‘0010’ | Physical Port 3 is mapped to Logical Port 2 |
| | ‘0011’ | Physical Port 3 is mapped to Logical Port 3 |
| | ‘0100’ to ‘1111’ | Illegal; Do Not Use |

### 7.3.5.23 F4h-FBh: Reserved

| BYTE | BYTE NAME | DESCRIPTION |
|---|---|---|
| 7:0 | Reserved | Reserved. |

#### 7.3.5.24 FCh-FFh: Non-volatile Storage Signature

| BYTE | BYTE NAME | STRING | DESCRIPTION |
|---|---|---|---|
| 3:0 | NVSTORE_SIG | “ATA2” | This signature is used to verify the validity of the data in the configuration area. The signature must be set to ‘ATA2’ for USB2640i/USB2641i. |

### 7.3.6 I²C EEPROM

The I²C EEPROM interface implements a subset of the I²C Master Specification (Please refer to the Philips Semiconductor Standard I²C-Bus Specification for details on I²C bus protocols). The device’s I²C EEPROM interface is designed to attach to a single “dedicated” I²C EEPROM, and it conforms to the Standard-mode I²C Specification (100 kbps transfer rate and 7-bit addressing) for protocol and electrical compatibility.

**Note:** Extensions to the I²C Specification are not supported.

The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

#### 7.3.6.1 Implementation Characteristics

The device will only access an EEPROM using the sequential read protocol.

#### 7.3.6.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the SDA/SMBDATA & SCL/SMBCLK/CFG_SEL0 lines (per SMBus 1.0 Specification, and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

### 7.3.7 In-Circuit EEPROM Programming

The EEPROM can be programmed via automatic testing test equipment (ATE) by pulling nRESET low which tri-states the device’s EEPROM interface and allows an external source to program the EEPROM.

## 7.4 Default Configuration Option:

The SMSC device can be configured via its internal default configuration. Please see Section 7.3.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 7.1 for the internal default values that are loaded when this option is selected.

## 7.5 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR reset circuit or via the nRESET pin) and the second is a USB Bus Reset.

### 7.5.1 Internal POR Hardware Reset

All reset timing parameters are guaranteed by design.

### 7.5.2 External Hardware nRESET

A valid hardware reset is defined as assertion of nRESET for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than 500 µA of current from the upstream USB power source.

Assertion of nRESET (external pin) causes the following:

1. All downstream ports are disabled, and PRTCTL power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

#### 7.5.2.1 nRESET for EEPROM Configuration

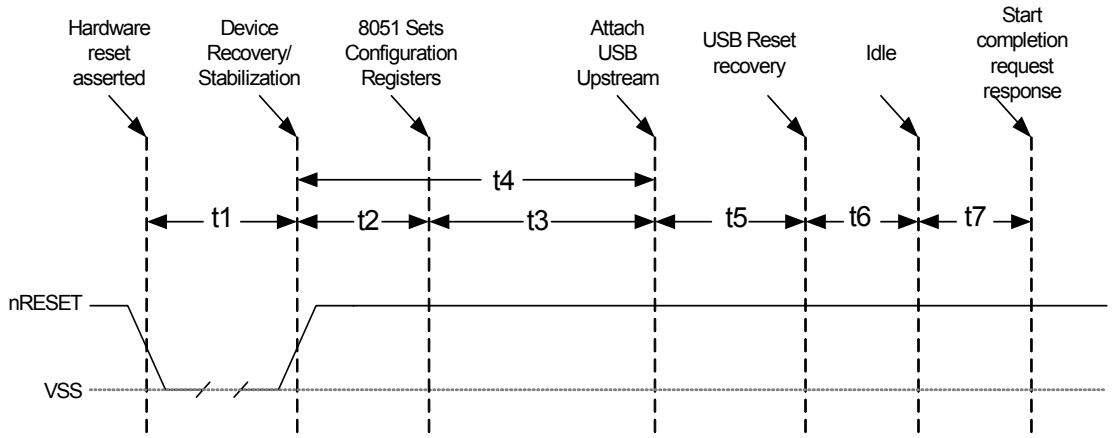



**Figure 7.1 nRESET Timing for EEPROM Mode**

**Table 7.6 nRESET Timing for EEPROM Mode**

| NAME | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| t1 | nRESET asserted. | 1 | | | µsec |
| t2 | Device recovery/stabilization. | | | 500 | µsec |
| t3 | 8051 programs device configuration | | 20 | 50 | msec |
| t4 | USB attach (See Note). | | | 100 | msec |
| t5 | Host acknowledges attach and signals USB reset. | 100 | | | msec |
| t6 | USB idle. | | Undefined | | msec |
| t7 | Completion time for requests (with or without data stage). | | | 5 | msec |

**Note:** All power supplies must have reached the operating levels mandated in Chapter 10, DC Parameters, prior to (or coincident with) the assertion of nRESET.

### 7.5.3 USB Bus Reset

In response to the upstream port signaling a reset to the device, the device does the following:

**Note:** The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to ‘0’.
2. Sets configuration to: Unconfigured.
3. Negates PRTCTL[3:2] to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the USB 2.0 Specification for behavior after completion of the reset sequence.

The host then configures the device and the device’s downstream port devices in accordance with the USB 2.0 Specification.

# Chapter 8 Pin Reset States

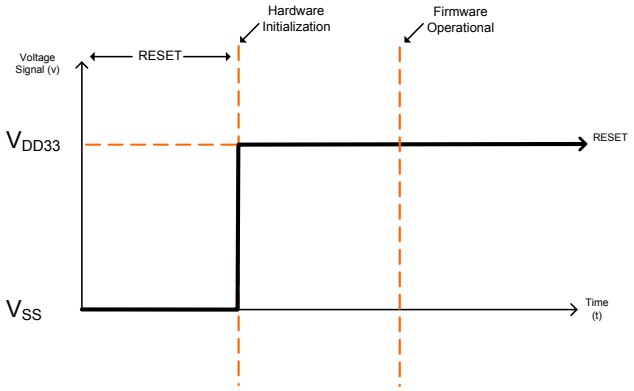



**Figure 8.1 Pin Reset States**

**Table 8.1 Legend for Pin Reset States Table**

| SYMBOL | DESCRIPTION |
|---|---|
| Y | Hardware enables function |
| 0 | Output low |
| 1 | Output high |
| -- | Hardware disables function |
| Z | Hardware disables output driver (high impedance) |
| PU | Hardware enables pull-up |
| PD | Hardware enables pull-down |
| HW | Hardware controls function, but state is protocol dependent |
| (FW) | Firmware controls function through registers |
| VDD | Hardware supplies power through pin, applicable only to CARD_PWR pin |
| none | Hardware disables pad |

## 8.1 Pin Reset States

**Table 8.2 USB2640i Pin Reset States**

| | | RESET STATE | | | |
|---|---|---|---|---|---|
| PIN | PIN NAME | FUNCTION | OUTPUT | PU/ PD | INPUT |
| 1 | USBDN_DM2 | USBDN_DM2 | 0 | PD | -- |
| 2 | USBDN_DP2 | USBDN_DP2 | 0 | PD | -- |

**Table 8.2 USB2640i Pin Reset States (continued)**

| | | RESET STATE | | | |
|---|---|---|---|---|---|
| **PIN** | **PIN NAME** | **FUNCTION** | **OUTPUT** | **PU/ PD** | **INPUT** |
| 3 | USBDN_DM3 | USBDN_DM3 | 0 | PD | -- |
| 4 | USBDN_DP3 | USBDN_DP3 | 0 | PD | -- |
| 6 | PRTCTL2 | PRTCTL | 0 | -- | -- |
| 7 | PRTCTL3 | PRTCTL | 0 | -- | -- |
| 8 | SPI_CE_n | SPI_CE_n | 1 | -- | -- |
| 9 | SPI_CLK / GPIO4 / SCL | GPIO | 0 | -- | -- |
| 10 | SPI_DO / GPIO5 / SDA / SPI_SPD_SEL | GPIO | Z | PD | Y |
| 11 | SPI_DI | SPI_DI | Z | PD | Y |
| 13 | xD_D4 / GPIO6 / SD_WP / MS_SCLK | GPIO | 0 | -- | -- |
| 14 | GPIO15 / SD_nCD | GPIO | Z | PU | Y |
| 17 | xD_D3 / SD_D1 / MS_D5 | none | Z | -- | -- |
| 18 | xD_D2 / SD_D0 / MS_D4 | none | Z | -- | -- |
| 19 | xD_D1 / SD_D7 / MS_D6 | none | Z | -- | -- |
| 20 | xD_D0 / SD_D6 / MS_D7 | none | Z | -- | -- |
| 21 | xD_nWP / SD_CLK / MS_BS | none | Z | -- | -- |
| 22 | xD_nWE | none | Z | -- | -- |
| 23 | xD_ALE / SD_D5 / MS_D1 | none | Z | -- | -- |
| 24 | xD_CLE / SD_CMD / MS_D0 | none | Z | -- | -- |
| 26 | xD_nCE | none | Z | -- | -- |
| 27 | xD_nRE | none | Z | -- | -- |
| 28 | xD_nB/R | none | Z | -- | -- |
| 29 | GPIO14 / xD_nCD | GPIO | Z | PU | Y |
| 30 | xD_D7 / SD_D4 / MS_D2 | none | Z | -- | -- |
| 31 | GPIO12 / MS_INS | GPIO | Z | PU | Y |
| 32 | xD_D6 / SD_D3 / MS_D3 | none | Z | -- | -- |
| 33 | xD_D5 / SD_D2 | none | Z | -- | -- |
| 35 | GPIO10(CARD_PWR) | GPIO | Z | -- | -- |

**Table 8.2 USB2640i Pin Reset States (continued)**

| | | RESET STATE | | | |
|---|---|---|---|---|---|
| **PIN** | **PIN NAME** | **FUNCTION** | **OUTPUT** | **PU/ PD** | **INPUT** |
| 36 | GPIO2 / RXD | GPIO | 0 | -- | -- |
| 37 | GPIO1 / LED / TXD | GPIO1 | 0 | -- | -- |
| 38 | nRESET | nRESET | Z | -- | Y |
| 39 | VBUS_DET | VBUS_DET | Z | -- | Y |
| 40 | TEST | TEST | Z | -- | Y |
| 42 | USB+ | USB+ | Z | -- | -- |
| 43 | USB- | USB- | Z | -- | -- |
| 44 | XTAL2 | | | | |
| 45 | XTAL1 (CLKIN) | | | | |
| 47 | RBIAS | | | | |

**Table 8.3 USB2641i Pin Reset States**

| | | RESET STATE | | | |
|---|---|---|---|---|---|
| **PIN** | **PIN NAME** | **FUNCTION** | **OUTPUT** | **PU/ PD** | **INPUT** |
| 1 | USBDN_DM2 | USBDN_DM2 | 0 | PD | -- |
| 2 | USBDN_DP2 | USBDN_DP2 | 0 | PD | -- |
| 3 | USBDN_DM3 | USBDN_DM3 | 0 | PD | -- |
| 4 | USBDN_DP3 | USBDN_DP3 | 0 | PD | -- |
| 6 | PRTCTL2 | PRTCTL | 0 | -- | -- |
| 7 | PRTCTL3 | PRTCTL | 0 | -- | -- |
| 8 | SPI_CE_n | SPI_CE_n | 1 | -- | -- |
| 9 | SPI_CLK / GPIO4 / SCL | GPIO | 0 | -- | -- |
| 10 | SPI_DO / GPIO5 / SDA / SPI_SPD_SEL | GPIO | Z | PD | Y |
| 11 | SPI_DI | SPI_DI | Z | PD | Y |
| 13 | GPIO6 / SD_WP / MS_SCLK | GPIO | 0 | -- | -- |
| 14 | GPIO15 / SD_nCD | GPIO | Z | PU | Y |
| 17 | SD_D1 / MS_D5 | none | Z | -- | -- |

**Table 8.3 USB2641i Pin Reset States (continued)**

| | | RESET STATE | | | |
|---|---|---|---|---|---|
| **PIN** | **PIN NAME** | **FUNCTION** | **OUTPUT** | **PU/ PD** | **INPUT** |
| 18 | SD_D0 / MS_D4 | none | Z | -- | -- |
| 19 | SD_D7 / MS_D6 | none | Z | -- | -- |
| 20 | SD_D6 / MS_D7 | none | Z | -- | -- |
| 21 | SD_CLK / MS_BS | none | Z | -- | -- |
| 23 | SD_D5 / MS_D1 | none | Z | -- | -- |
| 24 | SD_CMD / MS_D0 | none | Z | -- | -- |
| 29 | GPIO14 | GPIO | Z | PU | Y |
| 30 | SD_D4 / MS_D2 | none | Z | -- | -- |
| 31 | GPIO12 / MS_INS | GPIO | Z | PU | Y |
| 32 | SD_D3 / MS_D3 | none | Z | -- | -- |
| 33 | SD_D2 | none | Z | -- | -- |
| 35 | GPIO10(CARD_PWR) | GPIO | Z | -- | -- |
| 36 | GPIO2 / RXD | GPIO | 0 | -- | -- |
| 37 | GPIO1 / LED / TXD | GPIO1 | 0 | -- | -- |
| 38 | nRESET | nRESET | Z | -- | Y |
| 39 | VBUS_DET | VBUS_DET | Z | -- | Y |
| 40 | TEST | TEST | Z | -- | Y |
| 42 | USB+ | USB+ | Z | -- | -- |
| 43 | USB- | USB- | Z | -- | -- |
| 44 | XTAL2 | | | | |
| 45 | XTAL1 (CLKIN) | | | | |
| 47 | RBIAS | | | | |

# Chapter 9 AC Specifications

## 9.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

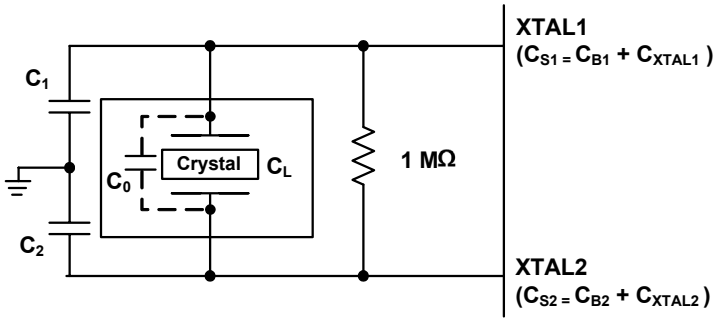



**Figure 9.1 Typical Crystal Circuit**

**Table 9.1 Crystal Circuit Legend**

| SYMBOL | DESCRIPTION | IN ACCORDANCE WITH |
|---|---|---|
| $C_0$ | Crystal shunt capacitance | Crystal manufacturer's specification (See Note 9.1) |
| $C_L$ | Crystal load capacitance | |
| $C_B$ | Total board or trace capacitance | OEM board design |
| $C_S$ | Stray capacitance | SMSC IC and OEM board design |
| $C_{XTAL}$ | XTAL pin input capacitance | SMSC IC |
| $C_1$ | Load capacitors installed on OEM board | Calculated values based on Figure 9.2, "Capacitance Formulas" (See Note 9.2) |
| $C_2$ | | |

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

**Figure 9.2 Capacitance Formulas**

**Note 9.1** $C_0$ is usually included (subtracted by the crystal manufacturer) in the specification for $C_L$ and should be set to '0' for use in the calculation of the capacitance formulas in Figure 9.2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between XTAL1 and XTAL2. For an accurate calculation of $C_1$ and $C_2$, take the parasitic capacitance between traces XTAL1 and XTAL2 into account.

**Note 9.2** Each of these capacitance values is typically approximately 18 pF.

## 9.2 Ceramic Resonator

24 MHz ± 350 ppm

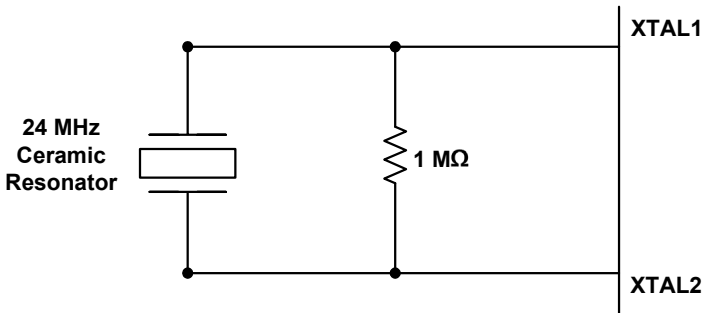



**Figure 9.3 Ceramic Resonator Usage with SMSC IC**

## 9.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms.

The external clock is recommended to conform to the signaling level designated in the JESD76-2 specification on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

### 9.3.1 $I^2C$ EEPROM

Frequency is fixed at 58.6 kHz ± 20%

### 9.3.2 USB 2.0

The SMSC device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification for more information.

# Chapter 10 DC Parameters

## 10.1 Maximum Guaranteed Ratings

| PARAMETER | SYMBOL | MIN | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Storage Temperature | $T_{STOR}$ | -55 | 150 | °C | |
| Lead Temperature | | | | °C | Please refer to JEDEC specification J-STD-020D. |
| 3.3 V supply voltage | $V_{DD33}$ | -0.5 | 4.0 | V | |
| Voltage on USB+ and USB- pins | | -0.5 | (3.3 V supply voltage + 2) ≤ 6 | V | |
| Voltage on GPIO10 | | -0.5 | $V_{DD33}$ + 0.3 | V | When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as $V_{DD33}$ is less than 3.63 V and $T_A$ is less than 70°C. |
| Voltage on any signal pin | | -0.5 | $V_{DD33}$ + 0.3 | V | |
| Voltage on XTAL1 | | -0.5 | 3.6 | V | |
| Voltage on XTAL2 | | -0.5 | 2.0 | V | |

**Note 10.1** Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

**Note 10.2** When powering this device from laboratory or system power supplies the Absolute Maximum Ratings must not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, a clamp circuit should be used.

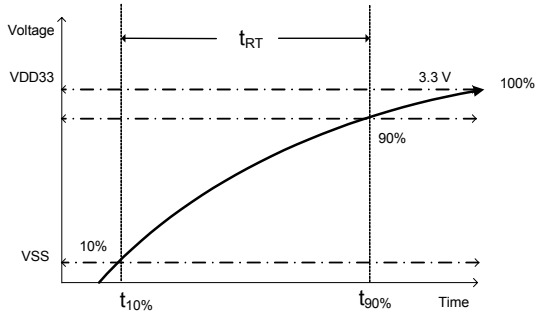



**Figure 10.1 Supply Rise Time Models**

## 10.2 Operating Conditions

| PARAMETER | SYMBOL | MIN | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | 85 | °C | Ambient temperature in still air. |
| 3.3 V supply voltage | $V_{DD33}$ | 3.0 | 3.6 | V | A 3.3 V regulator with an output tolerance of 1% must be used if the output of the internal power FETs must support a 5% tolerance. |
| 3.3 V supply rise time | $t_{RT}$ | 0 | 400 | µs | (Figure 10.1) |
| Voltage on USB+ and USB- pins | | -0.3 | 5.5 | V | If any 3.3 V supply voltage drops below 3.0 V, then the MAX becomes:<br>(3.3 V supply voltage) + 0.5 ≤ 5.5 |
| Voltage on any signal pin | | -0.3 | $V_{DD33}$ | V | |
| Voltage on XTAL1 | | -0.3 | 2.0 | V | |
| Voltage on XTAL2 | | -0.3 | 2.0 | V | |

## 10.3 DC Electrical Characteristics

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **I, IPU, IPD Type Input Buffer** | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| Pull Down | PD | | 72 | | µA | |
| Pull Up | PU | | 58 | | µA | |
| **IS Type Input Buffer** | | | | | | |
| Low Input Level | $V_{ILI}$ | | | 0.8 | V | TTL Levels |
| High Input Level | $V_{IHI}$ | 2.0 | | | V | |
| Hysteresis | $V_{HYSI}$ | | 420 | | mV | |
| **ICLK Input Buffer** | | | | | | |
| Low Input Level | $V_{ILCK}$ | | | 0.5 | V | |
| High Input Level | $V_{IHCK}$ | 1.4 | | | V | |
| Input Leakage | $I_{IL}$ | -10 | | +10 | µA | $V_{IN}$ = 0 to $V_{DD33}$ |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **Input Leakage** | | | | | | |
| (All I and IS buffers) | | | | | | |
| Low Input Leakage | $I_{IL}$ | -10 | | +10 | µA | $V_{IN}$ = 0 |
| High Input Leakage | $I_{IH}$ | -10 | | +10 | µA | $V_{IN}$ = $V_{DD33}$ |
| **O12 Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA @ $V_{DD33}$= 3.3 V |
| High Output Level | $V_{OH}$ | $V_{DD33}$ - 0.4 | | | V | $I_{OH}$ = -12 mA @ $V_{DD33}$= 3.3 V |
| Output Leakage | $I_{OL}$ | -10 | | +10 | µA | $V_{IN}$ = 0 to $V_{DD33}$ (Note 10.3) |
| **I/O12, I/O12PU & I/O12PD Type Buffer** | | | | | | |
| Low Output Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA @ $V_{DD33}$= 3.3 V |
| High Output Level | $V_{OH}$ | $V_{DD33}$ - 0.4 | | | V | $I_{OH}$ = -12 mA @ $V_{DD33}$= 3.3 V |
| Output Leakage | $I_{OL}$ | -10 | | +10 | µA | $V_{IN}$ = 0 to $V_{DD33}$ (Note 10.3) |
| Pull Down | PD | | 72 | | µA | |
| Pull Up | PU | | 58 | | µA | |
| **IO-U** | | | | | | (Note 10.4) |
| **I-R** | | | | | | (Note 10.5) |
| **Integrated Power FET Set to 100 mA** | | | | | | |
| Output Current (Note 10.6) | $I_{OUT}$ | 100 | | | mA | $Vdrop_{FET}$ = 0.22 V |
| Short Circuit Current Limit | $I_{SC}$ | | | 140 | mA | $Vout_{FET}$ = 0 V |
| On Resistance (Note 10.6) | $R_{DSON}$ | | | 2.1 | Ω | $I_{FET}$ = 70 mA |
| Output Voltage Rise Time | $t_{DSON}$ | | | 800 | µs | $C_{LOAD}$ = 10 µF |

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| **Integrated Power FET Set to 200 mA** | | | | | | |
| Output Current (Note 10.6) | $I_{OUT}$ | 200 | | | mA | $Vdrop_{FET}$ = 0.46 V |
| Short Circuit Current Limit | $I_{SC}$ | | | 181 | mA | $Vout_{FET}$ = 0 V |
| On Resistance (Note 10.6) | $R_{DSON}$ | | | 2.1 | Ω | $I_{FET}$ = 70 mA |
| Output Voltage Rise Time | $t_{DSON}$ | | | 800 | µs | $C_{LOAD}$ = 10 µF |
| Supply Current Unconfigured | | | | | | |
| Hi-Speed Host<br>Full Speed Host | $I_{CCINTHS}$<br>$I_{CCINITFS}$ | | 65<br>60 | 80<br>75 | mA<br>mA | |
| Supply Current Active | $I_{CC}$ | | 280 | 315 | mA | |
| Supply Current Suspend | $I_{CSBYI}$ | | 420 | 650 | µA | |
| Supply Current Reset | $I_{RST}$ | | 205 | 425 | µA | |

**Note 10.3** Output leakage is measured with the current pins in high impedance.

**Note 10.4** See the USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

**Note 10.5** RBIAS is a 3.3 V tolerant analog pin.

**Note 10.6** Output current range is controlled by program software. The software disables the FET during short circuit condition.

## 10.4 Capacitance $T_A$ = 25°C; fc = 1 MHz; $V_{DD33}$ = 3.3 V

**Table 10.1 Pin Capacitance**

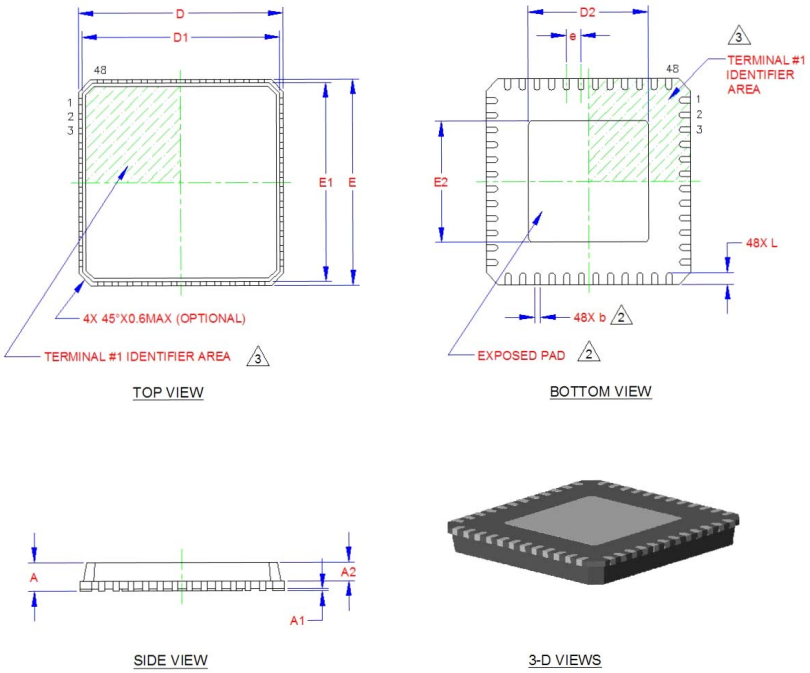
| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITION |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Clock Input Capacitance | $C_{XTAL}$ | | | 2 | pF | All pins (except USB pins and pins under test) are tied to AC ground. |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

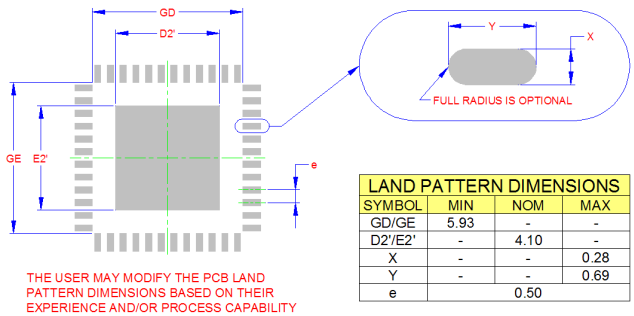
# Chapter 11 GPIO Usage

**Table 11.1 USB2640i/USB2641i GPIO Usage**

| NAME | ACTIVE LEVEL | SYMBOL | DESCRIPTION |
|---|---|---|---|
| GPIO1 | H | TxD / LED | Serial port transmit line / LED indicator |
| GPIO2 | H | RxD | Serial port receive line |
| GPIO4 | H | SCK | Serial EEPROM clock |
| GPIO5 | H | SDA | Serial EEPROM data |
| GPIO6 | L | SD_WP | Secure Digital card write protect detect |
| GPIO10 | L | CRD_PWR_CTRL | Card power control |
| GPIO12 | L | MS_nCD | Memory Stick card detect |
| GPIO14 | L | xD_nCD | xD-Picture card detect |
| GPIO15 | L | SD_nCD | Secure Digital card detect |

# Chapter 12 Package Outline




| LAND PATTERN DIMENSIONS | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| GD/GE | 5.93 | - | - |
| D2'/E2' | - | 4.10 | - |
| X | - | - | 0.28 |
| Y | - | - | 0.69 |
| e | | 0.50 | |

| COMMON DIMENSIONS | | | | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTE | REMARK |
| A | 0.70 | - | 1.00 | - | OVERALL PACKAGE HEIGHT |
| A1 | 0 | 0.02 | 0.05 | - | STANDOFF |
| A2 | - | - | 0.90 | - | MOLD CAP THICKNESS |
| D/E | 6.85 | 7.00 | 7.15 | - | X/Y BODY SIZE |
| D1/E1 | 6.55 | - | 6.95 | - | X/Y MOLD CAP SIZE |
| D2/E2 | 4.00 | 4.10 | 4.20 | 2 | X/Y EXPOSED PAD SIZE |
| L | 0.30 | - | 0.50 | - | TERMINAL LENGTH |
| b | 0.18 | 0.25 | 0.30 | 2 | TERMINAL WIDTH |
| e | 0.50 BSC | | | - | TERMINAL PITCH |

**NOTES:**
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

**Figure 12.1 USB2640i/USB2641i 48-Pin QFN**

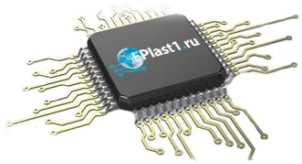
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

**Телефон:** 8 (812) 309 58 32 (многоканальный)
**Факс:** 8 (812) 320-02-42
**Электронная почта:** org@eplast1.ru
**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.