

VFD CONTROLLER DRIVER

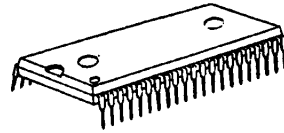
■ GENERAL DESCRIPTION

The NJU3421A is a VFD (Vacuum Fluorescent Display) Controller Driver with key scan function.

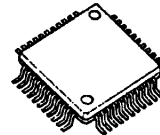
It contains display data RAM, address counter, command register, high voltage drivers, and serial interface circuit.

The display data, the command data and the key scanning data can be transmitted with the serial interface circuit, and VFD driving voltage can operate up to 45V. The NJU3421A is useful for car audio, VCR and other VFD application items.

■ PACKAGE OUTLINE



NJU3421AL



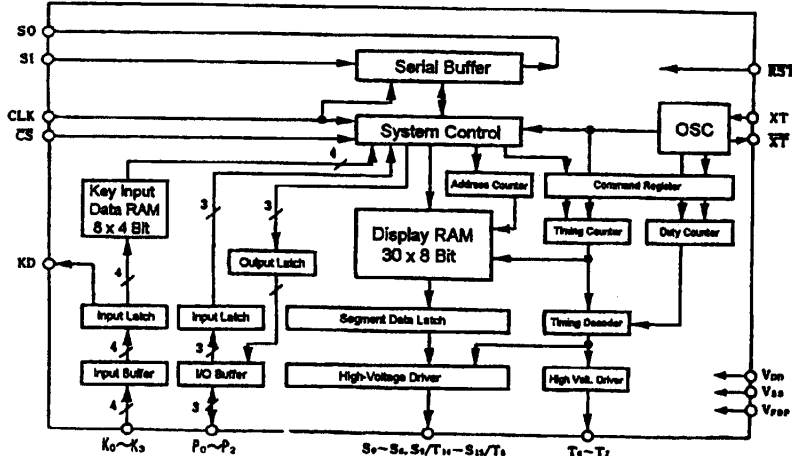
NJU3421AF

■ FEATURES

- VFD Driving Voltage  $|V_{DD}-V_{FOP}| \leq 45V$
- Display Mode 9 Segments Display  $\times$  15 Digits  
16 Segments Display  $\times$  8 Digits
- Serial Interface
- Display ON/OFF Function
- Key Scan Function 8  $\times$  4 Keys max.
- Display Data RAM 30  $\times$  8 Bits
- Key Input Data RAM 8  $\times$  4 Bits
- Key Input Detecting Function
- High Driving Current(I/O Ports)  $I_o=10mA$  max.
- Oscillation Circuit on-chip
- Power On Initialization
- Operating Voltage 5V  $\pm$  10%
- Package Outline SDIP 42 / QFP 44-A1 / BumpChip
- C-MOS Technology

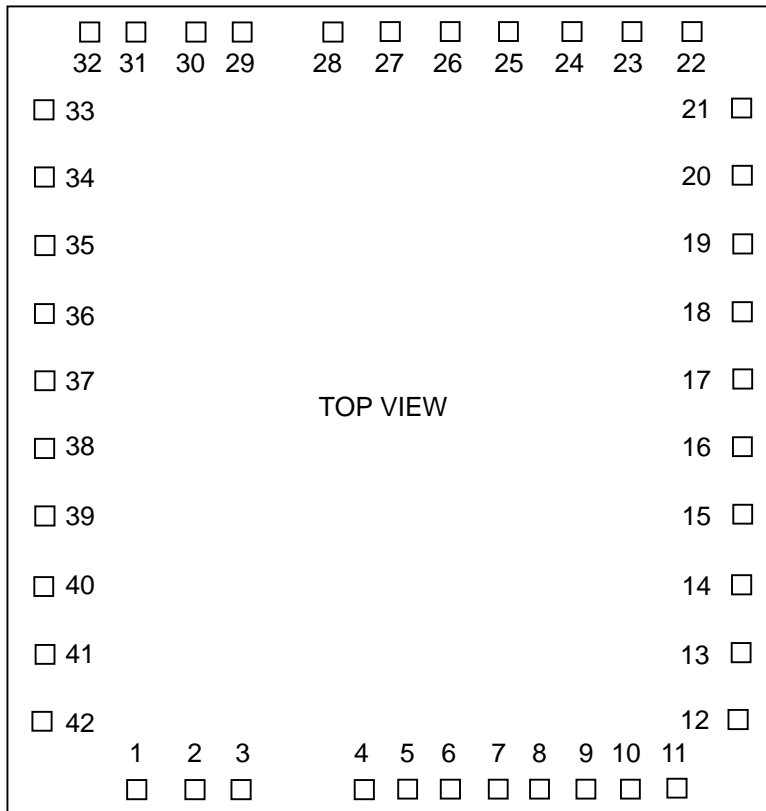
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■ BLOCK DIAGRAM



# NJU3421A

## ■ PAD LOCATION



Chip Thickness : 400 $\mu$ m  
 Chip Center : X=0 $\mu$ m, Y=0 $\mu$ m  
 Chip Size : X= 3.40 mm, Y= 3.45 mm  
 Bump Size : 103.0  $\mu$ m x 103.0  $\mu$ m  
 Bump Height : 15 $\mu$ m(Typ)  
 Bump Material : Au  
 Sub striate : N

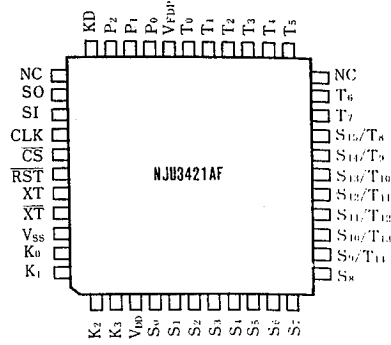
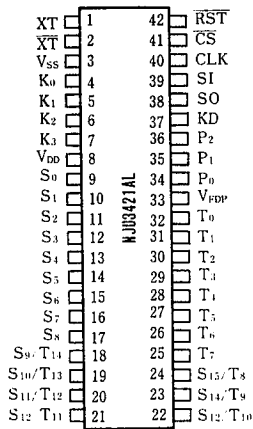
## ■ PAD CORDINATES

Chip Size 3.40 x 3.45 mm(Chip Center X=0 $\mu$ m, Y=0 $\mu$ m)

PAD No.	Terminal	X= $\mu$ m	Y= $\mu$ m
1	K2	-1215	-1444
2	K3	-939	-1444
3	V <sub>DD</sub>	-744	-1444
4	S0	-510	-1506
5	S1	-286	-1506
6	S2	-62	-1506
7	S3	162	-1506
8	S4	386	-1506
9	S5	610	-1506
10	S6	834	-1506
11	S7	1058	-1506
12	S8	1481	-1314
13	S9/T14	1481	-1023
14	S10/T13	1481	-773
15	S11/T12	1481	-523
16	S12/T11	1481	-273
17	S13/T10	1481	44
18	S14/T9	1481	324
19	S15/T8	1481	604
20	T7	1481	884
21	T6	1481	1164

PAD No.	Terminal	X= $\mu$ m	Y= $\mu$ m
22	T5	1407	1506
23	T4	1133	1506
24	T3	859	1506
25	T2	585	1506
26	T1	311	1506
27	T0	37	1506
28	V <sub>FDP</sub>	-145	1506
29	P0	-484	1423
30	P1	-675	1423
31	P2	-1011	1423
32	KD	-1227	1423
33	SO	-1418	1100
34	SI	-1419	883
35	CLK	-1419	603
36	CS	-1419	407
37	RST	-1419	127
38	XT	-1419	-153
39	XT	-1419	-446
40	V <sub>SS</sub>	-1419	-653
41	K0	-1419	-880
42	K1	-1419	-1156

## ■ PIN CONFIGURATION



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## ■ TERMINAL DESCRIPTION

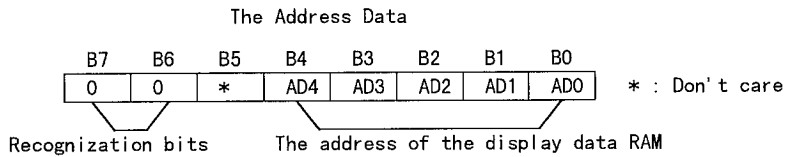
NO.		SYMBOL	FUNCTION
SDIP42	QFP44-A1		
8 3 33	3 42 29	$V_{DD}$ $V_{SS}$ $V_{FDP}$	POWER SOURCE GND VFD Driving Voltage
1, 2	40, 41	$XT, \bar{X}T$	Oscillation Terminals. For external clock operation, The clock should be input on XT terminal.
4~7	43, 44, 1, 2	$K_0 \sim K_3$	Key Input Terminals(Pull-Down Resistance)
37	33	KD	Key Input Detecting Terminal. When key input, "H" level is output from this terminal.
9~17 18~24 25~32	4~12 13~19 20, 21, 23~28	$S_0 \sim S_8$ $S_9/T_{14} \sim S_{15}/T_8$ $T_7 \sim T_0$	Segment Output Terminals(Pull-Down Resistance) Segment/Timing Output Terminals(Pull-Down Resistance) Timing Output Terminals(Pull-Down Resistance)
42	39	$\bar{R}ST$	Reset Terminal (Pull-UP Resistance) "L":Reset
34~36	30~32	$P_0 \sim P_2$	I/O Ports (Pull-Up Resistance) Output:High current Output(LED Display is available) Input:Available by all "H" output setting.
38	35	SO	Serial Data Output Terminal. The key scan data or the I/O port output data is output.
39	36	SI	Serial Data ( Address, I/O Ports, Command, Display ) input Terminal.
40	37	CLK	Shift Clock Input Terminal.
41	38	$\bar{C}S$	Chip Select Input Terminal. "L":Activated.
-	22, 34	NC	Non Connection.

■ FUNCTION DESCRIPTION

(1) Address Counter

The address counter addresses the display data RAM which data are sent by the serial data transmission. When the first word of the serial data is recognized as the address of the display data RAM (The upper two bits of a byte must be "00" ), the lower 5bits are set up into the address counter as the address of the display data RAM. The data of the display data RAM which are input sequentially are set into the specified address and the address counter increments.

Though the address counter consists of the 5-bit counter, the effective range is from "00000" (00<sub>H</sub>) to "11101" (1D<sub>H</sub>) and the invalid range is from "11110" (1E<sub>H</sub>) and "11111" (1F<sub>H</sub>). The address of "11111" (1F<sub>H</sub>) is incremented to "00000" (00<sub>H</sub>).



The mapping of the display data RAM

	B7	B6	B5	B4	B3	B2	B1	B0	
00 <sub>H</sub>									
02 <sub>H</sub>									
04 <sub>H</sub>									
06 <sub>H</sub>									
08 <sub>H</sub>									
0A <sub>H</sub>									
0C <sub>H</sub>									
0E <sub>H</sub>									
10 <sub>H</sub>									
12 <sub>H</sub>									
14 <sub>H</sub>									
16 <sub>H</sub>									
18 <sub>H</sub>									
1A <sub>H</sub>									
1C <sub>H</sub>									
1E <sub>H</sub>	*	*	*	*	*	*	*	*	
	S <sub>7</sub>	S <sub>6</sub>	S <sub>5</sub>	S <sub>4</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	
01 <sub>H</sub>									T <sub>0</sub>
03 <sub>H</sub>									T <sub>1</sub>
05 <sub>H</sub>									T <sub>2</sub>
07 <sub>H</sub>									T <sub>3</sub>
09 <sub>H</sub>									T <sub>4</sub>
0B <sub>H</sub>									T <sub>5</sub>
0D <sub>H</sub>									T <sub>6</sub>
0F <sub>H</sub>									T <sub>7</sub>
11 <sub>H</sub>									T <sub>8</sub>
13 <sub>H</sub>									T <sub>9</sub>
15 <sub>H</sub>									T <sub>10</sub>
17 <sub>H</sub>									T <sub>11</sub>
19 <sub>H</sub>									T <sub>12</sub>
1B <sub>H</sub>									T <sub>13</sub>
1D <sub>H</sub>									T <sub>14</sub>
1F <sub>H</sub>	*	*	*	*	*	*	*	*	T <sub>15</sub>
	S <sub>15</sub>	S <sub>14</sub>	S <sub>13</sub>	S <sub>12</sub>	S <sub>11</sub>	S <sub>10</sub>	S <sub>9</sub>	S <sub>8</sub>	

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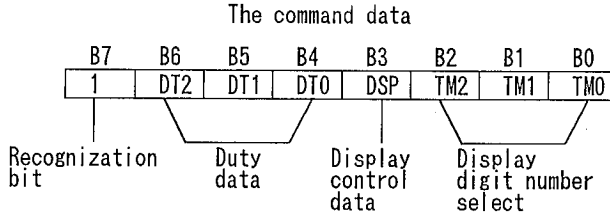
 Don't Care

## (2) COMMAND REGISTER

The Command Register is the register for setting the status of Display Duty, Display Digit Number and Display ON/OFF.

When the first word of serial transmitted data is recognized as the command data (The upper one bit of a byte must be "1".), the lower 7 bits are set into the command register. After the command data are received the timing counter is initialized and then the input command is executed. During the initialization of the timing counter and the command execution, the display can be off. Therefore, the frequent command transmission causes the flicker of the display.

The default status of the display mode is display-off by the power on initialization function.



(2-1) Duty set

DT2	DT1	DT0	Timing signal Duty
0	0	0	2/16
0	0	1	4/16
0	1	0	6/16
0	1	1	8/16
1	0	0	10/16
1	0	1	12/16
1	1	0	14/16
1	1	1	15/16

(2-2) Display control set

DSP	Display
0	OFF
1	ON

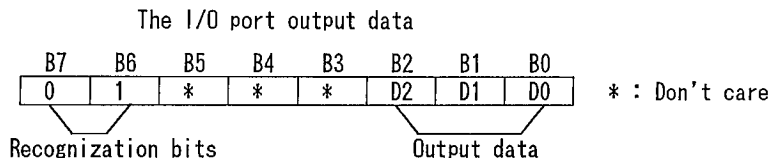
(2-3) Display digit number set

TM2	TM1	TM0	Digits
0	0	0	8
0	0	1	9
0	1	0	10
0	1	1	11
1	0	0	12
1	0	1	13
1	1	0	14
1	1	1	15

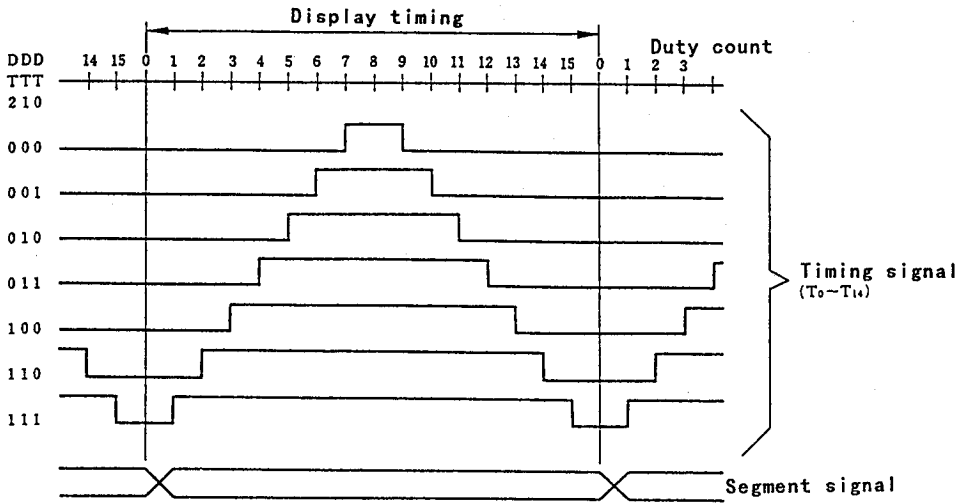
## (3) I/O Port

The NJU3421A incorporates three I/O ports. As the output type of these three ports is the constructed by the N-channel and open-drain type FET of the low on-resistance and the pull-up resistor, the output driver can drive the LED. When "H" level is set with the I/O port output data, these I/O ports can be used as the input mode.

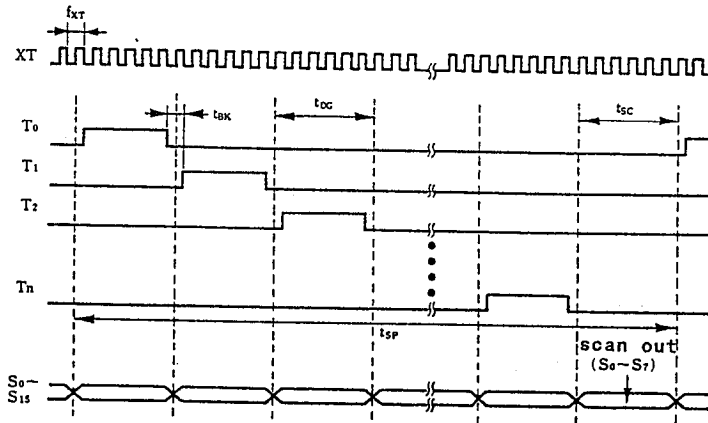
When the first word of serial data is recognized as the I/O port output data (the upper two bits of a byte must be "01"), the status of the data of the lower three bits are output from the I/O port.



## ■ TIMING SIGNAL / DUTY CHANGE WAVEFORM



## ■ DISPLAY TIMING CHART



- |                                    |                                                      |
|------------------------------------|------------------------------------------------------|
| Oscillation frequency              | : $f_{XT}$                                           |
| Minimum blanking time (Duty 15/16) | : $t_{BK} = (1/f_{XT}) \times 96$                    |
| 1character display time            | : $t_{DC} = t_{BK} \times 16$                        |
| key scanning time                  | : $t_{SC} = t_{DC}$                                  |
| 1cycle display time                | : $t_{SP} = t_{DC} \times \text{character} + t_{SC}$ |

## (4) KEY INPUT CIRCUIT

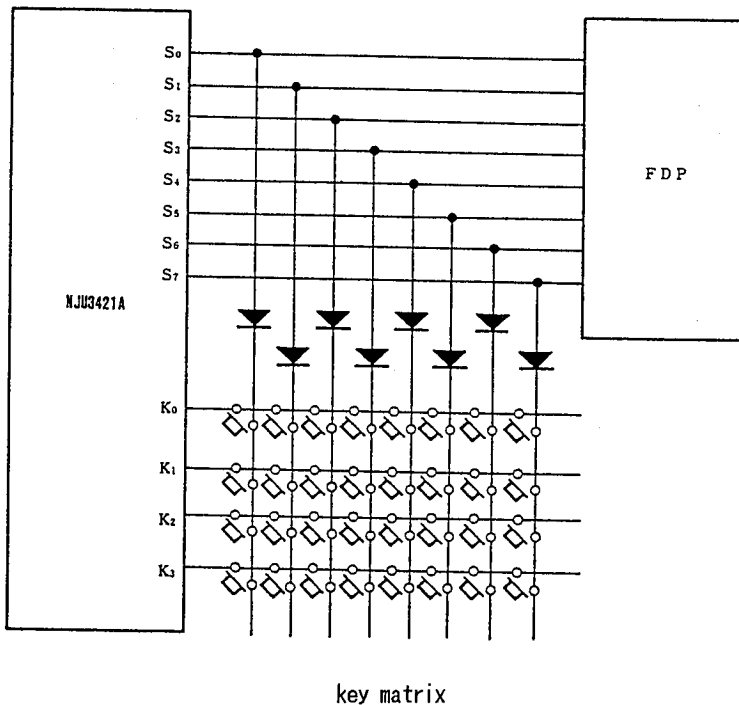
The key input circuit is constructed with the key scanning outputs (8 outputs) which are appropriated from the segment output ( $S_0$  to  $S_7$ ) for the display, the key input terminals (4 terminals) and the key switches as shown below. When the key scanning signal is output during the key pushed, the key input terminal receives the same level ("H") of the key scanning signal. If the keys are not pushed, the key input terminal receives "L" level at any time because of its pull-down resistor.

The received key data are stored in the key data RAM in sequence and the data can be get by the serial data transmission.

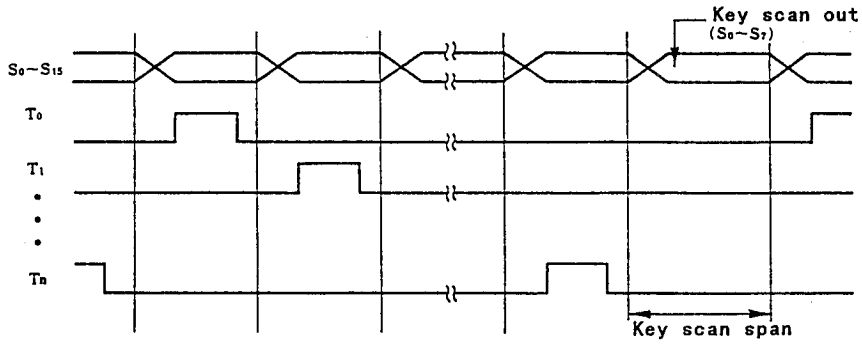
The key input detecting function lets the key input detecting output terminal goes to "H" level when any key pushes. The "H" level output of the key input detecting output terminal is continued during the key pushed.

## (4-1) Key condition vs Key input terminal level

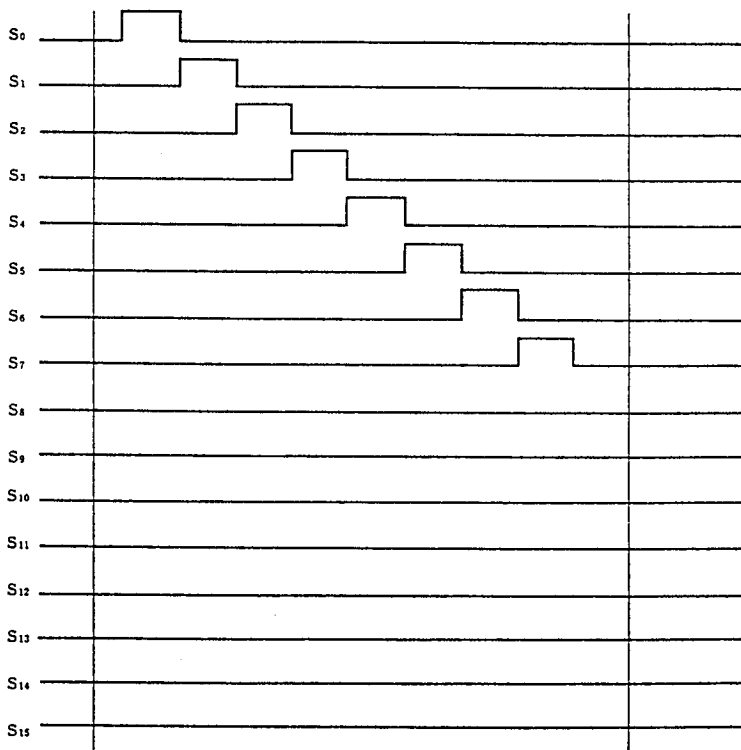
key condition	input level
key pushed	"H"
not key pushed	"L"



## ■ FDP DISPLAY OUTPUT WAVEFORM



## ■ ENLARGED KEY SCAN SPAN





## (5) SERIAL DATA TRANSMISSION

The data transmission with the external can be executed by the serial interface circuit only. This interface circuit requires the external shift clock input and can execute the bi-direction (input/output) action synchronously as shown below.

The serial data are grouped at a word which equalles to a byte (8 bits) for this device. The serial interface circuit is activated when the CS terminal is set to "L" level. While the CS is "L", the words of the serial data are able to transmitted using the shift clock ( the CLK terminal) and the serial data input or output (the SI or SO terminal) synchronously.

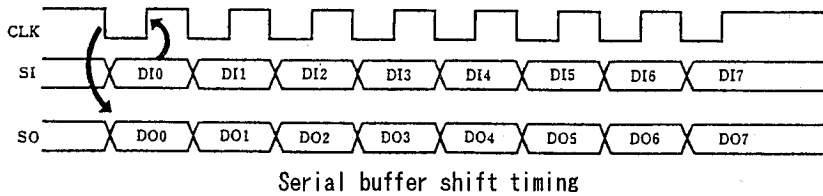
On the data input status, the first transmitted word must be the address, the command or the I/O port output data. When the first word is the address data, the following words should be the display data. When the first word is the command or I/O port output data, the following words, if transmitted, are ineffective.

On the data output status, the transmitted word incorporates the key data corresponding to the lower 4 bits and the I/O port input data corresponding to the upper 4 bits ( The MSB is invalid). The key data of the first word means the data by scanning the  $S_0$ , these of the second word means the data by scanning the  $S_1$ , ... finally, these of the 8th word means the data by scanning the  $S_7$ . The I/O port input data means the last status data. For getting all key matrix data ( 8 x 4 max.), the data transmission of the 8 words is required.

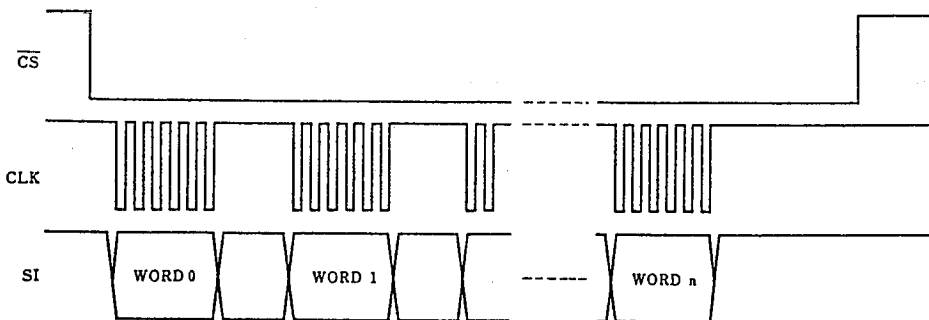
After the key data transmission is ignored at less than 8 words, the next key data transmission is reset to the first ( $S_0$  scanning) word.

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## ■ CLK and SI/SO TIMING CHART



## ■ SERIAL TRANSMISSION FORMAT



## (5-1) SERIAL INPUT DATA

		The address data								
		B7	B6	B5	B4	B3	B2	B1	B0	
		0	0	*	AD4	AD3	AD2	AD1	AD0	* : Don't care
		The command data								
WORD 0		B7	B6	B5	B4	B3	B2	B1	B0	
		1	DT2	DT1	DT0	DSP	TM2	TM1	TMO	
		The I/O port output data								
		B7	B6	B5	B4	B3	B2	B1	B0	
		0	1	*	*	*	D2	D1	D0	* : Don't care

WORD 1~n Display data are required when WORD 0 = address data  
Any data are become ineffective when WORD 0 = not address data

## (5-2) SERIAL OUTPUT DATA

		Serial output data								
		B7	B6	B5	B4	B3	B2	B1	B0	
WORD 0~7		*	P2	P1	P0	K3	K2	K1	K0	* : Don't care
		(Key scanning data: S <sub>0</sub> ~S <sub>7</sub> )								

WORD 8~n Ineffective data

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	CONDITIONS	UNIT
Operating Voltage	V <sub>DD</sub>	-0.3 ~ +7.0		V
Input Voltage	V <sub>IN</sub>	-0.3 ~ V <sub>DD</sub> +0.3		V
Output Voltage	V <sub>OUT</sub>	-0.3 ~ V <sub>DD</sub> +0.3		V
VFD Driving Voltage	V <sub>FDP</sub>	V <sub>DD</sub> -40~V <sub>DD</sub> +0.3		V
"H" level Output Current	I <sub>OH</sub>	-5	For a terminal except the display terminals	mA
	I <sub>ODH1</sub>	-15	For a terminal, S <sub>0</sub> ~S <sub>7</sub> Terminals only	
	I <sub>ODH2</sub>	-35	For a terminal, T <sub>0</sub> ~T <sub>7</sub> , S <sub>a</sub> /T <sub>1,6</sub> ~S <sub>1,6</sub> /T <sub>e</sub> Terminals only	
"H" level Total Output Current	Σ I <sub>OH</sub>	-40	Sum of the output terminal except the display Terminals	mA
	Σ I <sub>ODH</sub>	-100	Sum of the Display Terminals	
"L" level Output Current	I <sub>OLC</sub>	20	For a terminal, P <sub>0</sub> ~P <sub>1</sub> Terminals only	mA
"L" level Total Output Current	Σ I <sub>OL</sub>	100	Sum of the Output terminals	mA
Power Dissipation	P <sub>D</sub>	SDIP: 250 QFP: 300		mW
Operating Temperature Range	T <sub>opr</sub>	-30 ~ + 80		°C
Storage Temperature Range	T <sub>stg</sub>	-55 ~ +125		°C

## ■ ELECTRICAL CHARACTERISTICS

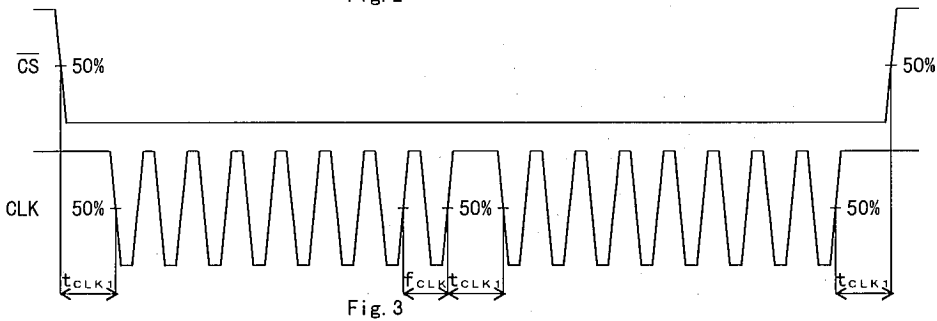
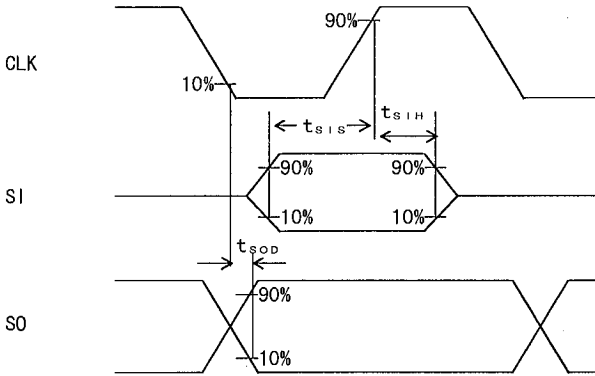
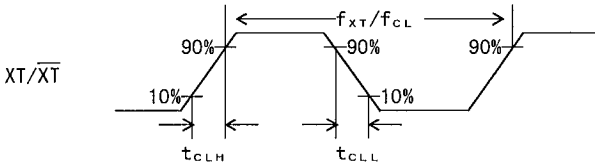
 ( Ta=25°C, V<sub>SS</sub>=0V )

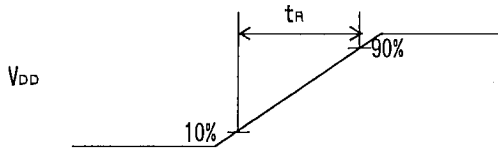
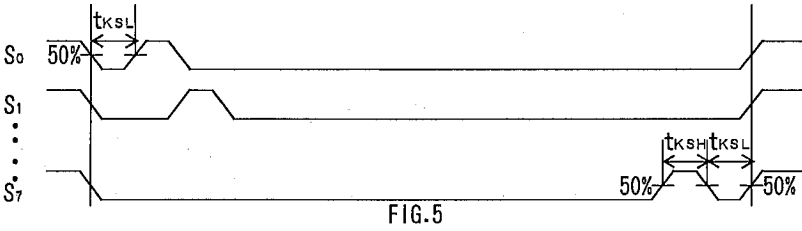
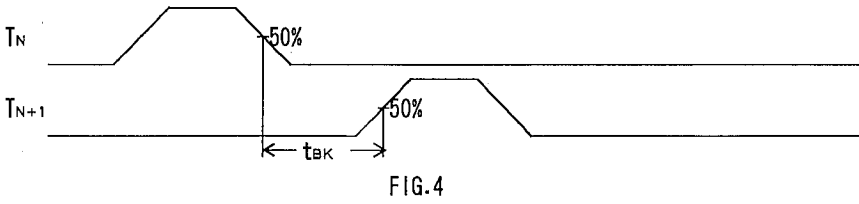
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V <sub>DD</sub>	V <sub>DD</sub> Terminal	4.5		5.5	V
"H" Level Input Voltage	V <sub>IH1</sub>	XT, $\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SI, CLK, P <sub>0</sub> ~P <sub>2</sub> Terminals	0.8V <sub>DD</sub>			V
	V <sub>IH2</sub>	K <sub>0</sub> ~K <sub>3</sub> Terminals	0.4V <sub>DD</sub>			V
"L" Level Input Voltage	V <sub>IL1</sub>	XT, $\overline{\text{RST}}$ , $\overline{\text{CS}}$ , SI, CLK, P <sub>0</sub> ~P <sub>2</sub> Terminals			0.2V <sub>DD</sub>	V
	V <sub>IL2</sub>	K <sub>0</sub> ~K <sub>3</sub> Terminals			0.16V <sub>DD</sub>	V
"H" Level Output Voltage	V <sub>OH1</sub>	KD, S0 Terminals V <sub>DD</sub> =4.5V, I <sub>OH1</sub> =-0.5mA	4.0			V
	V <sub>OH2</sub>	KD, S0 Terminals V <sub>DD</sub> =4.5V, I <sub>OH2</sub> =-1.2mA	3.5			V
"L" Level Output Voltage	V <sub>OL1</sub>	KD, S0 Terminals V <sub>DD</sub> =4.5V, I <sub>OL1</sub> =+1.8mA			0.4	V
	V <sub>OL2</sub>	KD, S0 Terminals V <sub>DD</sub> =4.5V, I <sub>OL2</sub> =+3.6mA			0.6	
	V <sub>OL3</sub>	P <sub>0</sub> ~P <sub>2</sub> Terminals V <sub>DD</sub> =4.5V, I <sub>OL3</sub> =+10mA			0.4	
Input Off Leak Current	I <sub>Iz</sub>	$\overline{\text{CS}}$ , CLK, SI Terminals V <sub>DD</sub> =5.5V, V <sub>I</sub> =0 or 5.5V			±1	μA
Display Output Current	I <sub>OH</sub>	S <sub>0</sub> ~S <sub>8</sub> Terminals V <sub>DD</sub> =4.5V, V <sub>OH</sub> =V <sub>DD</sub> -2.5V	-7			mA
		S <sub>9</sub> /T <sub>14</sub> ~S <sub>15</sub> /T <sub>8</sub> , T <sub>0</sub> ~T <sub>7</sub> Term. V <sub>DD</sub> =4.5V, V <sub>OH</sub> =V <sub>DD</sub> -2.5V	-15			
Pull-Up Resistance	R <sub>UR</sub>	$\overline{\text{RST}}$ Terminal V <sub>DD</sub> =5.0V, V <sub>I</sub> =V <sub>SS</sub>	140		260	kΩ
	R <sub>UP</sub>	P <sub>0</sub> ~P <sub>2</sub> Terminals V <sub>DD</sub> =5.0V, V <sub>I</sub> =V <sub>SS</sub>	10		20	
Pull-Down resistance	R <sub>DK</sub>	K <sub>0</sub> ~K <sub>3</sub> Terminals V <sub>DD</sub> =5.0V, V <sub>I</sub> =V <sub>SS</sub>	20		50	kΩ
	R <sub>DST</sub>	S <sub>0</sub> ~S <sub>8</sub> , S <sub>9</sub> /T <sub>14</sub> ~S <sub>15</sub> /T <sub>8</sub> , T <sub>0</sub> ~T <sub>7</sub> V <sub>DD</sub> =5.0V, V <sub>O</sub> =V <sub>SS</sub> , V <sub>FDP</sub> =V <sub>DD</sub> -40V	70		200	
Logic Operating Current	I <sub>DD1</sub>	V <sub>SS</sub> Terminal, V <sub>DD</sub> =5.0V, 4MHz Ceramic resonator, C <sub>1</sub> =C <sub>2</sub> =27pF Output Open, All Segment or Timing Output is OFF		1	2	mA
Display Operating Current	I <sub>DD2</sub>	V <sub>FDP</sub> Terminal, V <sub>DD</sub> =5.0V, Output Open except S <sub>0</sub> ~S <sub>8</sub> , T <sub>0</sub> ~T <sub>7</sub> S <sub>9</sub> /T <sub>14</sub> ~S <sub>15</sub> /T <sub>8</sub> All Segment or Timing Output is ON		7	10	mA

## ■ AC Characteristics

 (  $T_a=25^\circ\text{C}$ ,  $V_{OD}=5V\pm 10\%$ ,  $V_{SS}=0V$  )

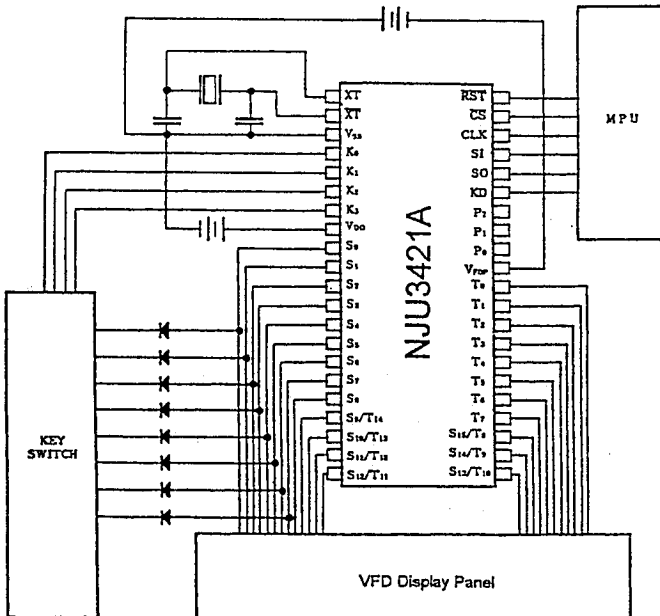
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation Frequency	$f_{XT}$	Fig. 1	1	4	5	MHz
External Clock Input	$f_{CL}$					
External Clock Rise Time	$t_{CLH}$				20	ns
External Clock Fall Time	$t_{CLL}$			20	ns	
Serial Input Setup Time	$t_{SIS}$	Fig. 2	60			ns
Serial Input Hold Time	$t_{SIH}$		10			ns
Serial Output Delay Time	$t_{SOD}$	Fig. 2, Load=50pF			120	ns
Shift Clock Frequency	$f_{CLK}$	Fig. 3			$f_{XT}/3$	MHz
Shift Clock Interval Time	$t_{CLKI}$		10			us
Minimum Blanking Time	$t_{BK}$	Fig. 4, @ $f_{XT}=4\text{MHz}$	20		30	us
"L" level Time	$t_{KSL}$	Fig. 5, @ $f_{XT}=4\text{MHz}$ , Key scan	20			us
"H" level Time	$t_{KSH}$		20		30	us
Power Rise Time	$t_r$	Fig. 6	0.05		50	ms
Reset Pulse Width	$t_{RST}$		10			us





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■ APPLICATION CIRCUIT



## MEMO

**[CAUTION]**

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