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FDMS2D4N03S

N-Channel PowerTrench[®] SyncFET[™]

30 V, 163 A, 1.8 mΩ

Features

- Max $r_{DS(on)}$ = 1.8 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 28\text{ A}$
- Max $r_{DS(on)}$ = 2.34 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 26\text{ A}$
- High Performance Technology for Extremely Low $r_{DS(on)}$
- SyncFET[™] Schottky Body Diode
- 100% UIL Tested
- RoHS Compliant

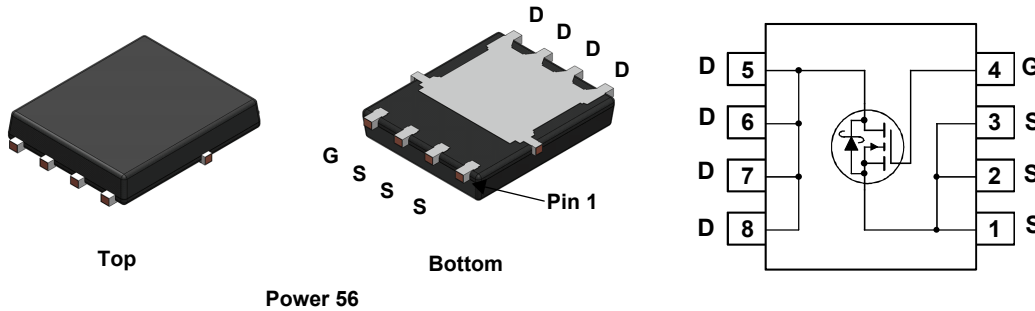


General Description

The FDMS2D4N03S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic schottky body diode.

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±12	V
I_D	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	163
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	103
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	28
	-Pulsed	(Note 4)	694
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	216 mJ
P_D	Power Dissipation	$T_C = 25\text{ °C}$	74 W
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.5
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2D4N03S	FDMS2D4N03S	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		18		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 1\text{ mA}$	1.0	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 28\text{ A}$		1.4	1.8	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 26\text{ A}$		1.7	2.34	
		$V_{GS} = 10\text{ V}, I_D = 28\text{ A}, T_J = 125\text{ }^\circ\text{C}$		2.0	2.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 28\text{ A}$		200		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		4670	6540	pF
C_{oss}	Output Capacitance			1395	1955	pF
C_{riss}	Reverse Transfer Capacitance			63	120	pF
R_g	Gate Resistance		0.1	0.5	1.5	Ω

Switching Characteristics

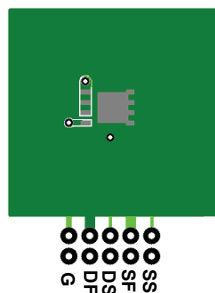
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 28\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		15	28	ns	
t_r	Rise Time			4	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns	
t_f	Fall Time			3	10	ns	
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$		63	88	nC	
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 15\text{ V},$ $I_D = 28\text{ A}$		28	40	nC
Q_{gs}	Gate to Source Charge				9.8		nC
Q_{gd}	Gate to Drain "Miller" Charge				4.9		nC

Drain-Source Diode Characteristics

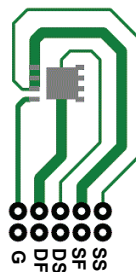
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.65	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 28\text{ A}$ (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 28\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		37	59	ns
Q_{rr}	Reverse Recovery Charge			51	81	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



50 $^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. E_{AS} of 216 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$; N-ch; $L = 3\text{ mH}, I_{AS} = 12\text{ A}, V_{DD} = 30\text{ V}, V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}, I_{AS} = 39\text{ A}$.

4. Pulsed I_D please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

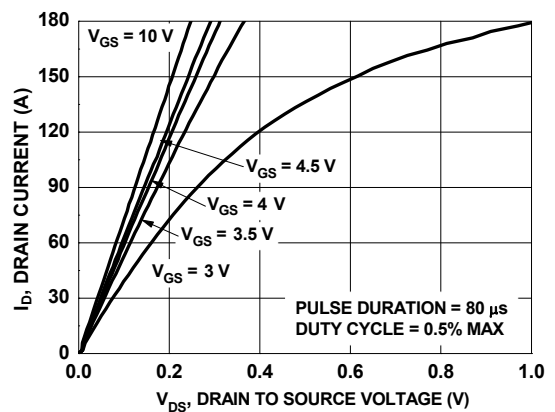


Figure 1. On Region Characteristics

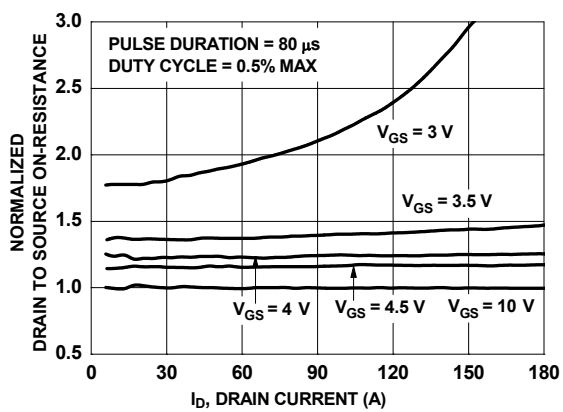


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

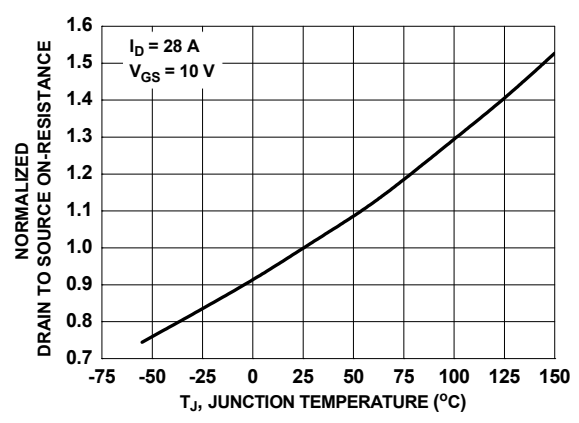


Figure 3. Normalized On Resistance vs. Junction Temperature

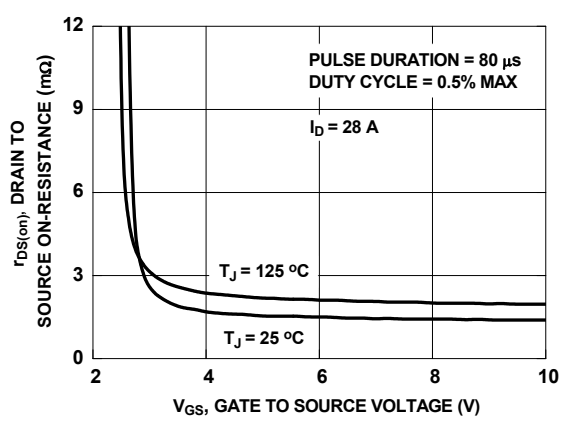


Figure 4. On-Resistance vs. Gate to Source Voltage

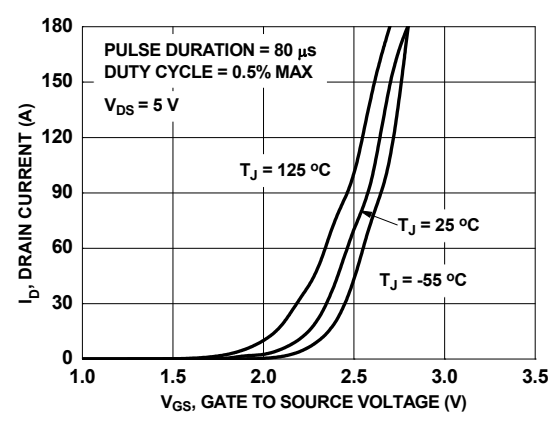


Figure 5. Transfer Characteristics

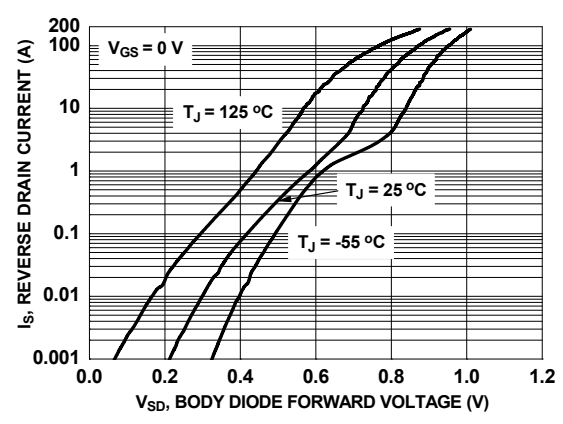


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

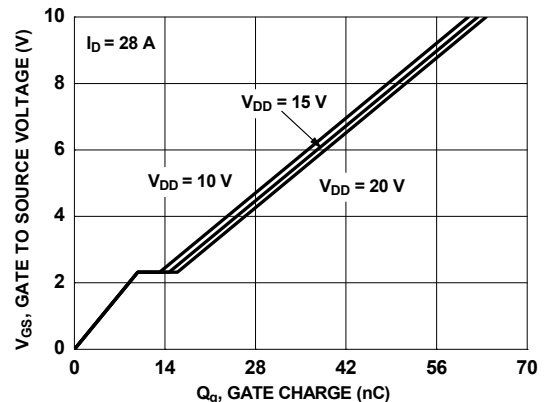


Figure 7. Gate Charge Characteristics

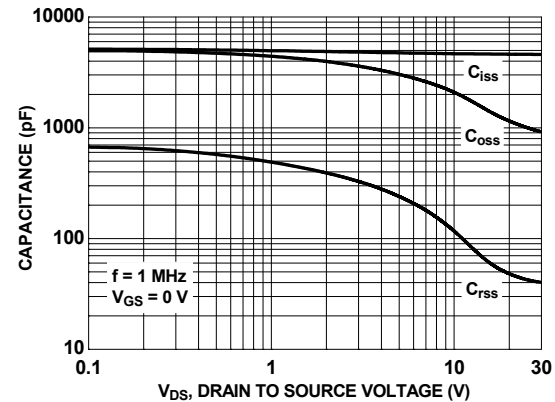


Figure 8. Capacitance vs. Drain to Source Voltage

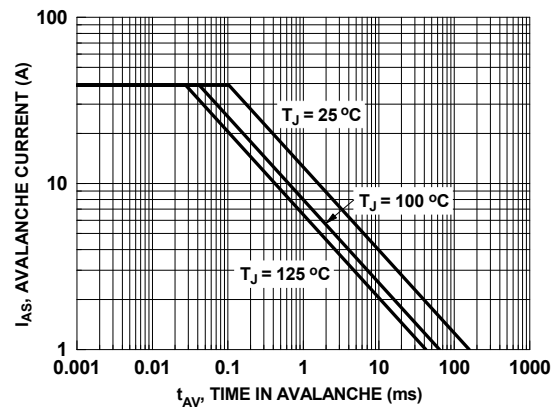


Figure 9. Unclamped Inductive Switching Capability

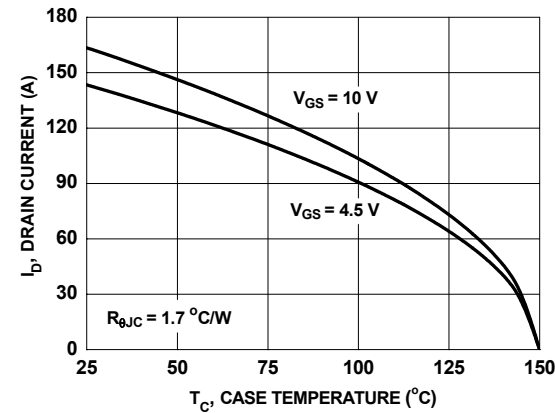


Figure 10. Maximum Continuous Drain Current vs Case Temperature

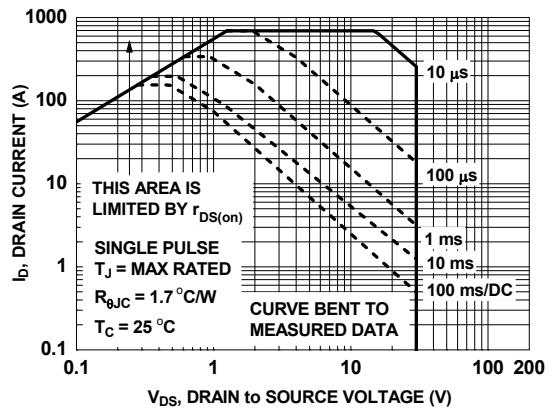


Figure 11. Forward Bias Safe Operating Area

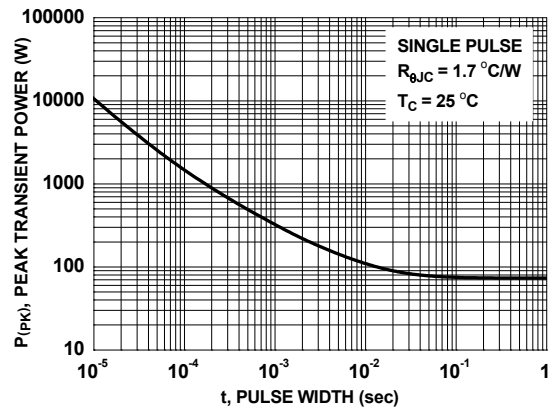


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

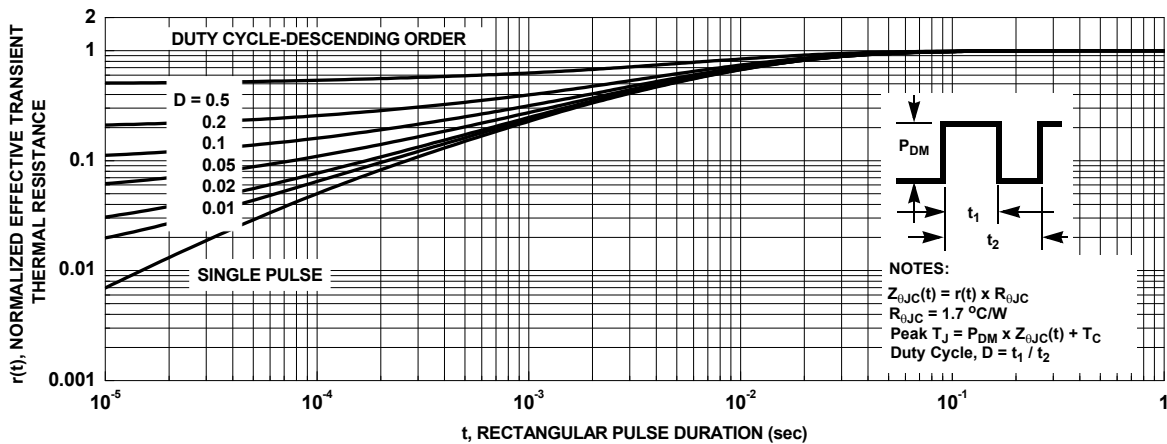


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET[™] Schottky body diode Characteristics

Fairchild's SyncFET[™] process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS2D4N03S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

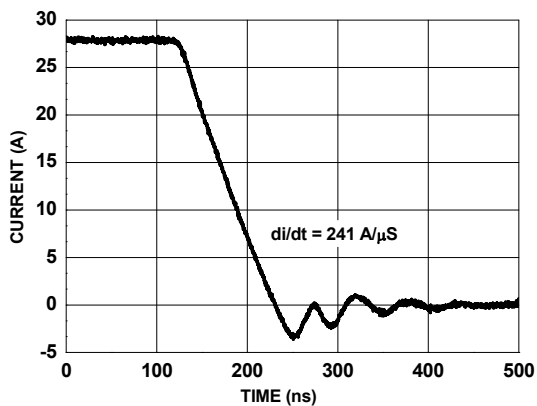


Figure 14. FDMS2D4N03S SyncFET[™] Body Diode Reverse Recovery Characteristic

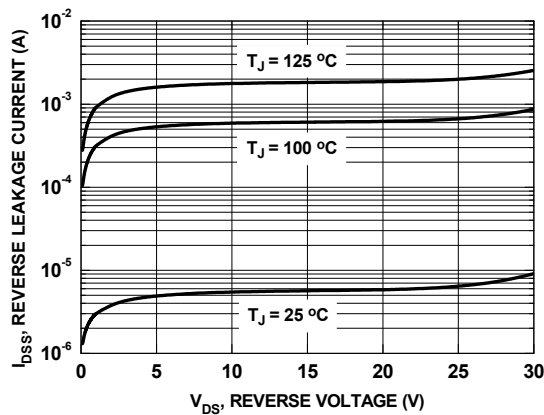
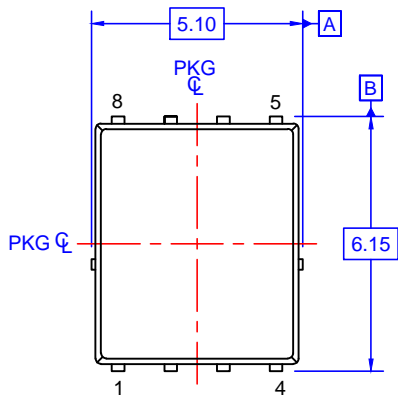
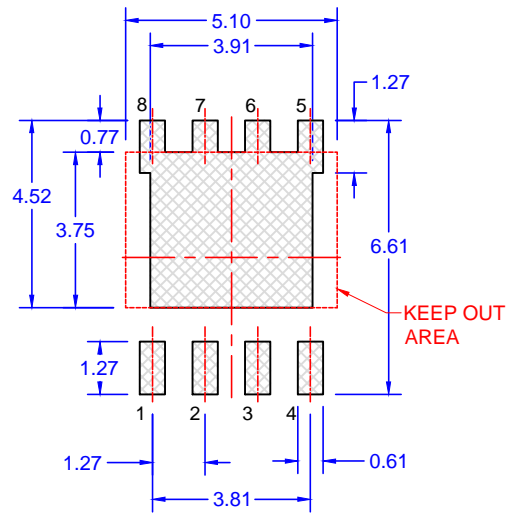


Figure 15. SyncFET[™] Body Diode Reverse Leakage vs. Drain-Source Voltage

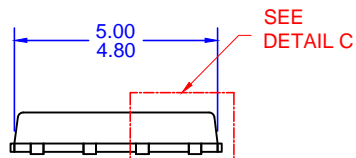
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A



TOP VIEW



LAND PATTERN RECOMMENDATION

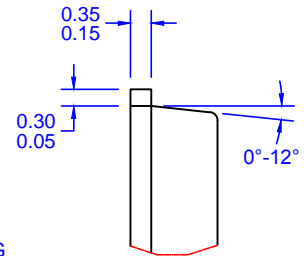


SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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