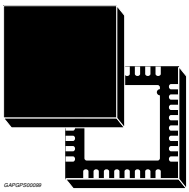
# STA5630

## Low power GPS RF front-end

**Data brief – production data**

## Features

- Integrated LNA
- Low power consumption (< 25 mW)
- 1.8 V supply voltage
- GPS and Galileo compliant
- Minimum external components
- Serial interface
- 3 bits A/D converter
- CMOS 65 nm technology
- Standard QFN-32 package
- Ambient temperature range: -40 °C to +85 °C



**VFQFPN32**

## Description

The STA5630 is a fully integrated RF front-end able to down-convert either the GPS L1 signal from 1575.42 MHz to 4.092 MHz.

The STA5630 embeds high performance LNA minimizing external component count. The chip uses state of the art CMOS 65 nm technology.

A 3-bit ADC converts the IF signal to Sign (SIGN) and Magnitude (MAG0 and MAG1). The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The STA5630 accepts a range of reference clocks (10 to 52 MHz) and generates a 16.368 MHz sampling clock (GPS_CLK) for the baseband. The STA5630 embeds LDO to supply the internal core of the device facilitating requirements to external power supply.

High performance, low power, and cost effective device, the STA5630 is the ideal solution for automotive, cellular and consumer battery powered applications.

**Table 1. Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STA5630TR | STA5630 | VFQFPN32 | Tape and reel |
| STA5630ATR (1) | STA5630A | VFQFPN32 | Tape and reel |

1. Automotive Grade.

# Contents

# 1 Applications

Three main applications cases are considered and described hereafter.

The first uses a passive antenna and only a single RF SAW in front of the internal LNA. It targets low cost and medium performance applications. In this case LNA is ON and RFA could be set at minimum gain if heavy blocker signals are present.

The second uses a passive antenna and two RF SAWs. It maximizes the performances in presence of severe blockers. In this case LNA is ON and RFA is set at maximum gain.

The third case uses an active antenna. This solution targets applications where the GPS antenna is far from the RF front-end. In this case the signal can be fed into either LNA or RFA input depending on the application conditions.

STA5630 is suitable for baseband requiring 16.368/4.092 clock/RF interface and one, two or three bits samples. It accepts reference clocks (TCXO) in the range of 10-52 MHz and delivers a TCXO buffered copy to the baseband.

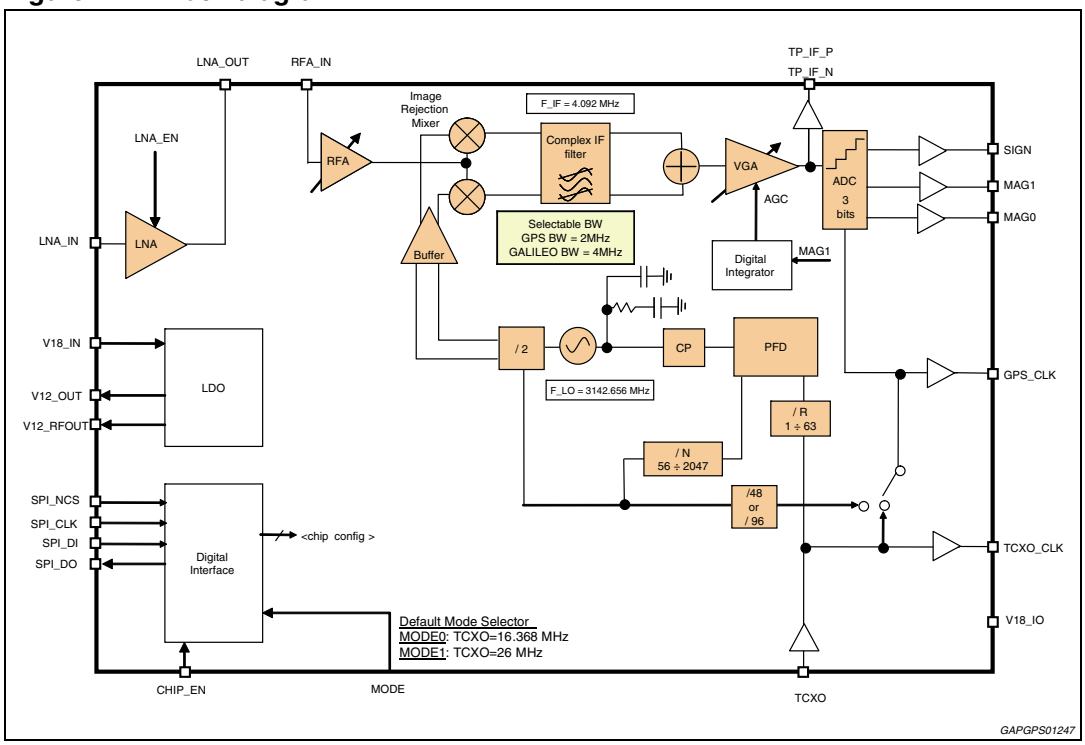
The STA5630 has two default modes selectable by an external pin (MODE):

- MODE 0: the chip is configured to use 16.368 MHz as reference frequency,
- MODE 1: the chip is configured to use 26 MHz as reference frequency.

Other modes are programmed through the serial interface

## 1.1 Block diagram

**Figure 1. Block diagram**



# 2 Pin description

**Table 2. Pin list description**

| Pin # | Pin name | Description | Type |
|---|---|---|---|
| 1 | TP_IF_P | RF/IF receiver chain test positive output | Analog output |
| 2 | V12_RFA | RF amplifier (RFA) power supply (1.2V) | Supply pin |
| 3 | RFA_IN | RFA input, DC coupled | Analog input |
| 4 | V12_IF | IF section power supply (1.2V) | Supply pin |
| 5 | V12_OUT | LDO IF/DIG output. Power supply (1.2V) delivered for IF/ADC/DIG_TCXO/VCO/VDD_IO VCC | Output |
| 6 | V12_RF_OUT | LDO RF output: Power supply (1.2V) delivered for LNA/RFA/MIXER VCC | Output |
| 7 | V18_IN | LDOs power supply (1.8V) | Supply pin |
| 8 | V12_LNA | Low noise amplifier (LNA) power supply (1.2V) | Supply pin |
| 9 | LNA_OUT | LNA output | Analog output |
| 10 | GND | Ground | Ground |
| 11 | LNA_IN | LNA input, DC coupled | Analog input |
| 12 | GND | Ground | Ground |
| 13 | CHIP_EN | Chip Enable | Digital input |
| 14 | MODE | Power-On Default Configuration Selector | Digital input |
| 15 | V18_IO | I/Os power supply (1.8V) | Supply pin |
| 16 | GPS_CLK | GPS clock (16.368MHz) | Digital output |
| 17 | MAG0 | Mag0 data (Last significant bit) | Digital output |
| 18 | MAG1 | Mag1 data | Digital output |
| 19 | SIGN | Sign data (most significant bit) | Digital output |
| 20 | SPI_CLK | Serial Parallel Interface Clock | Digital input |
| 21 | SPI_NCS | Serial Parallel Interface Chip Select (Active Low - 1.8V domain) | Digital input |
| 22 | SPI_DI | Serial Parallel Interface Data Input | Digital input |
| 23 | SPI_DO | Serial Parallel Interface Data Output | Digital output |
| 24 | TCXO_CLK | TCXO Buffered Output | Digital output |
| 25 | V12_IO | Power supply for I/Os digital section (1.2V) | Supply pin |
| 26 | GND_IO | I/Os Ground | Ground |
| 27 | TCXO_IN | TCXO Input, DC coupled | Analog input |
| 28 | V12_DIG | Digital section and TCXO buffer input power supply (1.2V) | Supply pin |
| 29 | V12_VCO | VCO power supply (1.2V) | Supply pin |
| 30 | V12_ADC | ADC section power supply (1.2V) | Supply pin |
| 31 | V12_MIX | Mixer power supply (1.2V) | Supply pin |
| 32 | TP_IF_N | RF/IF receiver chain test negative output | Analog output |
| EP | GND | Ground | Ground |

**Figure 2. Pin connection diagram (bottom view)**

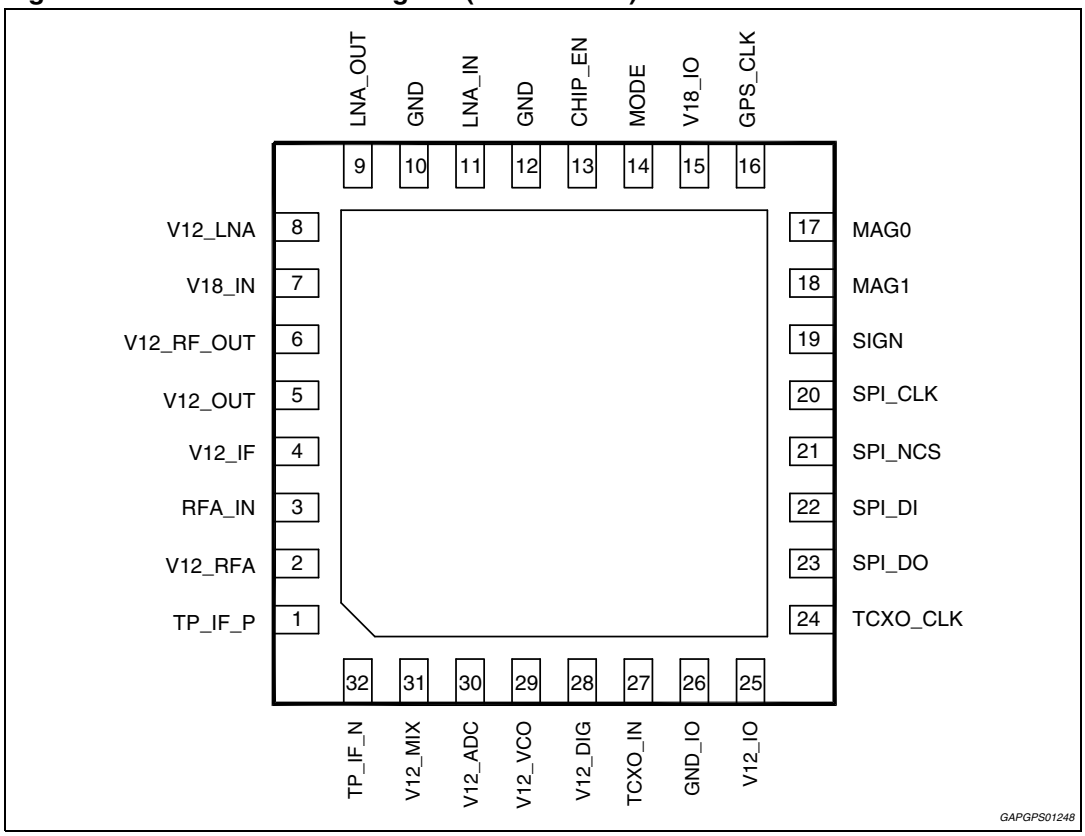


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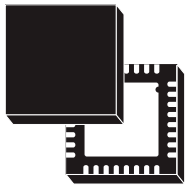
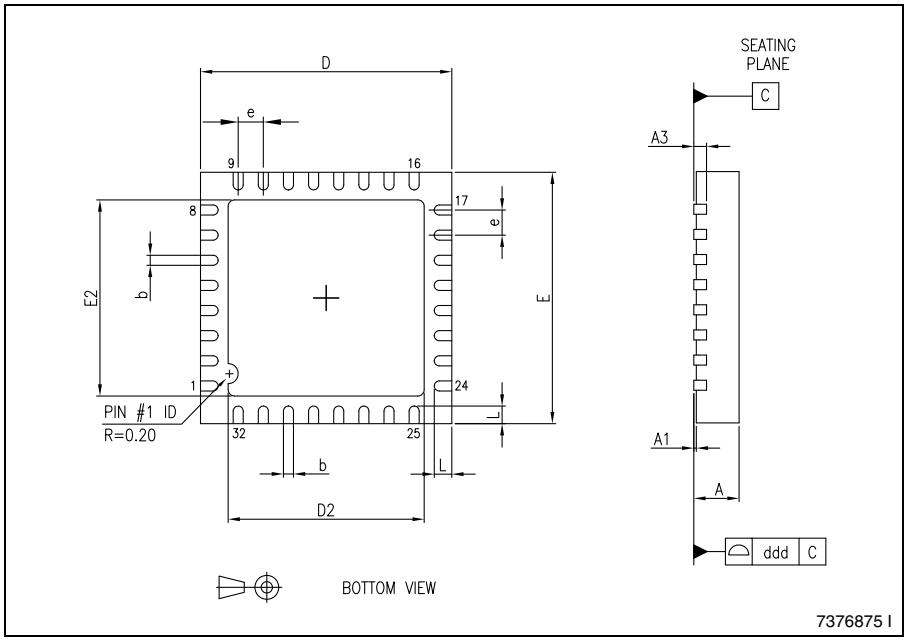
**Figure 3. VFQFPN32 (5x5x1.0 mm) mechanical data and package dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A3 | | 0.200 | | | 0.0079 | |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E2 | 3.500 | 3.600 | 3.700 | 0.1378 | 0.1417 | 0.1457 |
| e | | 0.500 | | | 0.0197 | |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | | | 0.050 | | | 0.0020 |

**OUTLINE AND MECHANICAL DATA**



**VFQFPN32 (5x5x1.0mm)**
**V**ery **F**ine **Q**uad **F**lat **P**ackage **N**o lead




GAPGPS00105

# 4 Revision history

Table 3. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 22-Jul-2009 | 1 | Initial release. |
| 03-Mar-2010 | 2 | Updated: *Features on page 1*;<br>Updated: *Figure 1: Block diagram on page 3*;<br>Updated: *Section 2: Pin description on page 4*. |
| 27-Jun-2012 | 3 | Updated: *Features on page 1* and *Table 1: Device summary on page 1*. |
| 17-Sep-2013 | 4 | Updated Disclaimer |

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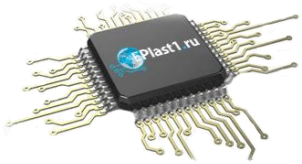


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