LM79LXXAC Series 3-Terminal Negative Regulators

Check for Samples: LM79L05, LM79L05AC, LM79L12, LM79L12AC, LM79L15, LM79L15AC

FEATURES

- **Preset Output Voltage Error is Less than ±5% Overload, Line and Temperature**
- **Specified at an Output Current of 100mA**
- **Easily Compensated with a Small 0.1μF Output**
  - **Capacitor**
- **Internal Short-Circuit, Thermal and Safe Operating Area Protection**
- **Easily Adjustable to Higher Output Voltages**
- **Maximum Line Regulation Less than 0.07% V_{OUT}/V**
- **Maximum Load Regulation Less than 0.01% V_{OUT}/mA**
- **See AN-1112 (SNVA009) for DSBGA Considerations**

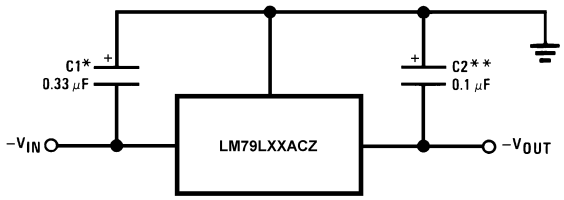
DESCRIPTION

The LM79LXXAC series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V with output current capabilities in excess of 100mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, when combined with a minimum output capacitor of 0.1μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead TO package, the 8-lead SOIC package, and the 6-Bump DSBGA package.

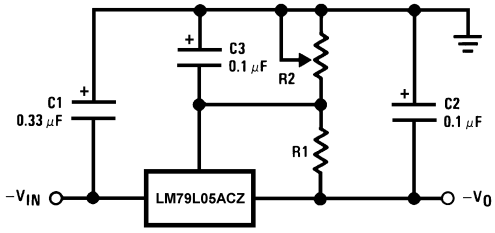
For output voltages other than the pre-set -5V, -12V and -15V, the LM137L series provides an adjustable output voltage range from -1.2V to -47V.

Typical Applications



*Required if the regulator is located far from the power supply filter. A 1μF aluminum electrolytic may be substituted.
**Required for stability. A 1μF aluminum electrolytic may be substituted.

Figure 1. Fixed Output Regulator



$-V_0 = -5V - (5V/R1 + I_Q) \cdot R2$,
$5V/R1 > 3\ I_Q$

Figure 2. Adjustable Output Regulator

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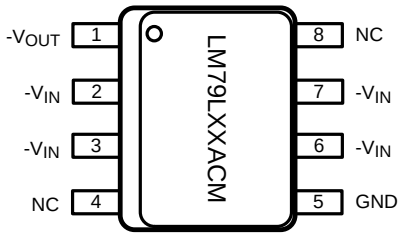
Connection Diagram



Pins labeled 'NC' on LM79LXXACM 8-Lead SOIC (pin 4 and pin 8) are Open, no internal connection.

Figure 3. 8-Lead SOIC Narrow (D)
Top View

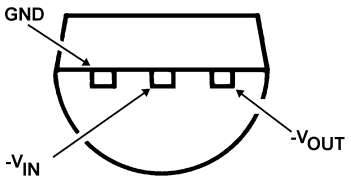


Figure 4. 3–Lead TO (LP)
Bottom View

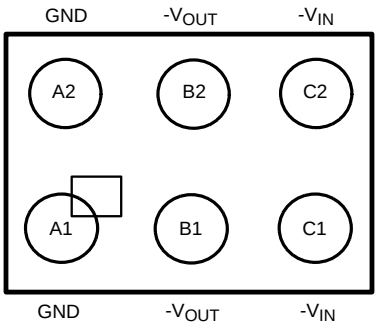


Figure 5. 6-Bump DSBGA
Top View (Bump Side Down)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2]

Input Voltage	
V_O = −5V, −12V, −15V	−35V
Internal Power Dissipation [3]	Internally Limited
Operating Temperature Range	0°C to +70°C
Maximum Junction Temperature	+125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Thermal resistance of TO-3 (LP) package is 60°C/W θ_{JC}, 232°C/W θ_{JA} at still air, and 88°C/W at 400 ft/min of air. The θ_{JA} of the LM78LXX in the 6-Bump DSBGA package is 114°C/W when mounted on a 4-Layer JEDEC test board (JESD 51-7). The θ_{JA} of the LM78LXX in the SOIC-8 (D) package is 180°C/W in still air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

Electrical Characteristics [1]

T_A = 0°C to +70°C unless otherwise noted.

Output Voltage			−5V			−12V			−15V			
Input Voltage (unless otherwise noted)			−10V			−17V			−20V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
V_O	Output Voltage	T_J = 25°C, I_O = 100mA	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	V
		1mA ≤ I_O ≤ 100mA	−5.25		−4.75	−12.6		−11.4	−15.75		−14.25	
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(−20 ≤ V_{IN} ≤ −7.5)			(−27 ≤ V_{IN} ≤ −14.8)			(−30 ≤ V_{IN} ≤ −18)			
		1mA ≤ I_O ≤ 40mA	−5.25		−4.75	−12.6		−11.4	−15.75		−14.25	
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(−20 ≤ V_{IN} ≤ −7)			(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)			
ΔV_O	Line Regulation	T_J = 25°C, I_O = 100mA			60			45			45	mV
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(−20 ≤ V_{IN} ≤ −7.3)			(−27 ≤ V_{IN} ≤ −14.6)			(−30 ≤ V_{IN} ≤ −17.7)			V
		T_J = 25°C, I_O = 40mA			60			45			45	mV
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(−20 ≤ V_{IN} ≤ −7)			(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)			V
ΔV_O	Load Regulation	T_J = 25°C			50			100			125	mV
		1mA ≤ I_O ≤ 100mA										
ΔV_O	Long Term Stability	I_O = 100mA		20			48			60		mV/khrs
I_Q	Quiescent Current	I_O = 100mA		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	1mA ≤ I_O ≤ 100mA			0.3			0.3			0.3	mA
		1mA ≤ I_O ≤ 40mA			0.1			0.1			0.1	
		I_O = 100mA			0.25			0.25			0.25	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}	(−20 ≤ V_{IN} ≤ −7.5)			(−27 ≤ V_{IN} ≤ −14.8)			(−30 ≤ V_{IN} ≤ −18)			V
V_n	Output Noise Voltage	T_J = 25°C, I_O = 100mA f = 10Hz − 10kHz		40			96			120		μV
$\Delta V_{IN}/\Delta V_O$	Ripple Rejection	T_J = 25°C, I_O = 100mA f = 120Hz	50			52			50			dB
	Input Voltage Required to Maintain Line Regulation	T_J = 25°C, I_O = 100mA			−7.3			−14.6			−17.7	V
		I_O = 40mA			−7.0			−14.5			−17.5	V

(1) To ensure constant junction temperature, low duty cycle pulse testing is used.

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Typical Performance Characteristics

Maximum Average Power Dissipation (TO)

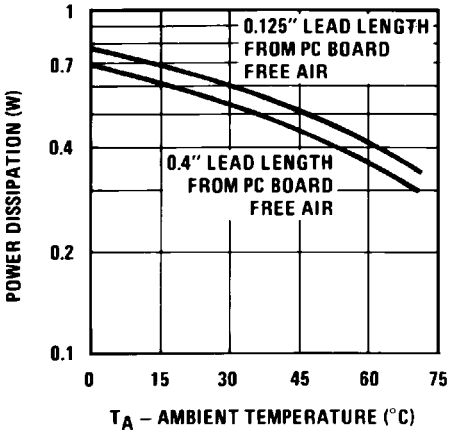

Figure 6.

Peak Output Current

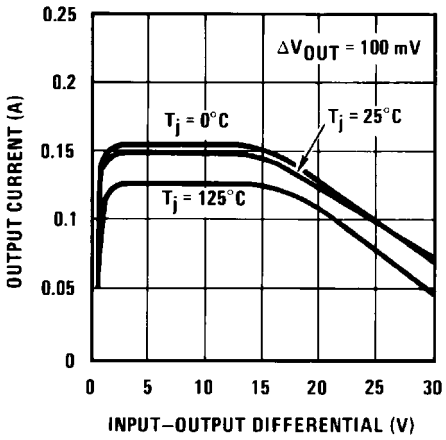

Figure 7.

Short Circuit Output Current

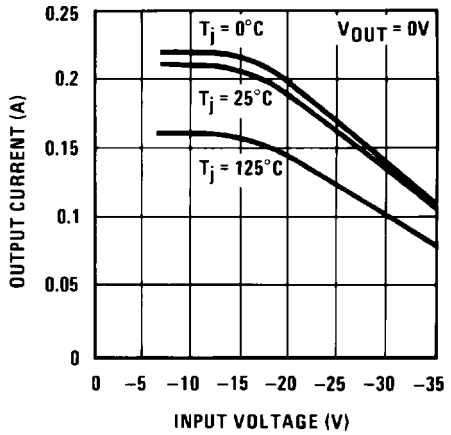

Figure 8.

Dropout Voltage

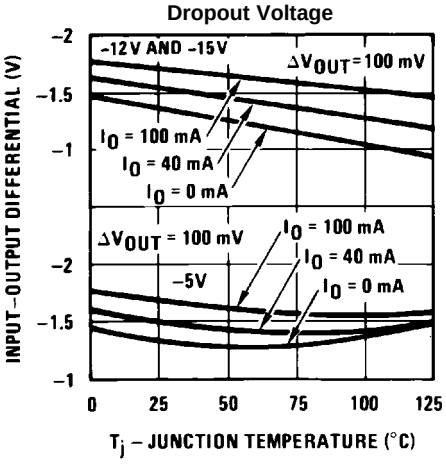

Figure 9.

Ripple Rejection

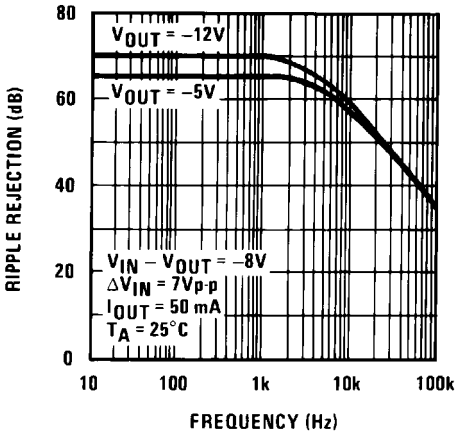

Figure 10.

Output Voltage vs. Temperature (Normalized to 1V @ 25°C)

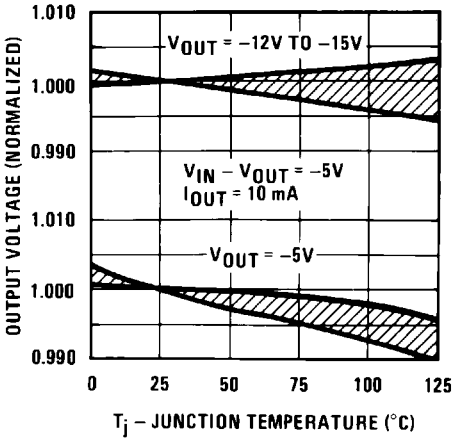

Figure 11.

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Typical Performance Characteristics (continued)

Quiescent Current

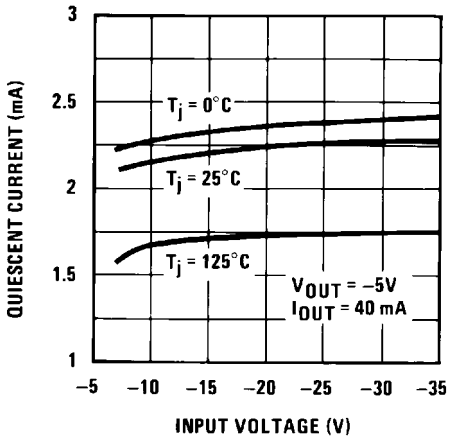

Figure 12.

Output Impedance

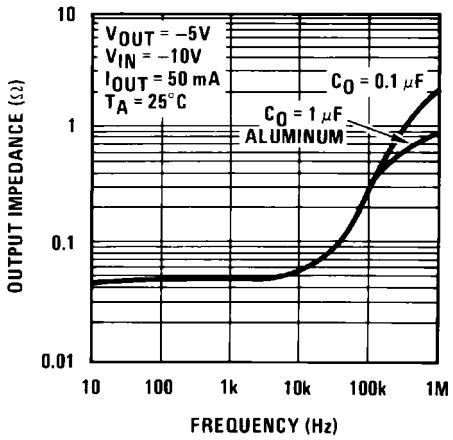

Figure 13.

TYPICAL APPLICATIONS

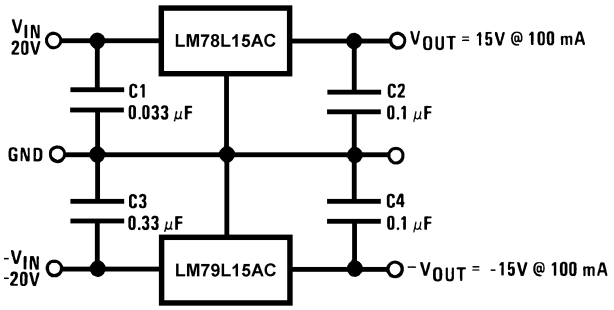

Figure 14. ±15V, 100mA Dual Power Supply

Schematic Diagrams

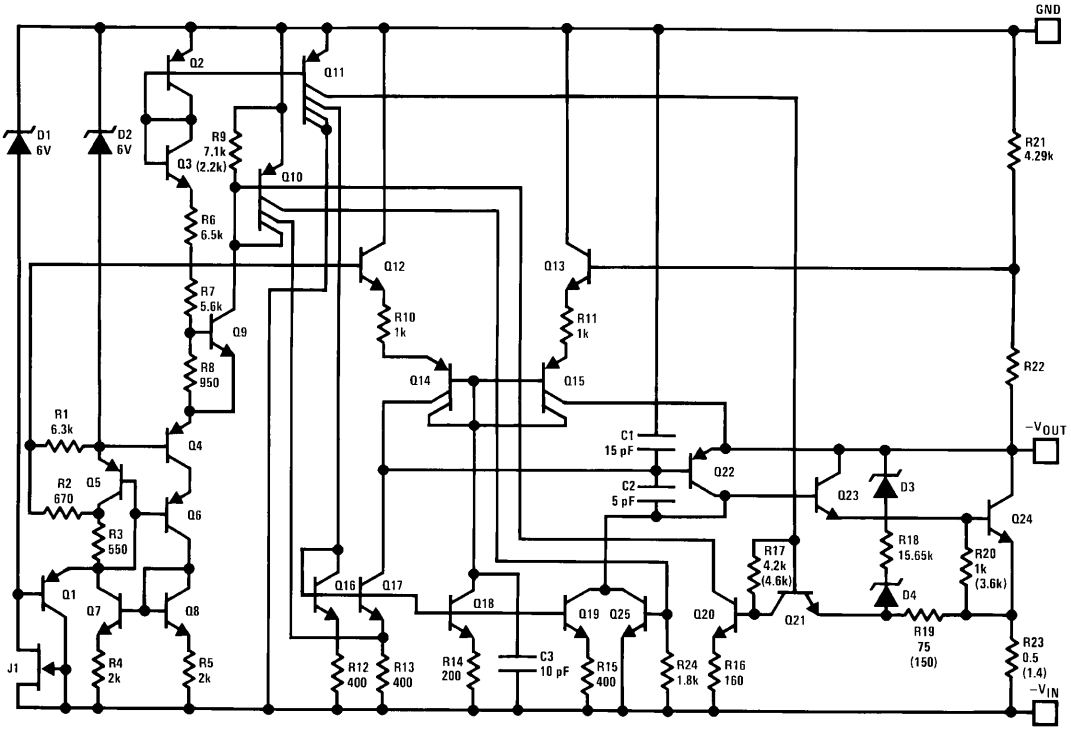

Figure 15. −5V Schematic Diagram

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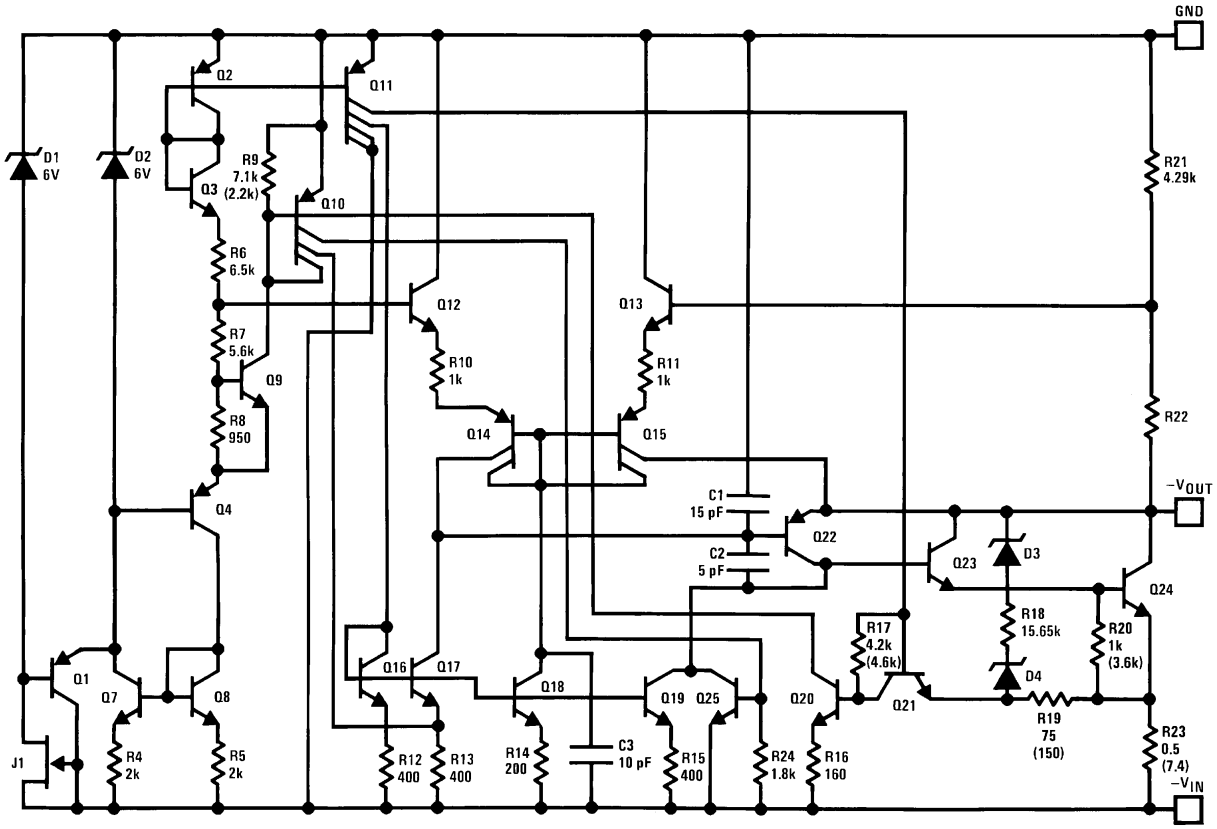

Figure 16. −12V and −15V Schematic Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
1.004.022	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM79L 05ACM	Samples
LM79L05ACM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM79L 05ACM	Samples
LM79L05ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 05ACM	Samples
LM79L05ACMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM79L 05ACM	Samples
LM79L05ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 05ACM	Samples
LM79L05ACTL/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 70	P B	Samples
LM79L05ACTLX/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	0 to 70	P B	Samples
LM79L05ACZ/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SNCU	Level-1-NA-UNLIM		320L 79L05	Samples
LM79L05ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	SNCU	Level-1-NA-UNLIM	0 to 70	320L 79L05	Samples
LM79L12ACM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM79L 12ACM	Samples
LM79L12ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 12ACM	Samples
LM79L12ACMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM79L 12ACM	Samples
LM79L12ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 12ACM	Samples
LM79L12ACZ/LFT4	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SNCU	Level-1-NA-UNLIM		320L 79L12	Samples
LM79L12ACZ/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	SNCU	Level-1-NA-UNLIM		320L 79L12	Samples
LM79L12ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	SNCU	Level-1-NA-UNLIM	0 to 70	320L 79L12	Samples
LM79L15ACM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM79L 15ACM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM79L15ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 15ACM	Samples
LM79L15ACMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM79L 15ACM	Samples
LM79L15ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM79L 15ACM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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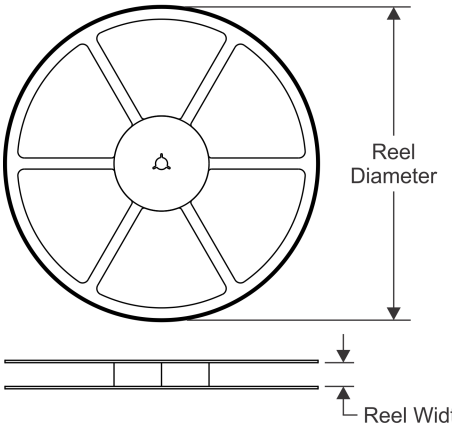
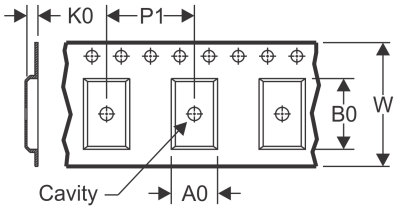
TAPE AND REEL INFORMATION

REEL DIMENSIONS

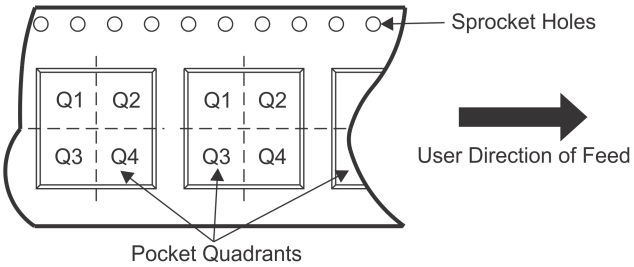


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

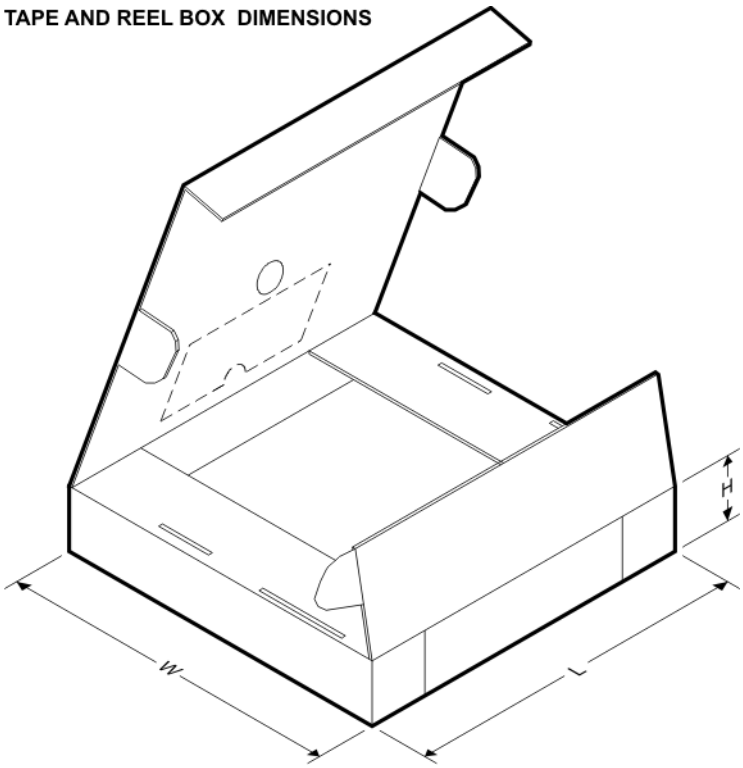
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM79L05ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM79L05ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM79L05ACTL/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.09	1.88	0.76	4.0	8.0	Q1
LM79L05ACTLX/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.09	1.88	0.76	4.0	8.0	Q1
LM79L12ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM79L12ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM79L15ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM79L15ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

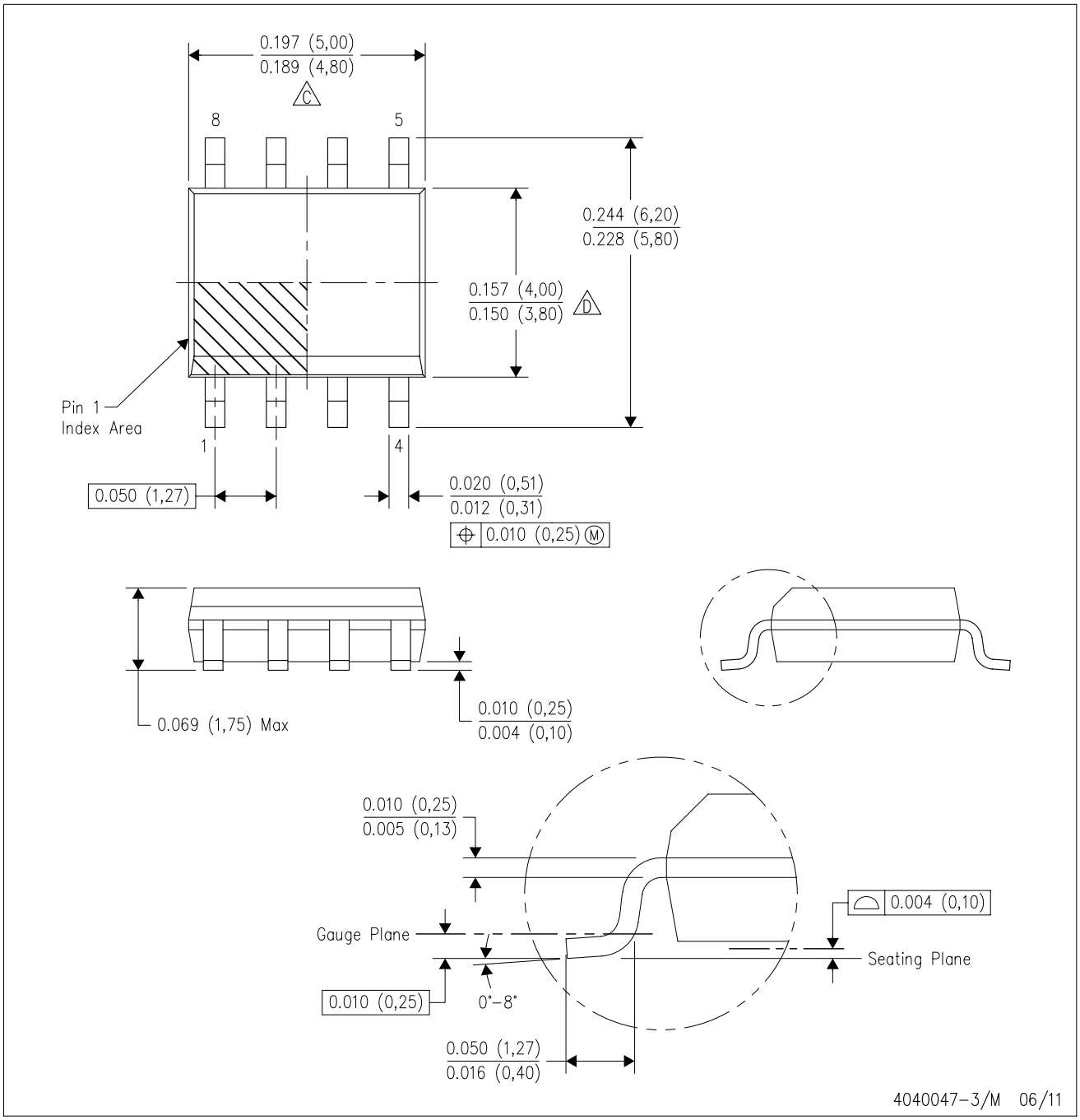
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

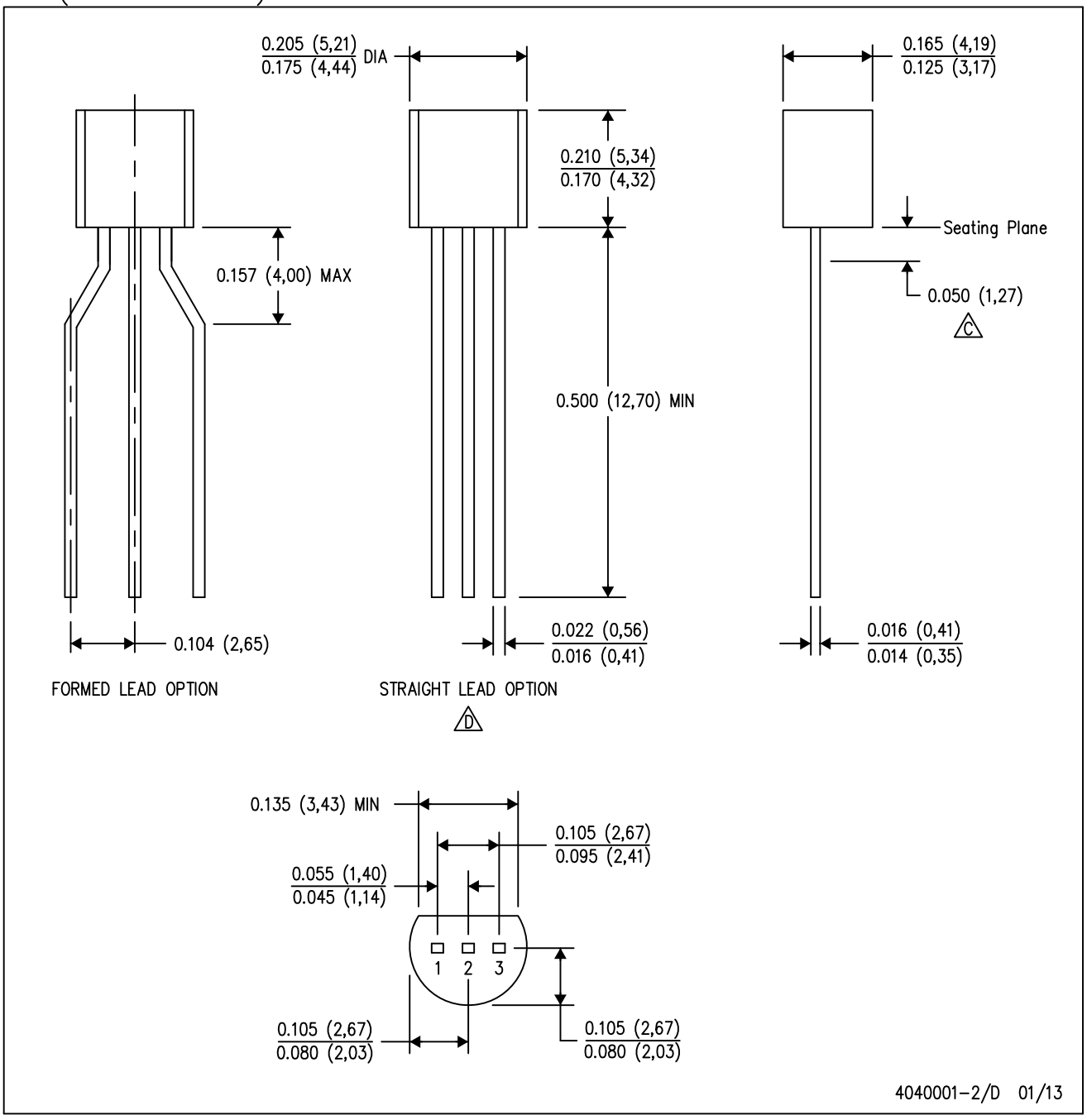
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM79L05ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM79L05ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM79L05ACTL/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LM79L05ACTLX/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LM79L12ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM79L12ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM79L15ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM79L15ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



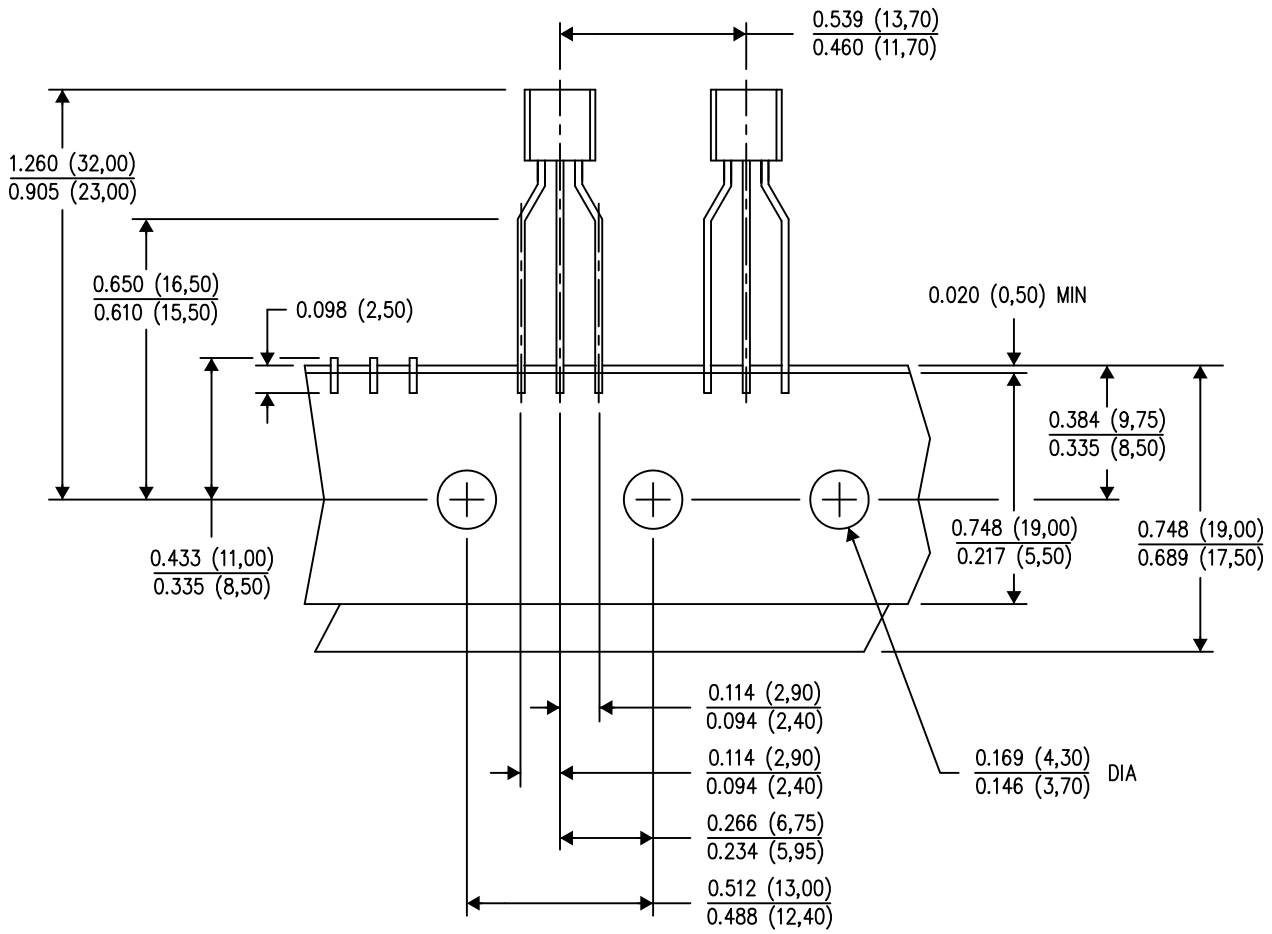
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO–226 Variation AA (TO–226 replaces TO–92).
E. Shipping Method:
Straight lead option available in either bulk pack or tape & reel.
Formed lead option available in tape & reel or ammo pack.
Specific products can be offered in limited combinations of shipping mediums and lead options.
Consult product folder for more information on available options.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE

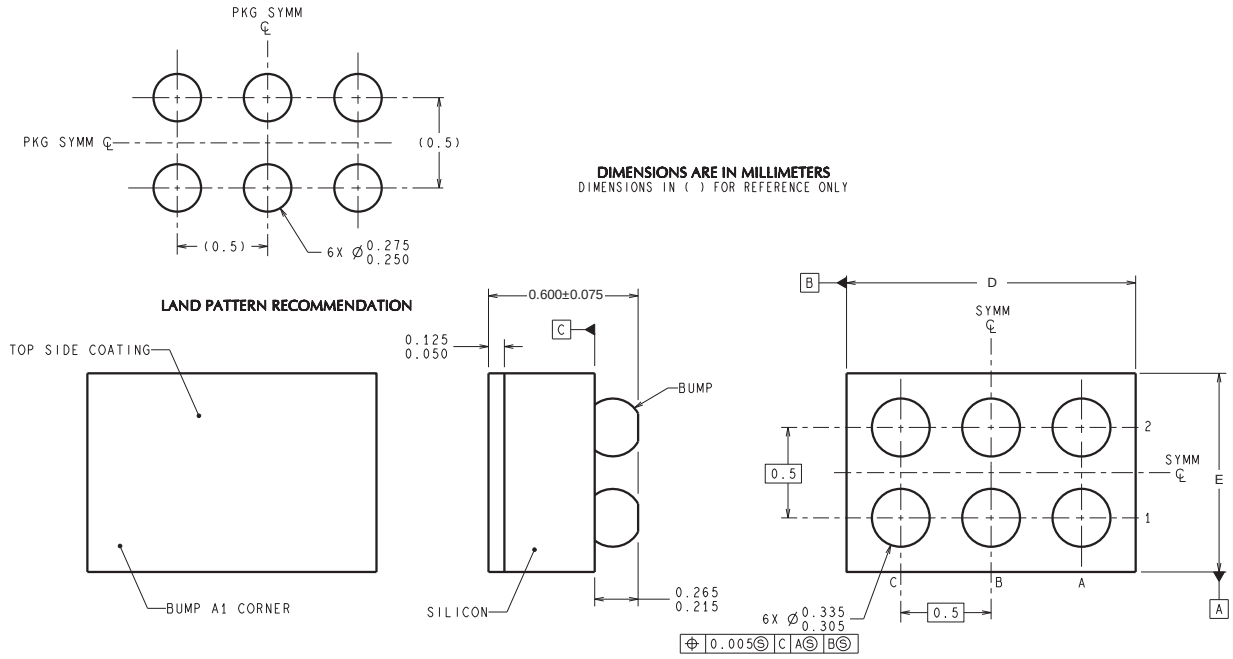


TAPE & REEL

4040001–3/D 01/13

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Formed Lead Option package.

YZR0006



TLA06XXX (Rev C)

D: Max = 1.845 mm, Min =1.784 mm

E: Max = 1.057 mm, Min =0.996 mm

4215044/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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