# LC87F17C8A

**CMOS LSI**

## 8-bit Microcontroller with USB Full-Speed Host/Device Controller

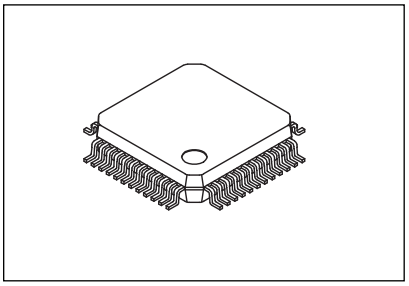
### 128K-byte Flash ROM / 8192-byte RAM / 48-pin

ON Semiconductor®

www.onsemi.com

### Feature

- USB 2.0 Full Speed Host/Device Controller × 2 ports
- Digital Audio Interface
- Infrared Remote Control Receiver
- 12-bit ADC × 12 channels
- USB Voltage Regulator Integrated
- Power-ON Reset/Low-Voltage Detect Reset



SQFP48(7X7)

### Function Descriptions

1) Ports
   - I/O ports 31
   - USB ports 4 (UAD+, UAD–, UBD+, UBD–)
   - Power supply pins 6 (VSS1 to 3, VDD1 to 3)

2) Timers × 7 channels
   - Timer 0 : 16-bit timer/counter with 2 capture registers.
   - Timer 1 : 16-bit timer/counter that supports PWM/toggle output
   - Timer 4 : 8-bit timer with a 6-bit prescaler
   - Timer 5 : 8-bit timer with a 6-bit prescaler
   - Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
   - Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
   - Base timer for Watch (32.768kHz crystal oscillation)

3) SIO × 5 channels
   - SIO0 : Synchronous serial interface
     Automatic continuous data transmission
   - SIO1 : 8-bit asynchronous/synchronous serial interface
   - SIO4 : CRC16 calculator circuit built in
   - SMIIC0 : Single-master $I^2C$/8-bit synchronous SIO
   - SMIIC1 : Single-master $I^2C$/8-bit synchronous SIO

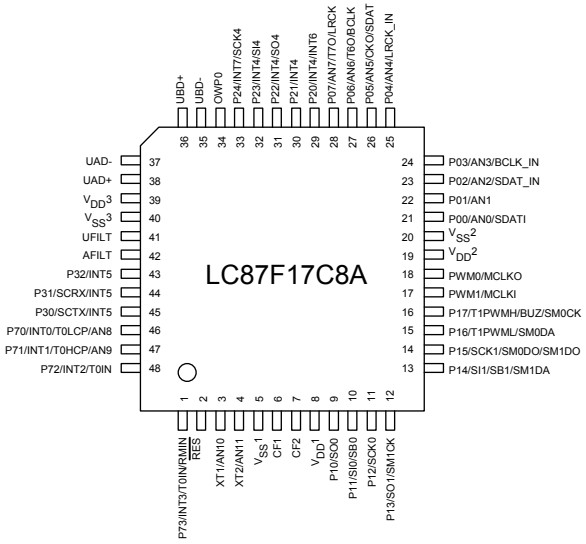
4) Full Duplex UART
   - SCUART2 : 8-level receive FIFO buffer

5) PWM: Variable frequency 12-bit PWM × 2 channels

6) USB Controller
   - Host : Supports Full-Speed and Low-Speed
   - Device : Supports up to 9 endpoints. Full-Speed.

7) Digital Audio Interface
   - fs : 8kHz/11.025kHz/12kHz/16kHz/22.05kHz/24kHz/32kHz/44.1kHz/48kHz/96kHz
   - Left justified/right justified/ $I^2S$ format selectable

8) Infrared Remote Controller Receiver
   - Supports data encoding systems such as PPM and Manchester encoding.




Pin Assignment
(Top view)

### Application

- iPod/iPhone Docking Station

* iPod and iPhone are trademarks of Apple Inc., registered in the U.S. and other countries.

* This product is licensed from Silicon Storage Technology, Inc. (USA).

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 36 of this data sheet.

■ Ports

| | |
|---|---|
| • I/O ports | 31 (P00 to P07, P10 to P17, P20 to P24, P30 to P32, P70 to P73, PWM0, PWM1, XT2) |
| • USB ports | 4 (UAD+, UAD–, UBD+, UBD–) |
| • Dedicated oscillator ports | 2 (CF1, CF2) |
| • Input-only port (also used for the oscillator) | 1 (XT1) |
| • PLL filter pins | 2 (UFILT, AFILT) |
| • Reset pin | 1 (RES) |
| • Debugger-dedicated pin | 1 (OWP0) |
| • Power supply pins | 6 ($V_{SS}$1 to 3, $V_{DD}$1 to 3) |

■ Timers

- Timer 0 : 16-bit timer/counter with 2 capture registers
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3 : 16-bit counter (with two 16-bit capture registers)
- Timer 1 : 16-bit timer/counter that supports PWM/toggle output
  - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter with an 8-bit prescaler (with toggle output)
  - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler (with toggle output) (Toggle output also possible from low-order 8 bits.)
  - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle output) (Low-order 8 bits can be used as a PWM output.)
- Timer 4 : 8-bit timer with a 6-bit prescaler
- Timer 5 : 8-bit timer with a 6-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  - <1> The clock can be selected from among a subclock (32.768 kHz crystal oscillator), low-speed RC oscillator clock, system clock, and timer 0 prescaler output.
  - <2> Interrupts programmable in 5 different time schemes.

■ Serial Interfaces

- SIO0 : Synchronous serial interface
  - <1> LSB first/MSB first selectable
  - <2> Transfer clock cycle : 4/3 to 512/3 tCYC
  - <3> Continuous automatic data transmission (1 to 256 bits can be specified in 1-bit units) (Suspension and resumption of data transfer possible in 1-byte units)
- SIO1 : 8-bit asynchronous/synchronous serial interface
  - Mode 0 : Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clock)
  - Mode 1 : Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
  - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clock)
  - Mode 3 : Bus mode 2 (start detection, 8 data bits, stop detection)
- SIO4 : Synchronous serial interface
  - <1> LSB first/MSB first selectable
  - <2> Transfer clock cycle : 4/3 to 1020/3 tCYC
  - <3> Continuous automatic data transmission (1 to 8192 bytes can be specified in 1-byte units) (Suspension and resumption of data transmission possible in 1-byte units or in word units)
  - <4> Clock polarity can be selected.
  - <5> CRC16 calculator circuit built- in
- SMIIC0 : Single-master $I^2C$/8-bit synchronous SIO
  - Mode 0 : Communication in single-master mode.
  - Mode 1 : 8-bit synchronous serial I/O (data MSB first)

• SMIIC1 : Single-master $I^2C$/8-bit synchronous SIO
Mode 0 : Communication in single-master mode.
Mode 1 : 8-bit synchronous serial I/O (data MSB first)

■ Full Duplex UART

• SCUART2
<1> Data length : 7/8 bits selectable
<2> Stop bits : 1/2 bits selectable
<3> Parity bits : None/even parity/odd parity selectable
<4> Baudrate : 8/3 to 8192/3 tCYC
<5> LSB first/MSB first mode selectable
<6> Capable of Smart card interface
<7> 8-level receive FIFO buffer

■16-bit Cyclic Redundancy Check (CRC) Calculator

<1> User-programmable CRC polynomial equation
<2> 1 to 256 bytes can be specified
<3> LSB first/MSB first selectable

■ AD Converter: 12 bits × 12 channels

■ PWM: Variable frequency 12-bit PWM × 2 channels

■ Infrared Remote Control Receiver Circuit

<1> Noise rejection function (noise filter time constant: Approx. 120μs when the 32.768 kHz crystal oscillator is selected as the reference clock)
<2> Supports data encoding systems such as PPM (Pulse Position Modulation) and Manchester encoding.
<3> X'tal HOLD mode release function

■ USB Interface

• Host Controller × 2 ports
<1> Supports Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) operation.
<2> Supports four transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer).

• Device Controller
<1> Supports Full-Speed operation.
<2> Supports up to 9 endpoints

| Endpoint | | EP0 | EP1 | EP2 | EP3 | EP4 | EP5 | EP6 | EP7 | EP8 |
|---|---|---|---|---|---|---|---|---|---|---|
| Transfer Type | Control | ○ | - | - | - | - | - | - | - | - |
| | Bulk | - | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | Interrupt | - | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| | Isochronous | - | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Max. payload | | 64 | 64 | 64 | 64 | 64 | 64 | 64 | 1023 | 1023 |

■ Audio Interface

<1> Sampling frequencies (fs) : 8 kHz/11.025 kHz/12 kHz/16 kHz/22.05 kHz/24 kHz/32 kHz/44.1 kHz/48 kHz/96kHz
<2> Master clock : 256 fs/384 fs
<3> Bit clock : 48 fs/64 fs
<4> Data bit length : 16 bits/18 bits/20 bits/24 bits
<5> LSB first/MSB first selectable.
<6> Left justified/right justified/$I^2S$ format selectable

■ Watchdog Timer

• Internal counter watchdog timer
<1> Capable of generating an internal reset on an overflow of the timer running on the low-speed RC oscillator clock, or subclock.
<2> Operation in HALT/HOLD mode can be selected from among “continue count operation,” “suspend operation,” and “retain the count value.”

■ Clock Output Function

<1> Can output a clock with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillator clock selected as the system clock.
<2> Can output the source oscillator clock for the subclock.

■ Interrupts

- 49 sources, 10 vectors
  <1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt level is not accepted.
  <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address is given priority.

| No. | Vector | Level | Interrupt Source |
|---|---|---|---|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4/UHC-A bus active/UHC-B bus active/USB bus active/remote control receive |
| 4 | 0001BH | H or L | INT3/INT5/base timer/AIF asynchronous counter |
| 5 | 00023H | H or L | T0H/INT6/UHC-A device connected, disconnected, resumed/SMIIC1 |
| 6 | 0002BH | H or L | T1L/T1H/INT7/AIF start/SMIIC0/UHC-B device connected, disconnected, resumed/ AIF FIFO empty |
| 7 | 00033H | H or L | SIO0/USB bus reset/USB suspend/SCUART2 receive completed/SCUART2 receive FIFO full |
| 8 | 0003BH | H or L | SIO1/SIO4/USB endpoint/USB-SOF/ SCUART2 buffer empty/SCUART2 transmission completed/AIF end |
| 9 | 00043H | H or L | ADC/T6/T7/UHC-ACK/UHC-NAK/UHC error/UHC-STALL |
| 10 | 0004BH | H or L | Port 0/PWM0/PWM1/T4/T5/UHC-SOF/CRC |

- Priority levels X > H > L
- When interrupts of the same level occur at the same time, the interrupt with the lowest vector address is given priority.

■ Subroutine Stack Levels : Up to 4096 levels (The stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillator Circuit and PLL

- Medium-speed RC oscillator circuit (internal): For system clock (approx. 1 MHz)
- Low-speed RC oscillator circuit (internal) : For system clock, timer, and watchdog timer (approx. 30 kHz)
- CF oscillator circuit : For system clock
- Crystal oscillator circuit : For system clock and time-of-day clock
- PLL circuit (internal) : For USB interface (see Fig. 5) and audio interface (see Fig. 6)

■ Internal Reset Functions

- Power-on reset (POR) function
  <1> POR is activated at power-on.
  <2> POR release voltage can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) by setting options.
- Low voltage detection reset (LVD) function
  <1> LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a threshold level.
  <2> The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, and 4.28V) can be selected by setting options.

■ Standby Function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
  (1) Oscillators do not stop automatically.
  (2) There are three ways of releasing HOLD mode.
  <1> Setting the reset pin to a low level.
  <2> Generating a reset signal by watchdog timer or low-voltage detection
  <3> Occurrence of an interrupt
- HOLD mode : Suspends instruction execution and operation of the peripheral circuits.
  (1) The PLL, CF, RC and crystal oscillators automatically stop operation.
  Note : Low-speed RC oscillator is controlled directly by the watchdog timer and its oscillation in standby mode is also controlled.
  (2) There are five ways of releasing HOLD mode.
  <1> Setting the reset pin to a low level
  <2> Generating a reset signal by the watchdog timer or low-voltage detection
  <3> Establishing an interrupt source at one of INT0, INT1, INT2, INT4, and INT5 pins
  * INT0 and INT1 HOLD mode release is available only when level detection is configured.
  <4> Establishing an interrupt source at port 0
  <5> Establishing an bus active interrupt source in the USB host control circuit
- X'tal HOLD mode : Suspends instruction execution and the operation of the peripheral circuits except the base timer and infrared remote control receiver circuit.
  (1) The PLL, CF and RC oscillators automatically stop operation.
  Note : Low-speed RC oscillator is controlled directly by the watchdog timer and its oscillation in standby mode is also controlled.
  Note : The low-speed RC oscillator retains the state that is established on entry into X'tal HOLD mode if the base timer is running with the low-speed RC oscillator selected as the base timer input clock source.
  (2) The state of crystal oscillator established when the X'tal HOLD mode is entered is retained.
  (3) There are seven ways of releasing X'tal HOLD mode.
  <1> Setting the reset pin to a low level
  <2> Generating a reset signal by the watchdog timer or low-voltage detection
  <3> Establishing an interrupt source at one of INT0, INT1, INT2, INT4, and INT5 pins
  * INT0 and INT1 X’tal HOLD mode release is available only when level detection is configured.
  <4> Establishing an interrupt source at port 0
  <5> Establishing an interrupt source in the base timer circuit
  <6> Establishing an interrupt source in the infrared remote control receiver circuit
  <7> Establishing an bus active interrupt source in the USB host control circuit

■ Package Form

- SQFP48(7×7)  Pb-Free and Halogen Free product

■ Development Tools

- On-chip debugger : TCB87-Type C (1-wire communication cable) + LC87F17C8A

■ Flash ROM Programming Board

| Package | Programming Board |
|---|---|
| SQFP48 (7×7) | W87F55256SQ |

■ Flash ROM Programmer

| Maker | | Model | Supported Version | Device |
|---|---|---|---|---|
| Flash Support Group Company (FSG) | Single | AF9709C | Rev. 03.28 or later | 87F128JU |
| Flash Support Group Company (FSG) + Our company (Note 1) | Onboard single/ganged | AF9101/AF9103 (main unit) (FSG model)<br>SIB87 Type C (interface driver) (Our company model) | (Note 2) | LC87F17C8A |
| Our company | Single/ganged | SKK/SKK Type C (SanyoFWS) | Application version 1.08 and later Chip data version 2.47 and later | LC87F17C8 |
| | Onboard single/ganged | SKK-DBG Type C (SanyoFWS) | | |

(Further information on the AF series)

Flash Support Group Company (TOA ELECTRONICS, Inc.)
Phone: 053-459-1050
E-mail: sales@j- fsg.co.jp

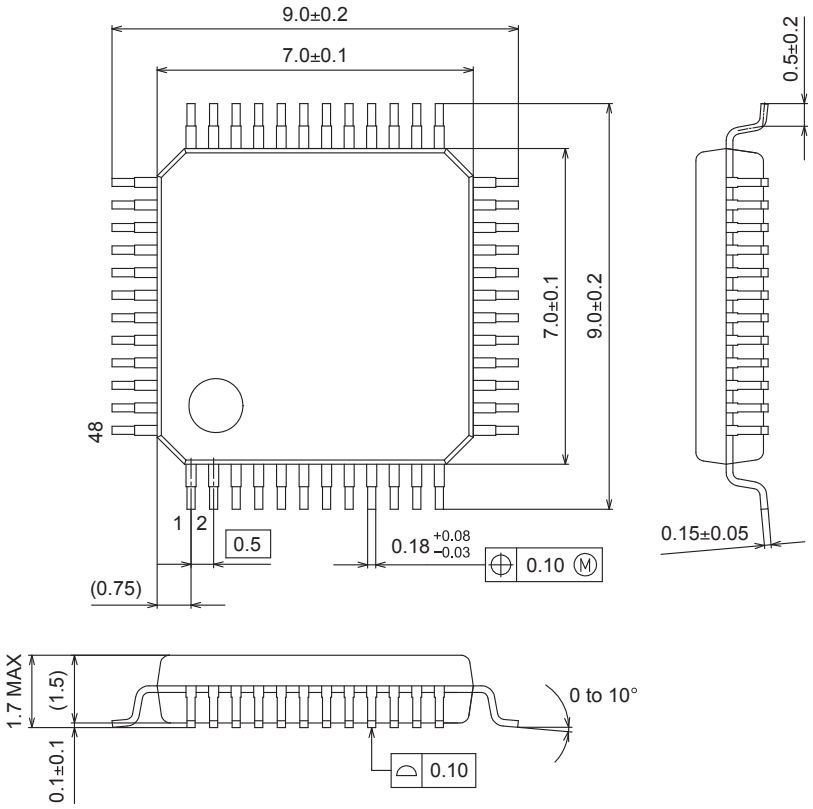
Note 1 : PC-less standalone onboard programming is possible using the FSG onboard programmer (AF9101/AF9103) and the serial interface driver (SIB87 Type C) provided by our company in pair.

Note 2 : Dedicated programming device and program are required depending on the programming conditions. Contact our company or FSG if you have any questions or difficulties regarding this matter.

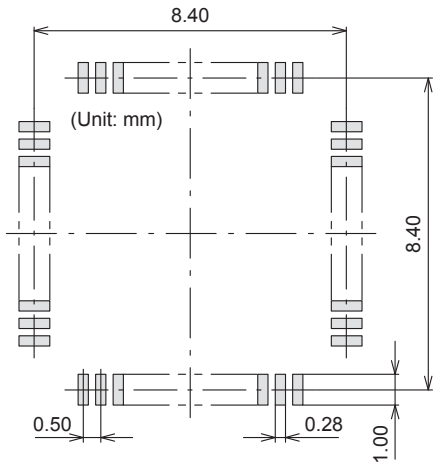
## Package Dimensions

unit : mm

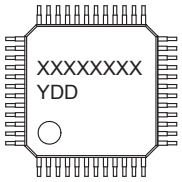
**SPQFP48 7x7 / SQFP48**
CASE 131AJ
ISSUE A



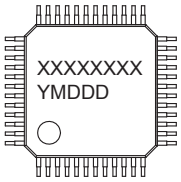

**SOLDERING FOOTPRINT***




**GENERIC MARKING DIAGRAM***




XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



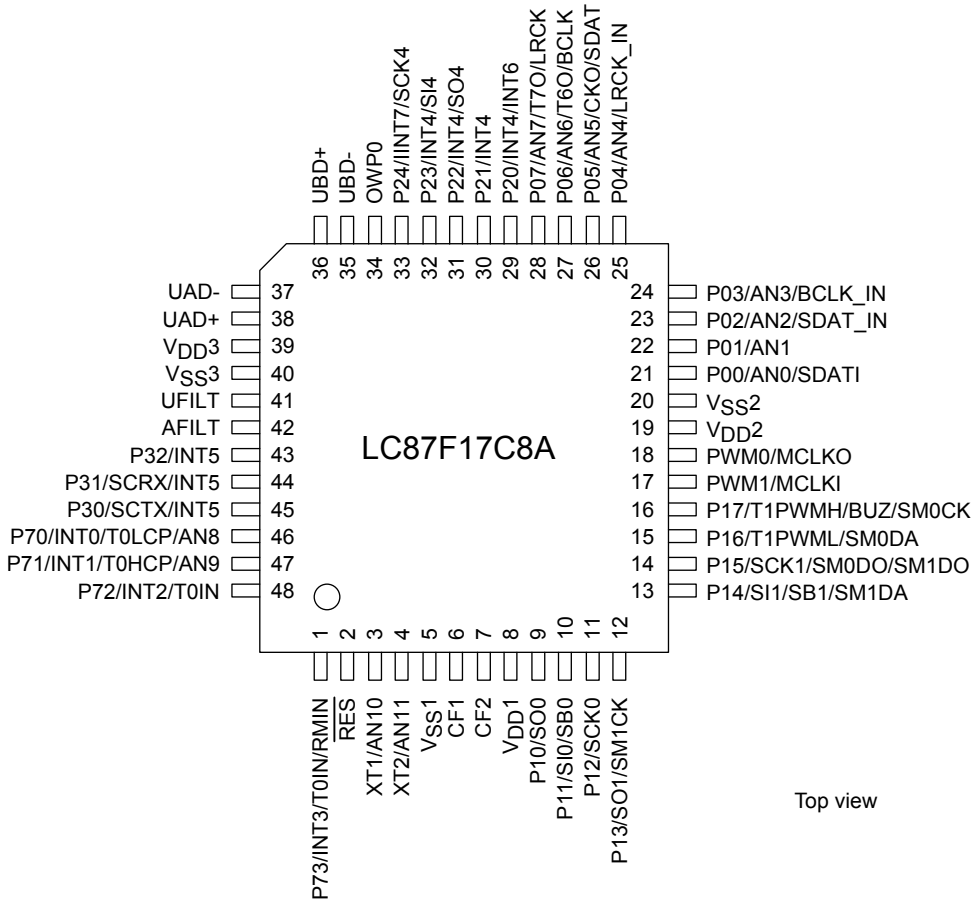

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## Pin Assignment

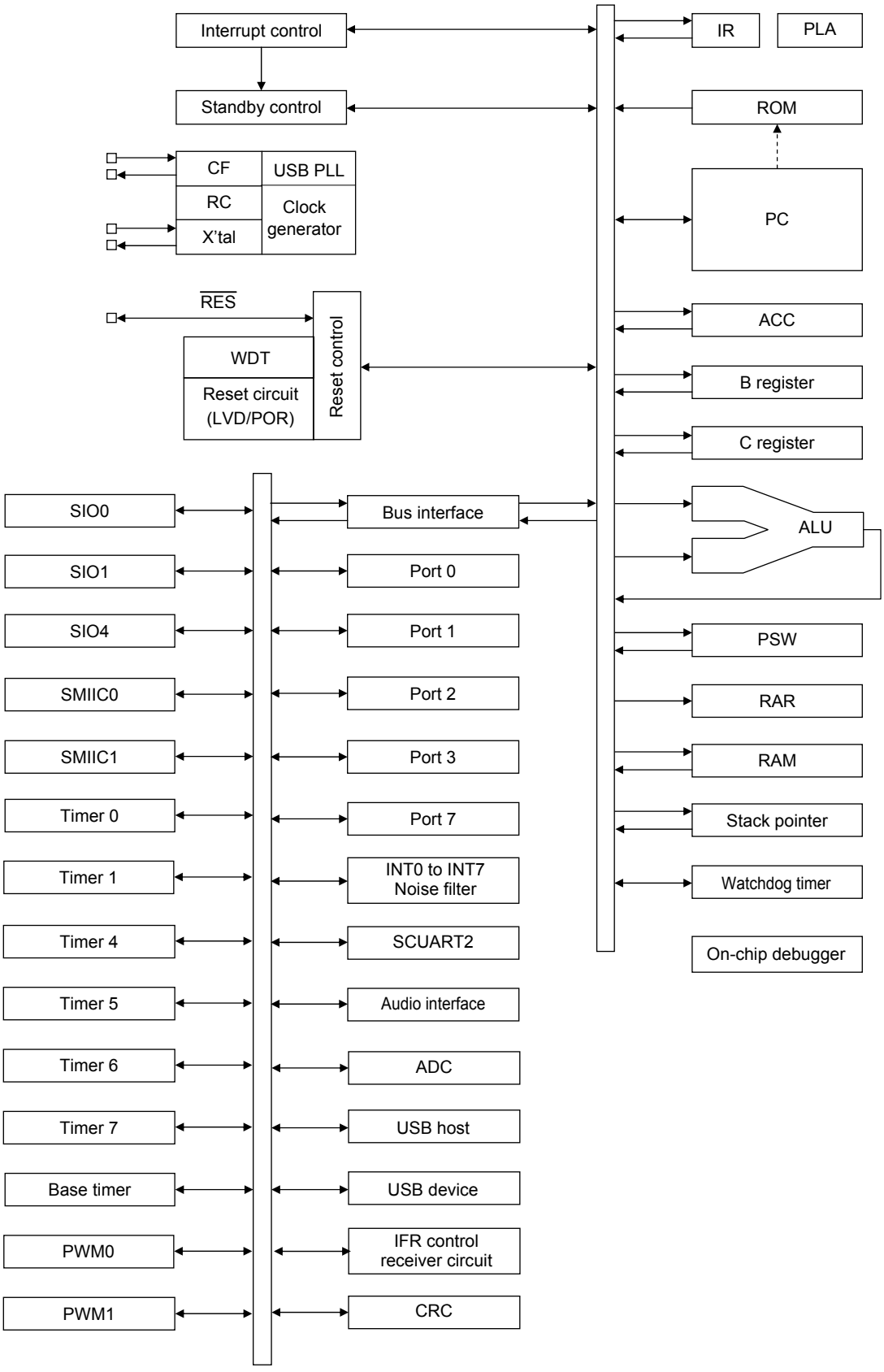



SQFP48(7×7) (Pb-Free and Halogen Free product)

| SQFP48 | NAME |
|---|---|
| 1 | P73/INT3/T0IN/RMIN |
| 2 | $\overline{\text{RES}}$ |
| 3 | XT1/AN10 |
| 4 | XT2/AN11 |
| 5 | $V_{SS}1$ |
| 6 | CF1 |
| 7 | CF2 |
| 8 | $V_{DD}1$ |
| 9 | P10/SO0 |
| 10 | P11/SI0/SB0 |
| 11 | P12/SCK0 |
| 12 | P13/SO1/SM1CK |
| 13 | P14/SI1/SB1/SM1DA |
| 14 | P15/SCK1/SM0DO/SM1DO |
| 15 | P16/T1PWML/SM0DA |
| 16 | P17/T1PWMH/BUZ/SM0CK |
| 17 | PWM1/MCLKI |
| 18 | PWM0/MCLKO |
| 19 | $V_{DD}2$ |
| 20 | $V_{SS}2$ |
| 21 | P00/AN0/SDATI |
| 22 | P01/AN1 |
| 23 | P02/AN2/SDAT_IN |
| 24 | P03/AN3/BCLK_IN |

| SQFP48 | NAME |
|---|---|
| 25 | P04/AN4/LRCK_IN |
| 26 | P05/AN5/CKO/SDAT |
| 27 | P06/AN6/T6O/BCLK |
| 28 | P07/AN7/T7O/LRCK |
| 29 | P20/INT4/INT6 |
| 30 | P21/INT4 |
| 31 | P22/INT4/SO4 |
| 32 | P23/INT4/SI4 |
| 33 | P24/INT7/SCK4 |
| 34 | OWP0 |
| 35 | UBD− |
| 36 | UBD+ |
| 37 | UAD− |
| 38 | UAD+ |
| 39 | $V_{DD}3$ |
| 40 | $V_{SS}3$ |
| 41 | UFILT |
| 42 | AFILT |
| 43 | P32/INT5 |
| 44 | P31/SCURX/INT5 |
| 45 | P30/SCUTX/INT5 |
| 46 | P70/INT0/T0LCP/AN8 |
| 47 | P71/INT1/T0HCP/AN9 |
| 48 | P72/INT2/T0IN |

## System Block Diagram



## Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$, $V_{SS}3$</td><td>-</td><td>_power supply</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$</td><td>-</td><td>+power supply</td><td>No</td></tr>
<tr><td>$V_{DD}3$</td><td>-</td><td>USB reference voltage</td><td>Yes</td></tr>
<tr><td>Port 0<br>P00 to P07</td><td>I/O</td><td>・8-bit I/O port<br>・I/O can be specified in 1-bit units<br>・Pull-up resistors can be turned on and off in 1-bit units.<br>・HOLD release input<br>・Port 0 interrupt input<br>・Pin functions<br>AD converter input port : AN0 to AN7 (P00 to P07)<br>P00 : audio interface SDAT input<br>P02 : audio through SDAT input<br>P03 : audio through BCLK input<br>P04 : audio through LRCK input<br>P05 : System clock output / audio interface SDAT I/O<br>P06 : Timer 6 toggle output / audio interface BCLK I/O<br>P07 : Timer 7 toggle output / audio interface LRCK I/O</td><td>Yes</td></tr>
<tr><td>Port 1<br>P10 to P17</td><td>I/O</td><td>・8-bit I/O port<br>・I/O can be specified in 1-bit units<br>・Pull-up resistors can be turned on and off in 1-bit units.<br>・Pin functions<br>P10 : SIO0 data output<br>P11 : SIO0 data input / bus I/O<br>P12 : SIO0 clock I/O<br>P13 : SIO1 data output / SMIIC1 clock I/O<br>P14 : SIO1 data input / bus I/O / SMIIC1 bus I/O / data input<br>P15 : SIO1 clock I/O / SMIIC0 data output (used in 3-wire SIO mode) /<br>SMIIC1 data output (used in 3-wire SIO mode)<br>P16 : Timer 1 PWML output / SMIIC0 bus I/O / data input<br>P17 : Timer 1 PWMH output / buzzer output / SMIIC0 clock I/O</td><td>Yes</td></tr>
<tr><td>Port 2<br>P20 to P24</td><td>I/O</td><td>・5-bit I/O port<br>・I/O can be specified in 1-bit units<br>・Pull-up resistors can be turned on and off in 1-bit units.<br>・Pin functions<br>P20 to P23 : INT4 input / HOLD release input / timer 1 event input /<br>timer 0L capture input / timer 0H capture input<br>P20 : INT6 input / timer 0L capture 1 input<br>P22 : SIO4 data I/O<br>P23 : SIO4 data I/O<br>P24 : INT7 input / timer 0H capture 1 input / SIO4 clock I/O<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT4</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT6</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT7</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 3<br>P30 to P32</td><td>I/O</td><td>・3-bit I/O port<br>・I/O can be specified in 1-bit units<br>・Pull-up resistors can be turned on and off in 1-bit units.<br>・Pin functions<br>P30 to P32 : INT5 input / HOLD release input / timer 1 event input /<br>timer 0L capture input / timer 0H capture input<br>P30 : SCUART2 transmit<br>P31 : SCUART2 receive<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT5</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 7<br>P70 to P73</td><td>I/O</td><td>・4-bit I/O port<br>・I/O can be specified in 1-bit units<br>・Pull-up resistors can be turned on and off in 1-bit units.<br>・Pin functions<br>P70 : INT0 input / HOLD release input / timer 0L capture input<br>P71 : INT1 input / HOLD release input / timer 0H capture input<br>P72 : INT2 input / HOLD release input / timer 0 event input /<br>timer 0L capture input / high-speed clock counter input<br>P73 : INT3 input (input with noise filter) / timer 0 event input /<br>timer 0H capture input / infrared remote control receiver input<br>AD converter input port: AN8 (P70), AN9 (P71)<br>Interrupt acknowledge types
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H Level</th><th>L Level</th></tr>
<tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr>
<tr><td>INT2</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
<tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>PWM0<br>PWM1</td><td>I/O</td><td>PWM0 and PWM1 output port<br>General-purpose input port<br>・Pin functions<br>PWM0 : Audio interface master clock output<br>PWM1 : Audio interface master clock input</td><td>No</td></tr>
<tr><td>UAD−<br>UAD+</td><td>I/O</td><td>USB-A port data I/O pin</td><td>No</td></tr>
<tr><td>UBD−<br>UBD+</td><td>I/O</td><td>USB-B port data I/O pin</td><td>No</td></tr>
<tr><td>UFILT</td><td>I/O</td><td>USB interface PLL filter circuit connection pin (see Fig.5)</td><td>No</td></tr>
<tr><td>AFILT</td><td>I/O</td><td>Audio interface PLL filter circuit connection pin (see Fig.6)</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input / internal reset output</td><td>No</td></tr>
<tr><td>XT1</td><td>I</td><td>・32.768 kHz crystal resonator input<br>・Pin functions<br>General-purpose input port<br>AD converter input port: AN10</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>・32.768 kHz crystal resonator output<br>・Pin functions<br>General-purpose I/O port<br>AD converter input port: AN11</td><td>No</td></tr>
<tr><td>CF1</td><td>I</td><td>Ceramic/crystal resonator input</td><td>No</td></tr>
<tr><td>CF2</td><td>O</td><td>Ceramic/crystal resonator output</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>Dedicated debugger port</td><td>No</td></tr>
</table>

## On-chip Debugger Pin Treatment

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation Manual."

### Recommended Unused Pin Treatment

| Pin Name | Recommended Unused Pin Treatment | |
|---|---|---|
| | Board | Software |
| P00 to P07 | Open | Set output low. |
| P10 to P17 | Open | Set output low. |
| P20 to P24 | Open | Set output low. |
| P30 to P32 | Open | Set output low. |
| P70 to P73 | Open | Set output low. |
| PWM0, PWM1 | Open | Set output low. |
| UAD+, UAD− | Open | Set output low. |
| UBD+, UBD− | Open | Set output low. |
| XT1 | Pull-down with a resistor of 100kΩ or lower. | - |
| XT2 | Open | Set output low. |
| OWP0 | Pull-down with a 100kΩ resistor. | - |

## Port Output Types

The table below lists the type of port output and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in output mode.

| Port Name | Option Selected in Units of | Option Type | Output Type | Pull-up Resistor |
|---|---|---|---|---|
| P00 to P07<br>P10 to P17<br>P20 to P24<br>P30 to P32 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | N-channel open drain | Programmable |
| P70 | - | No | N-channel open drain | Programmable |
| P71 to P73 | - | No | CMOS | Programmable |
| PWM0, PWM1 | - | No | CMOS | No |
| UAD+, UAD−<br>UBD+, UBD− | - | No | CMOS | No |
| XT1 | - | No | Input only | No |
| XT2 | - | No | 32.768kHz crystal resonator output (N-channel open drain when in general-purpose output mode) | No |

## User Option Table

| Option Name | Option to be Applied on | Flash-ROM Version | Option Selected in Units of | Option Selection |
|---|---|---|---|---|
| Port output type | P00 to P07 | ○ | 1 bit | CMOS |
| | | | | N-channel open drain |
| | P10 to P17 | ○ | 1 bit | CMOS |
| | | | | N-channel open drain |
| | P20 to P24 | ○ | 1 bit | CMOS |
| | | | | N-channel open drain |
| | P30 to P32 | ○ | 1 bit | CMOS |
| | | | | N-channel open drain |
| Program start address | - | ○ | - | 00000h |
| | | | | 1FE00h |
| USB regulator | USB regulator | ○ | - | Use |
| | | | | Non-use |
| | USB regulator (HOLD mode) | ○ | - | Use |
| | | | | Non-use |
| | USB regulator (HALT mode) | ○ | - | Use |
| | | | | Non-use |
| Low-voltage detection reset function | Detection function | ○ | - | Enable : Use |
| | | | | Disable : Non-use |
| | Detection level | ○ | - | 7 levels |
| Power-on reset function | Power-on reset level | ○ | - | 8 levels |

## USB Reference Power Option

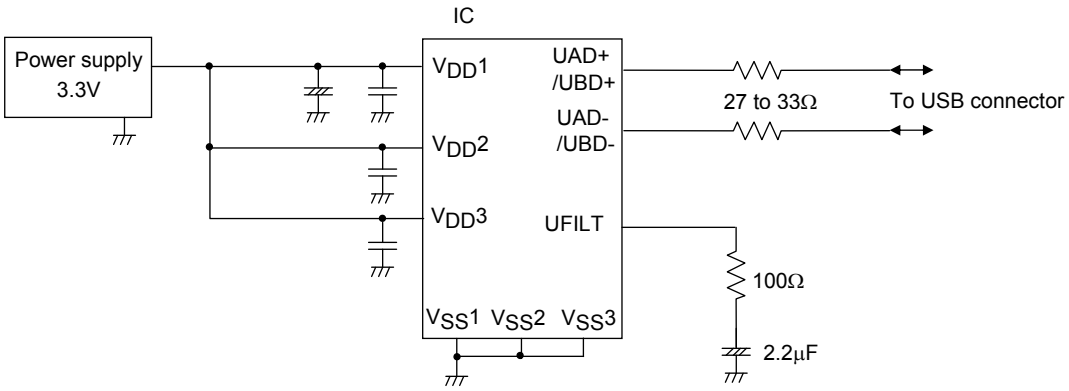
When a voltage 4.5 to 5.5V is supplied to $V_{DD}1$ and the internal USB reference voltage circuit is activated, the reference voltage for USB port output is generated. The active/inactive state of the reference voltage circuit can be switched by selecting an option. The procedure for making the option selection is described below.

| | | (1) | (2) | (3) | (4) |
|---|---|---|---|---|---|
| Option settings | USB regulator | Use | Use | Use | Non-use |
| | USB regulator at HOLD mode | Use | Non-use | Non-use | Non-use |
| | USB regulator at HALT mode | Use | Non-use | Use | Non-use |
| Reference voltage circuit state | Normal mode | Active | Active | Active | Inactive |
| | HOLD mode | Active | Inactive | Inactive | Inactive |
| | HALT mode | Active | Inactive | Active | Inactive |

- When the USB reference voltage circuit is made inactive, the level of the reference voltage for the USB port output is equal to $V_{DD}1$.
- Selection (2) or (3) can be used to set the reference voltage circuit inactive in HOLD or HALT mode.
- When the reference voltage circuit is activated, the current drain increases by approximately 100μA compared with when the reference voltage circuit is inactive.

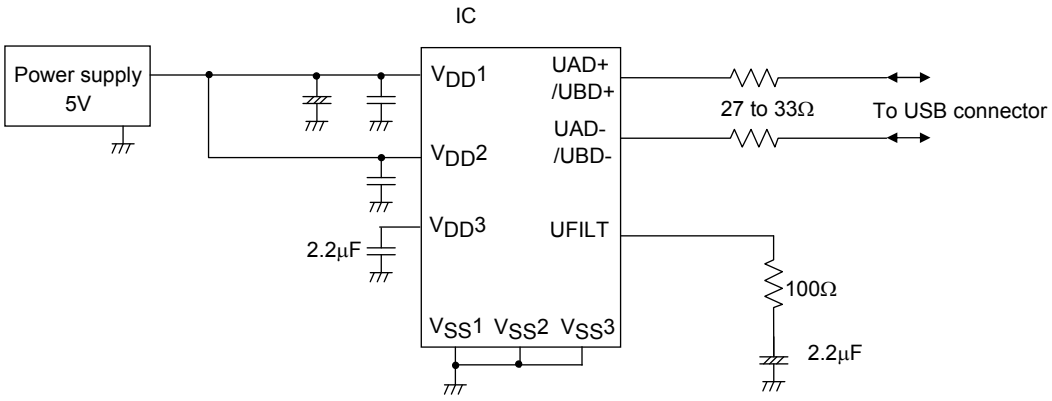
Example 1 : $V_{DD}1=V_{DD}2=3.3V$

- Inactivating the reference voltage circuit (selection (4)).
- Connecting $V_{DD}3$ to $V_{DD}1$ and $V_{DD}2$.




Example 2 : $V_{DD}1=V_{DD}2=5.0V$

- Activating the reference voltage circuit (selection (1)).
- Isolating $V_{DD}3$ from $V_{DD}1$ and $V_{DD}2$, and connecting capacitor between $V_{DD}3$ and $V_{SS}$.




Note : Do not apply the voltage of more than 3.6V to UAD+, UAD–, UBD+ and UBD– when the reference voltage circuit is active.

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | | Symbol | Pin/Remarks | Conditions | $V_{DD}$[V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|
| Maximum supply voltage | | $V_{DD}$ max | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | | −0.3 | | +6.5 | V |
| Input voltage | | $V_I$(1) | XT1, CF1, $\overline{RES}$ | | | −0.3 | | $V_{DD}$+0.3 | |
| Input/output voltage | | $V_{IO}$(1) | Ports 0, 1, 2, 3, 7<br>PWM0, PWM1,<br>XT2 | | | −0.3 | | $V_{DD}$+0.3 | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1, 2 | • When CMOS output type is selected<br>• Per 1 applicable pin | | −10 | | | mA |
| | | IOPH(2) | PWM0, PWM1 | • Per 1 applicable pin | | −20 | | | |
| | | IOPH(3) | Port 3<br>P71 to P73 | • When CMOS output type is selected<br>• Per 1 applicable pin | | −5 | | | |
| | Average output current (Note 1-1) | IOMH(1) | Ports 0, 1, 2 | • When CMOS output type is selected<br>• Per 1 applicable pin | | −7.5 | | | |
| | | IOMH(2) | PWM0, PWM1 | Per 1 applicable pin | | −15 | | | |
| | | IOMH(3) | Port 3<br>P71 to P73 | • When CMOS output type is selected<br>• Per 1 applicable pin | | −3 | | | |
| | Total output current | ΣIOAH(1) | Ports 0, 2 | Total current of all applicable pins | | −25 | | | |
| | | ΣIOAH(2) | Port 1<br>PWM0, PWM1 | Total current of all applicable pins | | −25 | | | |
| | | ΣIOAH(3) | Ports 0, 1, 2<br>PWM0, PWM1 | Total current of all applicable pins | | −45 | | | |
| | | ΣIOAH(4) | Port 3<br>P71 to P73 | Total current of all applicable pins | | −10 | | | |
| | | ΣIOAH(5) | UAD+, UAD−<br>UBD+, UBD− | Total current of all applicable pins | | −50 | | | |
| Low level output current | Peak output current | IOPL(1) | P02 to P07<br>Ports 1, 2<br>PWM0, PWM1 | Per 1 applicable pin | | | | 20 | |
| | | IOPL(2) | P00, P01 | Per 1 applicable pin | | | | 30 | |
| | | IOPL(3) | Ports 3, 7<br>XT2 | Per 1 applicable pin | | | | 10 | |
| | Average output current (Note 1-1) | IOML(1) | P02 to P07<br>Ports 1, 2<br>PWM0, PWM1 | Per 1 applicable pin | | | | 15 | |
| | | IOML(2) | P00, P01 | Per 1 applicable pin | | | | 20 | |
| | | IOML(3) | Ports 3, 7<br>XT2 | Per 1 applicable pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | Ports 0, 2 | Total current of all applicable pins | | | | 45 | |
| | | ΣIOAL(2) | Port 1<br>PWM0, PWM1 | Total current of all applicable pins | | | | 45 | |
| | | ΣIOAL(3) | Ports 0, 1, 2<br>PWM0, PWM1 | Total current of all applicable pins | | | | 80 | |
| | | ΣIOAL(4) | Ports 3, 7<br>XT2 | Total current of all applicable pins | | | | 15 | |
| | | ΣIOAL(5) | UAD+, UAD−<br>UBD+, UBD− | Total current of all applicable pins | | | | 50 | |

Note 1-1 : The average output current is an average of current values measured over 100ms intervals.

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| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Allowable power dissipation | Pd max | SQFP48(7×7) | Ta=–40 to +85°C | | | | 140 | mW |
| Operating ambient Temperature | Topr | | | | –40 | | +85 | °C |
| Storage ambient temperature | Tstg | | | | –55 | | +125 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## Allowable Operating Conditions at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Operating supply voltage (Note 2-1) | $V_{DD}(1)$ | $V_{DD}1=V_{DD}2=V_{DD}3$ | 0.245μs ≤ tCYC ≤ 200μs | | 3.0 | | 5.5 | V |
| | | | 0.245μs ≤ tCYC ≤ 0.383μs USB circuit active. | | 3.0 | | 5.5 | |
| | | | 0.490μs ≤ tCYC ≤ 200μs Except for onboard programming mode | | 2.7 | | 5.5 | |
| Memory retention supply voltage | VHD | $V_{DD}1=V_{DD}2=V_{DD}3$ | RAM and register contents are retained in HOLD mode | | 2.0 | | 5.5 | |
| High level input voltage | $V_{IH}(1)$ | Ports 0, 1, 2, 3, 7 PWM0, PWM1 | | 2.7 to 5.5 | $0.3V_{DD}$ +0.7 | | $V_{DD}$ | |
| | $V_{IH}(2)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.7 to 5.5 | $0.75V_{DD}$ | | $V_{DD}$ | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1, 2, 3, 7 | | 4.0 to 5.5 | $V_{SS}$ | | $0.1V_{DD}$ +0.4 | |
| | $V_{IL}(2)$ | | | 2.7 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 0 PWM0, PWM1 | | 4.0 to 5.5 | $V_{SS}$ | | $0.15V_{DD}$ +0.4 | |
| | $V_{IL}(4)$ | | | 2.7 to 4.0 | $V_{SS}$ | | $0.2V_{DD}$ | |
| | $V_{IL}(5)$ | XT1, XT2, CF1, $\overline{RES}$ | | 2.7 to 5.5 | $V_{SS}$ | | $0.25V_{DD}$ | |
| Instruction cycle time (Note 2-2) | tCYC | | | 3.0 to 5.5 | 0.245 | | 200 | μs |
| | | | USB circuit active. | 3.0 to 5.5 | 0.245 | | 0.383 | |
| | | | Except for onboard programming mode | 2.7 to 5.5 | 0.490 | | 200 | |

Note 2-1 : $V_{DD}$ must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2 : Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| External system clock frequency | FEXCF(1) | CF1 | • CF2 pin open<br>• System clock frequency division ratio =1/1<br>• External system clock duty =50±5% | 3.0 to 5.5 | 0.1 | | 12 | MHz |
| | | | • CF2 pin open<br>• System clock frequency division ratio =1/1<br>• External system clock duty =50±5% | 2.7 to 5.5 | 0.1 | | 6 | |
| Oscillation frequency range (Note 2-3) | FmCF | CF1, CF2 | 12MHz ceramic oscillation mode<br>See Fig. 1. | 3.0 to 5.5 | | 12 | | MHz |
| | FmRC | | Internal medium-speed RC oscillation | 2.7 to 5.5 | 0.5 | 1.0 | 2.0 | |
| | FmSRC | | Internal low-speed RC oscillation | 2.7 to 5.5 | 15 | 30 | 60 | kHz |
| | FsX'tal | XT1, XT2 | 32.768kHz crystal oscillation mode<br>See Fig. 2. | 2.7 to 5.5 | | 32.768 | | |

Note 2-3 : See Tables 1 and 2 for the oscillation constants.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## Electrical Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| High level input current | $I_{IH}(1)$ | Ports 0, 1, 2, 3, 7<br>RES<br>PWM0, PWM1 | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{DD}$<br>(Including output Tr's off leakage current) | 2.7 to 5.5 | | | 1 | μA |
| | $I_{IH}(2)$ | XT1, XT2 | Input port configuration<br>$V_{IN}=V_{DD}$ | 2.7 to 5.5 | | | 1 | |
| | $I_{IH}(3)$ | CF1 | $V_{IN}=V_{DD}$ | 2.7 to 5.5 | | | 15 | |
| Low level input current | $I_{IL}(1)$ | Ports 0, 1, 2, 3, 7<br>RES<br>PWM0, PWM1 | Output disabled<br>Pull-up resistor off<br>$V_{IN}=V_{SS}$<br>(Including output Tr's off leakage current) | 2.7 to 5.5 | –1 | | | |
| | $I_{IL}(2)$ | XT1, XT2 | Input port configuration<br>$V_{IN}=V_{SS}$ | 2.7 to 5.5 | –1 | | | |
| | $I_{IL}(3)$ | CF1 | $V_{IN}=V_{SS}$ | 2.7 to 5.5 | –15 | | | |
| High level output voltage | $V_{OH}(1)$ | Ports 0, 1, 2, 3<br>P71 to P73 | $I_{OH}$=–1mA | 4.5 to 5.5 | $V_{DD}$–1 | | | V |
| | $V_{OH}(2)$ | | $I_{OH}$=–0.4mA | 3.0 to 5.5 | $V_{DD}$–0.4 | | | |
| | $V_{OH}(3)$ | | $I_{OH}$=–0.2mA | 2.7 to 5.5 | $V_{DD}$–0.4 | | | |
| | $V_{OH}(4)$ | PWM0, PWM1<br>P05 to P07<br>(Note 3-1) | $I_{OH}$=–10mA | 4.5 to 5.5 | $V_{DD}$–1.5 | | | |
| | $V_{OH}(5)$ | | $I_{OH}$=–1.6mA | 3.0 to 5.5 | $V_{DD}$–0.4 | | | |
| | $V_{OH}(6)$ | | $I_{OH}$=–1mA | 2.7 to 5.5 | $V_{DD}$–0.4 | | | |
| Low level output voltage | $V_{OL}(1)$ | P00, P01 | $I_{OL}$=30mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(2)$ | | $I_{OL}$=5mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(3)$ | | $I_{OL}$=2.5mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}(4)$ | Ports 0, 1, 2<br>PWM0, PWM1<br>XT2 | $I_{OL}$=10mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}(5)$ | | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(6)$ | | $I_{OL}$=1mA | 2.7 to 5.5 | | | 0.4 | |
| | $V_{OL}(7)$ | Ports 3, 7 | $I_{OL}$=1.6mA | 3.0 to 5.5 | | | 0.4 | |
| | $V_{OL}(8)$ | | $I_{OL}$=1mA | 2.7 to 5.5 | | | 0.4 | |
| Pull-up resistance | Rpu(1) | Ports 0, 1, 2, 3, 7 | $V_{OH}=0.9V_{DD}$ | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | Rpu(2) | | | 2.7 to 4.5 | 18 | 50 | 150 | |
| Hysteresis voltage | VHYS | RES<br>Ports 1, 2, 3, 7 | | 2.7 to 5.5 | | $0.1V_{DD}$ | | V |
| Pin capacitance | CP | All pins | For pins other than those under test :<br>$V_{IN}=V_{SS}$<br>f=1MHz<br>Ta=25°C | 2.7 to 5.5 | | 10 | | pF |

Note 3-1 : When the CKO system clock output function (P05) or the audio interface output function (P05 to P07) is used.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## Serial I/O Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

### 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | $V_{DD}$ [V] | Specification min | typ | max | unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Serial clock | Input clock | Frequency | tSCK(1) | SCK0(P12) | See Fig. 8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(1) | | | | 1 | | | |
| | | High level pulse width | tSCKH(1) | | | | 1 | | | |
| | | | tSCKHA(1a) | | • Continuous data transmission/ reception mode<br>• USB, AIF, SIO4, CRC not used at the same time.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 4 | | | |
| | | | tSCKHA(1b) | | • Continuous data transmission/ reception mode<br>• USB used at the same time<br>• AIF, SIO4, CRC not used at the same time.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 7 | | | |
| | | | tSCKHA(1c) | | • Continuous data transmission/ reception mode<br>• USB, AIF, SIO4, CRC used at the same time.<br>• See Fig. 8.<br>• (Note 4-1-2) | | 9 | | | |
| | Output clock | Frequency | tSCK(2) | SCK0(P12) | • When CMOS output type is selected.<br>• See Fig. 8. | 2.7 to 5.5 | 4/3 | | | tCYC |
| | | Low level pulse width | tSCKL(2) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(2) | | | | 1/2 | | | |
| | | | tSCKHA(2a) | | • Continuous data transmission/ reception mode<br>• USB, AIF, SIO4, CRC not used at the same time.<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) + (10/3)tCYC | tCYC |
| | | | tSCKHA(2b) | | • Continuous data transmission/ reception mode<br>• USB used at the same time<br>• AIF, SIO4, CRC not used at the same time.<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) + (19/3)tCYC | |
| | | | tSCKHA(2c) | | • Continuous data transmission/ reception mode<br>• USB, AIF, SIO4, CRC used at the same time<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(2) +2tCYC | | tSCKH(2) + (25/3)tCYC | |

Note 4-1-1 : These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-1-2 : In an application where the serial clock input is to be used in continuous data transmission/reception mode, the time from SI0RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.

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| Parameter | | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial input | Data setup time | | tsDI(1) | SB0(P11), SI0(P11) | • Must be specified with respect to rising edge of SIOCLK<br>• See Fig. 8. | 2.7 to 5.5 | 0.03 | | | μs |
| | Data hold time | | thDI(1) | | | | 0.03 | | | |
| Serial output | Input clock | Output delay time | tdDO(1) | SO0(P10), SB0(P11) | • Continuous data transmission/ reception mode<br>• (Note 4-1-3) | 2.7 to 5.5 | | | (1/3)tCYC +0.05 | |
| | | | tdDO(2) | | • Synchronous 8-bit mode<br>• (Note 4-1-3) | | | | 1tCYC +0.05 | |
| | Output clock | | tdDO(3) | | (Note 4-1-3) | | | | (1/3)tCYC +0.05 | |

Note 4-1-3 : Must be specified with respect to falling edge of SIOCLK. Must be defined as the time up to the beginning of output state change in open drain output mode. See Fig. 8.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig. 8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | • When CMOS output type is selected.<br>• See Fig. 8. | 2.7 to 5.5 | 2 | | | |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(2) | SB1(P14), SI1(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 8. | 2.7 to 5.5 | 0.03 | | | μs |
| | Data hold time | | thDI(2) | | | | 0.03 | | | |
| Serial output | Output delay time | | tdDO(4) | SO1(P13), SB1(P14) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time up to the beginning of output state change in open drain output mode.<br>• See Fig. 8. | 2.7 to 5.5 | | | (1/2)tCYC +0.05 | |

Note 4-2-1 : These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

### 3. SIO4 Serial I/O Characteristics (Note 4-3-1)

| Parameter | | | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(5) | SCK4(P24) | See Fig. 8. | 2.7 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(5) | | | | 1 | | | |
| | | High level pulse width | tSCKH(5) | | | | 1 | | | |
| | | | tSCKHA(5a) | | • USB, SIO0 continuous transfer mode, AIF, CRC not used at the same time.<br>• See Fig. 8.<br>• (Note 4-3-2) | | 4 | | | |
| | | | tSCKHA(5b) | | • USB used at the same time.<br>• SIO0 continuous transfer mode, AIF, CRC not used at the same time.<br>• See Fig. 8.<br>• (Note 4-3-2) | | 7 | | | |
| | | | tSCKHA(5c) | | • USB, SIO0 continuous transfer mode used at the same time.<br>• AIF, CRC not used at the same time.<br>• See Fig. 8.<br>• (Note 4-3-2) | | 10 | | | |
| | Output clock | Frequency | tSCK(6) | SCK4(P24) | • When CMOS output type is selected.<br>• See Fig. 8. | 2.7 to 5.5 | 4/3 | | | tSCK |
| | | Low level pulse width | tSCKL(6) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(6) | | | | 1/2 | | | |
| | | | tSCKHA(6a) | | • USB, SIO0 continuous transfer mode, AIF, CRC not used at the same time.<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(6) + (5/3)tCYC | | tSCKH(6) + (10/3)tCYC | tCYC |
| | | | tSCKHA(6b) | | • USB used at the same time.<br>• SIO0 continuous transfer mode, AIF, CRC not used at the same time.<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(6) + (5/3)tCYC | | tSCKH(6) + (19/3)tCYC | |
| | | | tSCKHA(6c) | | • USB, SIO0 continuous transfer mode used at the same time<br>• AIF, CRC not used at the same time.<br>• When CMOS output type is selected.<br>• See Fig. 8. | | tSCKH(6) + (5/3)tCYC | | tSCKH(6) + (28/3)tCYC | |

Note 4-3-1 : These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-3-2 : In an application where the serial clock input is to be used, the time from SI4RUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA when continuous data transmission/reception is started.

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| Parameter | | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial input | Data setup time | tsDI(3) | SO4(P22), SI4(P23) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 8. | 2.7 to 5.5 | 0.03 | | | μs |
| | Data hold time | thDI(3) | | | | 0.03 | | | |
| Serial output | Output delay time | tdDO(5) | SO4(P22), SI4(P23) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time up to the beginning of output state change in open drain output mode<br>• See Fig. 8. | 2.7 to 5.5 | | | (1/3)tCYC +0.05 | |

### 4-1. SMIIC0/SMIIC1 Simple SIO Mode I/O Characteristics (Note 4-4-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | Specification | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCK(7) | SM0CK(P17), SM1CK(P13) | See Fig. 8. | 4/3 | | | tCYC |
| | | Low level pulse width | tSCKL(7) | | 2.7 to 5.5 | 2/3 | | | |
| | | High level pulse width | tSCKH(7) | | | 2/3 | | | |
| | Output clock | Frequency | tSCK(8) | SM0CK(P17), SM1CK(P13) | • When CMOS output type is selected.<br>• See Fig. 8. | 4/3 | | | |
| | | Low level pulse width | tSCKL(8) | | 2.7 to 5.5 | 1/2 | | | tSCK |
| | | High level pulse width | tSCKH(8) | | | 1/2 | | | |
| Serial input | Data setup time | | tsDI(4) | SM0DA(P16), SM1DA(P14) | • Must be specified with respect to rising edge of SIOCLK.<br>• See Fig. 8. | 0.03 | | | μs |
| | Data hold time | | thDI(4) | | 2.7 to 5.5 | 0.03 | | | |
| Serial output | Output delay time | | tdDO(6) | SM0DA(P16), SM0DO(P15), SM1DA(P14), SM1DO(P15) | • Must be specified with respect to falling edge of SIOCLK.<br>• Must be specified as the time to the beginning of output state change.<br>• See Fig. 8. | | | (1/3)tCYC +0.05 | |

Note 4-4-1 : These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

## 4-2. SMIIC0/SMIIC1 $I^2C$ Mode I/O Characteristics (Note 4-5-1)

| Parameter | | | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Serial clock | Input clock | Frequency | tSCL | SM0CK(P17), SM1CK(P13) | See Fig. 10. | 2.7 to 5.5 | 5 | | | Tfilt |
| | | Low level pulse width | tSCLL | | | | 2.5 | | | |
| | | High level pulse width | tSCLH | | | | 2 | | | |
| | Output clock | Frequency | tSCLx | SM0CK(P17), SM1CK(P13) | Must be specified as the time up to the beginning of output state change. | 2.7 to 5.5 | 10 | | | |
| | | Low level pulse width | tSCLLx | | | | 1/2 | | | tSCL |
| | | HIghlevel pulse width | tSCLHx | | | | 1/2 | | | |
| SM0CK, SM0DA, SM1CK, SM1DA pin input spike suppression time | | | tsp | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | | | 1 | Tfilt |
| Bus relinquish time between start and stop | input | | tBUF | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | 2.5 | | | Tfilt |
| | Output | | tBUFx | | • Standard clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 5.5 | | | µs |
| | | | | | • High-speed clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 1.6 | | | |
| Start, restart condition hold time | input | | tHD;STA | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | • When SMIIC register control bit SHDS=0<br>• See Fig. 10. | 2.7 to 5.5 | 2.0 | | | Tfilt |
| | | | | | • When SMIIC register control bit SHDS=1<br>• See Fig. 10. | | 2.5 | | | |
| | Output | | tHD;STAx | | • Standard clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 4.1 | | | µs |
| | | | | | • High-speed clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 1.0 | | | |
| Restart condition setup time | input | | tSU;STA | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | 1.0 | | | Tfilt |
| | Output | | tSU;STAx | | • Standard clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 5.5 | | | µs |
| | | | | | • High-speed clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 1.6 | | | |

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| Parameter | | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Stop condition setup time | input | tSU;STO | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | 1.0 | | | Tfilt |
| | Output | tSU;STOx | | • Standard clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 4.9 | | | µs |
| | | | | • High-speed clock mode<br>• Must be specified as the time up to the beginning of output state change. | | 1.1 | | | |
| Data hold time | Input | tHD;DAT | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | 0 | | | Tfilt |
| | Output | tHD;DATx | | Must be specified as the time up to the beginning of output state change. | | 1 | | 1.5 | |
| Data setup time | Input | tSU;DAT | SM0CK(P17), SM0DA(P16), SM1CK(P13), SM1DA(P14) | See Fig. 10. | 2.7 to 5.5 | 1 | | | Tfilt |
| | Output | tSU;DATx | | Must be specified as the time up to the beginning of output state change. | | 1tSCL-1.5Tfilt | | | |

Note 4-5-1 : These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-5-2 : The value of Tfilt is determined by bits 7 and 6 (BRP1 and BRP0) of the SMIC0BRG/SMIC1BRG register and the system clock frequency.

| BRP1 | BRP0 | Tfilt |
|---|---|---|
| 0 | 0 | (1/3) tCYC×1 |
| 0 | 1 | (1/3) tCYC×2 |
| 1 | 0 | (1/3) tCYC×3 |
| 1 | 1 | (1/3) tCYC×4 |

Set the value of the BRP1 and BRP0 bits so that the value of Tfilt falls within the following value range :

250 ns ≥ Tfilt > 140 ns

Note 4-5-3: For standard clock mode operation, set up the SMIC0BRG/SMIC1BRG register so that the following conditions are satisfied :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 1

SCL frequency value ≤ 100 kHz

For high-speed clock mode operation, set up the SMIC0BRG/SMIC1BRG register so that the following conditions are satisfied :

250 ns ≥ Tfilt > 140 ns

BRDQ (bit5) = 0

SCL frequency value ≤ 400 kHz

## Pulse Input Conditions at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70),<br>INT1(P71),<br>INT2(P72),<br>INT4(P20 to P23),<br>INT5(P30 to P32),<br>INT6(P20),<br>INT7(P24) | • Interrupt source flag can be set.<br>• Event inputs for timer 0/1 are enabled. | 2.7 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3(P73) when noisefilter time constant is 1/1. | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.7 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3(P73) when noisefilter time constant is 1/32. | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.7 to 5.5 | 64 | | | |
| | tPIH(4)<br>tPIL(4) | INT3(P73) when noisefilter time constant is 1/128. | • Interrupt source flag can be set.<br>• Event inputs for timer 0 are enabled. | 2.7 to 5.5 | 256 | | | |
| | tPIL(5) | RMIN(P73) | Recognized as a signal by infrared remote control receiver circuit | 2.7 to 5.5 | 4 | | | RMCK<br>(Note 5-1) |
| | tPIL(6) | $\overline{RES}$ | Resetting is enabled. | 2.7 to 5.5 | 200 | | | μs |

Note 5-1 : Denotes the reference frequency of the infrared remote control receiver circuit (1tCYC to 128tCYC or source oscillation frequency of the subclock)

## AD Converter Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12-bit AD Converter Mode>

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Resolution | N | AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2) | | 3.0 to 5.5 | | 12 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±16 | LSB |
| Conversion time | TCAD | | See conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 32 | | 115 | μs |
| | | | | 3.0 to 5.5 | 64 | | 115 | |
| Analog input voltage range | VAIN | | | 3.00 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | μA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | –1 | | | |

<8-bit AD Converter Mode>

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | unit |
| Resolution | N | AN0(P00) to AN7(P07) AN8(P70) AN9(P71) AN10(XT1) AN11(XT2) | | 3.0 to 5.5 | | 8 | | bit |
| Absolute accuracy | ET | | (Note 6-1) | 3.0 to 5.5 | | | ±1.5 | LSB |
| Conversion time | TCAD | | See conversion time calculation formulas. (Note 6-2) | 4.0 to 5.5 | 20 | | 90 | μs |
| | | | | 3.0 to 5.5 | 40 | | 90 | |
| Analog input voltage range | VAIN | | | 3.0 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| A Analog port input current | IAINH | | VAIN=$V_{DD}$ | 3.0 to 5.5 | | | 1 | μA |
| | IAINL | | VAIN=$V_{SS}$ | 3.0 to 5.5 | –1 | | | |

Conversion time calculation formulas :

12-bits AD Converter Mode : TCAD (Conversion time) = ((52/(AD division ratio))+2) ×□(1/3) ×□tCYC

8-bits AD Converter Mode : TCAD (Conversion time) = ((32/(AD division ratio))+2) ×□(1/3) ×□tCYC

<Recommended Operating Conditions>

| External Oscillator FmCF [MHz] | Supply Voltage Range $V_{DD}$ [V] | System Clock Division (SYSDIV) | Cycle Time tCYC [ns] | AD Frequency Division Ratio (ADDIV) | Conversion Time (TCAD) [μs] | |
|---|---|---|---|---|---|---|
| | | | | | 12-bit AD | 8-bit AD |
| 12 | 4.0 to 5.5 | 1/1 | 250 | 1/8 | 34.8 | 21.5 |
| | 3.0 to 5.5 | 1/1 | 250 | 1/16 | 69.5 | 42.8 |

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process until the time the conversion result register is loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is doubled in the following cases :

- The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.
- The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

## Power-on Reset (POR) Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|
| | | | Option selected voltage | min | typ | max | unit |
| POR release voltage | PORRL | Select from option (Note 7-1) | 1.67V | 1.55 | 1.67 | 1.79 | V |
| | | | 1.97V | 1.85 | 1.97 | 2.09 | |
| | | | 2.07V | 1.95 | 2.07 | 2.19 | |
| | | | 2.37V | 2.25 | 2.37 | 2.49 | |
| | | | 2.57V | 2.45 | 2.57 | 2.69 | |
| | | | 2.87V | 2.75 | 2.87 | 2.99 | |
| | | | 3.86V | 3.73 | 3.86 | 3.99 | |
| | | | 4.35V | 4.21 | 4.35 | 4.49 | |
| Detection voltage unknown state | POUKS | See Fig. 12 (Note 7-2) | | | 0.7 | 0.95 | |
| Power supply rise time | PORIS | Power supply rise time from $V_{DD}$=0V to 1.6V | | | | 100 | ms |

Note 7-1 : The POR release level can be selected out of 8 levels only when LDV reset function is disabled.
Note 7-2 : POR is in unknown state before transistors start operation.

## Low Voltage Detection (LVD) Characteristics

at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Conditions | Specification | | | | |
|---|---|---|---|---|---|---|---|
| | | | Option selected voltage | min | typ | max | unit |
| LVD reset voltage (Note 8-2) | LVDET | Select from option. See Fig. 13. (Note 8-1) (Note 8-3) | 1.91V | 1.81 | 1.91 | 2.01 | V |
| | | | 2.01V | 1.91 | 2.01 | 2.11 | |
| | | | 2.31V | 2.21 | 2.31 | 2.41 | |
| | | | 2.51V | 2.41 | 2.51 | 2.61 | |
| | | | 2.81V | 2.71 | 2.81 | 2.91 | |
| | | | 3.79V | 3.69 | 3.79 | 3.89 | |
| | | | 4.28V | 4.18 | 4.28 | 4.38 | |
| LVD hysteresis width | LVHYS | | 1.91V | | 55 | | mV |
| | | | 2.01V | | 55 | | |
| | | | 2.31V | | 55 | | |
| | | | 2.51V | | 55 | | |
| | | | 2.81V | | 55 | | |
| | | | 3.79V | | 60 | | |
| | | | 4.28V | | 65 | | |
| Detection voltage unknown state | LVUKS | See Fig. 13. (Note 8-4) | | | 0.7 | 0.95 | V |
| Low voltage detection minimum width (Reply sensitivity) | TLVDW | LVDET-0.5V See Fig. 14. | | 0.2 | | | ms |

Note8-1 : The LVD reset level can be selected out of 7 levels only when the LVD reset function is enabled.

Note8-2 : LVD reset voltage specification values do not include hysteresis voltage.

Note8-3 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4 : LVD is in an unknown state before transistors start operation.

## Consumption Current Characteristics at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Normal mode consumption current (Note 9-1) (Note 9-2) | IDDOP(1) | $V_{DD}1 = V_{DD}2 = V_{DD}3$ | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation stopped<br>• Internal low-/medium-speed RC oscillation stopped<br>• USB circuit stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 9.8 | 18 | mA |
| | | | | 3.0 to 3.6 | | 5.7 | 11 | |
| | IDDOP(2) | | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation mode active<br>• Internal low-/medium-speed RC oscillation stopped<br>• USB circuit active<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 17 | 30 | |
| | | | | 3.0 to 3.6 | | 8.5 | 16 | |
| | IDDOP(3) | | • FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 6MHz side<br>• Internal low-/medium-speed RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 6.7 | 12 | |
| | | | | 3.0 to 3.6 | | 4.2 | 7.1 | |
| | | | | 2.7 to 3.0 | | 3.5 | 5.8 | |
| | IDDOP(4) | | • External oscillation FmCF stopped<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal medium-speed RC oscillation<br>• Internal low-speed RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 0.44 | 1.4 | |
| | | | | 3.0 to 3.6 | | 0.29 | 0.87 | |
| | | | | 2.7 to 3.0 | | 0.26 | 0.75 | |
| | IDDOP(5) | | • External oscillation FsX'tal /FmCF stopped<br>• System clock set to internal low-speed RC oscillation<br>• Internal medium-speed RC oscillation stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 28 | 153 | μA |
| | | | | 3.0 to 3.6 | | 18 | 80 | |
| | | | | 2.7 to 3.0 | | 16 | 66 | |
| | IDDOP(6) | | • External oscillation FmCF stopped<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low-/medium-speed RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 45 | 160 | |
| | | | | 3.0 to 3.6 | | 18 | 74 | |
| | | | | 2.7 to 3.0 | | 14 | 58 | |
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(1) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation stopped<br>• Internal low-/medium-speed RC oscillation stopped<br>• USB circuit stopped<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 4.0 | 7.0 | mA |
| | | | | 3.0 to 3.6 | | 2.2 | 3.8 | |

Note 9-1 : The consumption current value do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2 : The consumption current values do not include operational current of LVD (Low Voltage Detection) function if not specified.

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| Parameter | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(2) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 12MHz side<br>• Internal PLL oscillation active<br>• Internal low-/medium-speed RC oscillation stopped<br>• USB circuit active<br>•1/1 frequency division ratio | 4.5 to 5.5 | | 11 | 19 | mA |
| | | | | 3.0 to 3.6 | | 4.9 | 9.1 | |
| | IDDHALT(3) | | • HALT mode<br>• FmCF=12MHz ceramic oscillation mode<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 6MHz side<br>• Internal low-/medium-speed RC oscillation stopped<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 2.5 | 4.5 | |
| | | | | 3.0 to 3.6 | | 1.3 | 2.3 | |
| | | | | 2.7 to 3.0 | | 1.1 | 1.8 | |
| | IDDHALT(4) | | • HALT mode<br>• External oscillation FmCF stopped<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to internal medium-speed RC oscillation<br>• Internal low-speed RC oscillation stopped<br>•1/2 frequency division ratio | 4.5 to 5.5 | | 0.16 | 0.56 | |
| | | | | 3.0 to 3.6 | | 0.09 | 0.27 | |
| | | | | 2.7 to 3.0 | | 0.07 | 0.21 | |
| | IDDHALT(5) | | • HALT mode<br>• External oscillation FsX'tal /FmCF stopped<br>• System clock set to internal low-speed RC oscillation<br>• Internal medium-speed RC oscillation stopped.<br>• 1/1 frequency division ratio | 4.5 to 5.5 | | 7.2 | 111 | μA |
| | | | | 3.0 to 3.6 | | 4.0 | 56 | |
| | | | | 2.7 to 3.0 | | 3.4 | 46 | |
| | IDDHALT(6) | | • HALT mode<br>• External oscillation FmCF stopped<br>• FsX'tal=32.768kHz crystal oscillation mode<br>• System clock set to 32.768kHz side<br>• Internal low-/medium-speed RC oscillation stopped.<br>• 1/2 frequency division ratio | 4.5 to 5.5 | | 30 | 141 | |
| | | | | 3.0 to 3.6 | | 8.4 | 63 | |
| | | | | 2.7 to 3.0 | | 5.8 | 48 | |
| HOLD mode consumption current (Note 9-1) (Note 9-2 | IDDHOLD(1) | | • HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 0.30 | 91 | |
| | | | | 3.0 to 3.6 | | 0.22 | 46 | |
| | | | | 2.7 to 3.0 | | 0.21 | 38 | |
| | IDDHOLD(2) | | • HOLD mode<br>• LVD option selected<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 3.3 | 95 | |
| | | | | 3.0 to 3.6 | | 2.5 | 49 | |
| | | | | 2.7 to 3.0 | | 2.3 | 41 | |
| | IDDHOLD(3) | | • HOLD mode<br>• Internal timer type watchdog timer active (Internal low-speed RC oscillation circuit active)<br>• CF1=$V_{DD}$ or open (External clock mode) | 4.5 to 5.5 | | 0.88 | 95 | |
| | | | | 3.0 to 3.6 | | 0.47 | 47 | |
| | | | | 2.7 to 3.0 | | 0.42 | 39 | |

Note 9-1 : Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note 9- 2: The consumption current values do not include operational current of LVD (Low Voltage Detection) function if not specified.

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Pin/ Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| X'tal HOLD mode consumption current (Note 9-1) (Note 9-2 | IDDHOLD(4) | $V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$ | • X'tal HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• FsX'tal=32.768kHz crystal oscillation mode | 4.5 to 5.5 | | 26 | 135 | μA |
| | | | | 3.0 to 3.6 | | 6.1 | 60 | |
| | | | | 2.7 to 3.0 | | 3.8 | 46 | |
| | IDDHOLD(5) | | • X'tal HOLD mode<br>• CF1=$V_{DD}$ or open (External clock mode)<br>• FmSRC=30kHz internal low-speed RC oscillation mode | 4.5 to 5.5 | | 0.94 | 95 | |
| | | | | 3.0 to 3.6 | | 0.51 | 47 | |
| | | | | 2.7 to 3.0 | | 0.44 | 39 | |

Note 9-1 : Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2 : The consumption current values do not include operational current of LVD (Low Voltage Detection) function if not specified.

## USB Characteristics and Timing at Ta = –40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | | |
|---|---|---|---|---|---|---|
| | | | min | typ | max | unit |
| High level output | $V_{OH(USB)}$ | • 15kΩ±5% to GND | 2.8 | | 3.6 | V |
| Low level output | VOL(USB) | • 1.5kΩ±5% to 3.6V | 0.0 | | 0.3 | V |
| Output signal crossover voltage | $V_{CRS}$ | | 1.3 | | 2.0 | V |
| Differential input sensitivity | $V_{DI}$ | • \|(UAD+)–(UAD–)\|<br>• \|(UBD+)–(UBD–)\| | 0.2 | | | V |
| Differential input common mode range | $V_{CM}$ | | 0.8 | | 2.5 | V |
| High level input | $V_{IH(USB)}$ | | 2.0 | | 3.6 | V |
| Low level input | $V_{IL(USB)}$ | | 0.0 | | 0.8 | V |
| Rise time (full-speed) | $t_{FR}$ | $C_L$=50pF | 4 | | 20 | ns |
| Fall time (full-speed) | $t_{FF}$ | $C_L$=50pF | 4 | | 20 | ns |
| Rise time (low-speed) | $t_{LR}$ | $C_L$=200 to 600pF | 75 | | 300 | ns |
| Fall time (low-speed) | $t_{LF}$ | $C_L$=200 to 600pF | 75 | | 300 | ns |

## F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

| Parameter | Symbol | Pin/Remarks | Conditions | | Specification | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | $V_{DD}1$ | • Excluding power dissipation in the microcontroller block | 3.0 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erase operation | 3.0 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • Write operation | | | 40 | 60 | μs |

## Main System Clock Oscillation

The characteristics of a sample main system clock oscillator circuit shown in Table 1 are measured using an our oscillation characteristics evaluation board and external components with circuit constant values with which the resonator vendor confirmed normal and stable oscillation.

Table 1 shows the characteristics of a oscillator circuit when USB host function is not used. If USB host function is to be used, it is absolutely recommended to use a resonator that satisfies the precision and stability according to the USB standards (±500ppm)

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

| Nominal Frequency | Vendor Name | Resonator Name | Circuit Constant | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | C1 [pF] | C2 [pF] | Rd1 [Ω] | | typ [ms] | max [ms] | |
| 12MHz | MURATA | CSTCE12M0GH5L**-R0 | (33) | (33) | 470 | 3.0 to 5.5 | 0.1 | 0.5 | C1 and C2 integrated SMD type |

The oscillation stabilization time is required for the oscillator to get stabilized in the following cases (see Figure 4):

- Until oscillation is stabilized after $V_{DD}$ goes above the operating voltage lower limit
- Until oscillation is stabilized after the instruction for starting the main clock oscillator circuit is executed
- Until oscillation is stabilized after HOLD mode is released.
- Until oscillation is stabilized after X'tal HOLD mode is released with CFSTOP (OCR register, bit 0) set to 0 and oscillation is started.

## Subsystem Clock Oscillation

Table 2 shows the characteristics of a sample subsystem clock oscillator circuit that are measured using an our oscillation characteristics evaluation board and external components with circuit constant values with which the resonator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

| Nominal Frequency | Vendor Name | Resonator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | C3 [pF] | C4 [pF] | Rf [Ω] | Rd2 [Ω] | | typ [s] | max [s] | |
| 32.768kHz | EPSON TOYOCOM | MC-306 | 18 | 18 | Open | 680k | 2.7 to 5.5 | 1.1 | 3.0 | Applicable CL value=12.5pF SMD type |

The oscillation stabilization time is required for the oscillator to get stabilized in the following cases (see Figure 4) :

- Until oscillation is stabilized after the instruction for starting the subclock oscillator circuit is executed
- Until oscillation is stabilized after HOLD mode is released with EXTOSC (OCR register, bit 6) set to 1 and oscillation is started.

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

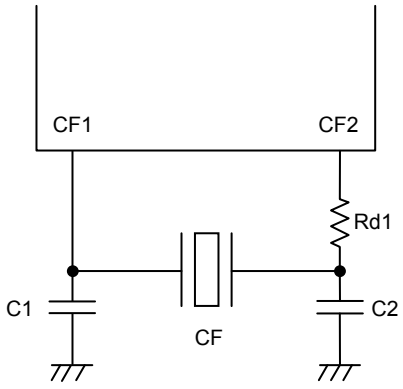



Figure 1 CF Oscillator Circuit

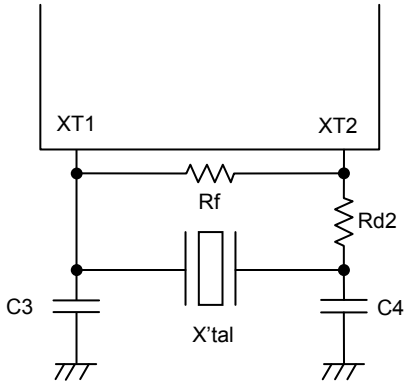



Figure 2 Crystal Oscillator Circuit

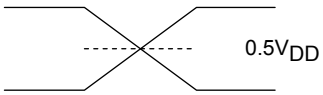
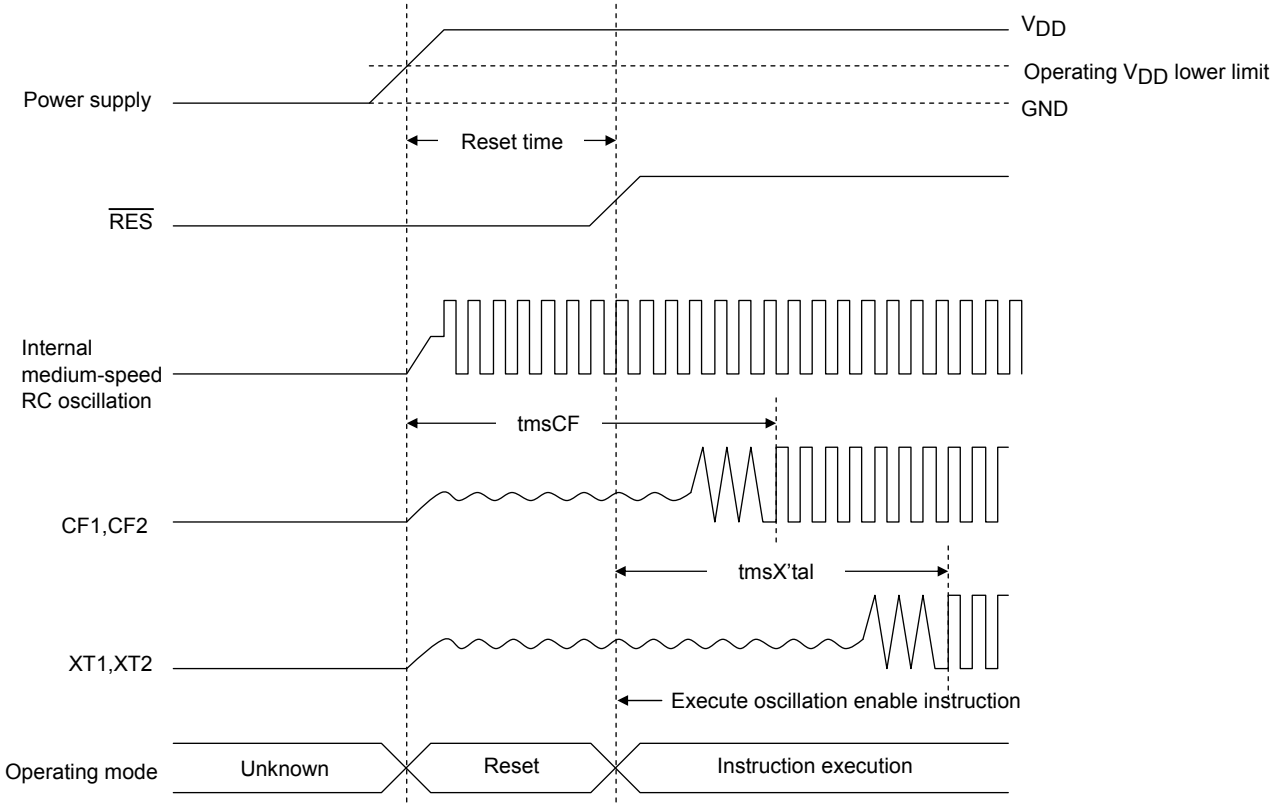
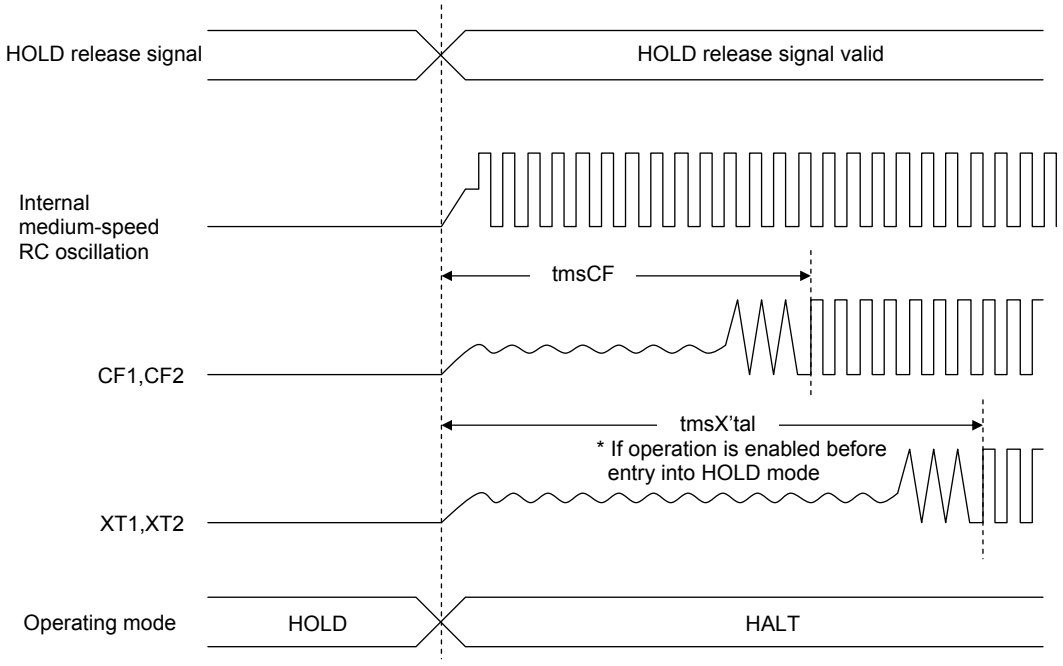



Figure 3 AC Timing Measurement Point

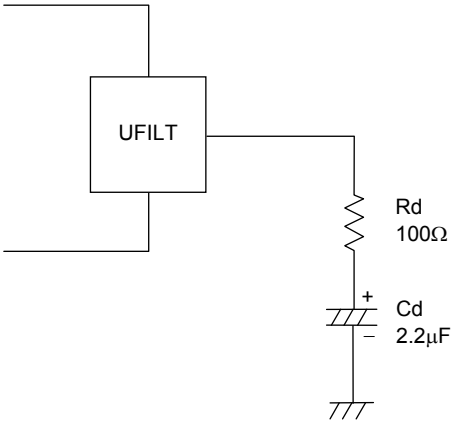



Reset Time and Oscillation Stabilization Time



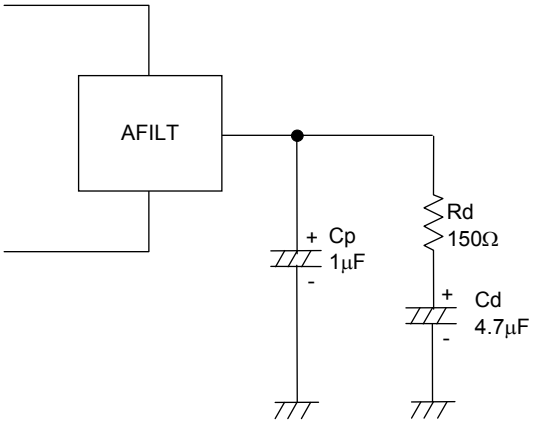

HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



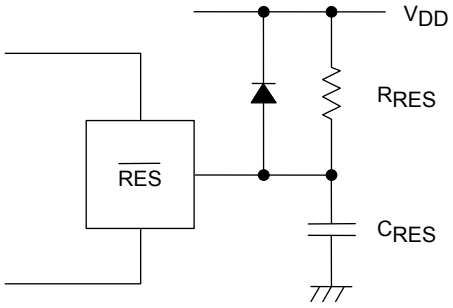

When using the internal PLL circuit to generate the 48MHz clock for USB, it is necessary to connect a filter circuit as shown in the left figure to the UFILT pin. After PLL is set, stabilization time of 20ms or longer must be secured.

Figure 5 External Filter Circuit for the Internal USB-dedicated PLL Circuit




To generate the master clock for the audio interface using the internal PLL circuit, it is necessary to connect a filter circuit as shown in the left figure to the AFILT pin.

Figure 6 External Filter Circuit for Audio Interface (Used with Internal PLL Circuit)




Note :
The external circuit differs depending on which of the power-on reset and low-voltage reset functions is to be used. Refer to the section on the reset functions in the user's manual.

Figure 7 Sample Reset Circuit

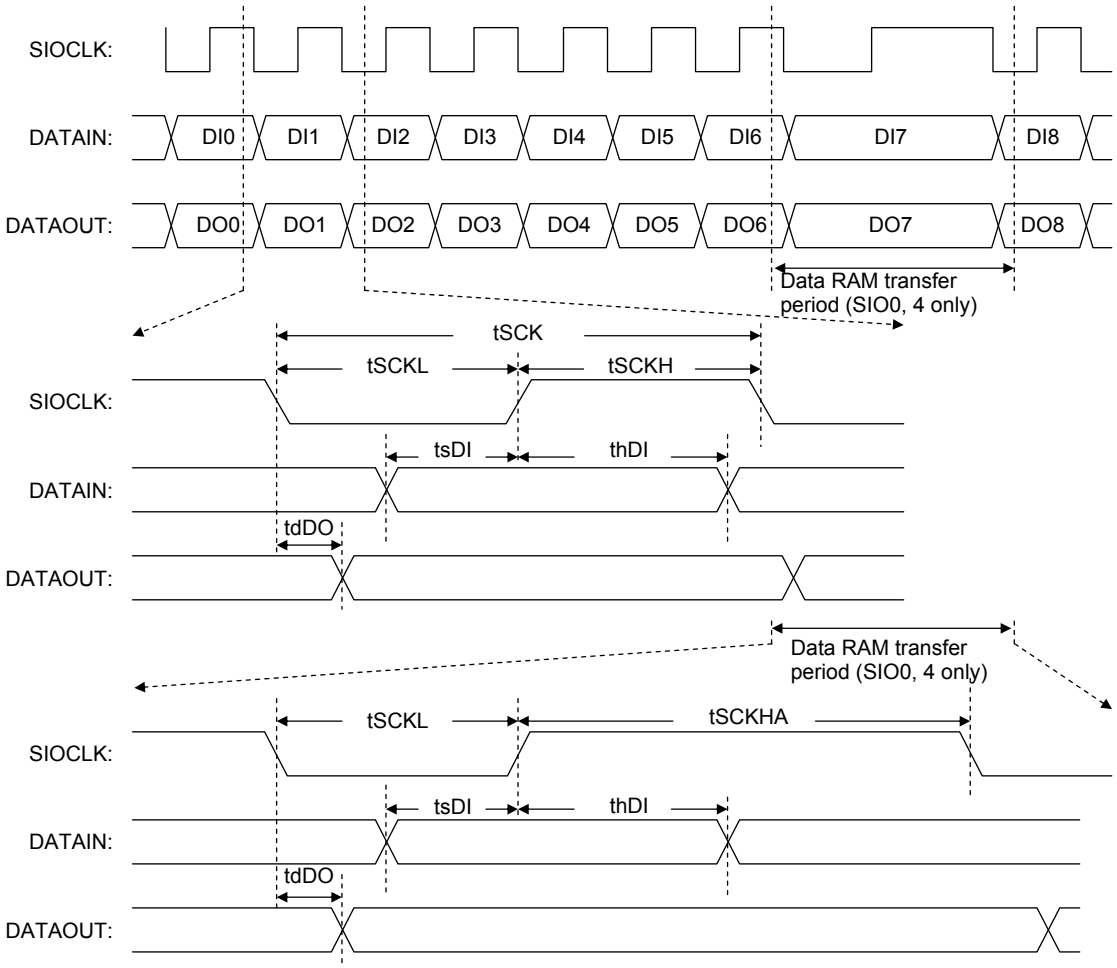



Figure 8 Serial I/O Waveform

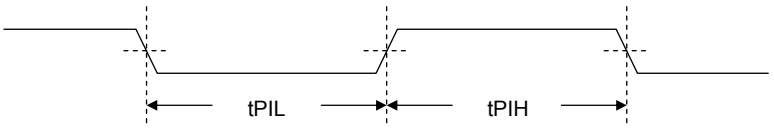



Figure 9 Pulse Input Timing Waveform

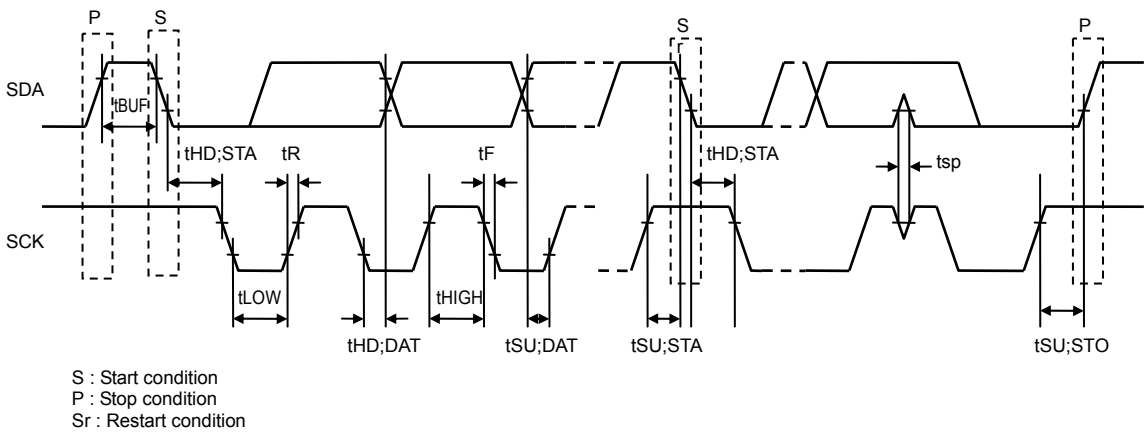



Figure 10 $I^2C$ Timing

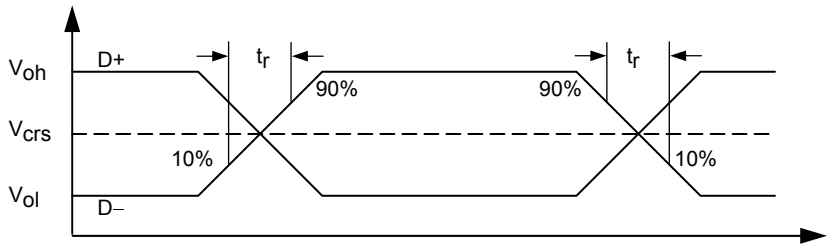



Figure 11 USB Data Signal Timing and Voltage Levels

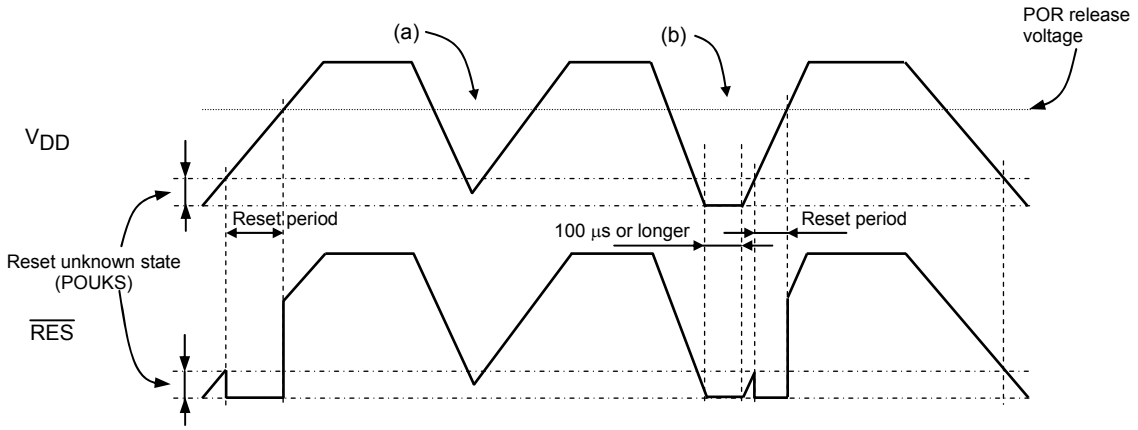



Figure 12 Sample Waveforms for POR-only (LVD deselected) Operation (Reset pin : Pull-up resistor $P_{RES}$ only)

- The POR function generates a reset only when the power is turned on starting at the $V_{SS}$ level.
- No stable reset will be generated if power is turned on again if the power level does not go down to the $V_{SS}$ level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function as explained below or implement an external reset circuit.
- A reset is generated only when power level goes down to the $V_{SS}$ level as shown in (b) and power is turned on again after this condition continues for 100 μs or longer.

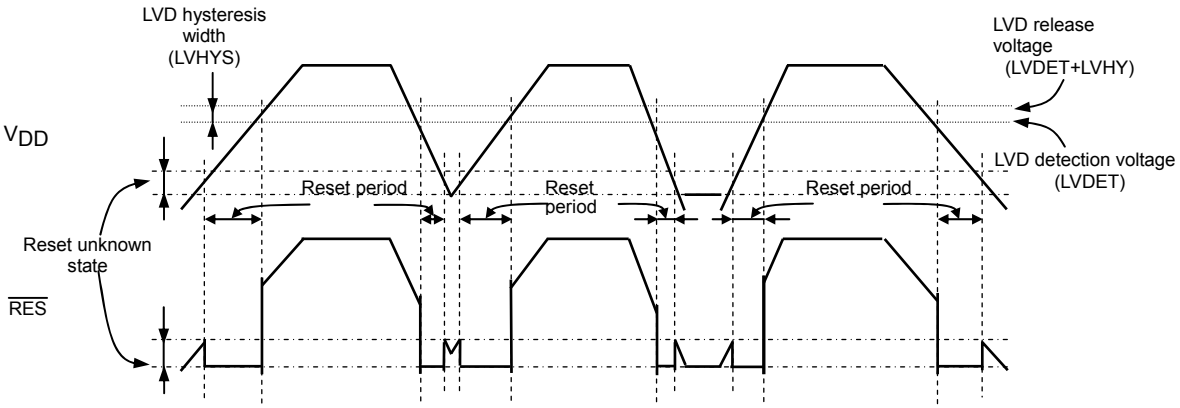



Figure 13 Sample Waveforms for POR+LVD Operation (Reset pin : Pull-up Resistor $P_{RES}$ Only)

- A reset is generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent repetitions of reset release and entry cycles near the detection level.

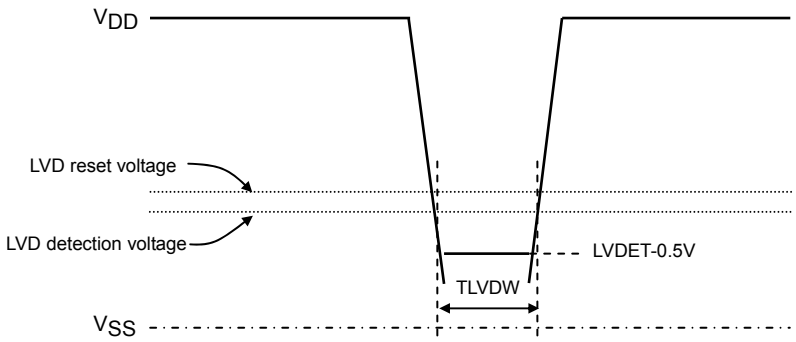



Figure 14 Minimum Low Voltage Detection Width (Sample Temporary Power Interruption/Fluctuation Waveform )

## ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---|---|---|
| LC87F17C8AUWA-2H | SPQFT48 7x7 / SQFP48<br>(Pb-Free / Halogen Free) | 2500 / Tray JEDEC |

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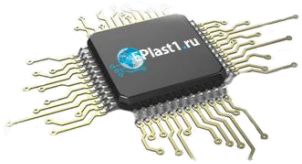


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