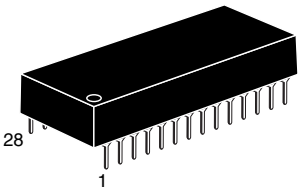
M48T35AV

3.3V, 256Kbit (32Kbit x 8) TIMEKEEPER® SRAM

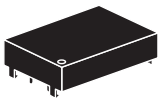
Features

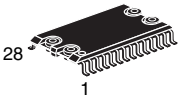
- Integrated, ultra low power SRAM, real-time clock, power-fail control circuit and battery
- BYTEWIDE™ RAM-like clock access
- BCD coded year, month, day, date, hours, minutes, and seconds
- Battery low flag ($\overline{BOK}$)
- Frequency test output for real-time clock
- Automatic power-fail chip deselect and write protection
- Write protect voltages
  (V_{PFD} = Power-fail deselect voltage):
  - M48T35AY: V_{CC} = 4.5 to 5.5V
    $4.2V \le V_{PFD} \le 4.5V$
  - M48T35AV: V_{CC} = 3.0 to 3.6V
    $2.7V \le V_{PFD} \le 3.0V$
- Self-contained battery and crystal in the CAPHAT™ DIP package
- SOIC package provides direct connection for a SNAPHAT® housing containing the battery and crystal
- SNAPHAT® housing (battery and crystal) is replaceable
- Pin and function compatible with JEDEC standard 32Kbit x 8 SRAMs
- RoHS compliant
  - Lead-free second level interconnect



PCDIP28 (PC)
battery/crystal
CAPHAT

SNAPHAT (SH)
battery/crystal





SOH28 (MH)

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1 Description

The M48T35AV TIMEKEEPER® RAM is a 32Kbit x 8 non-volatile static RAM and real-time clock. The monolithic chip is available in two special packages to provide a highly integrated battery backed-up memory and real-time clock solution.

The M48T35AV is a non-volatile pin and function equivalent to any JEDEC standard 32Kb x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 28-pin, 600mil DIP CAPHAT™ houses the M48T35AV silicon with a quartz crystal and a long-life lithium button cell in a single package.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process. Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in tape & reel form.

For the 28-lead SOIC, the battery/crystal package (e.g. SNAPHAT) part numbers are listed in *Table 17 on page 26*.

Figure 1. Logic diagram

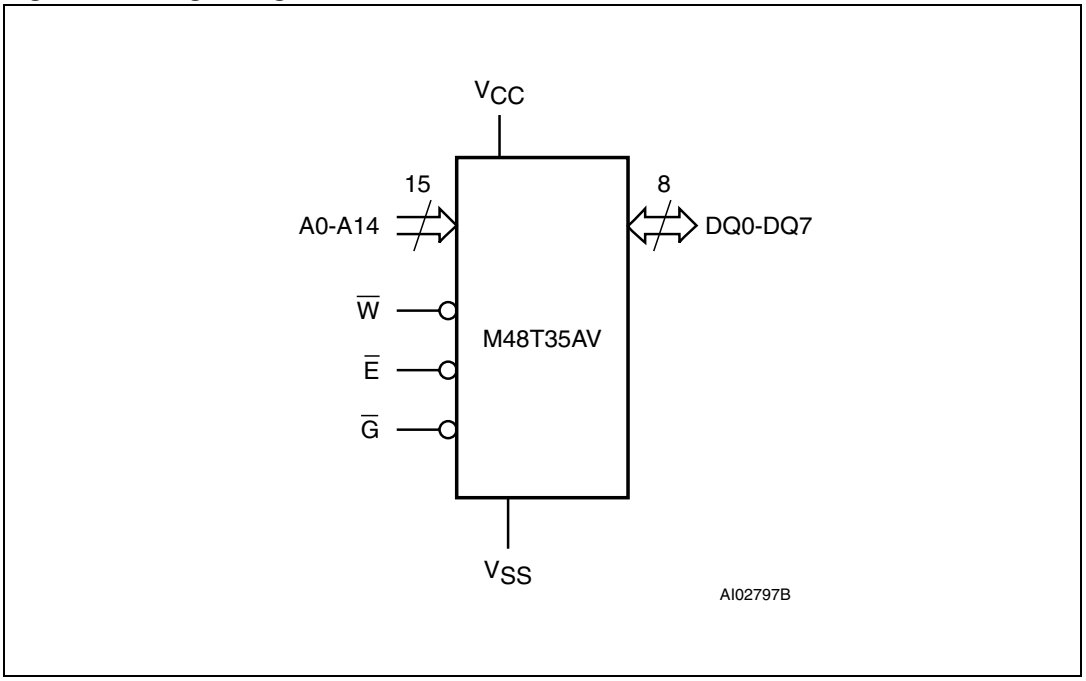


Table 1. Signal names

A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. DIP connections

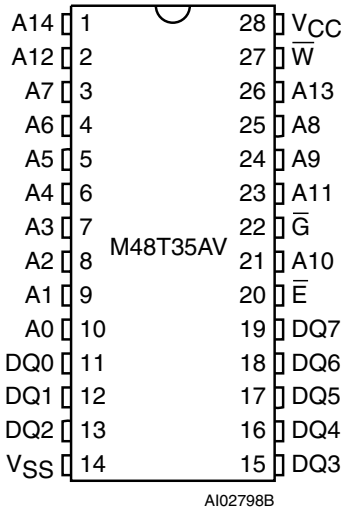


Figure 3. SOIC connections

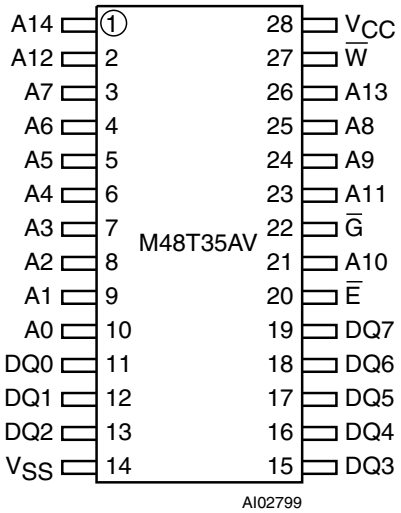
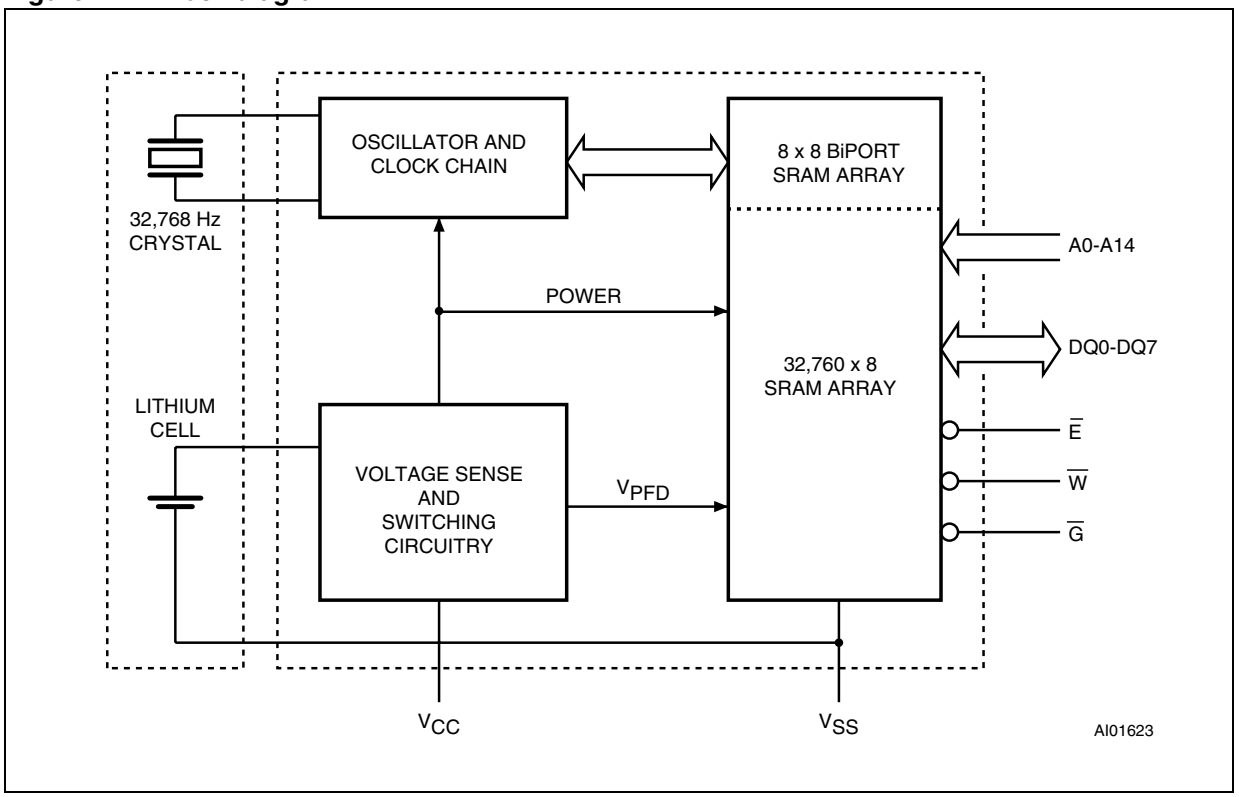


Figure 4. Block diagram



2 Operation modes

As *Figure 4 on page 7* shows, the static memory array and the quartz controlled clock oscillator of the M48T35AV are integrated on one silicon chip. The two circuits are interconnected at the upper eight memory locations to provide user accessible BYTEWIDE™ clock information in the bytes with addresses 7FF8h-7FFFh.

The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48T35AV includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T35AV also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 3V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the Battery Back-up Switchover Voltage (V_{SO}), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	3.0 to 3.6V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery back-up mode

1. See *Table 11 on page 21* for details.

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery back-up switchover voltage.

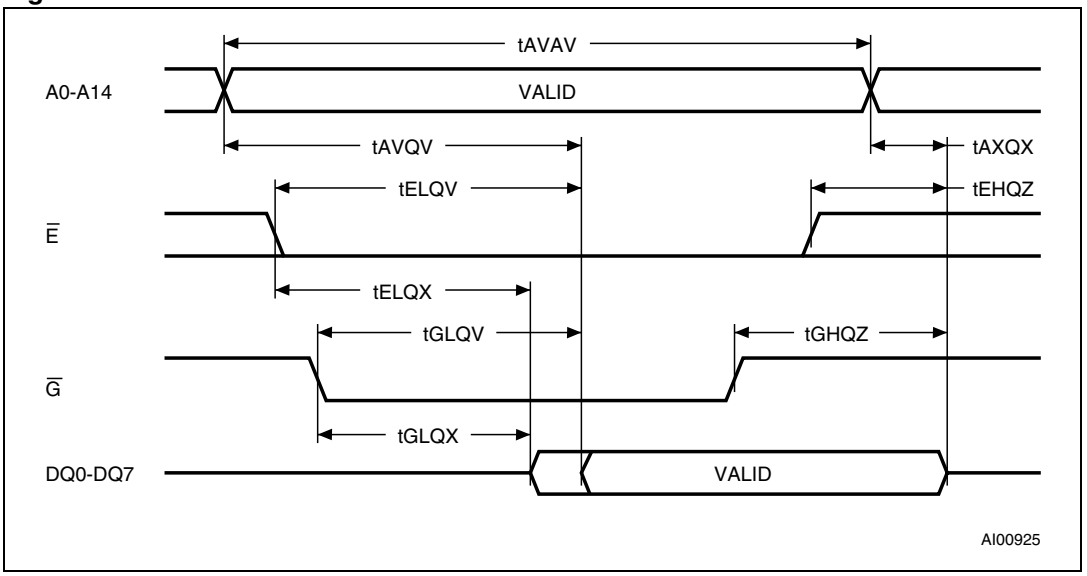
2.1 Read mode

The M48T35AV is in the READ Mode whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied.

If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Figure 5. Read mode AC waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Table 3. Read mode AC characteristics

Symbol	Parameter[1]	M48T35AV –100		Unit
		Min	Max	
t_{AVAV}	READ cycle time	100		ns
t_{AVQV}	Address valid to output valid		100	ns
t_{ELQV}	Chip enable low to output valid		100	ns
t_{GLQV}	Output enable low to output valid		50	ns
t_{ELQX}[2]	Chip enable low to output transition	10		ns
t_{GLQX}[2]	Output enable low to output transition	5		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		50	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		40	ns
t_{AXQX}	Address transition to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. C_L = 5pF.

2.2 Write mode

The M48T35AV is in the WRITE Mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; however, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. Write enable controlled, write mode AC waveform

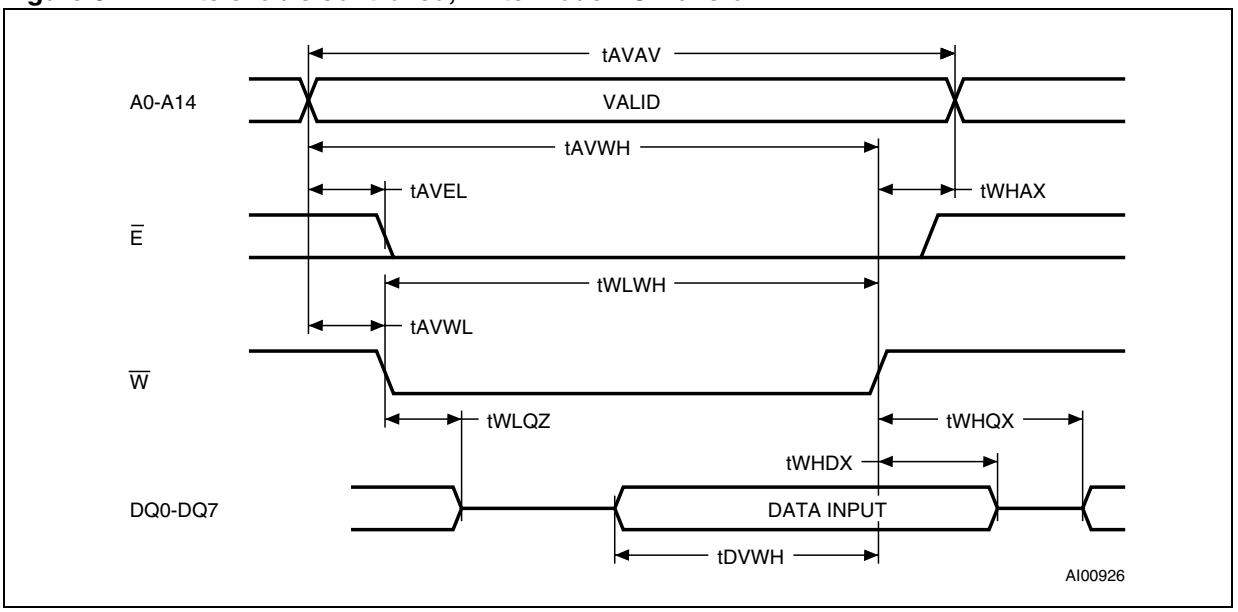


Figure 7. Chip enable controlled, write mode AC waveforms

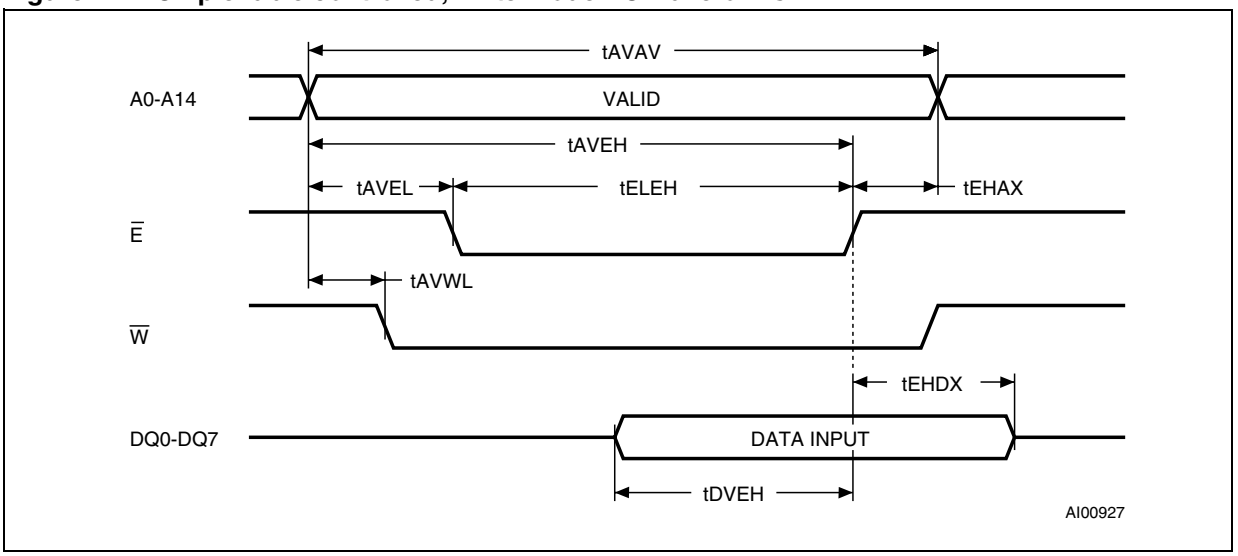


Table 4. Write mode AC characteristics

Symbol	Parameter[1]	M48T35AV		Unit
		Min	Max	
t_{AVAV}	WRITE cycle time	100		ns
t_{AVWL}	Address valid to WRITE enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	WRITE enable pulse width	80		ns
t_{ELEH}	Chip enable low to chip enable high	80		ns
t_{WHAX}	WRITE enable high to address transition	10		ns
t_{EHAX}	Chip enable high to address transition	10		ns
t_{DVWH}	Input valid to WRITE enable high	50		ns
t_{DVEH}	Input valid to chip enable high	50		ns
t_{WHDX}	WRITE enable high to input transition	5		ns
t_{EHDX}	Chip enable high to input transition	5		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		50	ns
t_{AVWH}	Address valid to WRITE enable high	80		ns
t_{AVEH}	Address valid to chip enable high	80		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. C_L = 5pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48T35AV operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), VPFD (min) window (see *Figure 13*, *Table 10*, and *Table 11 on page 21*). All outputs become high impedance, and all inputs are treated as “don't care.”

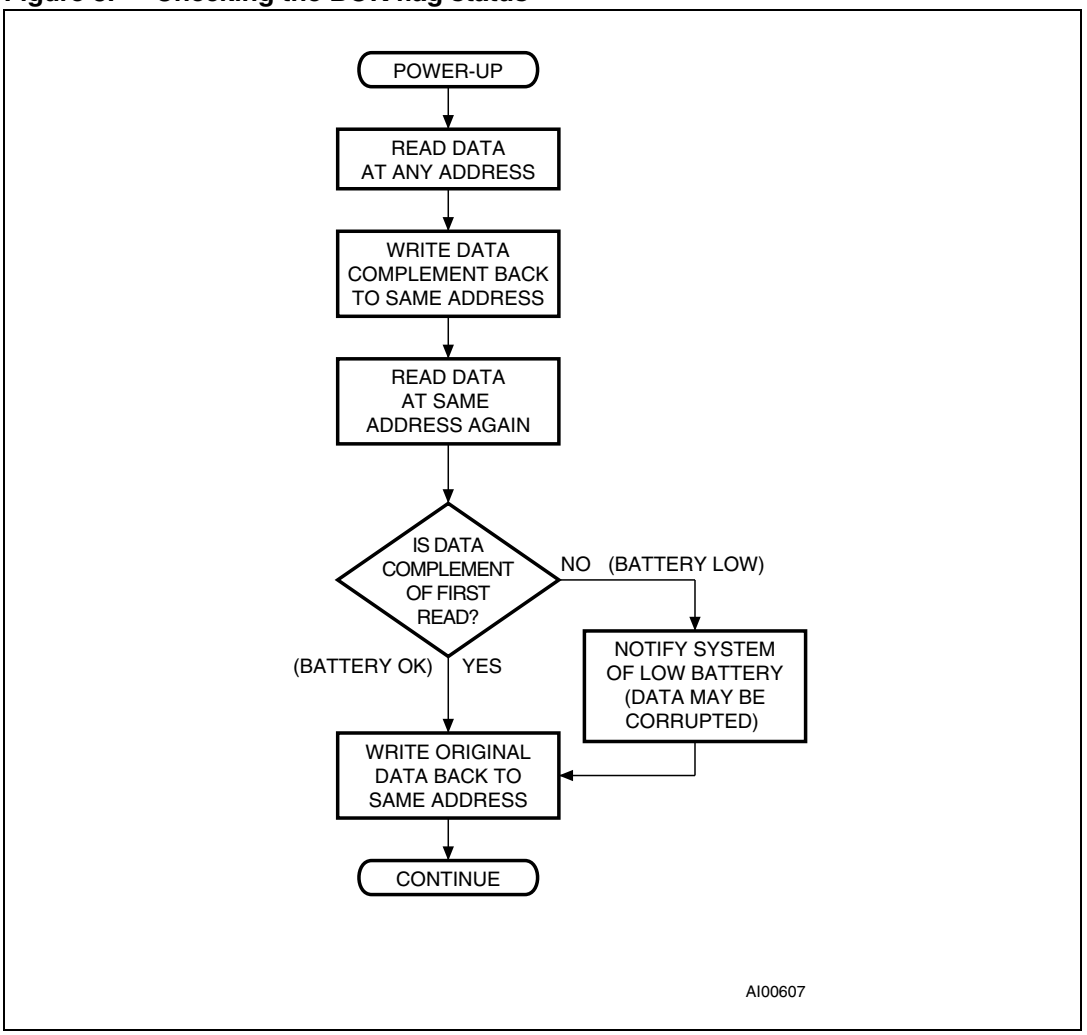
Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T35AV may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T35AV for an accumulated period of at least 7 years when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{rec} (min). $\overline{E}$ should be kept high as V_{CC} rises past V_{PFD} (min) to prevent inadvertent WRITE cycles prior to processor stabilization. Normal RAM operation can resume t_{rec} after V_{CC} exceeds V_{PFD} (max).

Also, as V_{CC} rises, the battery voltage is checked. If the voltage is less than approximately 2.5V, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first WRITE attempted will be blocked. The flag is automatically cleared after the first WRITE, and normal RAM operation resumes. *Figure 8* illustrates how a $\overline{BOK}$ check routine could be structured.

For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 8. Checking the $\overline{BOK}$ flag status



3 Clock operations

3.1 Reading the clock

Updates to the TIMEKEEPER® registers (see *Table 5*) should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control Register 7FF8h. As long as a '1' remains in that position, updating is halted.

After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a '0.'

3.2 Setting the clock

Bit D7 of the Control Register 7FF8h is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER® registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see*Table 5*). Resetting the WRITE Bit to a '0' then transfers the values of all time registers 7FF9h-7FFFh to the actual TIMEKEEPER counters and allows normal operation to resume. The FT Bit and the bits marked as '0' in *Table 5* must be written to '0' to allow for normal TIMEKEEPER and RAM operation. After the WRITE Bit is reset, the next clock update will occur within one second.

See the Application Note AN923, “TIMEKEEPER® Rolling Into the 21st Century” for information on Century Rollover.

3.3 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. The M48T35AV is shipped from STMicroelectronics with the STOP Bit set to a '1.' When reset to a '0,' the M48T35AV oscillator starts within 1 second.

Table 5. Register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 Years				Year				Year	00-99
7FFEh	0	0	0	10 M.	Month				Month	01-12
7FFDh	0	0	10 Date		Date				Date	01-31
7FFCh	0	FT	CEB	CB	0	Day			Century/day	00-01/01-07
7FFBh	0	0	10 Hours		Hours				Hours	00-23
7FFAh	0	10 minutes			Minutes				Minutes	00-59
7FF9h	ST	10 seconds			Seconds				Seconds	00-59
7FF8h	W	R	S	Calibration					Control	

Keys:

S = Sign bit

FT = Frequency test bit (must be set to '0' upon power for normal operation)

R = Read bit

W = Write bit

ST = Stop bit

0 = Must be set to '0'

CEB = Century enable bit

CB = Century bit

Note: When CEB is set to '1,' CB will toggle from '0' to '1' or from '1' to '0' at the turn of the century (dependent upon the initial value set).

When CEB is set to '0,' CB will not toggle. The WRITE Bit does not need to be set to write to CEB.

3.4 Calibrating the clock

The M48T35AV is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T35AV improves to better than +1/–2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see *Figure 9 on page 16*). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome “trim” capacitors. The M48T35AV design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 10 on page 16*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration Byte occupies the five lower order bits (D4-D0) in the Control Register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is the Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a

binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration Byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T35AV may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) Bit, the seventh-most significant bit in the Day Register is set to a '1,' and D7 of the Seconds Register is a '0' (Oscillator Running), DQ0 will toggle at 512 Hz during a READ of the Seconds Register. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the Calibration Byte for correction.

Note: Setting or changing the Calibration Byte does not affect the Frequency Test output frequency.

The FT Bit MUST be reset to '0' for normal clock operations to resume. The FT Bit is automatically Reset on power-down.

For more information on calibration, see Application Note AN934, “TIMEKEEPER® Calibration.”

3.5 Century bit

Bit D5 and D4 of Clock Register 7FFCh contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

Note: The WRITE Bit must be set in order to write to the CENTURY Bit.

Figure 9. Crystal accuracy across temperature

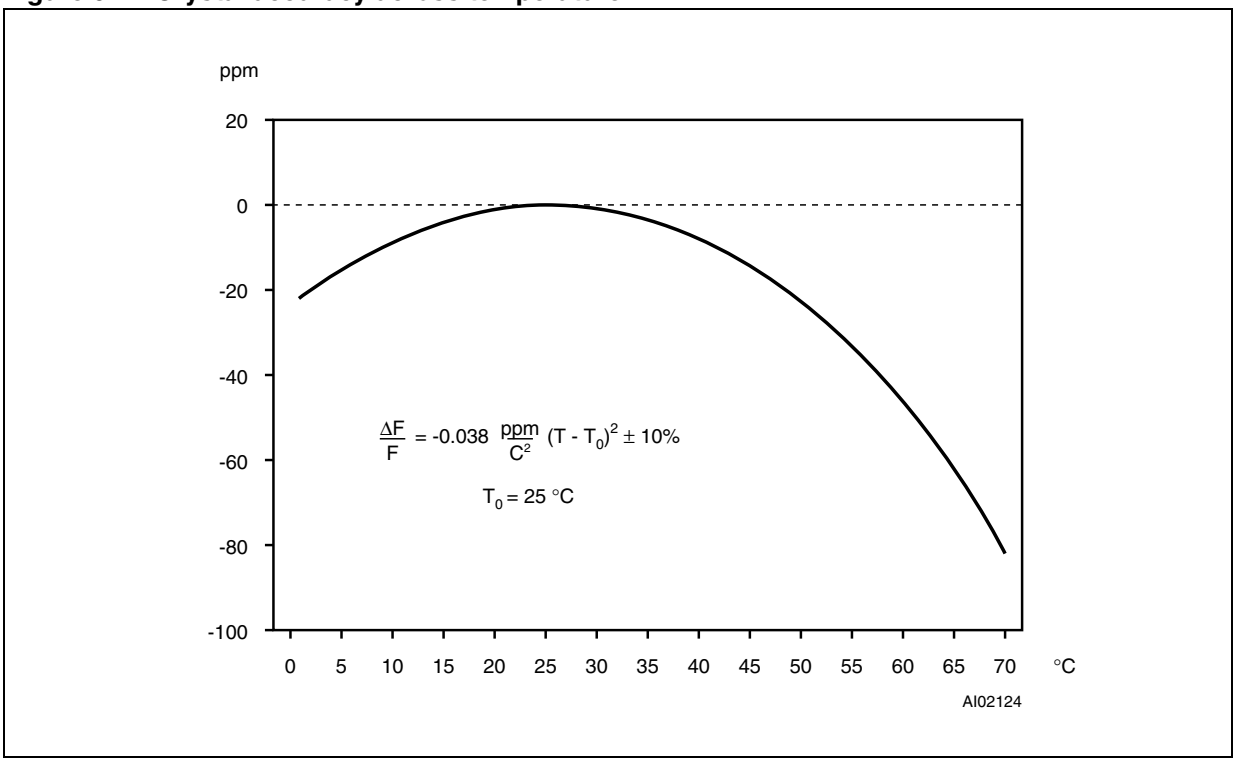
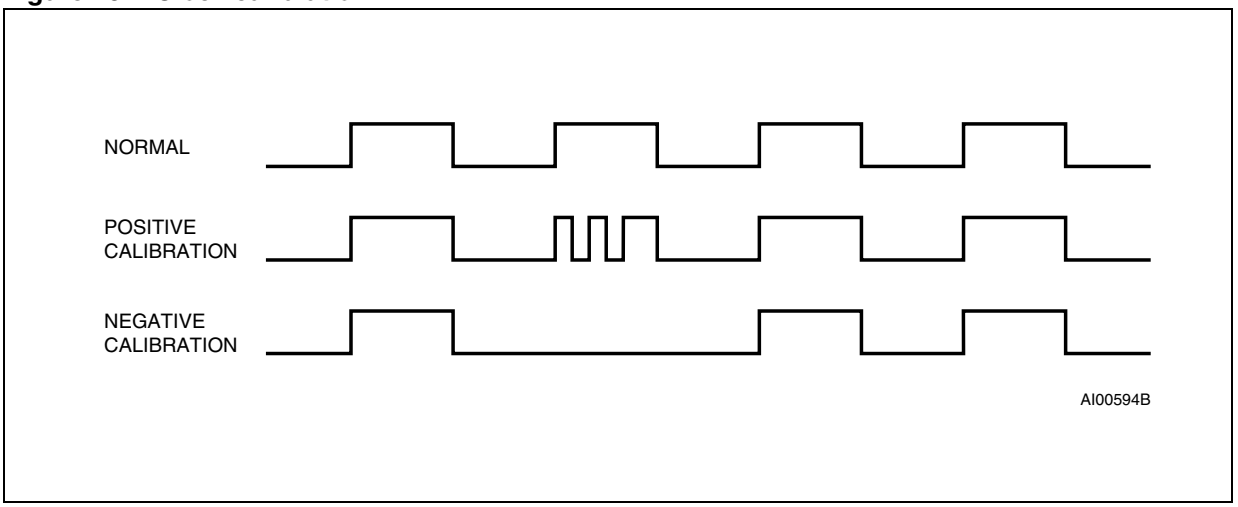


Figure 10. Clock calibration

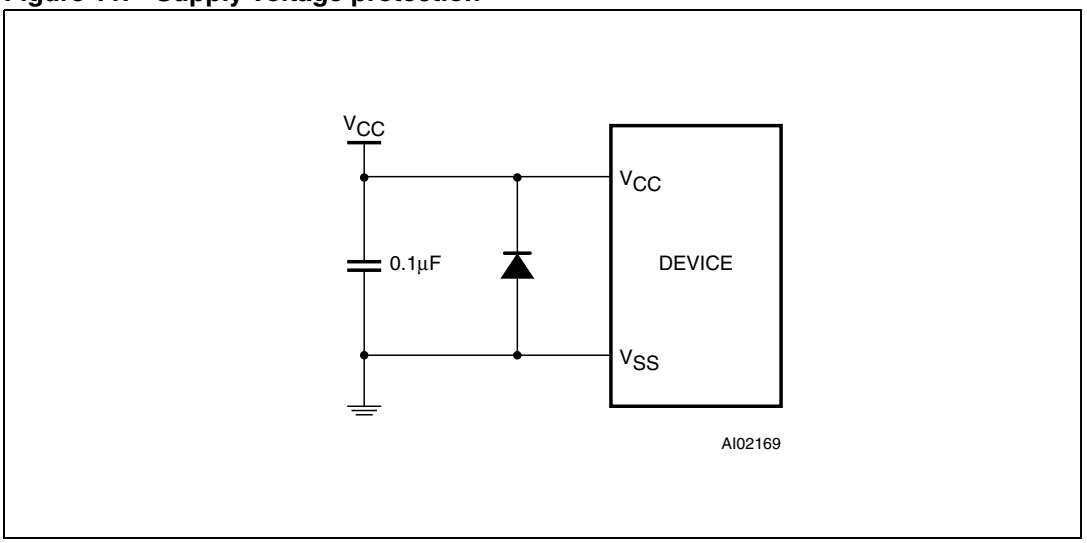


3.6 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A bypass capacitor value of 0.1µF (as shown in *Figure 11*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 11. Supply voltage protection



4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–40 to 85	°C
T_{SLD} (1)(2)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 4.6	V
V_{CC}	Supply voltage	–0.3 to 4.6	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. For DIP package: Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).
2. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7. Operating and AC measurement conditions

Parameter	M48T35AV	Unit
Supply voltage (V_{CC})	3.0 to 3.6	V
Ambient operating temperature (T_A)	0 to 70	°C
Load capacitance (C_L)	50	pF
Input rise and fall times	≤ 5	ns
Input pulse voltages	0 to 3	V
Input and output timing ref. voltages	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 12. AC measurement load circuit

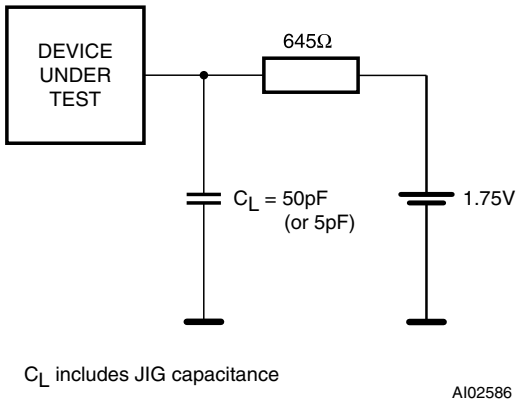


Table 8. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{OUT}(3)	Output capacitance		10	pF

1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

Table 9. DC characteristics

Symbol	Parameter	Test condition(1)	M48T35AV		Unit
			Min	Max	
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC}	Supply current	Outputs open		30	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		2	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		2	mA
V_{IL}(3)	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1mA	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. Outputs deselected.
3. Negative spikes of –1V allowed for up to 10ns once per cycle.

Figure 13. Power down/up mode AC waveforms

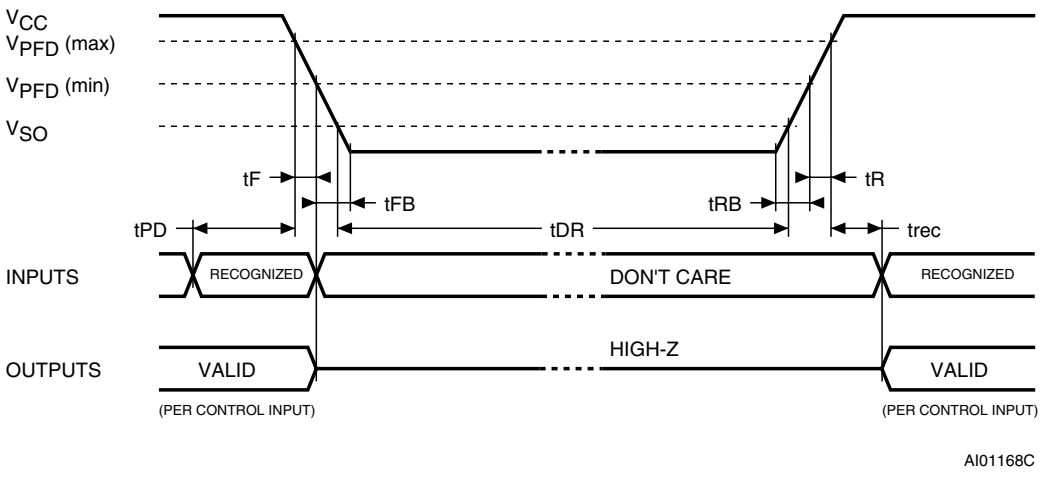


Table 10. Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	150		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{rec}	V_{PFD} (max) to inputs recognized	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 11. Power down/up trip points DC characteristics

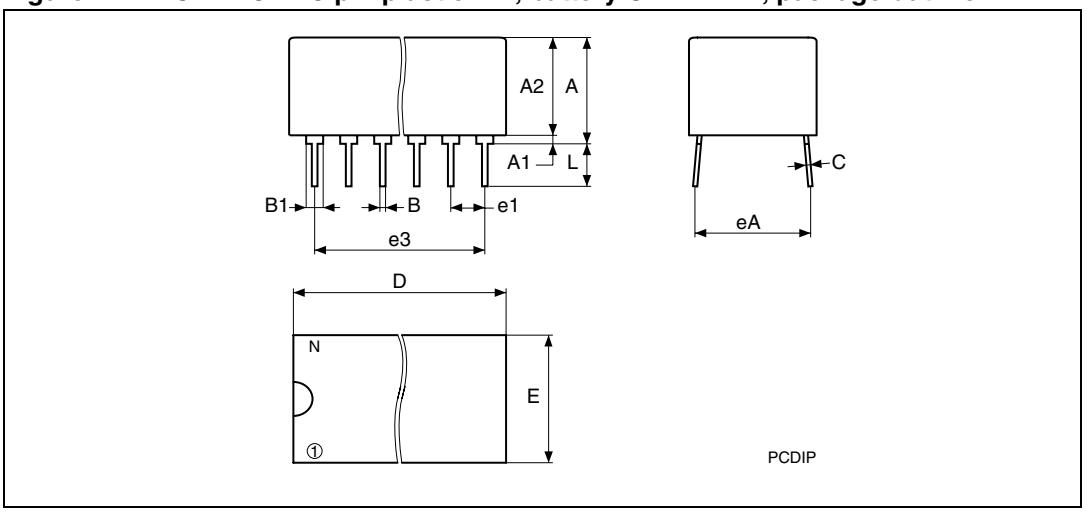
Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	2.7	2.9	3.0	V
V_{SO}	Battery back-up switchover voltage		V_{PFD} –100mV		V
t_{DR}[3]	Expected data retention time	10[4]			YEARS

1. Valid for ambient operating temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. All voltages referenced to V_{SS}.
3. At 25°C, V_{CC} = 0V.
4. CAPHAT and M4T32-BR12SH1 SNAPHAT only, M4T28-BR12SH1 SNAPHAT top t_{DR} = 7 years (typ).

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, package outline

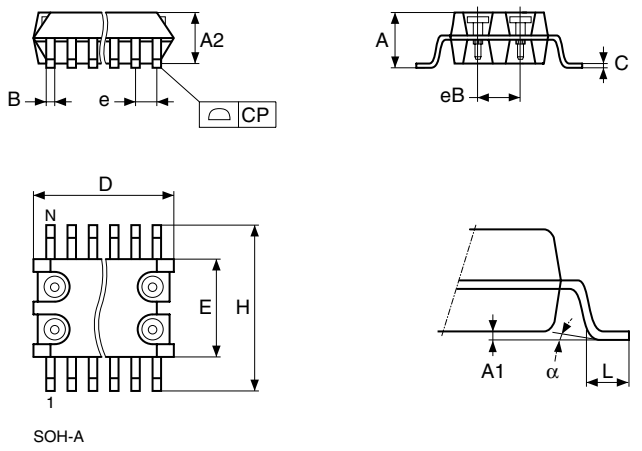


Note: Drawing is not to scale.

Table 12. PCDIP28 – 28-pin plastic DIP, battery CAPHAT™, pack. mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		39.37	39.88		1.550	1.570
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		29.72	36.32		1.170	1.430
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	28			28		

Figure 15. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, package outline

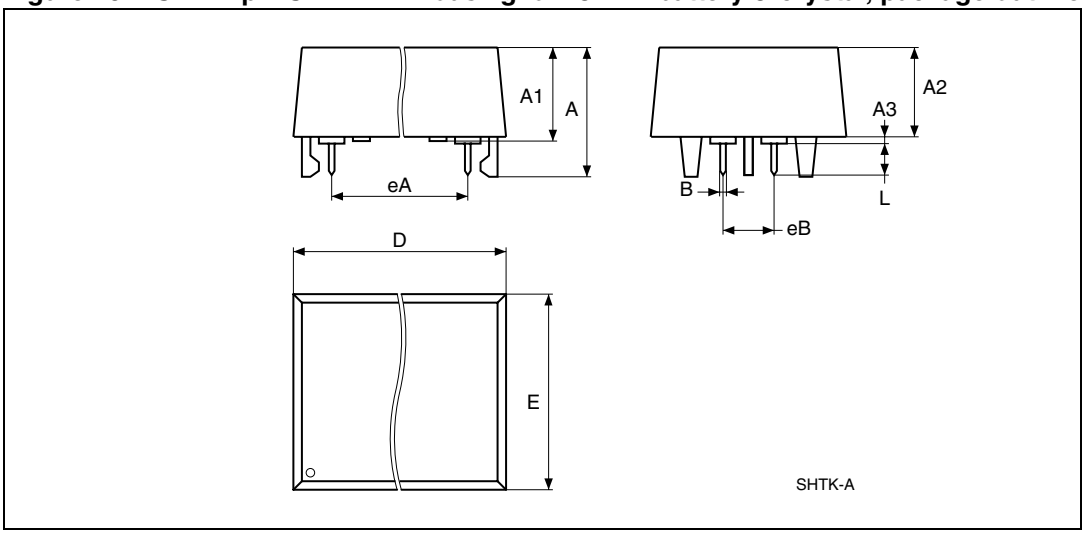


Note: Drawing is not to scale.

Table 13. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, pack. mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 16. SH – 4-pin SNAPHAT housing for 48mAh battery & crystal, package outline

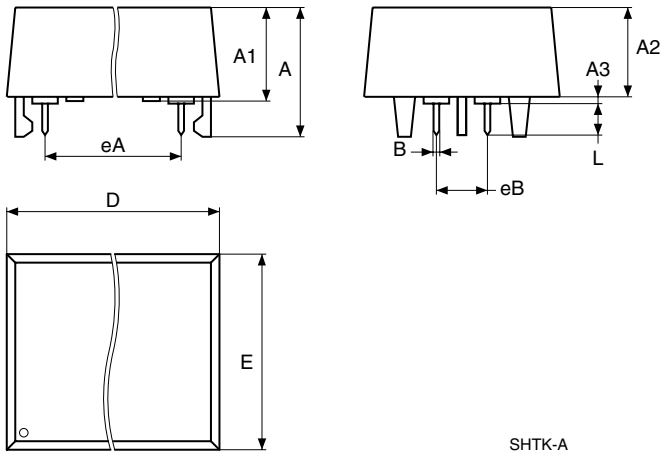


Note: Drawing is not to scale.

Table 14. SH – 4-pin SNAPHAT housing for 48mAh battery & crystal, pack. mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 17. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal, pack. outline



Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal, pack. mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 16. Ordering information scheme

Example: M48T 35AV –10 MH 1 E

Device type

M48T

Supply voltage and write protect voltage

35AV = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.7 to 3.0V

Speed

–10 = 100ns (35AV)

Package

PC = PCDIP28

MH(1) = SOH28

Temperature range

1 = 0 to 70°C

Shipping method

For SOH28:

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

For PCDIP28:

blank = tubes

1. The SOIC package (SOH28) requires the SNAPHAT® battery package which is ordered separately under the part number "M4TXX-BR12SHx" in plastic tubes (see *Table 17*).

Caution: Do not place the SNAPHAT battery package "M4TXX-BR12SH" in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 17. SNAPHAT battery table

Part number	Description	Package
M4T28-BR12SH1	Lithium battery (48mAh) SNAPHAT	SH
M4T32-BR12SH1	Lithium battery (120mAh) SNAPHAT	SH
M4T32-BR12SH6	Lithium battery (120mAh) SNAPHAT, -40 to +85°C crystal	SH

8 Revision history

Table 18. Document revision history

Date	Revision	Changes
Nov-1999	1.0	First Issue
21-Apr-2000	2.0	From Preliminary Data to Data Sheet
29-May-2000	2.1	t_{FB} change (*Table 10*)
20-Jul-2001	3.0	Reformatted; temp./voltage info. added to tables (*Table 8*, *9*, *3*, *4*, *10*, *11*); add Century Bit text
20-May-2002	3.1	Modify reflow time and temperature footnotes (*Table 6*)
31-Mar-2003	4.0	v2.2 template applied; data retention condition updated (*Table 11*)
01-Apr-2004	5.0	Reformatted; updated with lead-free package information (*Table 6*, *16*)
21-Nov-2007	6	Reformatted document; added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*, updated *Table 16*, *17*; removed M48T35AY and all references.

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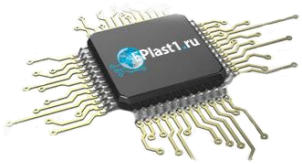

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