Click here for production status of specific part numbers.

MAX5995A/B/C

IEEE 802.3bt-Compliant, Powered Device Interface Controllers with Integrated 91W High-Power MOSFET

General Description

The MAX5995A/MAX5995B/MAX5995C provide a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at/bt standard in a Power-Over-Ethernet (PoE) system. The devices provide the PD with a detection signature, classification signature, and an integrated isolation power switch with startup inrush current control. During the startup period, the devices limit the current to 135mA (typ) before switching to the higher current limit (1800mA to 2400mA, typ) when the isolation power MOSFET is fully enhanced. The devices feature Multi-Event classification, Intelligent MPS (MAX5995B/MAX5995C), Autoclass (MAX5995C), and an input UVLO with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. The devices can withstand a maximum voltage of 100V at the input.

The devices support a Multi-Event classification method, as specified in the IEEE 802.3bt standard, and provide a signal to indicate from Type 1 to Type 4 Power Sourcing Equipment (PSE). The devices can detect the presence of a wall adapter power source connection and allow a smooth switch-over from the PoE power source to the wall power adapter.

The devices also provide a power-good (PG) signal, two-step current limit and foldback control, overtemperature protection. A sleep mode feature in the MAX5995A/MAX5995B minimizes low power consumption while generating the Maintain Power Signature (MPS) to maintain PSE connection. An Ultra-Low-Power sleep mode feature in the MAX5995A/MAX5995B further reduces power consumption while still generating MPS current. The MAX5995B/MAX5995C provides Intelligent Maintain Power Signature (IMPS) feature to automatically enable MPS current by detecting the port current. The devices feature a LED driver that is activated during sleep mode, Ultra-Low-Power sleep mode (MAX5995A/MAX5995B), and Intelligent MPS mode (MAX5995B/MAX5995C). Multi-Event indication feature provides patterned signals to indicate power level allocated from PSE to PD in 5 different scenarios. The MAX5995C provides Autoclass feature to enable advanced applications that allow the PSE to effectively optimize power allocation to PD.

The MAX5995A/MAX5995B/MAX5995C are available in a 16-pin, 5mm x 5mm, TQFN power package. These devices are rated over the -40°C to 125°C (MAX5995AATE/BATE/CATE) and -40°C to 85°C (MAX5995AETE/BETE/CETE) temperature ranges.

Applications

- IEEE 802.3bt Powered Devices
- VOIP Phones, IP Security Cameras
- Wireless Access Point
- Small Cell, Pico Cell
- Lighting
- Building Automation

Benefits and Features

- IEEE 802.3af/at/bt Compliant
- Type 1~4 PSE Classification Indicator or an External Wall Adapter Indicator Output
- Simplified Wall Adapter Interface
- Multi-Event Classification 0–8
- Intelligent MPS (MAX5995B/MAX5995C, Patent US9152161)
- Sleep Mode and Ultra-Low-Power Sleep Mode (MAX5995A/MAX5995B)
- 100V Input Absolute Maximum Rating
- Inrush Current Limit During Startup
- Current Limit During Normal Operation
- Current Foldback Protection
- Undervoltage Lockout at 36V
- LED Driver with Programmable LED Current (MAX5995A/MAX5995B)
- Overtemperature Protection
- Multi-Event Power Level Indication
- Autoclass Feature (MAX5995C)
- Thermally Enhanced, 5mm x 5mm, 16-Pin TQFN

19-100401; Rev 3; 7/19

maxim integrated™

Absolute Maximum Ratings

V_{DD} to V_{SS} ..... -0.3V to +100V
RTN, WAD, PG, MEC, DET to V_{SS} ..... -0.3V to +100V
CLSA, CLSB, $\overline{SL}$, $\overline{WK}$/AUC, $\overline{ULP}$, LED to V_{SS} ..... -0.3V to +6V
Maximum Current on CLSA, CLSB (100ms maximum) 100mA
Continuous Power Dissipation (T_A = +70°C) (Note 1) (TQFN (derate 28.6mW/°C above +70°C))
Multilayer Board 2285.7mW

Operating Temperature Range
MAX5995AETE/BETE/CETE .....-40°C to +85°C
MAX5995AATE/BATE/CATE .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300ºC
Soldering Temperature (reflow) .....+260°C

Note 1: Maximum power dissipation is obtained using JEDEC JESD51-5 and JESD51-7 specifications.

Note 2: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN-EP

Package Code	T1655+4
Outline Number	21-0140
Land Pattern Number	90-0121
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	35°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	2.7°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, MEC, WK and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C (MAX5995AATE/BATE/CATE) or -40°C to +85°C (MAX5995AETE/BETE/CETE), unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DETECTION MODE						
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 4)			10	µA
Effective Differential Input Resistance	dR	V_{IN} = 1.4V up to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = MEC (Note 5)	23.95	25	25.5	kΩ
CLASSIFICATION MODE						
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 6)	22	22.8	23.6	V
Classification Stability Time				0.2		ms
Classification Current	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 619Ω	0		3.96	mA
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, R_{CLS} = 118Ω	9.12		11.88	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 66.5Ω	17.2		19.8	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 43.2Ω	26.3		29.7	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 30.9Ω	36.4		43.6	
Mark Event Threshold	V_{THM}	V_{IN} falling	10.1	10.7	11.6	V
Hysteresis on Mark Event Threshold				0.82		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V < V_{IN} < 10.1V	1.0		3.5	mA
Reset Event Threshold	V_{THR}	V_{IN} falling	2.8	3.8	5.2	V
POWER MODE						
V_{IN} Supply Voltage Range					60	V
V_{IN} Supply Current	I_Q	Current through internal MOSFET = 0		0.25	0.75	mA
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising	34.3	35.4	36.6	V
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling	30			V
V_{IN} Turn-On/-Off Hysteresis	V_{HYST_UVLO}	(Note 7)	4.2			V
V_{IN} Deglitch Time	t_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 8)	30	120		µs
Inrush to Operating Mode Delay	t_{DELAY}	From PG pulled low to high when entering into power mode, V_{IN} = 48V, C_{OUT} = 47µF	90	96	102	ms
Isolation Power MOSFET On-Resistance	R_{ON_ISO}	I_{RTN} = 950mA, T_J = +25°C		0.1	0.2	Ω
		I_{RTN} = 950mA, T_J = +85°C		0.15	0.25	
		I_{RTN} = 950mA, T_J = +125°C		0.2		

Electrical Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, MEC, WK and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C (MAX5995AATE/BATE/CATE) or -40°C to +85°C (MAX5995AETE/BETE/CETE), unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RTN Leakage Current	I_{RTN_LKG}	V_{RTN} = 12.5V to 30V				10	µA
CURRENT LIMIT							
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{RTN} - V_{SS} = 1.5V		90	135	182	mA
Current Limit During Normal Operation	I_{LIM}	5 Event Detected	After inrush completed, V_{RTN} = 1V (Note 9)	1800	2400	3000	mA
		1 to 4 Event Detected	After inrush completed, V_{RTN} = 1V (Note 9)	1350	1800	2250	
Current Limit in Foldback Condition	I_{LIM_FLDBK}	Both during inrush and after inrush completed V_{RTN} - V_{SS} = 7.5V			53		mA
Foldback Threshold		V_{RTN} (Note 10)		6.5	7	7.5	V
LOGIC							
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 48V (referenced to RTN)		8	9	10	V
WAD Detection Threshold Hysteresis		V_{WAD} rising, V_{RTN} = 0V, V_{SS} unconnected			0.35		V
WAD Input Current	I_{WAD_LKG}	V_{WAD} = 10V (referenced to RTN)				3.5	µA
PG Sink Current		V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		125	230	375	µA
PG Off-Leakage Current		V_{PG} = 60V				1	µA
MEC							
Pulse Width of START Bit					256		µs
50% Pulse Width					512		µs
75% Pulse Width					768		µs
Repetitive Period					1024		µs
MEC Sink Current		V_{MEC} = 3.5V (referenced to RTN), V_{SS} disconnected		1	1.5	2.35	mA
MEC Off-Leakage Current		V_{MEC} = 48V				1	µA
SLEEP MODE/ULTRA-LOW-POWER SLEEP MODE (MAX5995A/MAX5995B)							
$\overline{WK}$ and $\overline{ULP}$ Logic Threshold	V_{TH}	$\overline{WK}$ falling and $\overline{ULP}$ rising and falling		1.5		3	V
$\overline{SL}$ Logic Threshold		$\overline{SL}$ falling		0.75	0.8	0.85	V
$\overline{SL}$ Current		R_{SL} = 0Ω			140		µA

Electrical Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, MEC, WK and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C (MAX5995AATE/BATE/CATE) or -40°C to +85°C (MAX5995AETE/BETE/CETE), unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED Current Amplitude	I_{LED}	$R_{\overline{SL}}$ = 60.4kΩ, V_{LED} = 3.5V (MAX5995A/MAX5995B)	10	10.5	11.5	mA
		$R_{\overline{SL}}$ = 30.1kΩ, V_{LED} = 3.75V	19.5	20.9	22.5	
		$R_{\overline{SL}}$ = 30.1kΩ, V_{LED} = 4V	19			
LED Current Programmable Range			10		20	mA
LED Current with Grounded SL		$V_{\overline{SL}}$ = 0V	20.5	24.5	28.5	mA
LED Current Frequency	f_{ILED}	Sleep and Ultra-Low-Power sleep modes		250		Hz
LED Current Duty Cycle	D_{ILED}	Sleep and Ultra-Low-Power sleep modes		25		%
V_{DD} Current Amplitude	I_{VDD}	Normal sleep mode, V_{LED} = 3.5V	10	11	12.2	mA
Internal Current Duty Cycle	D_{IVDD}	Normal and Ultra-Low-Power sleep modes		75		%
Internal Current Enable Time	$t_{\overline{ULP}}$	Ultra-Low-Power sleep mode	80	84	90	ms
Internal Current Disable Time	$t_{\overline{ULP}\_DIS}$	Ultra-Low-Power sleep mode	217	228	240	ms
$\overline{SL}$ Delay Time	$t_{\overline{SL}}$	Time $V_{\overline{SL}}$ must remain below the $\overline{SL}$ logic threshold to enter sleep and Ultra-Low-Power modes (MAX5995A)	5.4	6	6.6	s
AUTOCLASS (MAX5995C)						
AUTOCLASS Detection Time			76		87	ms
AUC (MAX5995C)						
AUC Pullup Current	I_{AUC_PUP}		8.5	9	9.5	µA
AUC Voltage Threshold	V_{AUC1}		0.47	0.5	0.53	V
	V_{AUC2}		1.73	1.8	1.87	
	V_{AUC3}		4.31	4.4	4.49	
MAINTAIN POWER SIGNATURE						
PoE MPS Current Rising Threshold	I_{MPS_RISE}	MAX5995B/MAX5995C		28.7		mA
PoE MPS Current Falling Threshold	I_{MPS_FALL}	MAX5995B/MAX5995C		24		mA
PoE MPS Current Threshold Hysteresis	I_{MPS_HYS}	MAX5995B/MAX5995C		4.3		mA
PoE MPS Time High	t_{MPS_HIGH}	Default for MAX5995A/MAX5995B, AUC floating for MAX5995C	80	84	90	ms
PoE MPS Time Low	t_{MPS_LOW}	Default for MAX5995A/MAX5995B, AUC floating for MAX5995C	217	228	240	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC 332K 1%tollerance to VSS (MAX5995C)	45	48	51	ms

Electrical Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω, and $R_{\overline{SL}}$ = 60.4kΩ. RTN, WAD, PG, MEC, WK and $\overline{ULP}$ unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C (MAX5995AATE/BATE/CATE) or -40°C to +85°C (MAX5995AETE/BETE/CETE), unless otherwise noted. Typical values are at T_A = +25ºC. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PoE MPS Time Low	t_{MPS_LOW}	AUC 332K 1% tolerance to V_{SS} (MAX5995C)	252	264	275	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC 121K 1% tolerance to V_{SS} (MAX5995C)	30	32	34	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC 121K 1% tolerance to V_{SS} (MAX5995C)	268	280	292	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC short to V_{SS} (MAX5995C)	14	16	18	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC short to V_{SS} (MAX5995C)	280	296	308	ms
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SD}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	V_{CDLY_HYS}	T_J falling		30		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 4: The input offset current is illustrated in *Detailed Desciption*.

Note 5: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}.

Note 6: Classification current is turned off whenever the device is in power mode.

Note 7: UVLO hysteresis is guaranteed by design, not production tested.

Note 8: A 20V glitch on input voltage, which takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY} does not cause the MAX5995A/MAX5995B/MAX5995C to exit power-on mode.

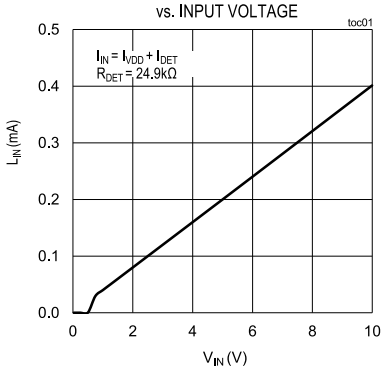
Note 9: Maximum current limit during normal operation is guaranteed by design; not production tested.

Note 10: In power mode, current-limit foldback is used to reduce the power dissipation in the isolation MOSFET during an overload condition across V_{DD} and RTN.

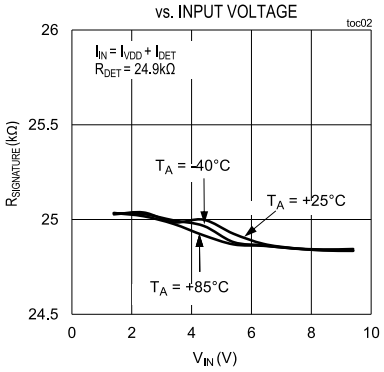
Typical Operating Characteristics

(V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSA} = 615Ω, R_{SL} = 60.4kΩ. RTN, WAD, MEC, WK, and ULP unconnected. All voltages are referenced to V_{SS}.)

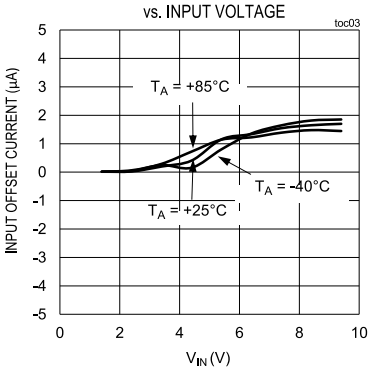
DETECTION CURRENT vs. INPUT VOLTAGE



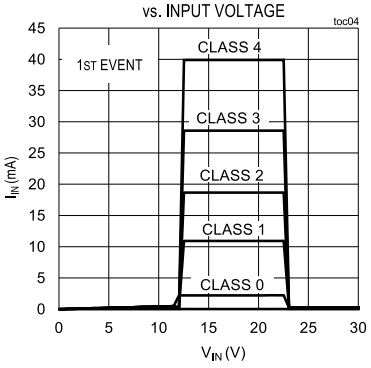
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



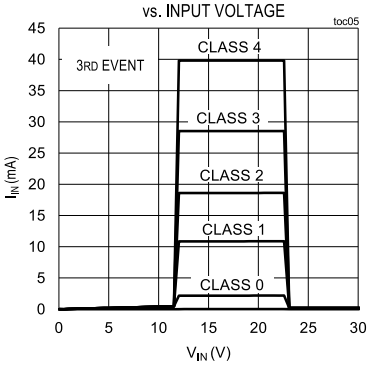
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



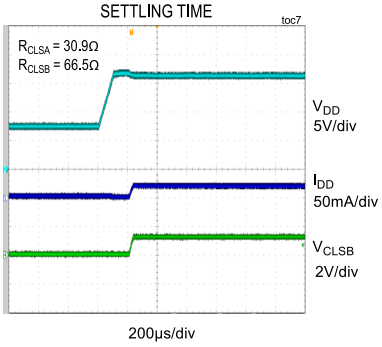
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



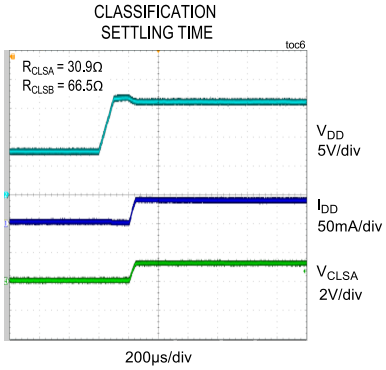
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



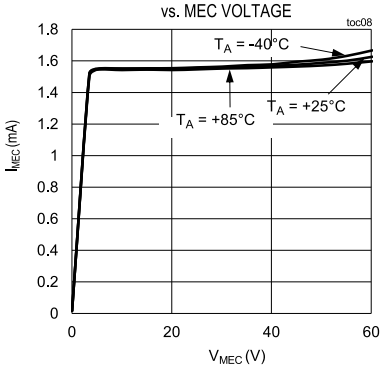
CLASSIFICATION SETTLING TIME



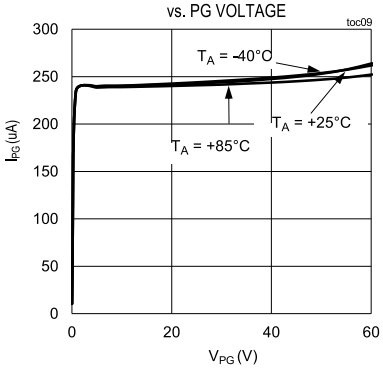
CLASSIFICATION SETTLING TIME



MEC SINK CURRENT vs. MEC VOLTAGE



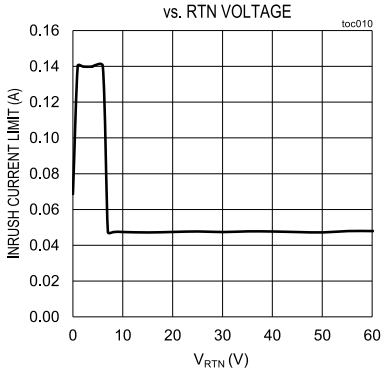
PG SINK CURRENT vs. PG VOLTAGE



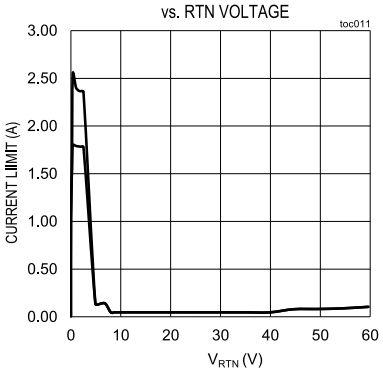
Typical Operating Characteristics (continued)

(V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSA} = 615Ω, R_{SL} = 60.4kΩ. RTN, WAD, MEC, WK, and ULP unconnected. All voltages are referenced to V_{SS}.)

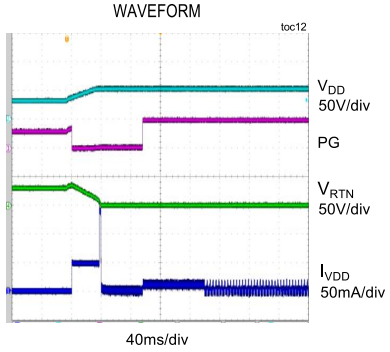
INRUSH CURRENT LIMIT vs. RTN VOLTAGE



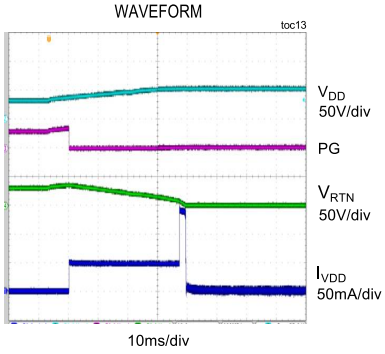
NORMAL OPERATION LIMIT vs. RTN VOLTAGE



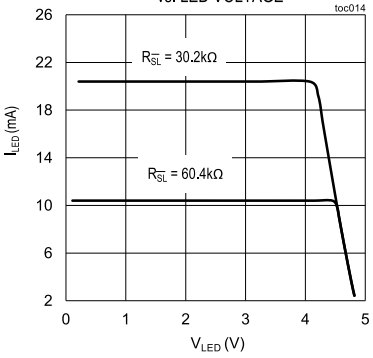
STARTUP INRUSH COTROL WAVEFORM



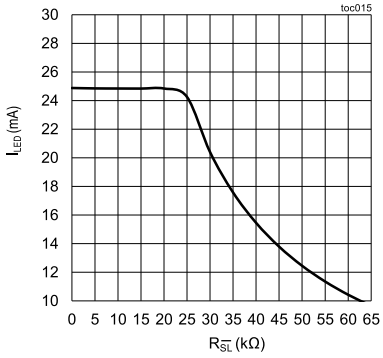
STARTUP INRUSH COTROL WAVEFORM



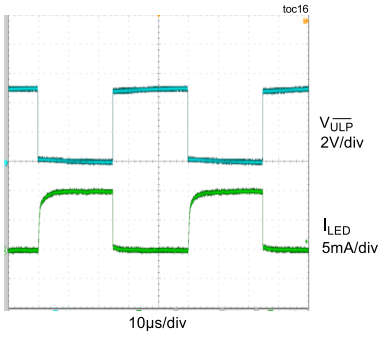
LED CURRENT vs. LED VOLTAGE



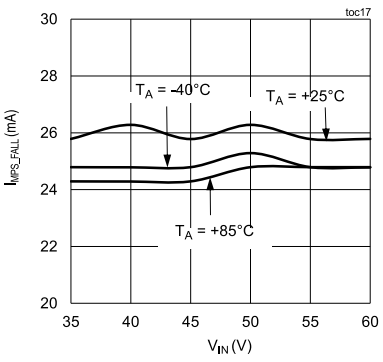
LED CURRENT vs. $R_{\overline{SL}}$



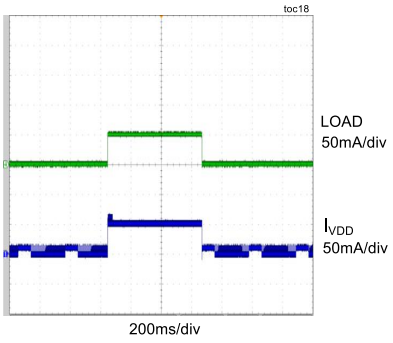
DRIVING LED WITH $\overline{ULP}$ IN POWER MODE



MPS CURRENT FALLING THRESHOLD vs. INPUT VOLTAGE



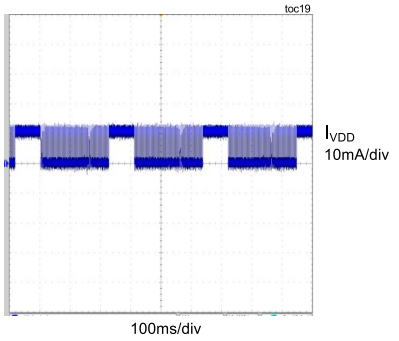
MPS CURRENT WAVEFORM WITH LOAD CHANGE



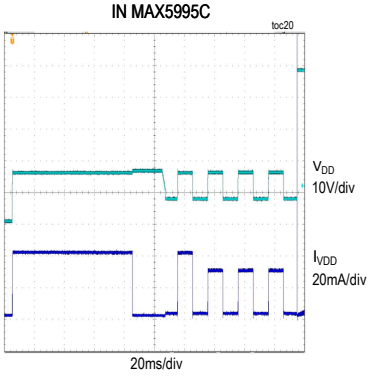
Typical Operating Characteristics (continued)

(V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSA} = 615Ω, R_{SL} = 60.4kΩ. RTN, WAD, MEC, WK, and ULP unconnected. All voltages are referenced to V_{SS}.)

MPS CURRENT WAVEFORM

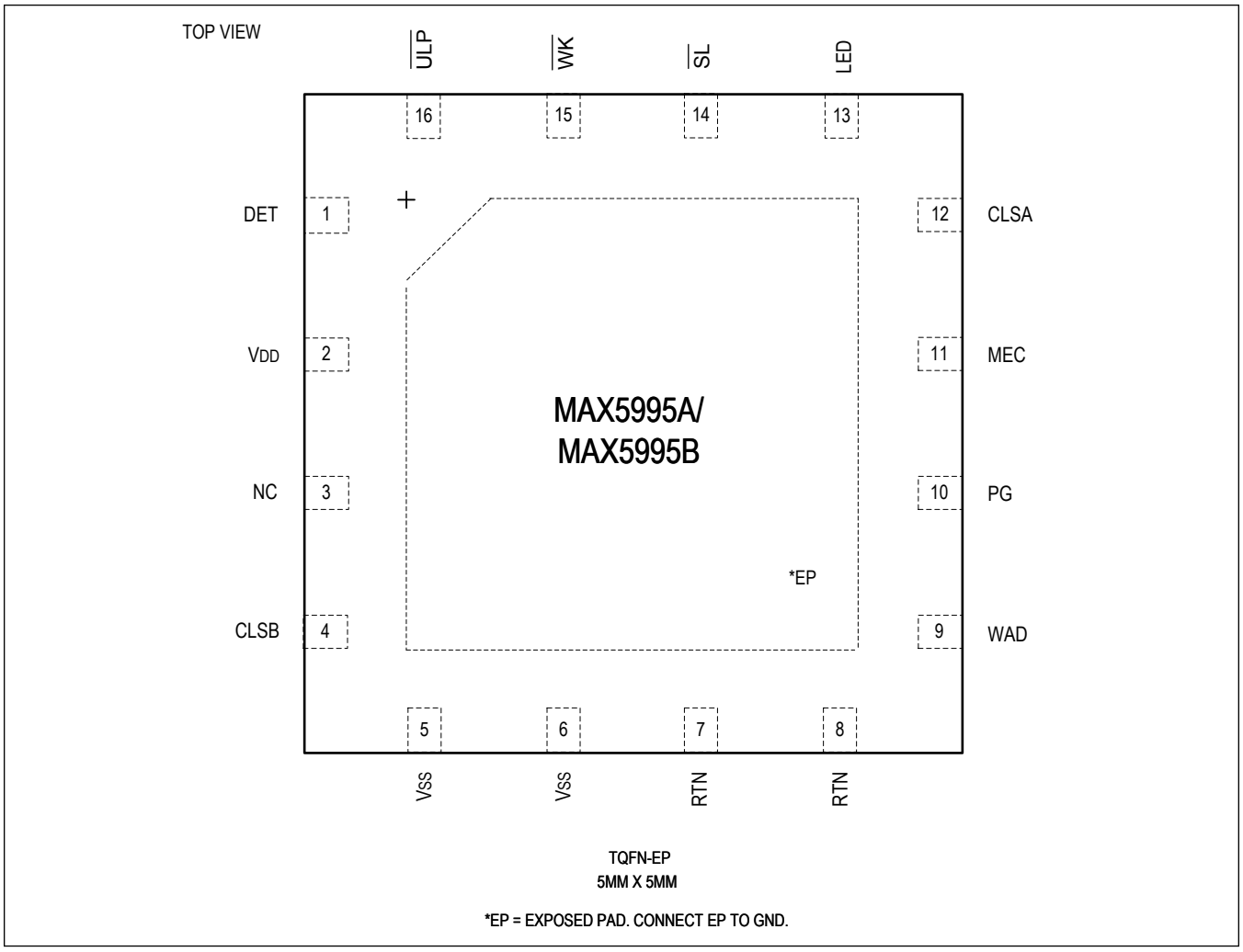


AUTOCLASS CLASSIFICATION IN MAX5995C

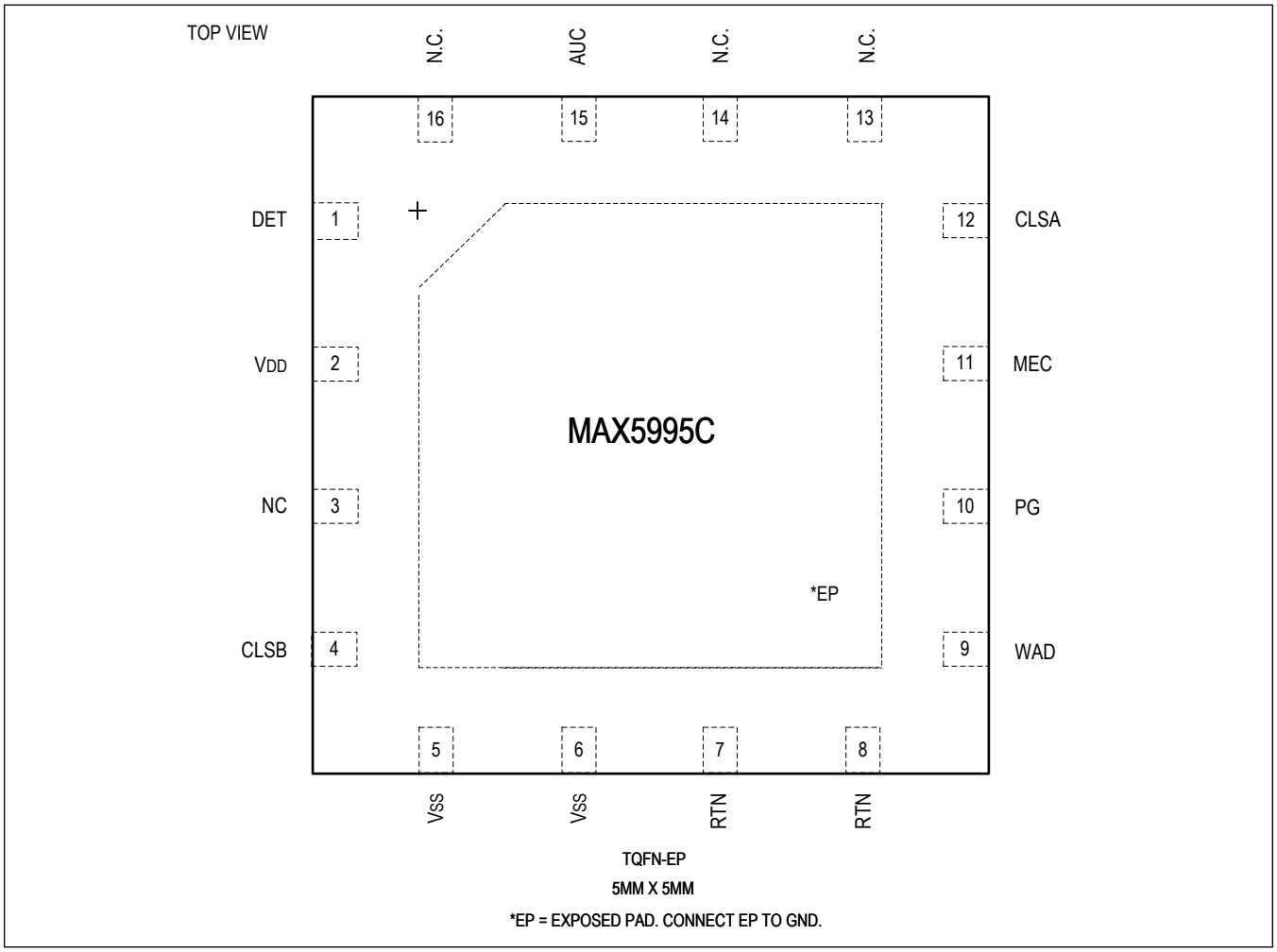


Pin Configurations

MAX5995A/B



MAX5995C


TOP VIEW
N.C.
AUC
N.C.
N.C.
16
15
14
13
DET
1
12
CLSA
VDD
2
11
MEC
MAX5995C
NC
3
10
PG
*EP
CLSB
4
9
WAD
5
6
7
8
VSS
VSS
RTN
RTN
TQFN-EP
5MM X 5MM
*EP = EXPOSED PAD. CONNECT EP TO GND.

Pin Description

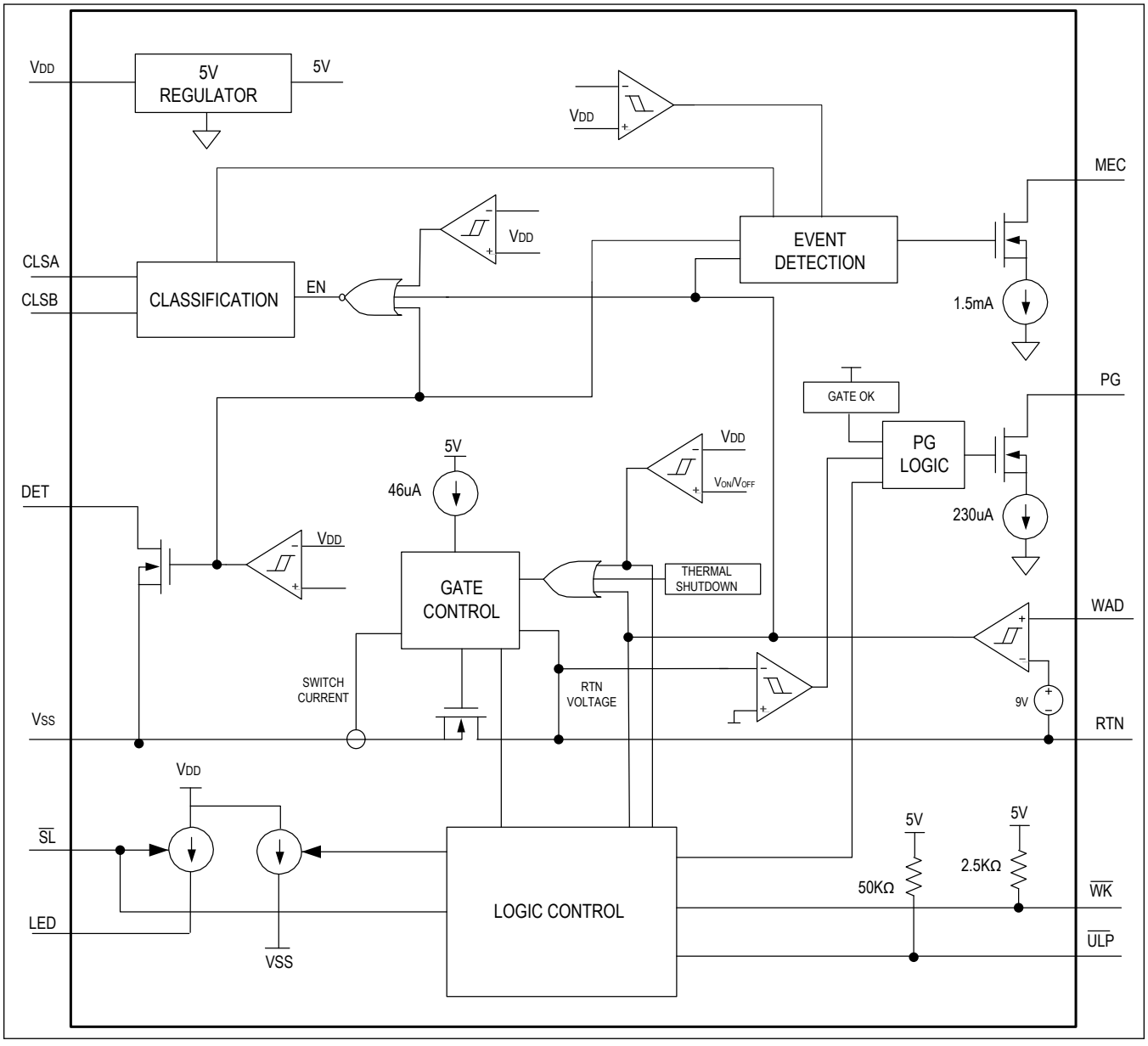
PIN		NAME	FUNCTION
MAX5995 A/B	MAX5995 C		
1	1	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to V_{DD}.
2	2	V_{DD}	Positive Supply Input. Connect minimum 68nF bypass capacitor between V_{DD} and V_{SS}.
3	3	NC	No Connection. Not internally connected.
4	4	CLSB	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSB to V_{SS} to set classification current for 3bt Standard. See the classification current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
5, 6	5, 6	V_{SS}	Negative Supply Input. V_{SS} connects to the source of the integrated isolation n-channel power MOSFET.
7, 8	7, 8	RTN	Drain of Isolation MOSFET. RTN connects to the drain of the integrated isolation n-channel power MOSFET. Connect RTN to the downstream DC-DC converter ground, as shown in the *Typical Application Circuit*.
9	9	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is present, the isolation n-channel power MOSFET turns off. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
10	10	PG	Open-Drain, Power-Good Indicator Output. PG sinks 230µA to disable the downstream DC-DC converter while turning on the MOSFET switch. PG current sink is disabled during detection, classification, and in the steady-state power mode. The PG current sink is turned on to disable the downstream DC-DC converter when the device is in sleep mode or Ultra-Low-Power sleep mode.
11	11	MEC	Multi-Event Classification or Wall Adapter Indication Output. This pin is an Open-drain output and it generates different duty cycle patterns to indicate 5 different power level allocated by PSE. It also generates specific pattern to indicate when a wall adapter supply, typically greater than 9V, is applied between WAD and RTN. MEC is turned off when the device is in sleep mode and Ultra-Low-Power mode.
12	12	CLSA	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSA to V_{SS} to set the classification current for 3at/af. See the classification current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification
13	—	LED	LED Driver Output. During sleep mode/Ultra-Low-Power sleep mode (MAX5995A/B) and MPS mode (MAX5995B/C), the LED sources a periodic current pulses at 250Hz with 25% duty cycle and the current amplitude is set by the resistor connected from $\overline{SL}$ to V_{SS}.
—	13	NC	Not Connected.
14	—	$\overline{SL}$	Sleep Mode Enable Input. In the MAX5995B, a falling edge on $\overline{SL}$ brings the device into sleep mode ($V_{\overline{SL}}$ must drop below 0.75V). In the MAX5995A, $V_{\overline{SL}}$ must remain below the threshold (0.75V) for a period of at least 6s after falling edge to bring the device into sleep mode. An external resistor ($R_{\overline{SL}}$) connected between $\overline{SL}$ and V_{SS} sets the LED current (I_{LED}) amplitude.
—	14	NC	Not Connected.
15	—	$\overline{WK}$	Wake Mode Enable Input. $\overline{WK}$ has an internal 2.5kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{WK}$ brings the device out of sleep mode or Ultra-Low-Power sleep mode and resume normal operation.
—	15	AUC	Connect a resistor (no worse than 1% accuracy) between AUC and V_{SS} to program the duty cycle of MPS current to further reduce the power consumption in MPS mode. There are 4 settings: floating (> 25%), 332kΩ (15%), 121kΩ (10%), and short to V_{SS} (5%).

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5995 A/B	MAX5995 C		
16	—	$\overline{ULP}$	Ultra-Low-Power Sleep Enable Input (in Sleep Mode). $\overline{ULP}$ has an internal 50kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{SL}$ in the MAX5995B (and a 6s period below the $\overline{SL}$ threshold in the MAX5995A), while $\overline{ULP}$ is asserted low enables Ultra-Low-Power sleep mode. When Ultra-Low-Power sleep mode is enabled, the power consumption of the device is reduced even lower than normal sleep mode to comply with Ultra-Low-Power sleep power requirements while still generating MPS current.
—	16	NC	Not Connected.
–	–	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

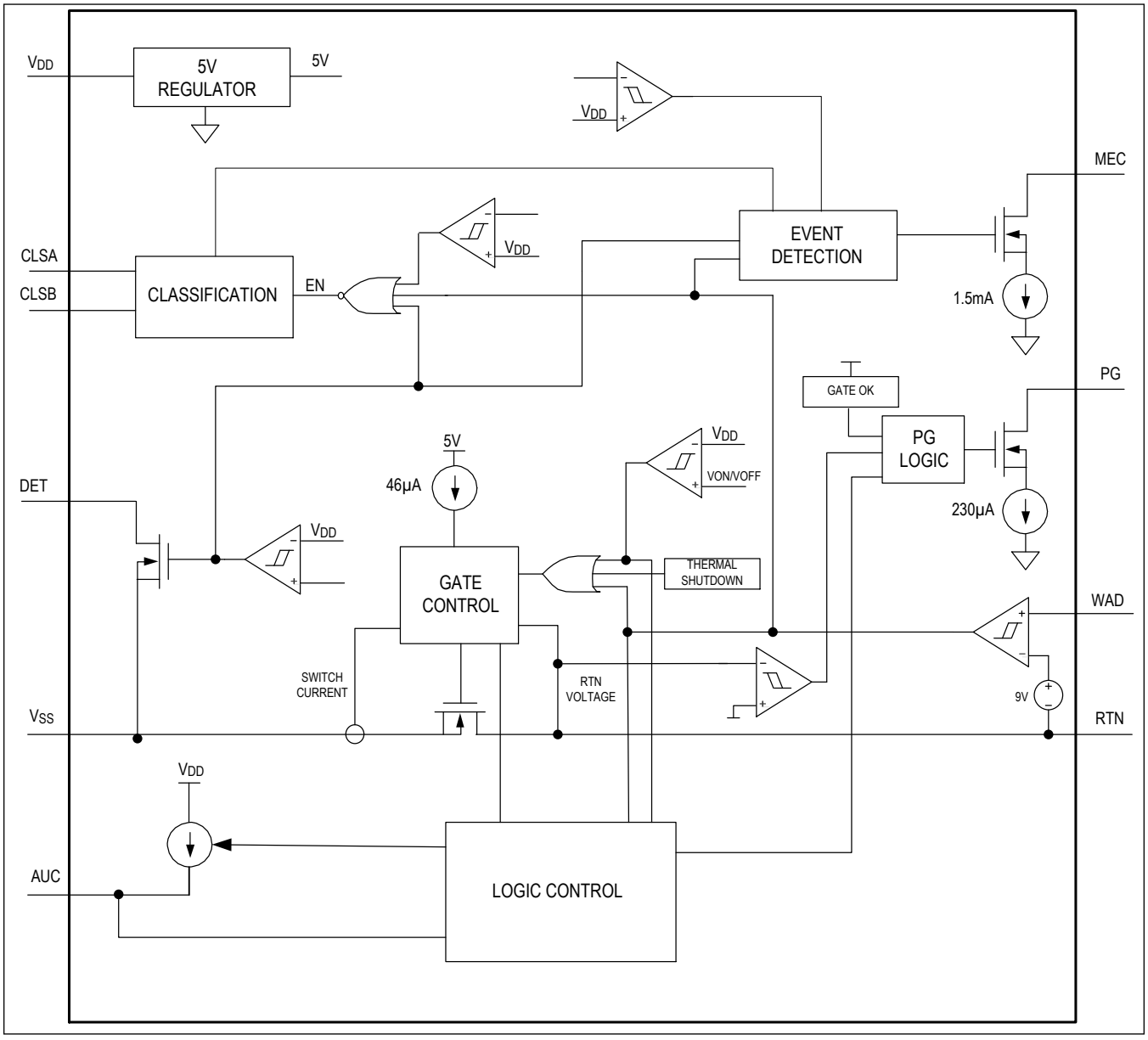
Functional Diagrams

MAX5995A/MAX5995B



Functional Diagrams (continued)

MAX5995C



Detailed Description

Operation Mode

Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the devices operate in four different modes: PD detection, PD classification, mark event, and PD power. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12.5V and 20.5V. The devices enter PD power mode once the input voltage exceeds V_{ON}.

Detection Mode

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor.

In detection mode, most of device internal circuitry is off and the offset current is less than 10µA. If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the devices (see the *Typical Application Circuit*). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution. Two external resistors connected CLSA/CLSB to V_{SS} set classification signature to the PSE and define the power consumption requested from the PD. R_{CLSA} sets classification current for the 1st and 2nd class events for 0~4 class PD complaint with IEEE 802.3af/at standard, and R_{CLSB} set classification current for the 3rd to 5th class event for 0~8 class PD complaint with IEEE 802.3bt standard.

The PSE classifies the PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.5V and 20.5V, the devices exhibit a series of events with current characteristic. Table 1 shows the R_{CLSA} and R_{CLSB} resistor values needed to set for PD class and the PD power consumption defined by standards. The PSE uses the number of class events and classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLSA} and R_{CLSB} and the supply current of the devices so the total current drawn by the PD is within the IEEE 802.3bt standard. The classification current is turned off whenever the device is in power mode.

Table 1. PSE Type and PD Class with Classification Resistor R_{CLSA} and R_{CLSB}

PD CLASS	POWER REQUESTED BY PD	R_{CLSA}	R_{CLSB}
0	12.95W	619	OPEN
1	3.84W	118	OPEN
2	6.49W	66.5	OPEN
3	12.95W	43.2	OPEN
4	25.5W	30.9	30.9
5	38.25W	30.9	619
6	51W	30.9	118
7	61W	30.9	66.5
8	71W	30.9	43.2

Multi-Event Classification and Detection

IEEE 802.3bt defines physical classification to allow a PD to communicate its power classification to the connected PSE and to allow the PSE to inform the PD of the PSE's available power. The PD classes (0~8) and PD power requests during Multi-Event Classification is configured by setting the R_{CLSA} and R_{CLSB} resistor values in Table 1. This configuration is compatible with IEEE 802.3af/at standard.

In a 1-Event classification, the PD is a 3af/at Class 0~3 PD. In a 2-Event classification, the PD is 3at Class 4 PD. In a 3-Event classification, the PD can be a 3bt PD at Class 0 to Class 4 depending on the classification current levels, and in this case the PD can take as high as 30W power from a 3bt PSE. In a 4-Event classification, the PD can be 3bt Class 5 PD with 45W, or 3bt Class 6 PD with 60W input power from PSE. If the third and fourth event the classification current are 10mA/20mA, it means PD power requests gets demotion from PSE. In a 5-Event classification, the PD can be 3bt PD Class 7 with 75W, Or a 3bt PD Class 8 with 90W input power from PSE.

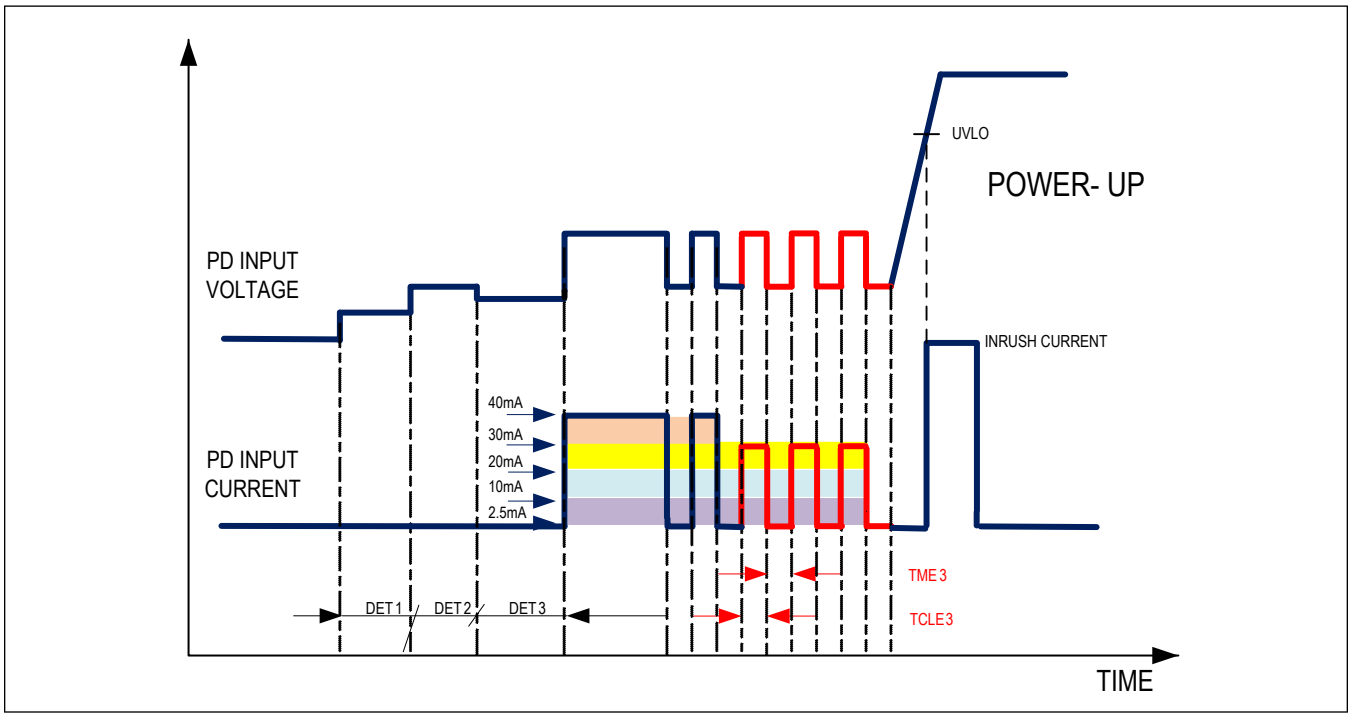


Figure 1. Multi-Event Classification

Power Mode

The MAX5995A/MAX5995B/MAX5995C enter power mode when V_{IN} rises above the undervoltage-lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the devices turn on the internal n-channel isolation MOSFET to connect V_{SS} to RTN with inrush current limit internally set to 53mA (typ) when V_{RTN} - V_{SS} > 7V and 135mA (typ) when V_{RTN} - V_{SS} < 7V. The isolation MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the isolation MOSFET is fully turned on, the devices change to the normal operation current limit. The open-drain power good output (PG) remains low for a t_{DELAY} time (*Electrical Characteristics*) until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. Note that using larger output capacitors will result in longer start-up t_{DELAY} time.

Power Demotion

The power demotion feature is provided for the situation where the power level PD requested is not available at the PSE. When power demotion occurs, the PD must operate in a reduced power mode while connected to lower power PSE. In Power Demotion mode, the PSE is going to provide the power that its classification indicates. For example, a 3af PSE only issue a single event even there is a Class 4 PD connected.

This feature is applicable in 4P PoE as well. For example, when a Class 5/6 PD connected to a PSE, the PSE only initiate 3-Event. It indicated the PSE supports 4P operation but can only deliver power up to 30W. Refer to Table 1 for more details.

Multi-Event Indication (MEC)

The device communicates its available power level to the system user through the MEC pin. The MEC pin state is a result of the number of classification/mark events, and whether the PD is in PoE or auxiliary power operation. The MEC pin can indicate power allocated from PSE to PD in 5 different cases.The devices uses a unique encoding method on the MEC pin to indicate the power levels that are higher than 12.95W. First pulse sent from MEC is START bit (256µs, 25% duty) for system to detect. Then the pattern of 2nd, 3rd, and 4th pulse width that is double or triple pulse width of the START bit (50% and 75% duty) is issued to indicate the type of PSE and power allocated from PSE. This pulse train is repeatable at certain frequency.

Number of event and the maximum power granted from the PSE at PD input are listed in Table 2. 1-Event and 2-Event are with IEEE802.3af/at standard. 3-Event, 4-Event, and 5-Event indicate PD Class (0~8) in IEEE802.3bt standard.

MEC is enabled after the isolation MOSFET is fully on until V_{IN} drops below the UVLO threshold. The MEC is turned off when the device is in sleep mode and Ultra-Low-Power mode.

Table 2. MEC Pattern with Number of Events and PD Class

NUMBER OF EVENTS	MAXIMUM POWER GRANTED AT PD INPUT
1	12.95W
2 or Adapter	25.5W
3	25.5W
4	38.25W, if R_{CLSB} = 619Ω; otherwise 51W
5	61W, if R_{CLSB} = 66.5Ω; otherwise 71W

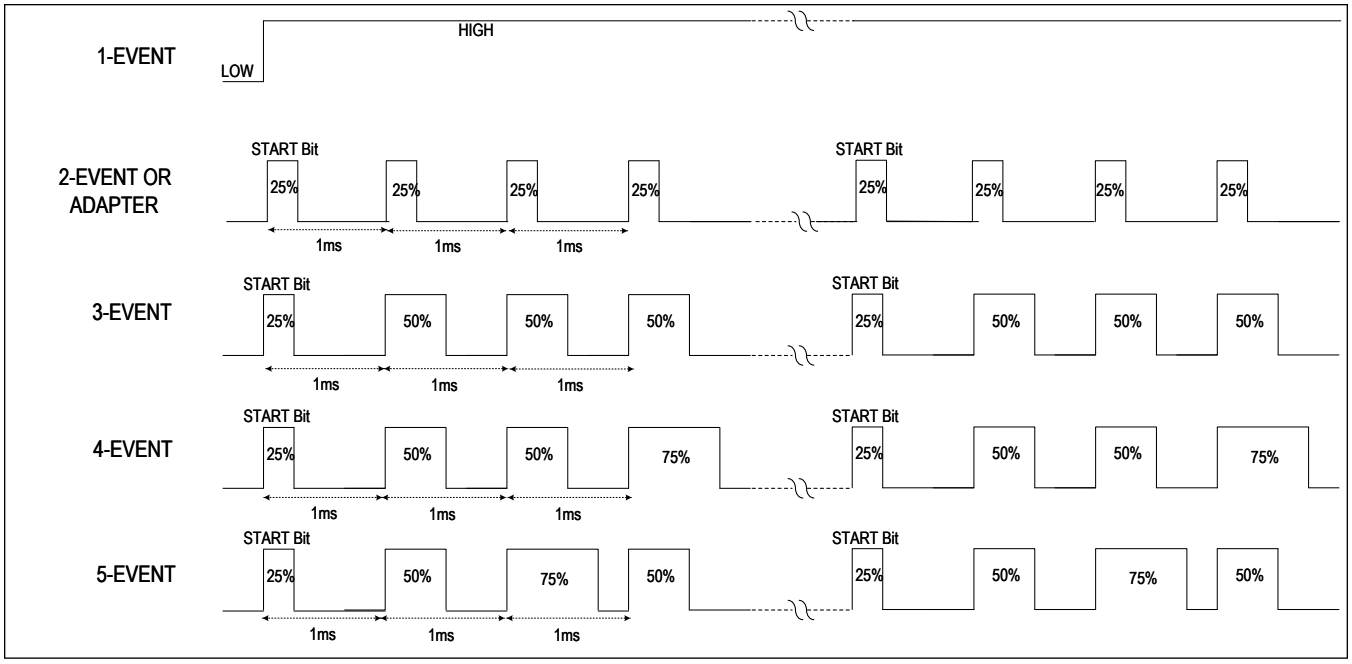


Figure 2. MEC Waveforms in Different Scenarios

Undervoltage Lockout

The MAX5995A/MAX5995B/MAX5995C operate up to a 60V supply voltage with a turn-on UVLO threshold (V_{ON}) at 35.4V and a turn-off UVLO threshold (V_{OFF}) at 30V. When the input voltage is above V_{ON}, the devices enter power mode and the internal MOSFET is turned on. When the input voltage goes below V_{OFF} for longer than t_{OFF_DLY}, the MOSFET turns off.

Intelligent MPS

The intelligent MPS feature is provided by MAX5995B/MAX5995C. It enables applications that require low power standby modes. The MPS current is generated to comply with the IEEE 802.3bt standard for PSE to maintain power on in standby modes. A minimum current (10mA) of the port is able to be maintained with MPS mode to avoid the power disconnection from the PSE. The devices automatically enter MPS mode when the port current is lower than 24mA (typ) and exit MPS mode when the port current is greater than 28.7mA (typ).

Below drawing shows intelligent MPS behavior. The MPS comparator is autozero comparator and it will sample the port current every 32µs. The MPS comparator is always switched on when the MOSFET is fully turned on. If MPS comparator falling threshold is triggered continuously within 320µs, the part enters MPS mode and MPS current is generated. Once the part enter MPS mode it waits for the TMPS timer to elapse before check the MPS comparator again.

In MPS mode, Intelligent MPS modulation scheme is shown in Figure 3 (MPS Duty Cycle is 25% or 84ms), and the LED driver output (LED) sources periodic current pulses at 250Hz with 25% duty cycle and current amplitude can be configured by an resistor ($R_{\overline{SL}}$) on $\overline{SL}$ pin. PG remains high to enable downstream dc-dc converter in MPS mode. Once MPS mode is entered, sleep mode or Ultra-Low-Power sleep mode will not take effect (MAX5995B).

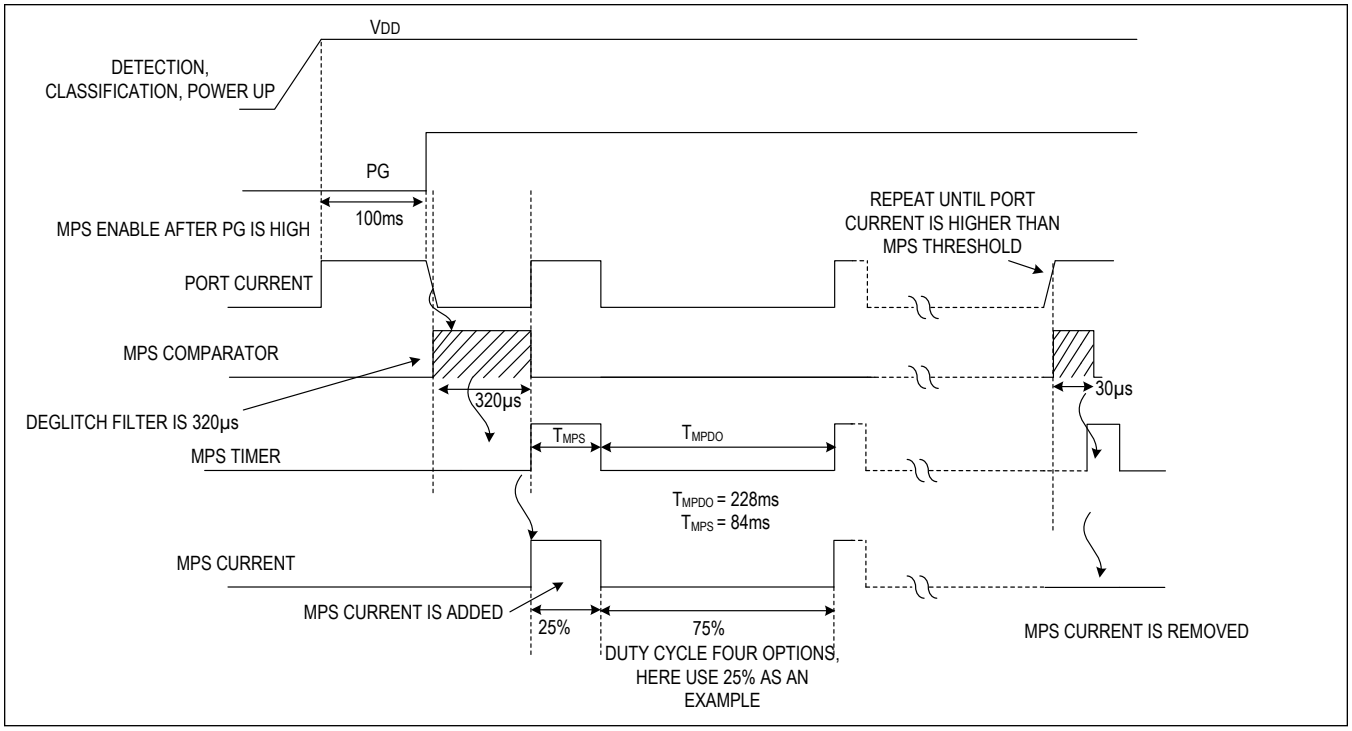


Figure 3. Intelligent MPS Behavior

Sleep and Ultra-Low-Power Sleep Modes (MAX5995A/MAX5995B)

The MAX5995A/MAX5995B feature a sleep mode, which pulls PG low to disable downstream DC-DC converters to minimize the power consumption of the overall PD system, while at the same time still keeps the internal MOSFET turned on and generate a MPS current at V_{DD} to remain the PSE connection. However, when MAX5995B Intelligent MPS is enabled, and once the device enters MPS mode, sleep mode or Ultra-Low-Power sleep mode will not take effect. In sleep mode, the LED driver output (LED) sources a pulsating current and current amplitude can be configured by an external resistor ($R_{\overline{SL}}$) on $\overline{SL}$ pin. To enable sleep mode, apply a falling edge to $\overline{SL}$ pin (MAX5995B) or hold $\overline{SL}$ pin low for a minimum of 6 seconds after a falling edge (MAX5995A).

An Ultra-Low-Power sleep mode allows the MAX5995A/MAX5995B to further reduce power consumption while still maintaining pulsed MPS current required by standard at V_{DD}. In Ultra-Low-Power sleep mode, the LED driver output (LED) sources periodic current pulses at 250Hz with 25% duty cycle and current amplitude can be configured by an resistor ($R_{\overline{SL}}$) on $\overline{SL}$ pin; the Ultra-Low-Power sleep enable input ULP is internally held high with a 50kΩ pullup resistor to the internal 5V bias of the MAX5995A/MAX5995B. To enable Ultra-Low-Power sleep mode, set ULP pin to logic-low and apply a falling edge to $\overline{SL}$ (MAX5995B) or hold $\overline{SL}$ low for a minimum of 6s (MAX5995A).

Apply a falling edge on the wake-mode enable input ($\overline{WK}$) to disable sleep or Ultra-Low-Power sleep mode and resume normal operation. The PG pin is pulled low when the devices are in sleep mode or Ultra-Low-Power sleep mode, and pulled high once enable $\overline{WK}$ to resume normal operation.

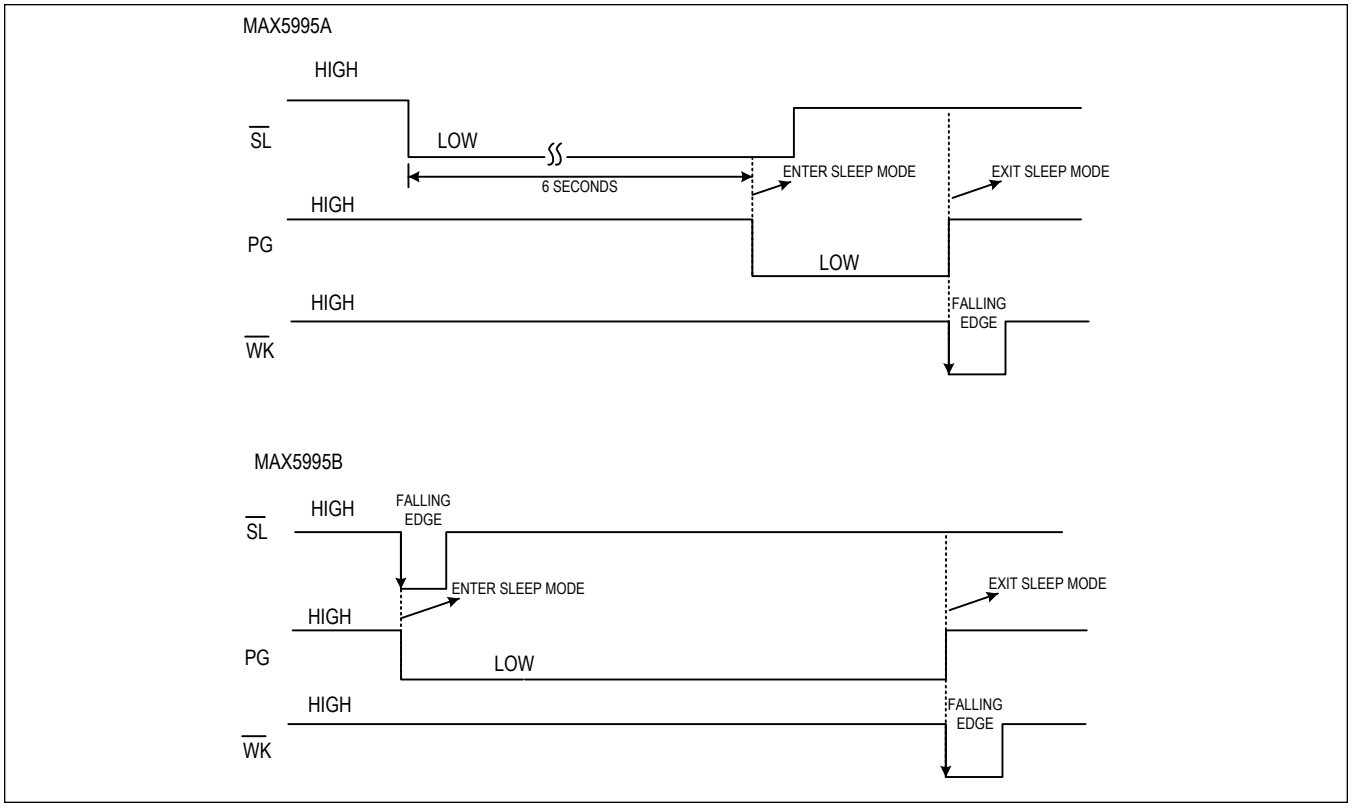


Figure 4. MAX5995A/MAX5995B Sleep Mode Behavior (Not in MPS Mode)

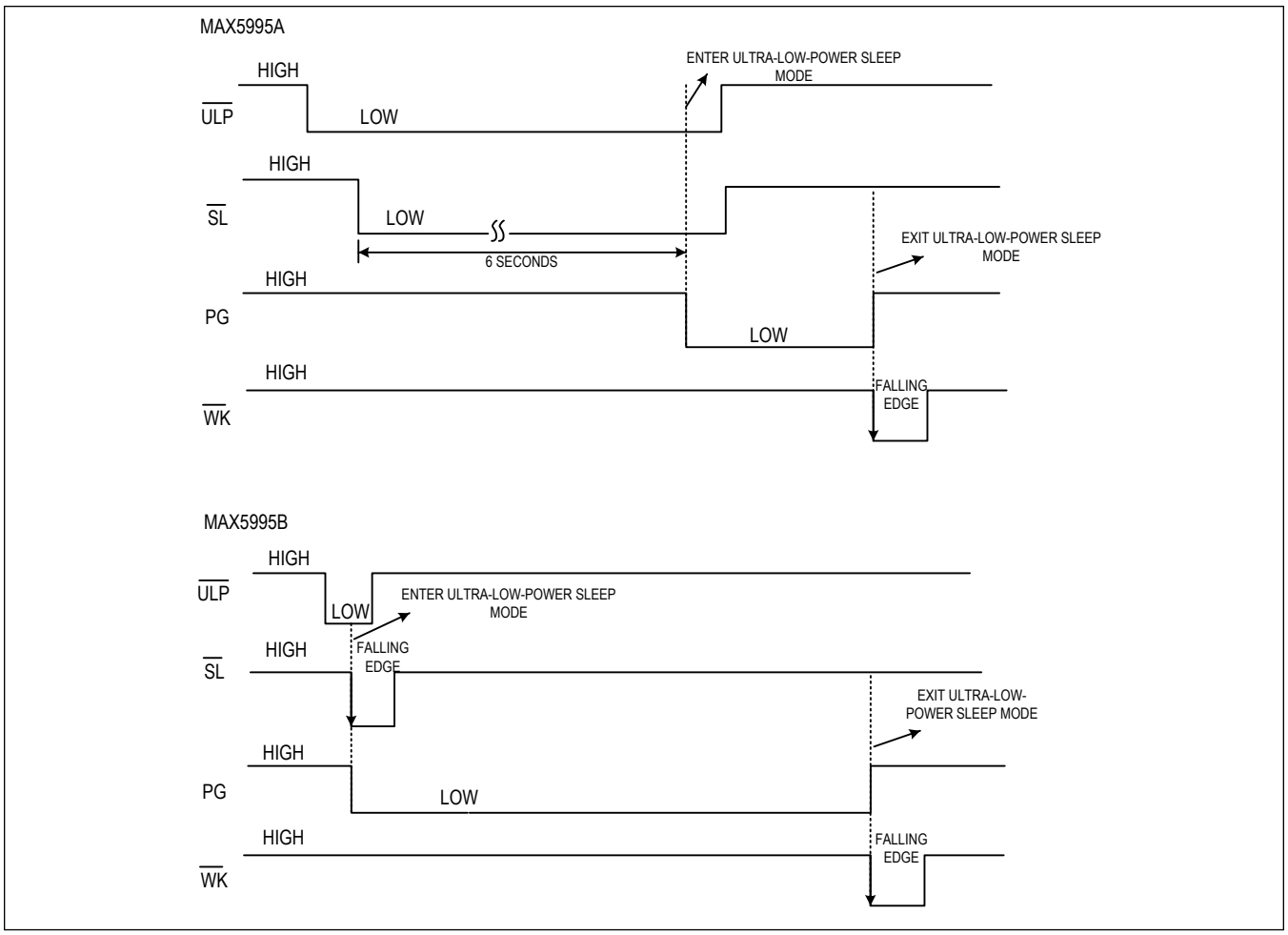


Figure 5. MAX5995A/MAX5995B Ultra-Low-Power Sleep Mode Behavior (Not in MPS Mode)

LED Driver (MAX5995A/MAX5995B)

The MAX5995A/MAX5995B drive an LED connected from the LED pin to V_{SS}. During sleep mode and Ultra-Low-Power sleep mode, the LED pin sources periodic current pulses at 250Hz with 25% duty cycle. The current amplitudes in both cases can be programmed from 10mA to 20mA by the resistor connected from $\overline{SL}$ to V_{SS} according to the following formula.

$$I_{LED} = \frac{645.75}{R_{\overline{SL}} + 1200}$$

Power-Good Output

An open-drain output (PG) is used to allow disabling downstream DC-DC converter until the n-channel isolation MOSFET is fully turned on. PG is pulled low to V_{SS} for a period of t_{DELAY} and until the internal isolation MOSFET is fully turned on. Using larger output capacitors will result in longer t_{DELAY} time. The PG is pulled low during sleep mode and Ultra-Low-Power sleep mode (in MAX5995A and MAX5995B not in MPS mode). PG is also pulled low in an overtemperature event and pulled high once the device comes out of thermal shutdown and resumes normal operation.

AUTOCLASS (MAX5995C)

In AUTOCLASS mode, the PSE is allowed to determine the actual maximum power consumption from the connected PD. When AUTOCLASS mode is enabled, during the first class event, the PD drops its current to class signature '0' no earlier than 76ms (min) and no later than 87ms (max). The AUTOCLASS feature is only enabled in MAX5995C.

In AUTOCLASS mode, connect a resistor (no worse than 1% accuracy) between AUC and V_{SS} to program the duty cycle of MPS current to further reduce the power consumption in MPS mode. There are four settings: floating (> 25%), 332kΩ (15%), 121kΩ (10%), and short to V_{SS} (5%)

Table 3. AUC Configuration for MPS Current

AUC Pin Configuration	MPS Duty Cycle
AUC floating	> 25%
Connect 332k between AUC and V_{SS}	15%
Connect 121k between AUC and V_{SS}	10%
Short AUC to VSS	5%

The device will start a 82ms Timer On the first Classification Event. If the PSE does not provide the Long First Event, then the PD will not be in AUTOCLASS mode and will not modulate IMPS duty-cycle current according the AUC status. In this case, I_{MPS} duty-cycle is the default value (> 25% pulses, as shown in Figure 6). If the PSE provide the Long First Event, the PD will truncate the classification current after 82ms to signature AUTOCLASS mode to the PSE, and then the PD will modulate the I_{MPS} duty-cycle current according to AUC status. I_{MPS} modulation scheme is shown in Figure 6.

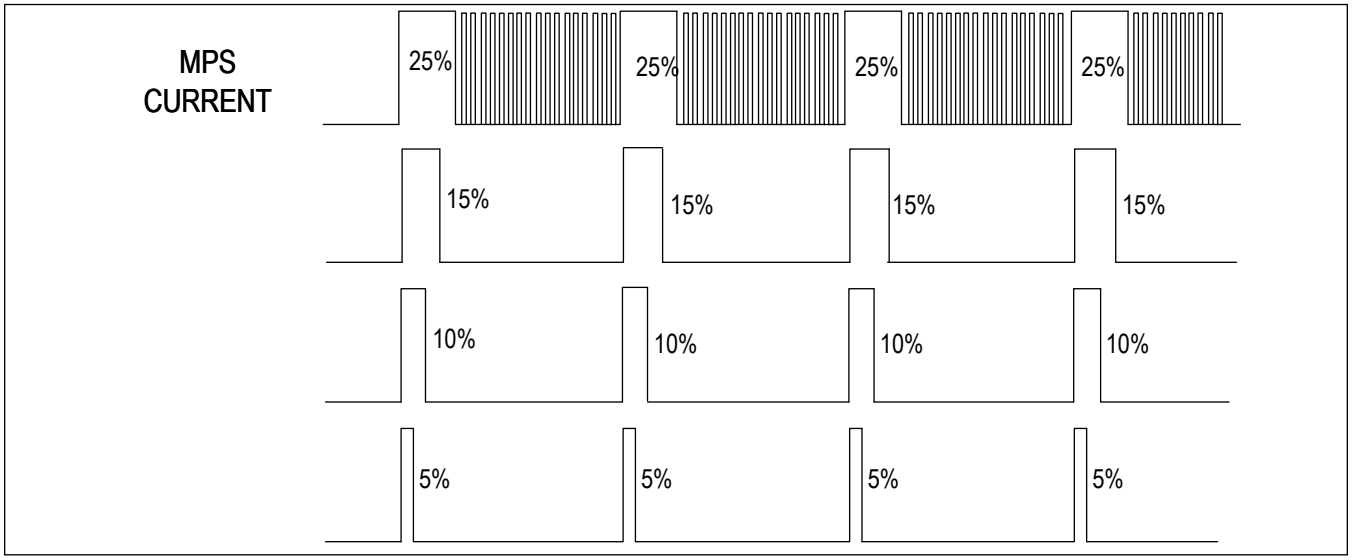


Figure 6. MPS Current with Different AUC Configuration

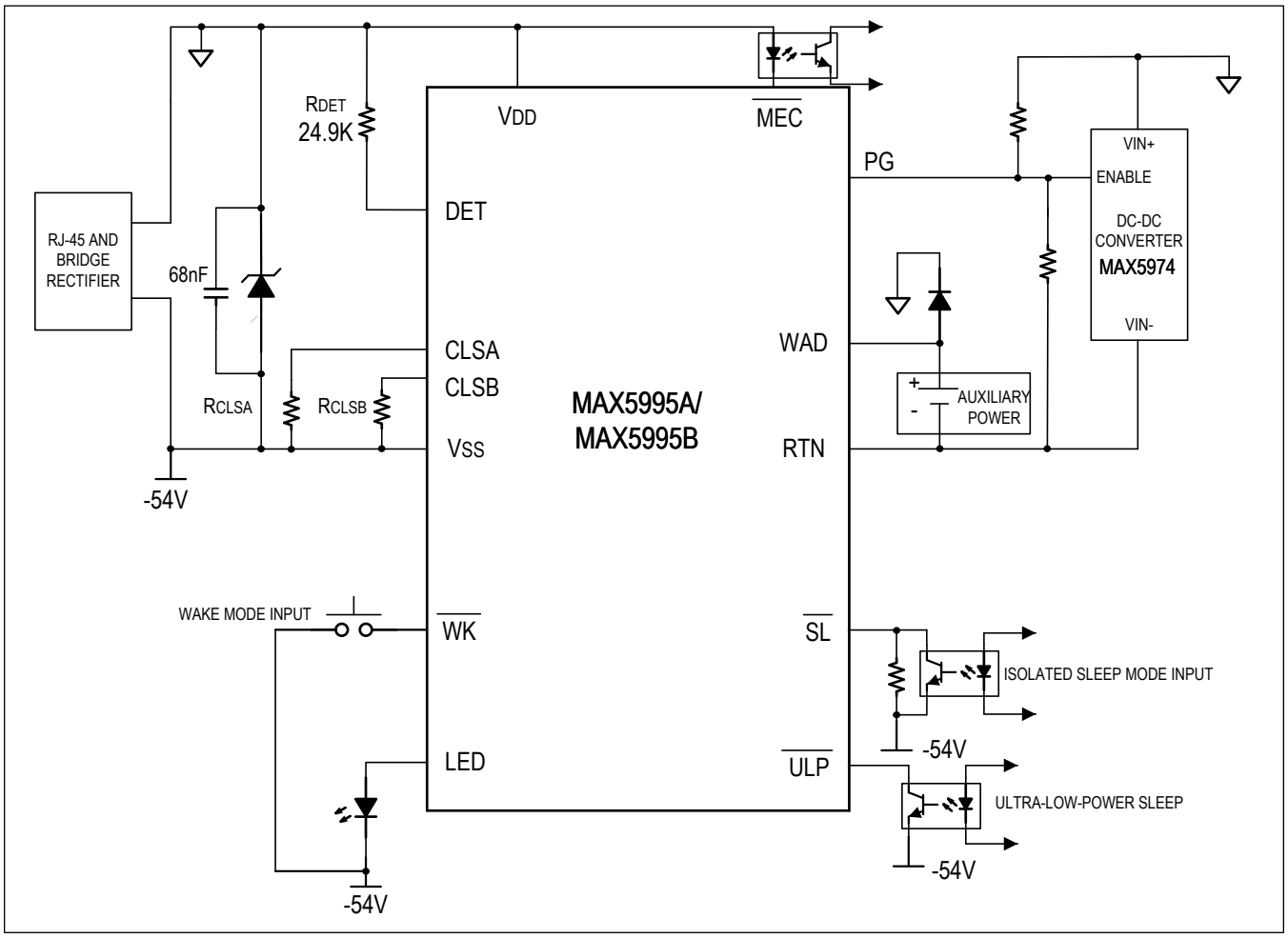
Thermal-Shutdown Protection

The MAX5995A/MAX5995B/MAX5995C include thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +150ºC, the devices turn off the internal power MOSFET, LED driver, and MEC current sink. When the junction temperature falls below +120ºC, the devices enter startup mode and then power mode. Startup mode ensures the downstream DC-DC converter is turned off by pulling PG low until the internal power MOSFET is fully turned on.

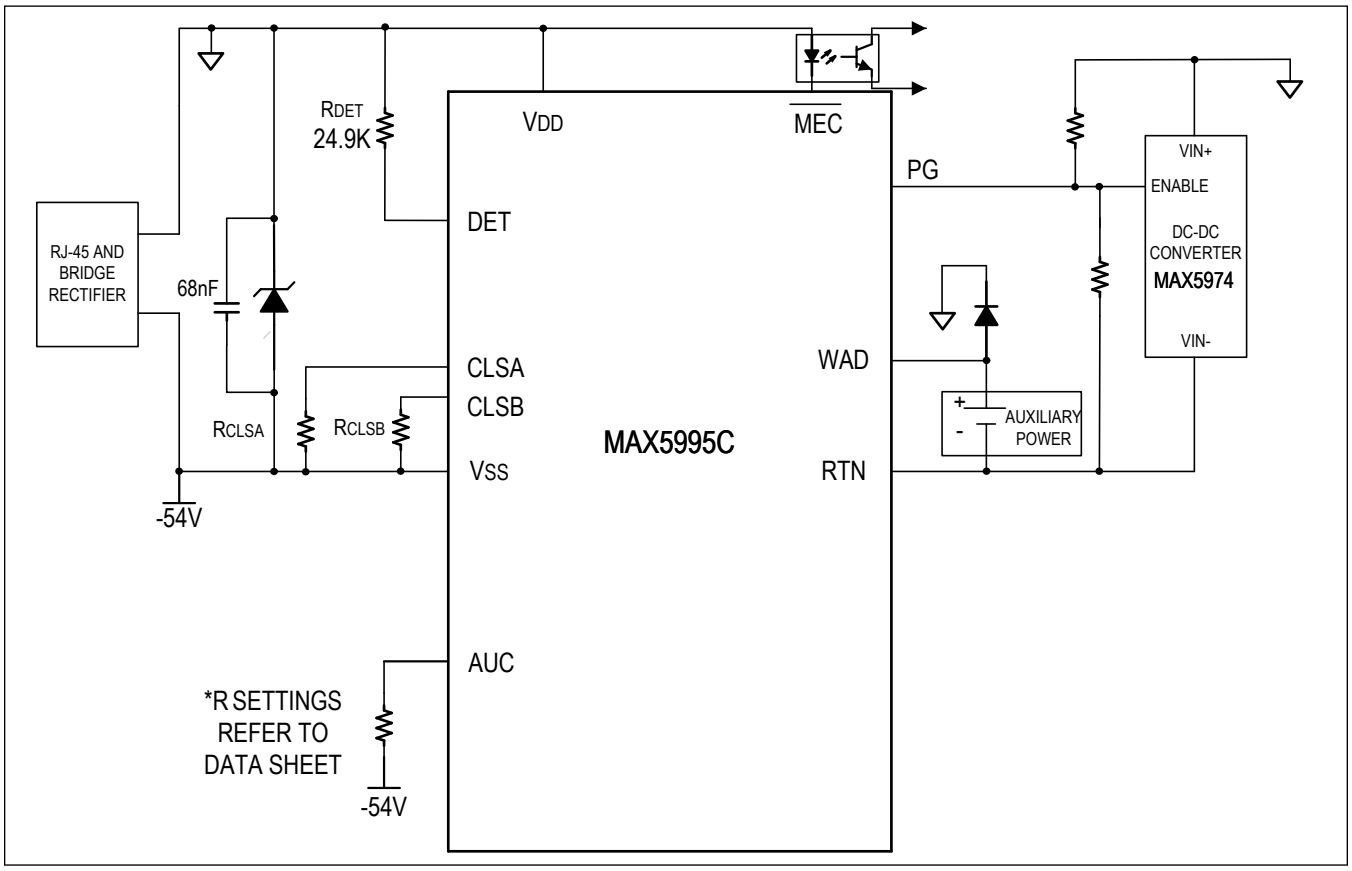
Wall Power Adapter Detection and Operation

The devices feature wall power adapter detection for applications where an auxiliary power source such as a wall power adapter is used to power the PD by connecting it to WAD pin to RTN. Once the input voltage (V_{DD} - V_{SS}) exceeds the mark event threshold, wall adapter detection is enabled.The devices give the priority to the WAD and smoothly switch the power supply to WAD when wall adapter is detected. The devices detect the wall power adapter when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is detected, the internal isolation MOSFET turns off, MEC current sink turns on to indicate certain pattern (see *Multi-Event Indication (MEC)*), the classification current is disabled if V_{IN} is in the classification range, and the Intelligent MPS comparator is turned off.

Typical Application Circuits



Typical Application Circuits (continued)



Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE	INTELLIGENT MPS	SLEEP/ULTRA-LOW-POWER MODE	6s FILTER DELAY ON $\overline{SL}$	AUTOCLASS
MAX5995AETE+**	-40°C to +85°C	16 TQFN-EP*	No	Yes	Yes	No
MAX5995BETE+	-40°C to +85°C	16 TQFN-EP*	Yes	Yes	No	No
MAX5995CETE+**	-40°C to +85°C	16 TQFN-EP*	Yes	No	No	Yes
MAX5995AATE+**	-40°C to +125°C	16 TQFN-EP*	No	Yes	Yes	No
MAX5995BATE+	-40°C to +125°C	16 TQFN-EP*	Yes	Yes	No	No
MAX5995CATE+**	-40°C to +125°C	16 TQFN-EP*	Yes	No	No	Yes

+ Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/18	Initial release	—
1	2/19	Updated *General Description, Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics, Pin Description, Functional Diagram, Detailed Description*, and *Ordering Information*	6, 7, 10, 14, 24
2	7/19	Updated *General Description, Absolute Maximum Ratings, Electrical Characteristics* conditions, and *Ordering Information*	1–6, 26
3	7/19	Updated *Ordering Information*	26

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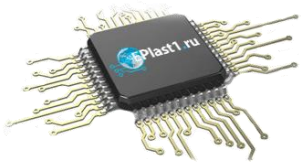
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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