

## RF power transistor, LDmoST plastic family

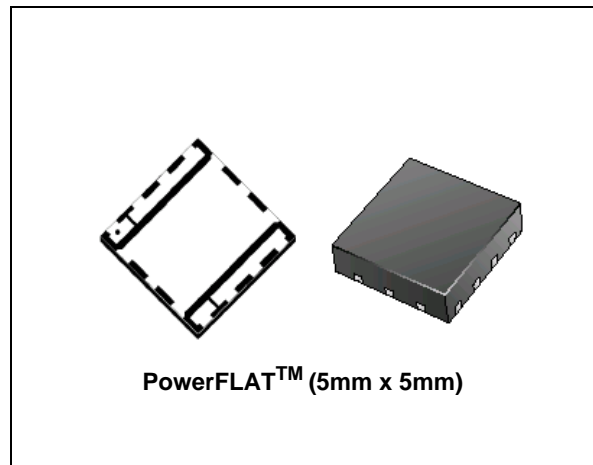
### Features

- Excellent thermal stability
- Common source configuration
- Broadband performances:  
 $P_{OUT} = 6\text{ W}$  with 13 dB gain @ 870 MHz
- Plastic package
- ESD protection
- Supplied in tape and reel
- In compliance with the 2002/95/EC european directive

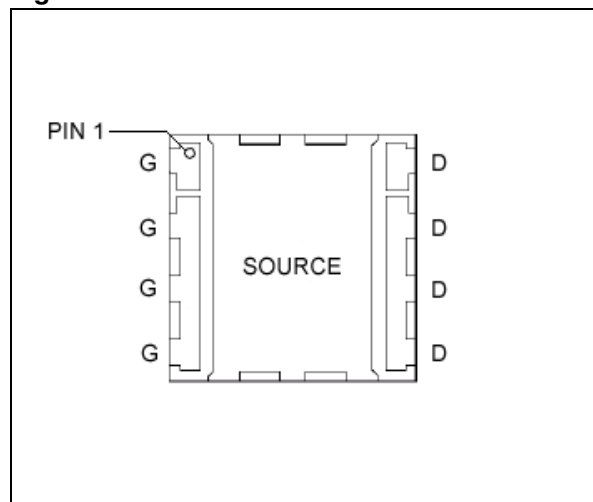
### Description

The PD84006L-E is a common source N-channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 7 V in common source mode at frequencies up to 1 GHz.

PD84006L-E's superior gain and efficiency makes it an ideal solution for portable radio and UHF RFID reader.



**Figure 1. Pin connection**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
PD84006L-E	84006	PowerFLAT™ (5mm x 5mm)	Tape and reel

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# 1 Electrical data

## 1.1 Maximum ratings

Table 2. Absolute maximum ratings ( $T_{CASE} = 25^{\circ}C$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	25	V
$V_{GS}$	Gate-source voltage	-0.5 to +15	V
$I_D$	Drain current	5	A
$P_{DISS}$	Power dissipation	31	W
$T_J$	Max. operating junction temperature	150	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

## 1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction - case thermal resistance	4	$^{\circ}C/W$

## 2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

### 2.1 Static

Table 4. Static

Symbol	Test conditions		Min	Typ	Max	Unit
$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	$V_{GS} = 5\text{ V}$	$V_{DS} = 0\text{ V}$			1	$\mu\text{A}$
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 150\text{ mA}$	3		4.3	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 1\text{ A}$		0.34		V
$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$		40		pF
$C_{OSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$		33		pF
$C_{RSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$		1.45		pF

### 2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
$P_{3dB}$	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 150\text{ mA}$ , $f = 870\text{ MHz}$	5	6		w
GPS	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 150\text{ mA}$ , $P_{OUT} = 2\text{ W}$ , $f = 870\text{ MHz}$	15			dB
nD	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 150\text{ mA}$ , $P_{OUT} = P_{3dB}$ , $f = 870\text{ MHz}$	50	60		%
Load mismatch	$V_{DD} = 9.5\text{ V}$ , $I_{DQ} = 150\text{ mA}$ , $P_{OUT} = 8\text{ W}$ , $f = 870\text{ MHz}$ All phase angles	20:1			VSWR

### 2.3 ESD protection characteristics

Table 6. ESD protection characteristics

Test conditions	Class
Human body model	2
Machine model	M3

### 2.4 Moisture sensitivity level

Table 7. Moisture sensitivity level

Test methodology	Rating
J-STD-020B	MSL 3

### 3 Impedance

Figure 2. Current conventions

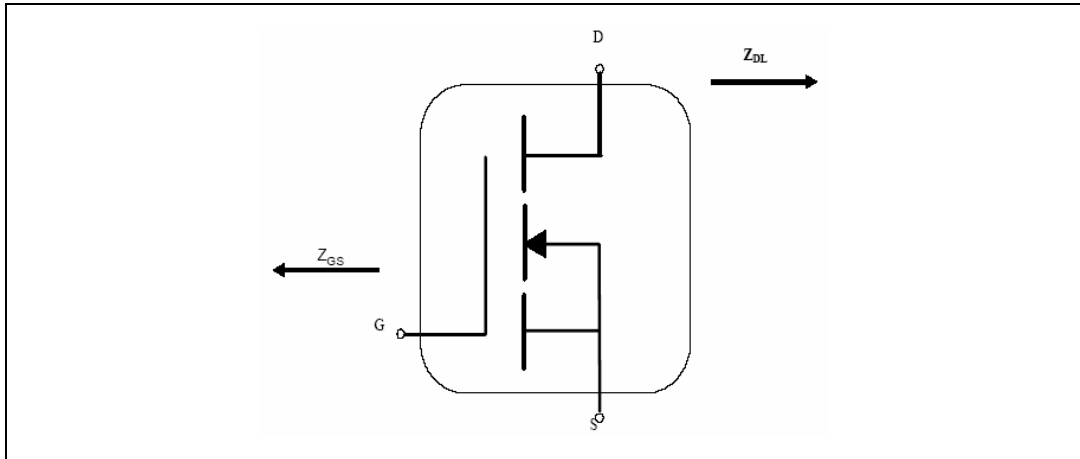
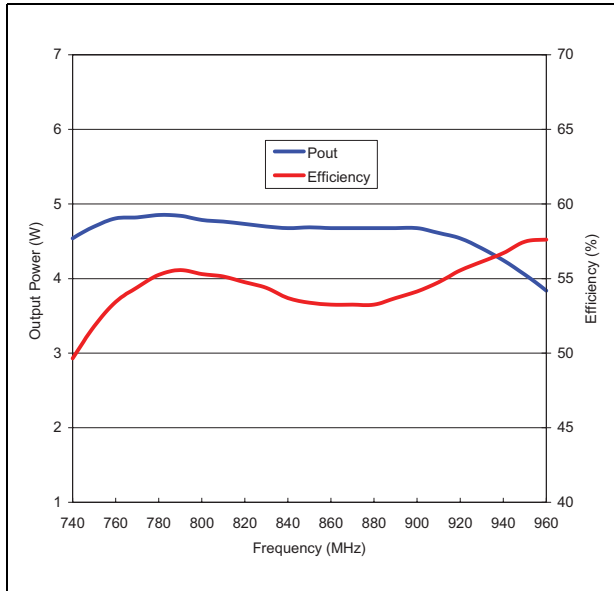


Table 8. Impedance data

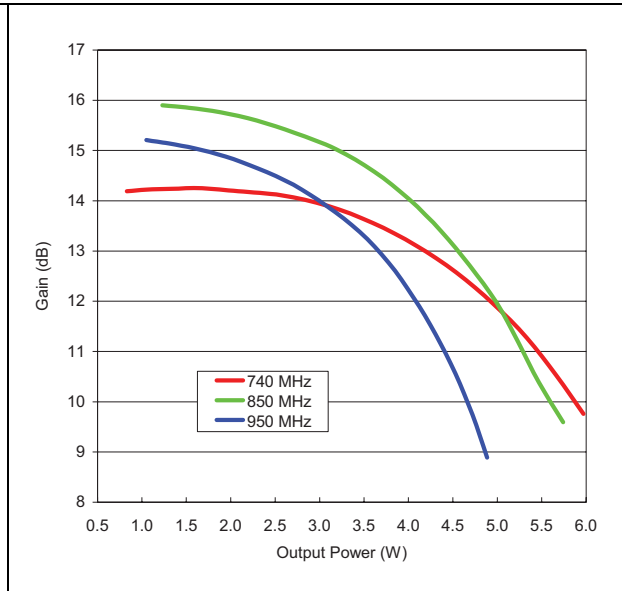
Freq. (MHz)	Z <sub>IN</sub> (Ω)	Z <sub>DL</sub> (Ω)
740	2,52 + j1,42	3,06 + j0,41
750	2,52 + j1,56	3,09 + j0,51
760	2,51 + j1,73	3,12 + j0,64
770	2,46 + j1,84	3,13 + j0,72
780	2,47 + j1,96	3,13 + j0,81
790	2,48 + j2,07	3,13 + j0,87
800	2,45 + j2,22	3,14 + j0,96
810	2,44 + j2,27	3,08 + j1,02
820	2,45 + 2,43	3,05 + j1,04
830	2,41 + j2,57	3,04 + j1,11
840	2,40 + j2,67	2,98 + j1,14
850	2,41 + j2,80	2,99 + j1,24
860	2,38 + j2,92	2,91 + j1,29
870	2,37 + j3,06	2,88 + j1,38
880	2,36 + j3,20	2,81 + j1,40
890	2,37 + j3,25	2,70 + j1,47
900	2,31 + j3,36	2,56 + j1,53
910	2,25 + j3,49	2,50 + j1,62
920	2,16 + j3,57	2,31 + j1,72
930	2,16 + j3,66	2,21 + j1,82
940	2,11 + j3,78	2,11 + j1,96
950	2,06 + j3,86	1,98 + j2,07

# 4 Typical performance

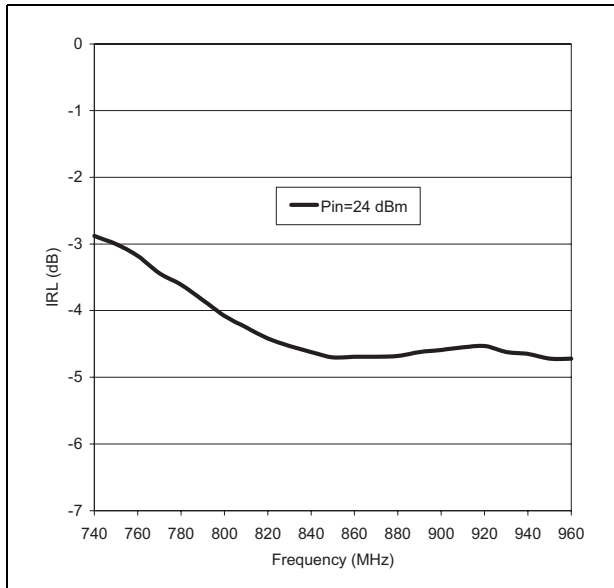
**Figure 3. Output power and efficiency vs frequency**  $V_{dd} = 7.2\text{ V}$ ,  $I_{dq} = 200\text{ mA}$   
 $P_{in} = 24\text{ dBm}$



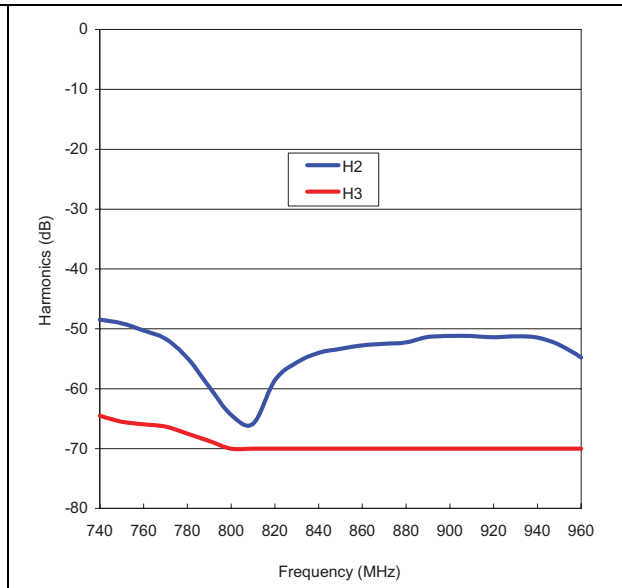
**Figure 4. Gain vs output power**  $V_{dd} = 7.2\text{ V}$ ,  $I_{dq} = 200\text{ mA}$



**Figure 5. Input return loss vs frequency**  $V_{dd} = 7.2\text{ V}$ ,  $I_{dq} = 200\text{ mA}$



**Figure 6. Harmonics vs frequency**  $V_{dd} = 7.2\text{ V}$ ,  $I_{dq} = 200\text{ mA}$ ,  $P_{in} = 24\text{ dBm}$



**Figure 7. Output power vs frequency and supply voltage  $P_{in} = 24\text{ dBm}$ ,  $I_{dq} = 200\text{ mA}$**

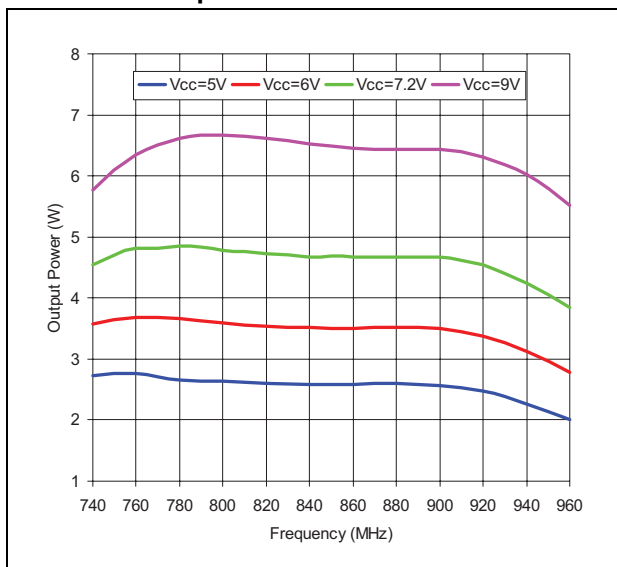






Table 9. Part list (continued)

Component ID	Description	Value	Case size	Manufacturer	Part code
R1	Resistor	56 $\Omega$	0603	Tyco electronics	
R2	Potentiometer	10 K $\Omega$		Bourns electronics	3214W-1-103E
R3	Resistor	1 K	0603	Tyco electronics	01623440-1
TL1	Transmission line	W=0.92mm	L= 13,50 mm		
TL2	Transmission line	W=0.92mm	L= 3,15 mm		
TL3	Transmission line	W=0.92mm	L= 2,90 mm		
TL4	Transmission line	W=0.92mm	L= 2,00 mm		
TL5	Transmission line	W=0.92mm	L= 2,20 mm		
TL6	Transmission line	W=0.92mm	L= 13,20 mm		
RF in, RF out	SMA-CONN	50 $\Omega$	60 mils	JOHNSON	142-0701-801
PD84006L-E	LDMOS			STMicroelectronics	PD84006L-E
Board	FR-4 THk=0.020" 2OZ Cu both sides				

## 6 Circuit layout and photo

Figure 9. Circuit layout

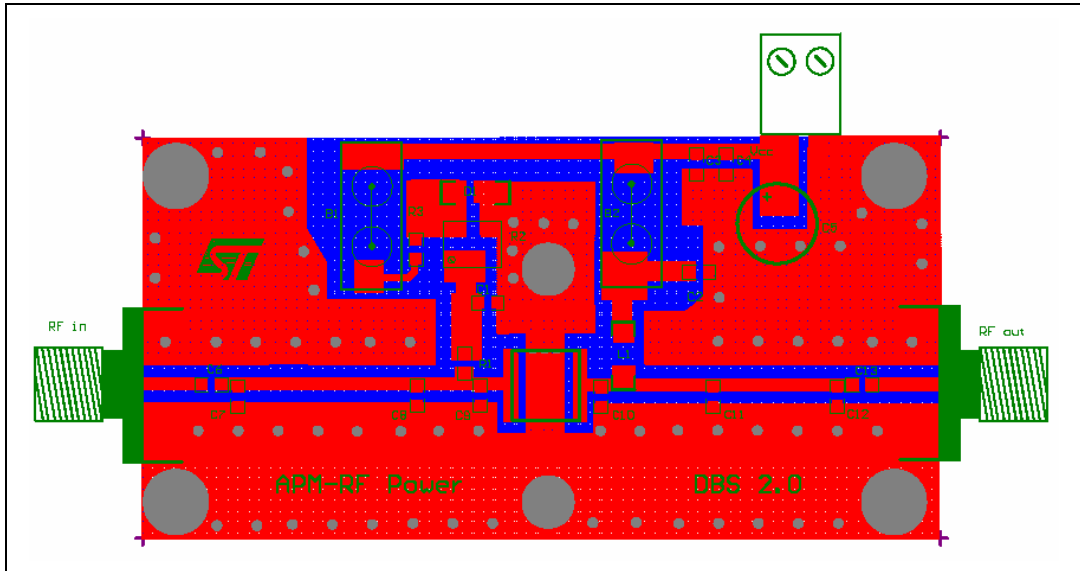
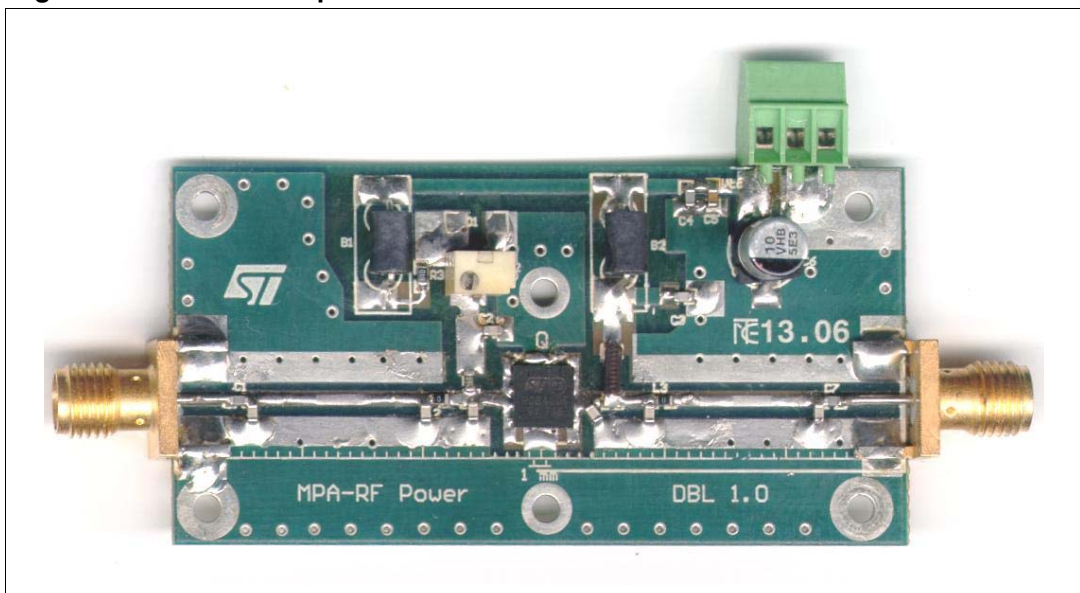


Figure 10. Demoboard photo



## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 10. Tape and reel dimensions

Dim.	Mm		
	Min.	Typ	Max.
Ao	5.15	5.25	5.35
Bo	5.15	5.25	5.35
Ko	1.0	1.1	1.2

Figure 11. Tape and reel dimensions

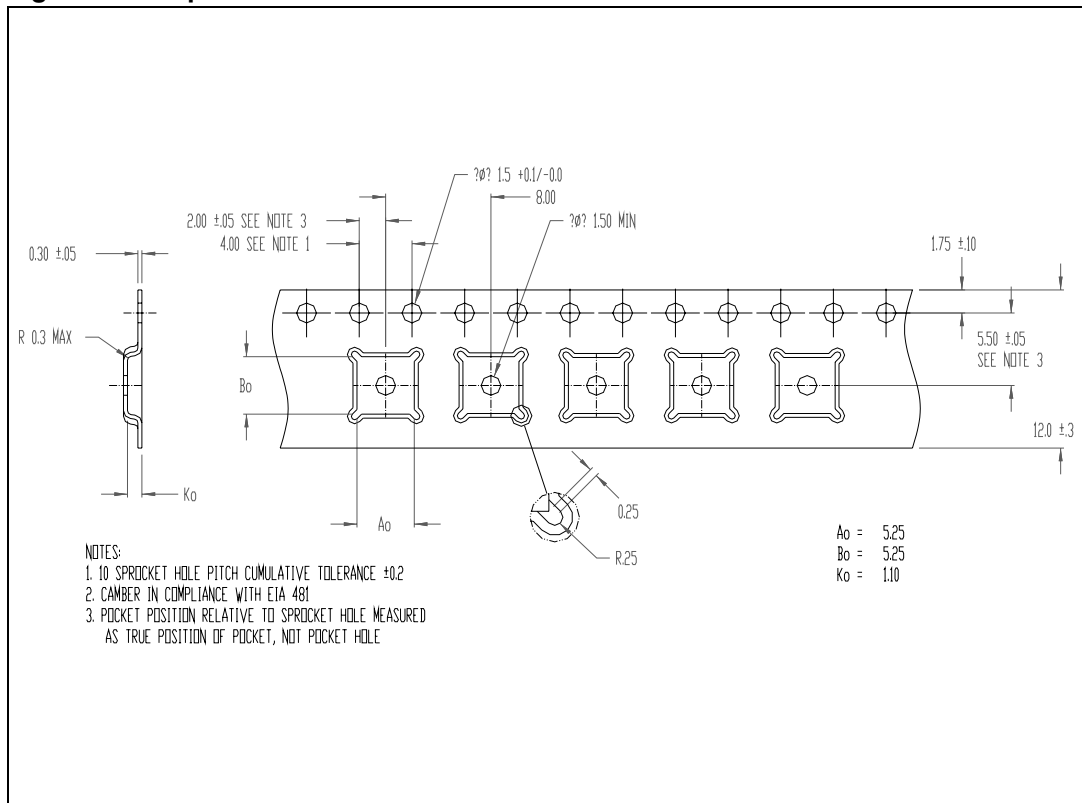
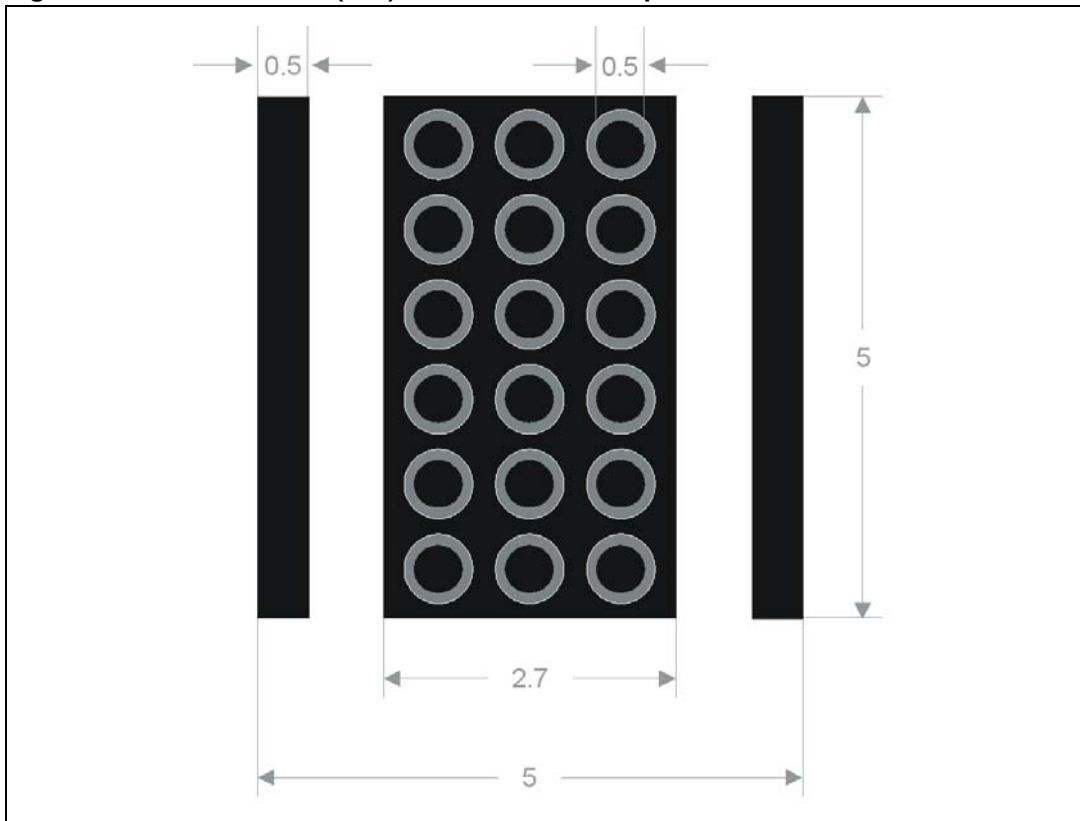


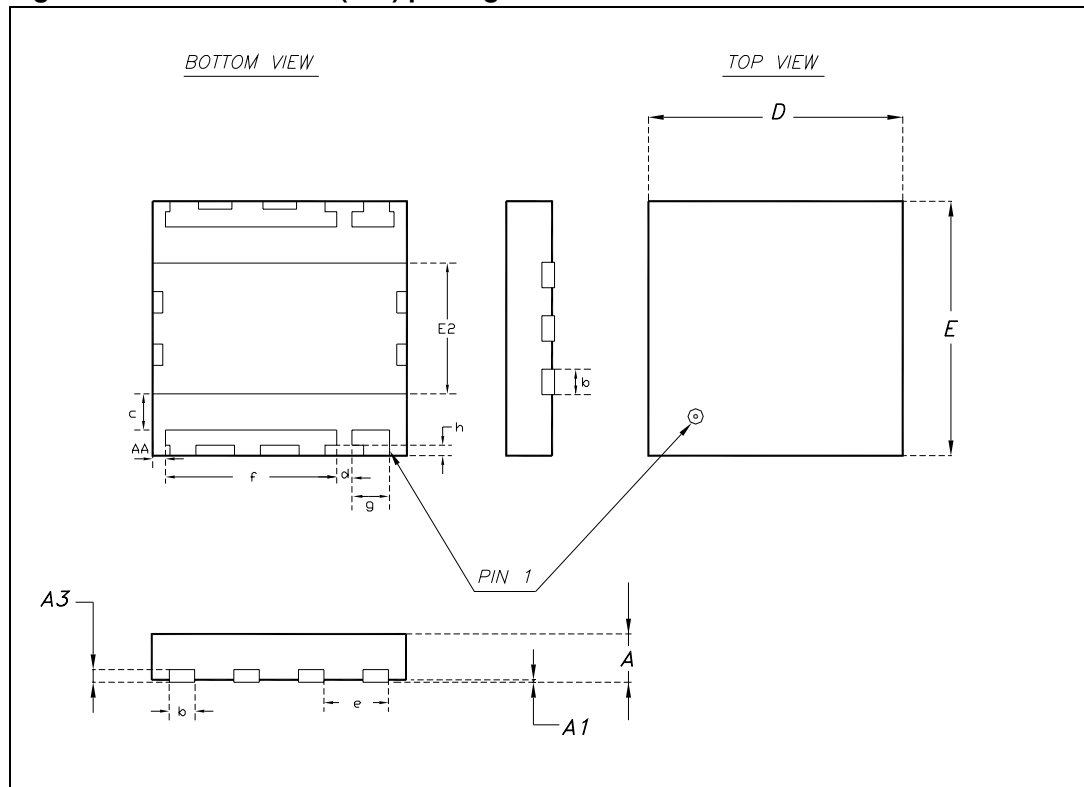
Figure 12. PowerFLAT™ (5x5) recommended footprint



**Table 11. PowerFLAT™ (5x5) mechanical data**

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

**Figure 13. PowerFLAT™ (5x5) package dimensions**



## 8 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
31-Jul-2007	1	First release
29-Jan-2008	2	Added: <i>Section 3: Impedance on page 5, Section 4: Typical performance on page 6, Section 5: Test circuit on page 8, Section 6: Circuit layout and photo on page 10</i>
15-Jul-2008	3	Marking change from 8406 to 84006 see <i>Table 1</i>
14-Dec-2010	4	Updated <i>Table 4</i> .

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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.