

General Description

The MIC2551A is a single chip transceiver that complies with the physical layer specifications of the Universal Serial Bus (USB) 2.0. It supports both full speed (12Mbps) and low speed (1.5Mbps) operation and introduces superior edge rate control, producing crisper eye diagrams, which ease the task of passing USB compliance testing.

A unique, patented, dual supply voltage operation allows the MIC2551A to reference the system I/F I/O signals to a supply voltage down to 1.6V while independently powered by the USB V_{BUS} . This allows the system interface to operate at its core voltage without addition of buffering logic and also reduce system operating current.

Features

- Compliant to USB Specification Revision 2.0 for full speed (12Mbps) and low speed (1.5Mbps) operation
- Compliant to IEC-61000-4.2 (Level 3)
- Separate I/O supply with operation down to 1.6V
- Integrated speed select termination supply
- Very-low power consumption to meet USB suspend-current requirements
- Small TSSOP and MLF[®] packages
- No power supply sequencing requirements
- Software controlled re-enumeration

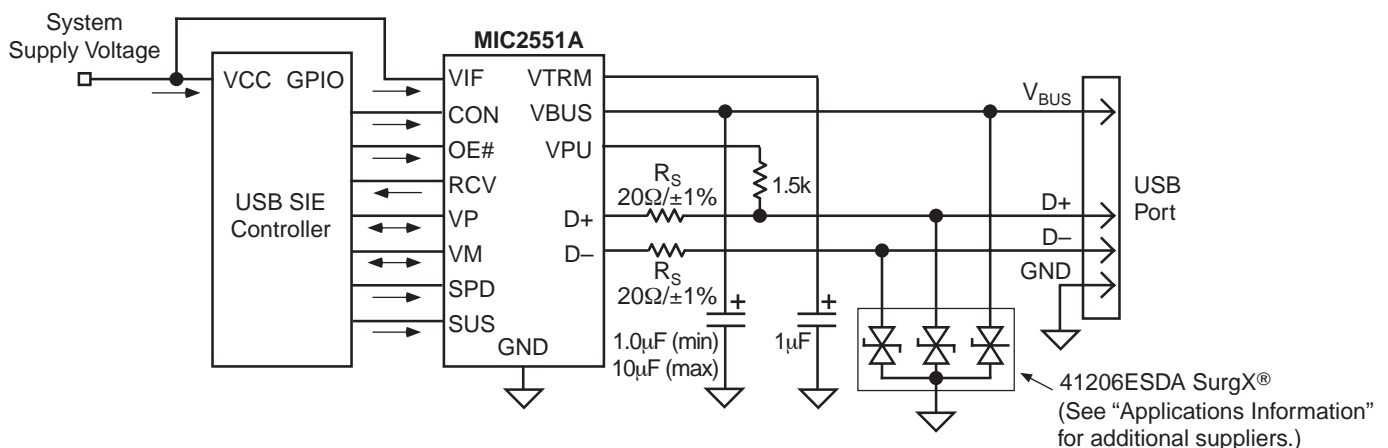
Applications

- PDAs
- Palmtops
- Cell phones

Ordering Information

Part Number		Package
Standard	Pb-Free	
MIC2551ABTS	MIC2551AYTS	14-Pin TSSOP
MIC2551ABML	MIC2551AYML	16-Pin MLF [®]

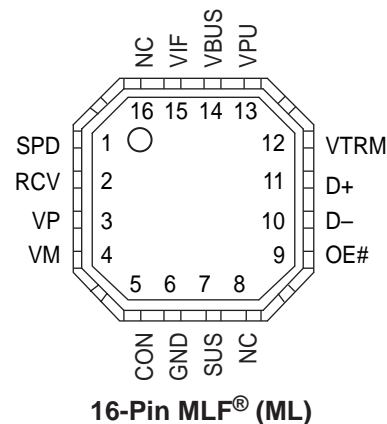
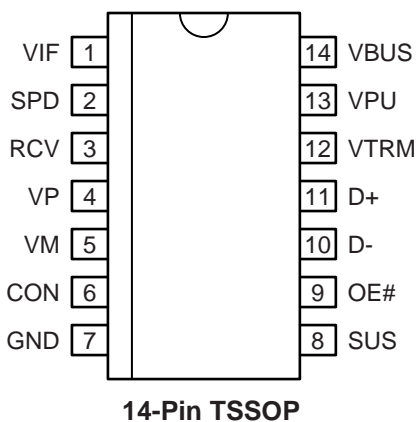
Typical Application



Typical Application Circuit

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Pin Configuration



Pin Description

Pin Number MIC2551ABTS	Pin Number MIC2551ABML	Pin Name	I/O	Pin Function
1	15	VIF	I	System Interface Supply Voltage: Used to provide reference supply voltage for system I/O interface signaling.
2	1	SPD	I	Edge Rate Control: A logic HIGH operates at edge rates for "full speed" operation. A logic LOW operates edge rates for "low speed" operation.
3	2	RCV*	O	Receive Data: Output for USB differential data.
4	3	VP*	I/O	If OE# = 1, VP = Receiver output (+) If OE# = 0, VP = Driver input (+)
5	4	VM*	I/O	If OE# = 1 VM, = Receiver output (-) If OE# = 0, VM = Driver input (-)
6	5	CON	I	CONNECT (Input): Controls state of VPU. Refer to VPU pin description for detail.
7	6	GND		Ground Reference.
8	7	SUS	I	Suspend: Active-High. Turns off internal circuits to reduce supply current.
9	9	OE#*	I	Output Enable: Active-Low. Enables the transceiver to transmit data onto the bus. When inactive, the transceiver is in the receive mode.
10/11	10/11	D-, D+*	I/O	Differential data lines conforming to the USB standard.
12	12	VTRM	O	3.3V Reference Supply Output: Requires a minimum 0.1 μ F decoupling capacitor for stability. A 1 μ F capacitor is recommended
13	13	VPU	O	Pull-up Supply Voltage Output: Used to connect 1.5k Ω pull-up speed detect resistor. If CON = 1, VPU is high impedance. If CON = 0, VPU = 3.3V.
14	14	VBUS	I	USB Bus Supply Voltage: Used to power USB transceiver and internal circuitry.
	8,16	NC		No connect.

* See Table 1 for description of logic states.

SUS	OE#	D+, D-	RCV	VP/VM	Function
0	0	Driving	Active	Active	Normal transmit mode.
0	1	Receiving	Active	Active	Normal receive mode.
1	0	Hi-Z	0	Not active	Low power state.
1	1	Hi-Z	0	Active	Receiving during suspend (low power state) (Note 1).

Note 1. During suspend VP and VM are active in order to detect out-of-band signaling conditions.

Table 1. Function Selection

OE# = 0:					
Input		Output			Result
VP	VM	D+	D-	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined
OE# = 1:					
Input		Output			Result
D+	D-	VP	VM	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

X - Undefined

Table 2. Truth Table During Normal Mode

DC Electrical Characteristics (Transceiver) (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Leakage Current						
I_{LO}	Hi-Z State Data Line Leakage (Suspend Mode)	$0V < V_{IN} < 3.3V$, SUS = 1	-10		10	μA
Input Levels						
V_{DI}	Differential Input Sensitivity	$ (D+) - (D-) $	0.2			V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis			200		mV
Output Levels						
V_{OL}	Static Output Low	$R_L = 1.5k\Omega$ to 3.6V			0.3	V
V_{OH}	Static Output High	$R_L = 15k\Omega$ to GND	2.8		3.6	V
Capacitance						
C_{IN}	Transceiver Capacitance	Pin to GND		10		pF
Z_{DRV}	Driver Output Resistance	Steady state drive	8	16	24	Ω

AC Electrical Characteristics (Notes 6, 7)**Driver Characteristics (Low Speed)**

T_R	Transition Rise Time	$C_L = 50pF$, Figure 2 $C_L = 600pF$	75		300	ns
T_F	Transition Fall Time	$C_L = 50pF$, Figure 2 $C_L = 600pF$	75		300	ns
T_R, T_F	Rise/Fall Time Matching	(T_R, T_F)	80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V

Driver Characteristics (Full Speed)

T_R	Transition Rise Time	$C_L = 50pF$, Figure 2	4		20	ns
T_F	Transition Fall Time	$C_L = 50pF$, Figure 2	4		20	ns
T_R, T_F	Rise/Fall Time Matching	(T_R, T_F)	90		111.11	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V

Transceiver Timing

t_{PVZ}	OE# to RCVR Tri-State Delay	Figure 1			15	ns
t_{PZD}	Receiver Tri-State to Transmit Delay	Figure 1	15			ns
t_{PDZ}	OE# to DRVR Tri-State Delay	Figure 1			15	ns
t_{PZV}	Driver Tri-State to Receive Delay	Figure 1	15			ns
t_{PLH} t_{PHL}	VP, VM to D+, D- Propagation Delay	Figure 4			15	ns
t_{PLH} t_{PHL}	D+, D- to RCV Propagation Delay	Figure 3			15	ns
t_{PLH} t_{PHL}	D+, D- to V_P, V_M Propagation Delay	Figure 3			8	ns

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

Note 4. Specification applies to the following pins: SUS, SPD, RCV, CON, RCV, VP, VM, OE#.

Note 5. Characterized specification(s), but not production tested.

Note 6. All AC parameters guaranteed by design but not production tested.

Note 7. Specification for packaged product only.

Timing Diagrams

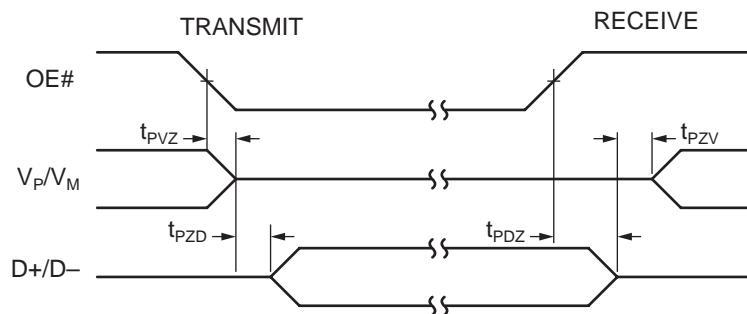


Figure 1. Enable and Disable Times

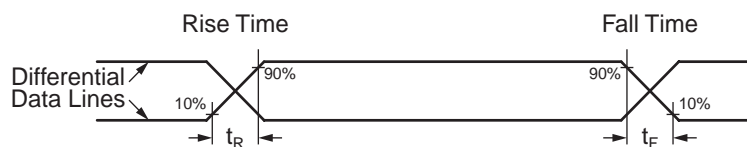


Figure 2. Rise and Fall Times

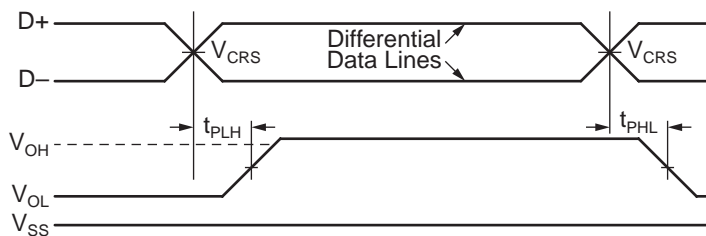


Figure 3. Receiver Propagation Delay

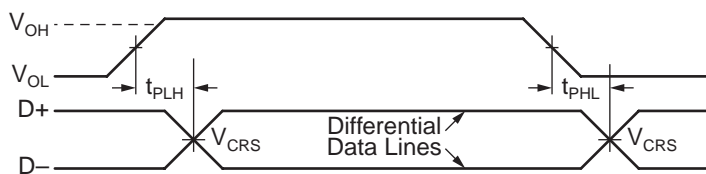


Figure 4. Driver Propagation Delay

Test Circuits

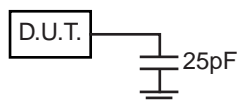


Figure 5. Load for V_p , V_m , RCV

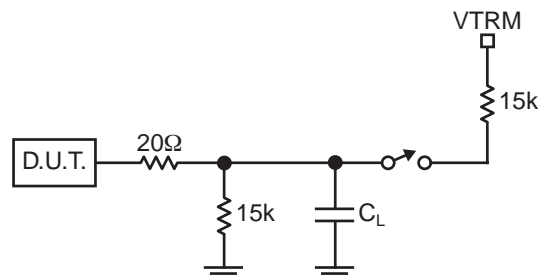
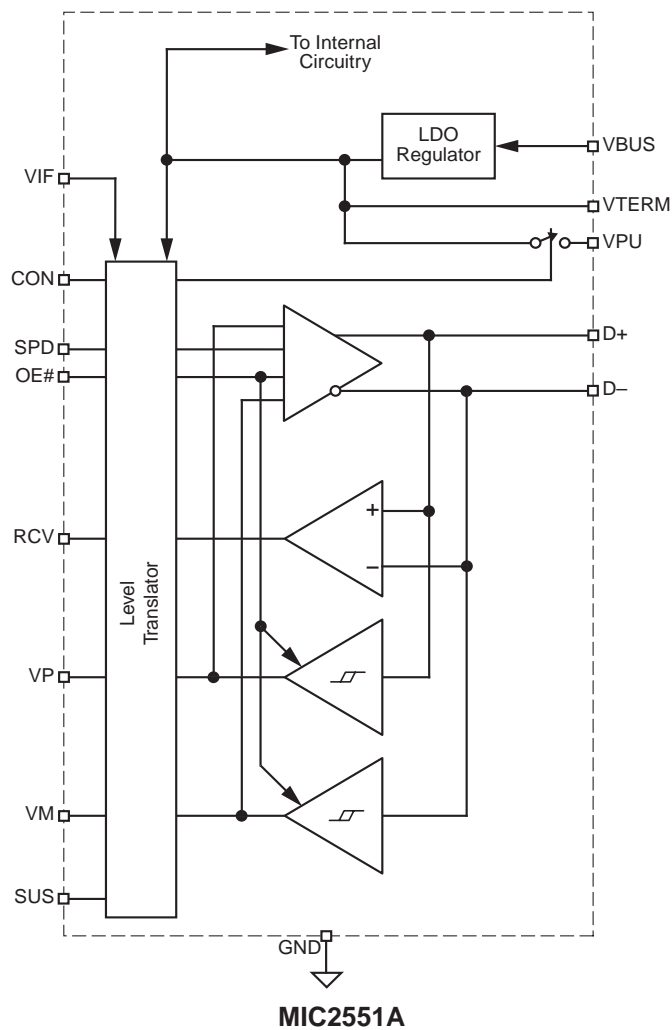


Figure 6. Load for $D+$, $D-$

Functional Diagram



Applications Information

The MIC2551A is designed to provide USB connectivity in mobile systems where available system supply voltages are not able to satisfy USB requirements. The MIC2551A can operate down to supply voltages of 1.6V and still meet USB physical layer specifications. As shown in the circuit above, the MIC2551A takes advantage of the USB supply voltage, V_{BUS} , to operate the transceiver. The system voltage, V_{IF} , is used to set the reference voltage used by the digital I/O lines interfacing to the system controller. Internal circuitry provides translation between the USB and system voltage domains. V_{IF} will typically be the main supply voltage rail for the controller.

In addition, a 3.3V, 10% termination supply voltage, (V_{PU}), is provided to support speed selection. V_{PU} can be disabled or enabled under software control via the CON input. This allows for software-controlled connect or disconnect states. A 1.5k resistor is required to be connected between this pin and the D+ or D- lines to respectively specify high speed or low speed operation.

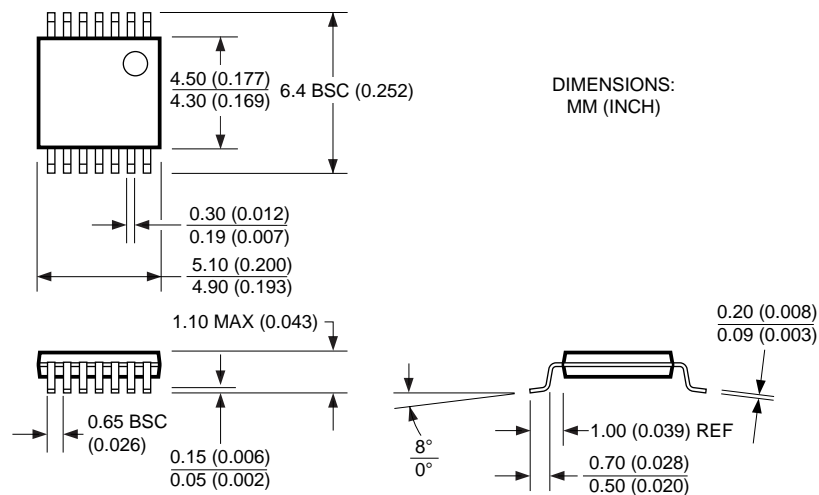
The use of ESD transient protection devices is not required for operation, but is recommended. The MIC2551A is ESD rated for 11kV at the VBUS and D+, D- pins and 2kV for all other pins.

PCB Layout Recommendations

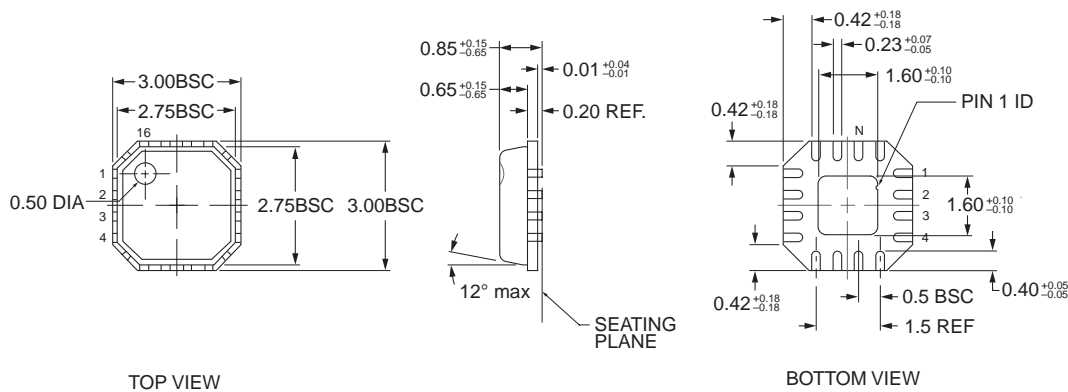
Although the USB standard and applications are not based in an impedance controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

- Match signal line traces (VP/VM, D+, D-) to 40ps, approximately $\frac{1}{3}$ inch if possible. FR-4 PCB material propagation is about 150ps/inch, so to minimize skew try to keep VP/VM, D+/D- traces as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5 – 2 widths. Place all other traces at >2 widths from all signal line traces.
- Maintain the same number of vias on each differential trace, keeping traces approximately at same separation distance along the line.
- Control signal line impedances to $\pm 10\%$.
- Keep R_S as close to the IC as possible, with equal distance between R_S and the IC for both D+ and D-.

Package Information

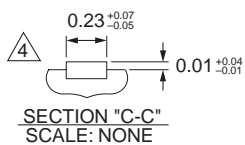
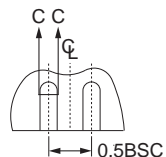


14-lead TSSOP (TS)



TOP VIEW

BOTTOM VIEW

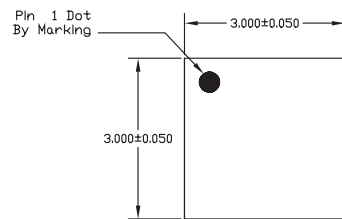


1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

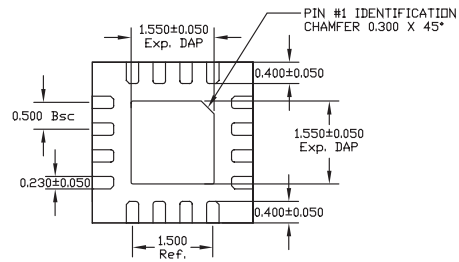
FOR EVEN TERMINAL/SIDE

Rev. 02

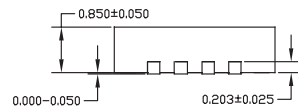
16-Pin MLF[®] (ML)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin MLF[®] (ML)

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