

## DESCRIPTION

The MP62340/MP62341 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62340/MP62341 analog switch has 80mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP62340/MP62341 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, then the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62340/MP62341 is available in 8-pin MSOP package with exposed pad and SOIC package without exposed pad.

## FEATURES

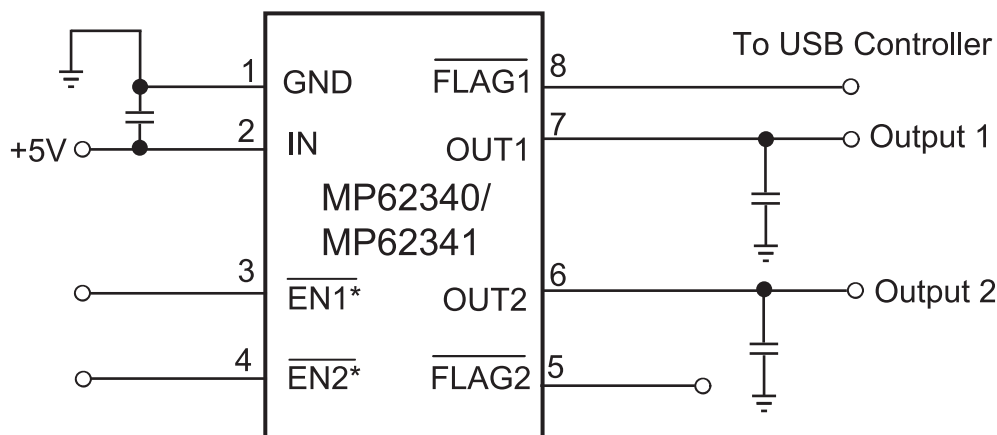
- 1A Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 140 μA Quiescent Current
- 80mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- Available in MSOP8E and SOIC8
- UL Approved—E322138

## APPLICATIONS

- PDAs
- Portable GPS
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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## TYPICAL APPLICATION



\* EN is active high for MP62341

## ORDERING INFORMATION

| Part Number | Enable      | Switch | Maximum Continuous Load Current | Typical Short-Circuit Current @ T <sub>A</sub> =25C | Package | Top Marking | Free Air Temperature Range (T <sub>A</sub> ) |
|-------------|-------------|--------|---------------------------------|-----------------------------------------------------|---------|-------------|----------------------------------------------|
| MP62340DS   | Active Low  | Dual   | 1A                              | 1.5A                                                | SOIC8   | 62340DS     | –40°C to +85°C                               |
| MP62340DH   |             |        |                                 |                                                     | MSOP8E  | 62340DH     |                                              |
| MP62341DS   | Active High |        |                                 |                                                     | SOIC8   | 62341DS     |                                              |
| MP62341DH   |             |        |                                 |                                                     | MSOP8E  | 62341DH     |                                              |

\* For Tape & Reel, add suffix –Z (e.g. MP62340DS -LF–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP62340DS -LF–Z)

## PACKAGE REFERENCE

|                                                                                                                                                |                                             |
|------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| <p><b>TOP VIEW</b></p> <p><b>SOIC8</b></p>                                                                                                     | <p><b>TOP VIEW</b></p> <p><b>MSOP8E</b></p> |
| <p align="center"><b>MP62340/MP62341</b></p> <p align="center"><b>Dual-Channel</b></p> <p align="center">(* EN is active high for MP62341)</p> |                                             |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                      |                 |
|----------------------------------------------------------------------|-----------------|
| IN.....                                                              | –0.3V to +6.0V  |
| EN, FLAG, OUT to GND .....                                           | –0.3V to +6.0V  |
| Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup> |                 |
| MSOP8E.....                                                          | 2.3W            |
| SOIC8.....                                                           | 1.4W            |
| Junction Temperature.....                                            | 150°C           |
| Lead Temperature .....                                               | 260°C           |
| Storage Temperature.....                                             | –65°C to +150°C |
| Operating Junction Temp (T <sub>J</sub> ) ...                        | –40°C to +125°C |

|                                          |                       |                       |
|------------------------------------------|-----------------------|-----------------------|
| <b>Thermal Resistance <sup>(3)</sup></b> | <b>θ<sub>JA</sub></b> | <b>θ<sub>JC</sub></b> |
| SOIC8 .....                              | 90 .....              | 42 ... °C/W           |
| MSOP8E .....                             | 55 .....              | 12 ... °C/W           |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-toambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (T<sub>J</sub> (MAX) – T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS <sup>(4)</sup>

$V_{IN}=5V$ ,  $T_A=+25^{\circ}C$ , unless otherwise noted.

| Parameter                                    | Condition                                                     | Min  | Typ | Max  | Units       |
|----------------------------------------------|---------------------------------------------------------------|------|-----|------|-------------|
| IN Voltage Range                             |                                                               | 2.7  |     | 5.5  | V           |
| Supply Current                               | One Channel Enabled, $I_{OUT}=0$ , One Switch ON              |      | 90  | 120  | $\mu A$     |
| Supply Current                               | Both Channels Enabled, $I_{OUT}=0$ , Both Switches ON         |      | 140 | 160  | $\mu A$     |
| Shutdown Current                             | Device Disable, $V_{OUT}=float$ , $V_{IN}=5.5V$               |      | 1   |      | $\mu A$     |
| Off Switch Leakage                           | Device Disable, $V_{IN}=5.5V$                                 |      | 1   |      | $\mu A$     |
| Current Limit                                |                                                               | 1.1  | 1.5 | 2.2  | A           |
| Trip Current                                 | Current Ramp (slew rate $\leq 100A/s$ ) on Output             | 1.6  | 1.7 | 2.4  | A           |
| Under-voltage Lockout                        | Rising Edge                                                   | 1.95 |     | 2.65 | V           |
| Under-voltage Hysteresis                     |                                                               |      | 250 |      | mV          |
| FET On Resistance                            | $I_{OUT}=100mA$ ( $-40^{\circ}C \leq T_J \leq 125^{\circ}C$ ) |      | 80  | 130  | m $\Omega$  |
| EN Input Logic High Voltage                  |                                                               | 2    |     |      | V           |
| EN Input Logic Low Voltage                   |                                                               |      |     | 0.8  | V           |
| FLAG Output Logic Low Voltage                | $I_{SINK}=5mA$                                                |      |     | 0.4  | V           |
| FLAG Output High Leakage Current             | $V_{IN}=V_{FLAG}=5.5V$                                        |      |     | 1    | $\mu A$     |
| Thermal Shutdown                             |                                                               |      | 140 |      | $^{\circ}C$ |
| Thermal Shutdown Hysteresis                  |                                                               |      | 20  |      | $^{\circ}C$ |
| $V_{OUT}$ Rising Time, $T_r$ <sup>(5)</sup>  | $V_{IN}=5.5V$ , $C_L=1\mu F$ , $R_L=5.5\Omega$                |      | 0.9 |      | ms          |
|                                              | $V_{IN}=2.7V$ , $C_L=1\mu F$ , $R_L=5.5\Omega$                |      | 1.7 |      | ms          |
| $V_{OUT}$ Falling Time, $T_f$ <sup>(6)</sup> | $V_{IN}=5.5V$ , $C_L=1\mu F$ , $R_L=5.5\Omega$                |      |     | 0.5  | ms          |
|                                              | $V_{IN}=2.7V$ , $C_L=1\mu F$ , $R_L=5.5\Omega$                |      |     | 0.5  | ms          |
| Turn On Time, $T_{on}$ <sup>(7)</sup>        | $C_L=100\mu F$ , $R_L=5.5\Omega$                              |      |     | 3    | ms          |
| Turn Off Time, $T_{off}$ <sup>(8)</sup>      | $C_L=100\mu F$ , $R_L=5.5\Omega$                              |      |     | 10   | ms          |
| FLAG Deglitch Time                           |                                                               | 4    | 8   | 15   | ms          |
| EN Input Leakage                             |                                                               |      | 1   |      | $\mu A$     |
| Reverse Leakage Current                      | $V_{OUT}=5.5V$ , $V_{IN}=GND$                                 |      | 0.2 |      | $\mu A$     |

### Notes:

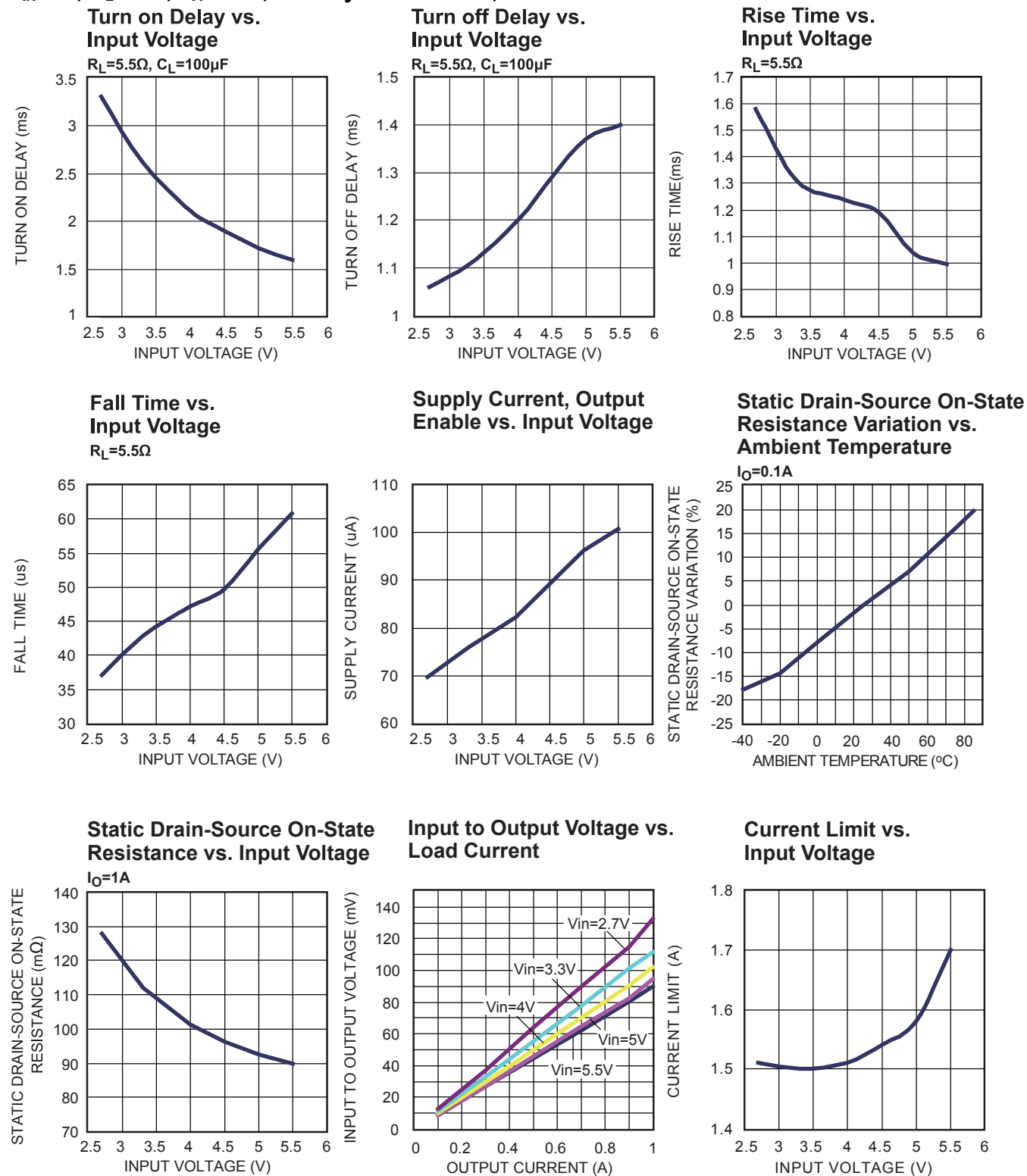
- 4) Production test at  $+25^{\circ}C$ . Specifications over the temperature range are guaranteed by design and characterization.
- 5) Measured from 10% to 90% output signal.
- 6) Measured from 90% to 10% output signal.
- 7) Measured from 50% EN signal to 90% output signal.
- 8) Measured from 50% EN signal to 10% output signal.

## PIN FUNCTIONS

| SOIC8<br>MSOP8E | Name                            | Description                                                                              |
|-----------------|---------------------------------|------------------------------------------------------------------------------------------|
| 1               | GND,<br>Exposed Pad<br>(MSOP8E) | Ground. MSOP8E includes exposed pad. Connect to GND plane for optimal thermal operation. |
| 2               | IN                              | Input Voltage. Accepts 2.7V to 5.5V input.                                               |
| 3               | $\overline{\text{EN1}}$         | Active Low: (MP62340), Active High: (MP62341)                                            |
| 4               | $\overline{\text{EN2}}$         | Active Low: (MP62340), Active High: (MP62341)                                            |
| 5               | FLAG2                           | IN-to-OUT2 Over-current, active-low output flag. Open-Drain.                             |
| 6               | OUT2                            | IN-to-OUT2 Power-Distribution Switch Output.                                             |
| 7               | OUT1                            | IN-to-OUT1 Power-Distribution Switch Output                                              |
| 8               | FLAG1                           | IN-to-OUT1 Over-current, active-low output flag. Open-Drain.                             |

# TYPICAL PERFORMANCE CHARACTERISTICS

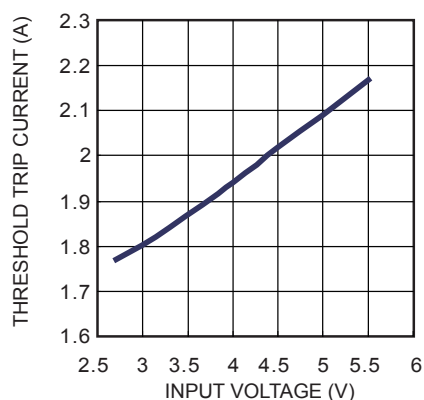
$V_{IN}=5V$ ,  $C_L=1\mu F$ ,  $T_A=25^\circ C$ , for only one channel, unless otherwise noted.



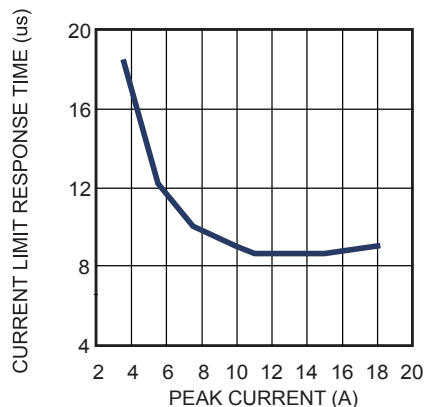
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}=5V$ ,  $C_L=1\mu F$ ,  $T_A=25^\circ C$ , for only one channel, unless otherwise noted.

Threshold Trip Current vs.  
Input Voltage

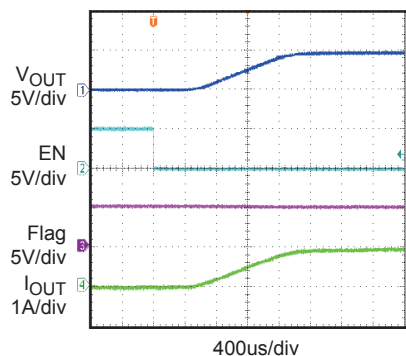


Current Limit Response Time  
vs. Peak Current



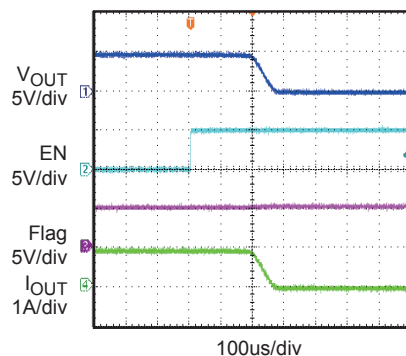
Turn On Delay and Rise Time  
with  $1\mu F$  Load

$I_{OUT}=1A$



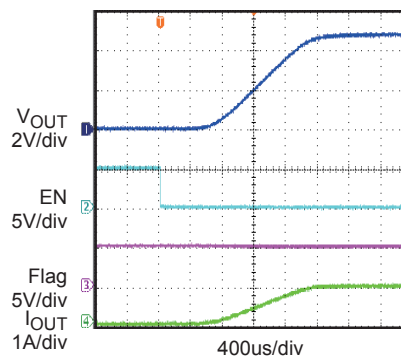
Turn Off Delay and Fall Time  
with  $1\mu F$  Load

$I_{OUT}=1A$



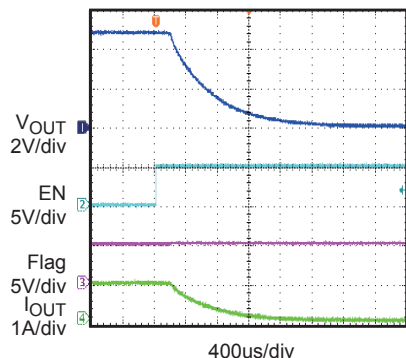
Turn On Delay and Rise Time  
with  $100\mu F$  Load

$I_{OUT}=1A$ ,  $C_L=100\mu F$

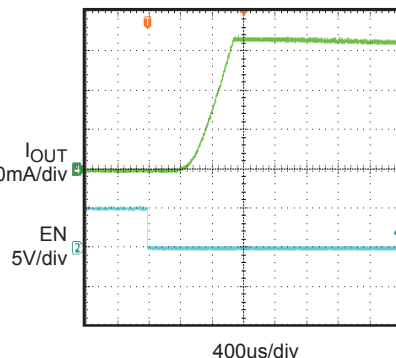


Turn Off Delay and Fall Time  
with  $100\mu F$  Load

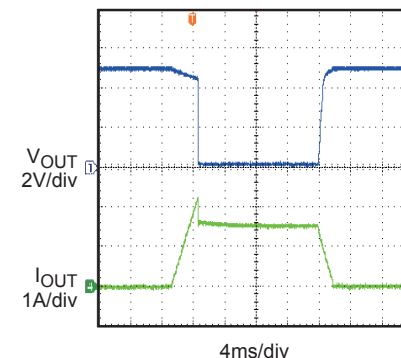
$I_{OUT}=1A$ ,  $C_L=100\mu F$



Short Circuit Current,  
Device Enabled into Short



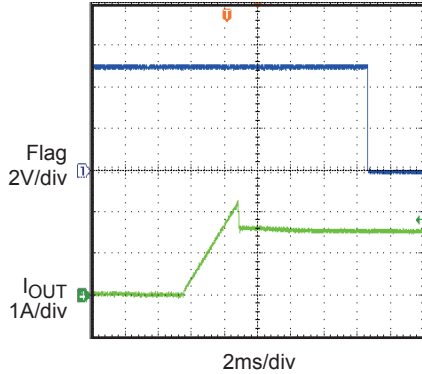
Threshold Trip Current with  
Ramped Load  
on Enabled Device



## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

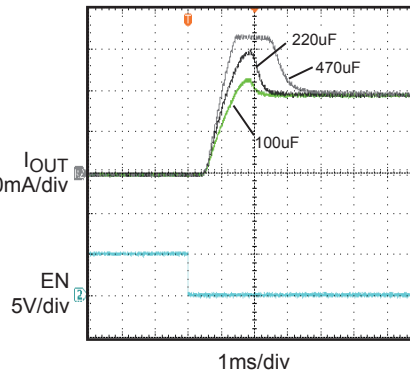
$V_{IN}=5V$ ,  $C_L=1\mu F$ ,  $T_A=25^\circ C$ , for only one channel, unless otherwise noted.

**Ramped Load  
on Enabled Device**

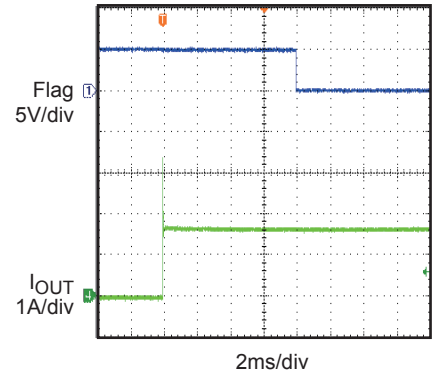


**Inrush Current with  
Different Load Capacitance**

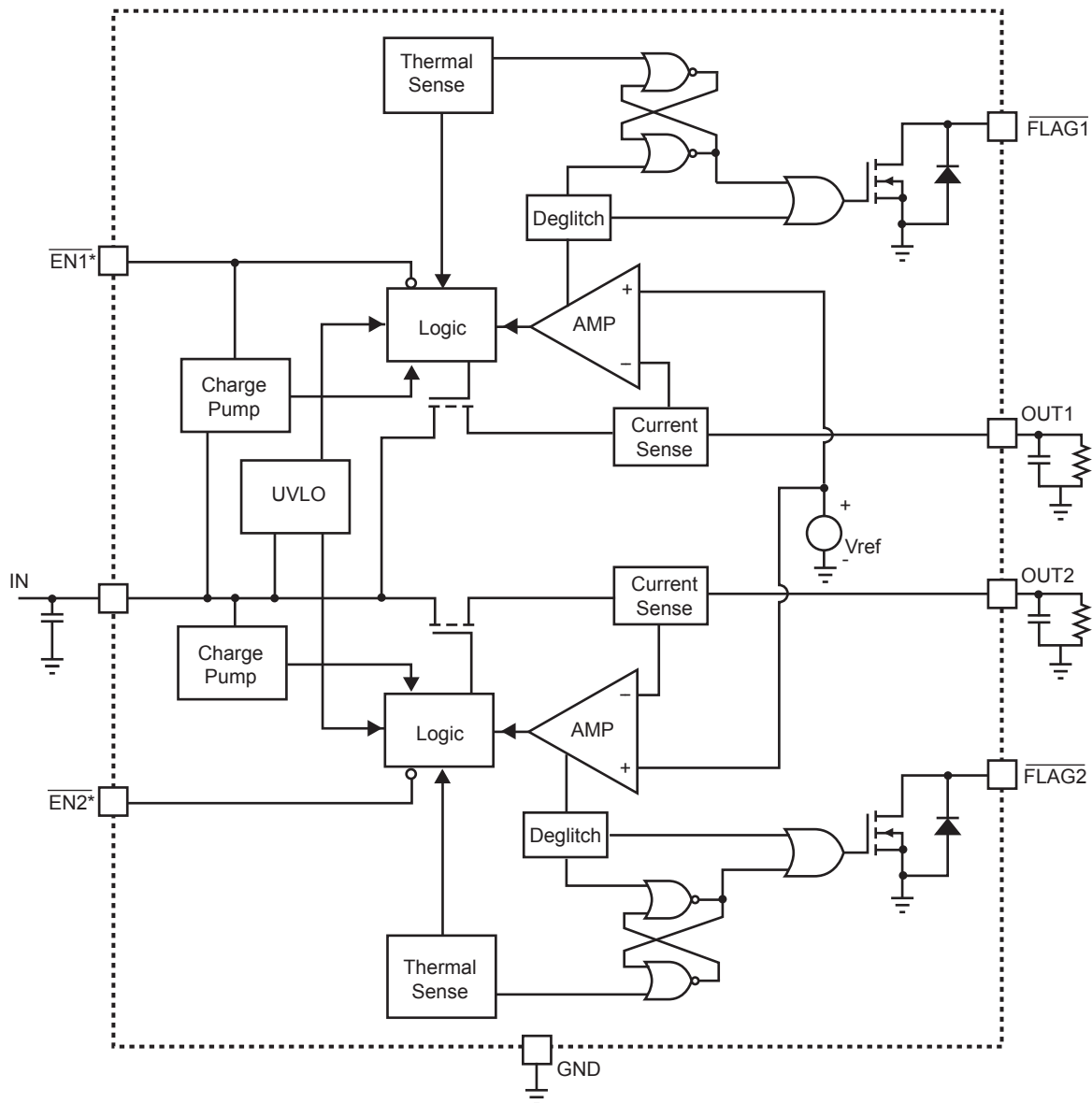
$I_{OUT}=1A$



**1Ω Load Connected to  
Enabled Device**



## FUNCTION BLOCK DIAGRAM



\* EN is active high for MP62341

Figure 2—Functional Block Diagram

## DETAILED DESCRIPTION

### Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62340/MP62341 switches into to a constant-current mode (current limit value). MP62340/MP62341 will be shutdown only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

- 1) The output has been shorted or overloaded before the device is enabled or input applied. MP62340/MP62341 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
- 3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. MP62340/MP62341 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

### Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or voltage lockout.

### Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temp. is internally monitored until the thermal limit is reached. Once this temp. is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

### Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62340/MP62341 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

### Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

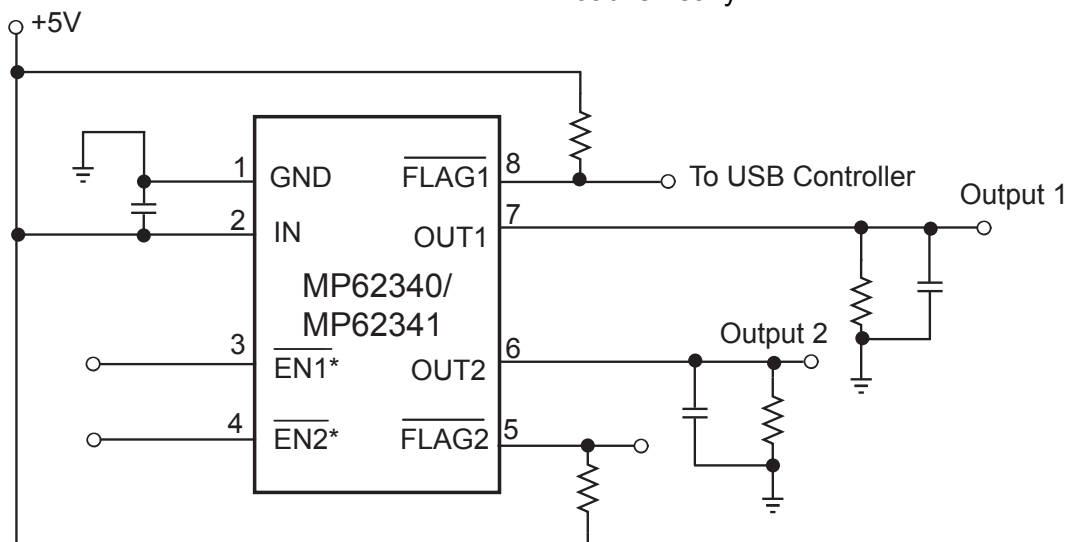
## APPLICATION INFORMATION

### Power-Supply Considerations

Over 10 $\mu$ F capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the

input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy.

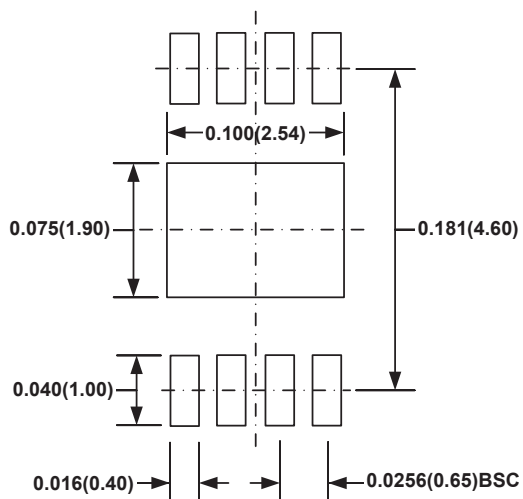
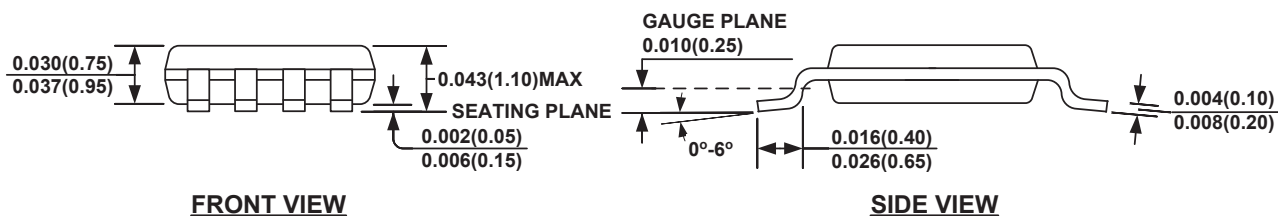
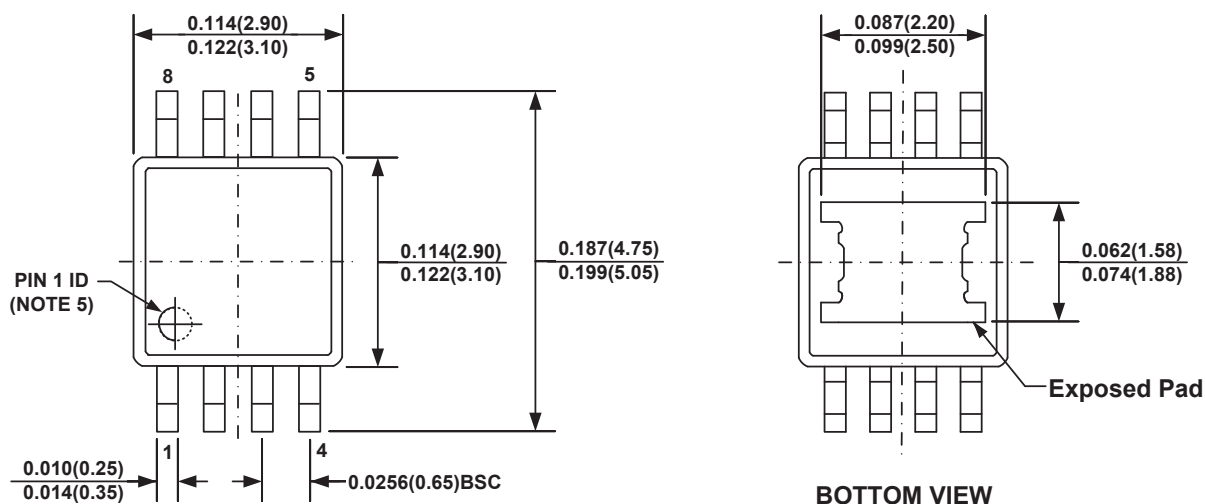


\* EN is active high for MP62341

Figure 3—Application Circuit

## PACKAGE INFORMATION

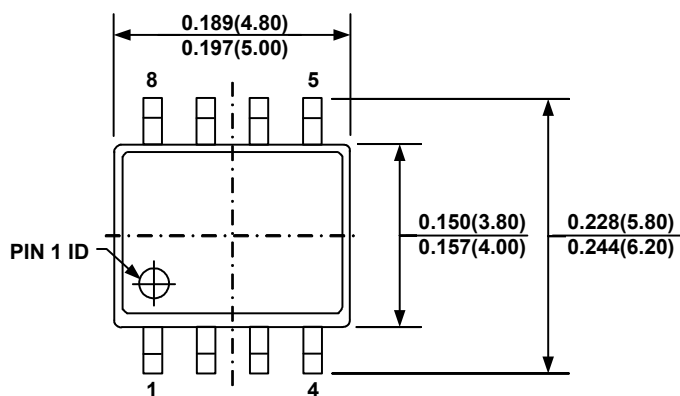
### MSOP8E (EXPOSED PAD)



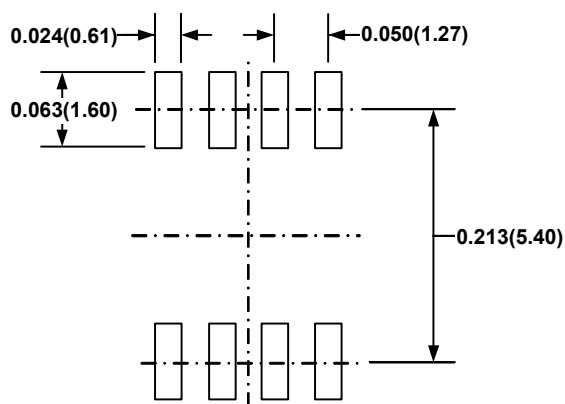
#### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
- 6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
- 7) DRAWING IS NOT TO SCALE.

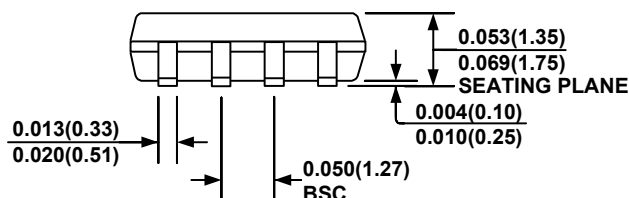
## SOIC8



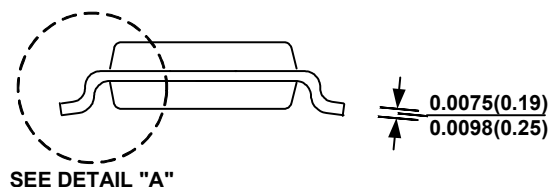
TOP VIEW



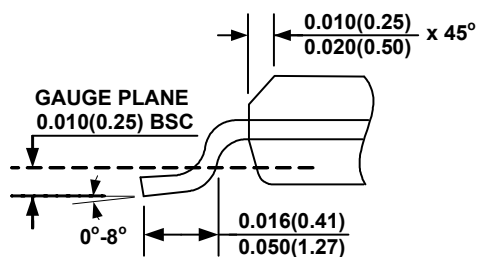
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

## NOTE:

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- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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**Факс:** 8 (812) 320-02-42

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**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.