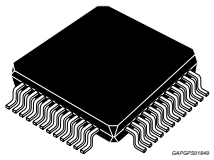
L9780

Wide range air fuel sensor control interface

Datasheet - production data



LQFP48

Features

- Voltage controlled current source (VCCS) pump cell driver with selectable voltage clamp, offset compensation, diagnostic (short to battery) and 2 output channels
- Impedance measurement of reference cell
- 10-bit multiplexed A/D converter
- Scaling amplifier with sample & hold and offset compensation
- Control voltage amplifier with sample & hold and offset compensation
- Synchronous or asynchronous functionality selectable via SPI
- Heater FET driver with diagnostic (short to battery, short to ground, open circuit)
- 4 possible levels for clean current
- SPI with fault detection
- Digital input and outputs compatible with 5 V or 3.3 V voltage supply
- 2 channels available to connect compensation networks
- Short to battery diagnostic on functional ground (pin SR)
- Short to battery/ground diagnostic on voltage from reference cell (pin INRC)
- -5 V internal supply
- 4 MHz internal oscillator
- Package: 48 pin LQFP
- Technology: BCD5s_70 V

Description

L9780 is an IC designed to interface a variety of wide range air fuel sensors.

The device manages the oxygen pump of the wide range air fuel sensor by means of a voltage controlled current source (VCCS). The reference for the VCCS is generated by a PI controller with external compensation network in order to adapt the device to different sensors. The user can choose between two different networks using the SPI interface. L9780 is fully compatible with most sensors on the market.

The internal timing state machine automatically manages all the operations needed for a right sequencing of the measurement process. All the main time values can be configured by SPI.

L9780 drives also an external FET used to control the sensor heater. The device protects the sensor and all the I/O against shorts and provides the diagnosis by SPI.

Table 1. Device summary

Order code	Package	Packing
L9780	LQFP48	Tray
L9780TR	LQFP48	Tape and reel

Contents

List of tables

List of figures

1 Pin description

Figure 1. Pin connection diagram (top view)

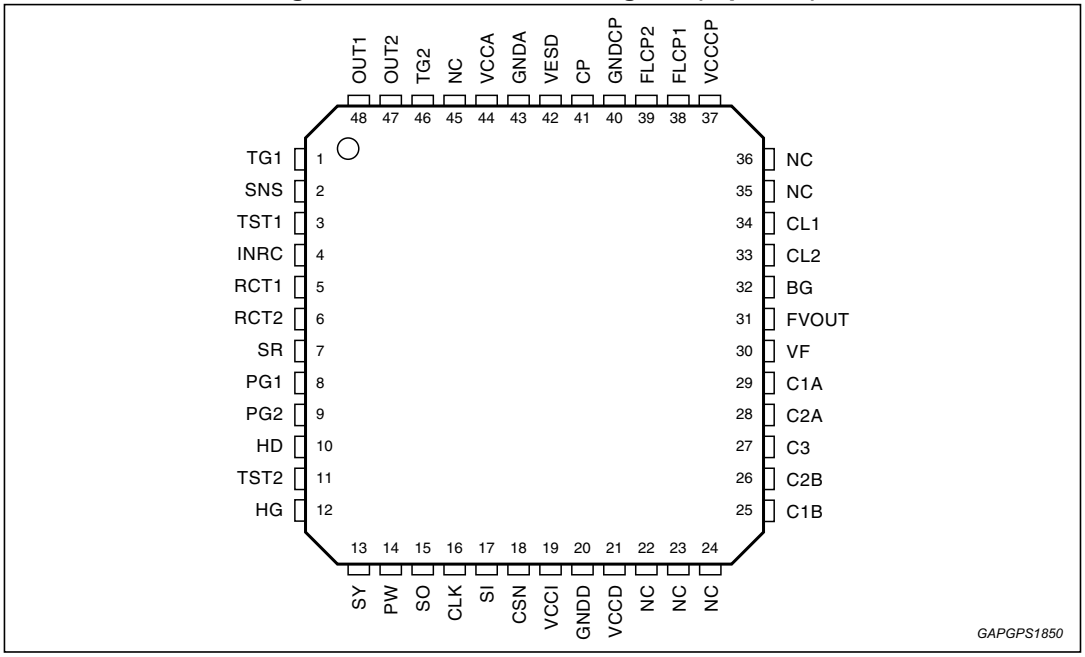


Table 2. Pin function

Pin number	Pin name	Pin description
1	TG1	Switching TAG resistor pin channel 1
2	SNS	VCCS sense pin
3	TST1	Test mode pin 1
4	INRC	Reference cell input
5	RCT1	Impedance test pin 1
6	RCT2	Impedance test amplifier input
7	SR	Sensor return
8	PG1	Protection fet gate channel 1
9	PG2	Protection fet gate channel 2
10	HD	Heater fet drain
11	TST2	Test mode pin 2
12	HG	Heater fet gate
13	SY	Synchronous mode pin
14	PW	Heater PWM input pin
15	SO	Serial data output
16	CLK	SPI clock
17	SI	Serial data input

Table 2. Pin function (continued)

Pin number	Pin name	Pin description
18	CSN	SPI chip select
19	VCCI	Digital transfer level supply
20	GNDD	Digital ground
21	VCCD	Digital supply
22	n.c.	Not connected pin
23	n.c.	Not connected pin
24	n.c.	Not connected pin
25	C1B	Compensation network pin1, side B
26	C2B	Compensation network pin2, side B
27	C3	Compensation network common pin
28	C2A	Compensation network pin2, side A
29	C1A	Compensation network pin1, side A
30	FV	VCCS filtered control voltage pin
31	FVOUT	Analog output
32	BG	Bandgap voltage
33	CL2	VCCS voltage clamp channel 2
34	CL1	VCCS voltage clamp channel 1
35	n.c.	Not connected pin
36	n.c.	Not connected pin
37	VCCCP	Charge pump supply
38	FLCP1	Charge pump floating pin 1
39	FLCP2	Charge pump floating pin 2
40	GNDCP	Charge pump analog ground
41	CP	-5V charge pump output
42	VESD	ESD reference voltage
43	GNDA	Analog ground
44	VCCA	Analog supply
45	n.c.	Not connected pin
46	TG2	Switching TAG resistor pin channel 2
47	OUT2	Pump cell output pin channel 2
48	OUT1	Pump cell output pin channel 1

2 Operating conditions

2.1 Maximum ratings

L9780 may not operate out of the maximum rating ranges. Once the correct situation is restored after one of the following conditions is not respected (but not exceeding the absolute maximum rating range) the part is still able to work with no damage.

Table 3. Maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage: VCCA, VCCD, VCCCP VCCI	 4.9 to 5.1 3.14 to 5.1	V
V_{ESD}	ESD reference	40	V
V_{in}	Input voltage HD, RCT1, RCT2, INRC SR, SNS CSN, SI, CLK, PW, SY	 0 to 40 -VCCA to VCCA 0 to VCCA	V
I_{in}	Input current VESD SR, RCT1, RCT2, SNS INRC HD OUT1, OUT2, TG1, TG2 (leakage for maximum short to battery voltage) SR, RCT1, RCT2, SNS, INRC, HD, OUT1, OUT2, TG1, TG2 (when the voltage is driven below the normal operating range) CSN, SI, CLK, PW, SY	 -20 10 50 150 350 -275 ±275	 mA µA µA µA µA µA µA
T_j	Junction temperature	-40 to 150	°C

2.2 Absolute maximum ratings

The part can be irreparably damaged if the voltages out of the absolute maximum ratings ranges are applied to the pins. The part at these ratings could not work properly.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_s	Supply voltage: VCCA, VCCD, VCCCP, VCCI	 -0.3 to +6.5	V
V_{ESD}	ESD reference	+53	V

Table 4. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{in}	Input voltage:		V
	HD	-0.3 to 53(1)	
	RCT1, RCT2, INRC	-0.3 to +40(1)	
	SR, SNS, TGx, OUTx	-VCCA to +40(1)	
	CSN, SI, CLK, PW, SY, SO	-0.3 to VCCI+0.3	
	C1B, C2B, C3, C2A, C1A, BG, CL2, CL1, FV, FVOUT, PG1, PG2, HG	-0.3 to VCCA+0.3	
	CP	-6.5 to +0.3	
	FLCP1	-0.3 to VCCCP+0.3	
	FLCP2	CP-0.3 to +0.3	
	TST1, TST2	-0.3 to 40(1)	
	|TGx – OUTx|	+16	
I_{in}	Input current:		
	VESD	-20	mA
	SR, RCT1, RCT2, SNS	10	µA
	INRC	50	µA
	HD	150	µA
	OUT1, OUT2, TG1, TG2 (leakage for maximum short to battery voltage)	500	µA
	SR, RCT1, RCT2, SNS, INRC, HD, OUT1, OUT2, TG1, TG2 (when the voltage is driven below the normal operating range)	-500	µA
	CSN, SI, CLK, PW, SY	±500	µA
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	+150	°C

1. Voltage at the pin cannot exceed V_{ESD}+0.3 V.

2.3 Operating temperature range

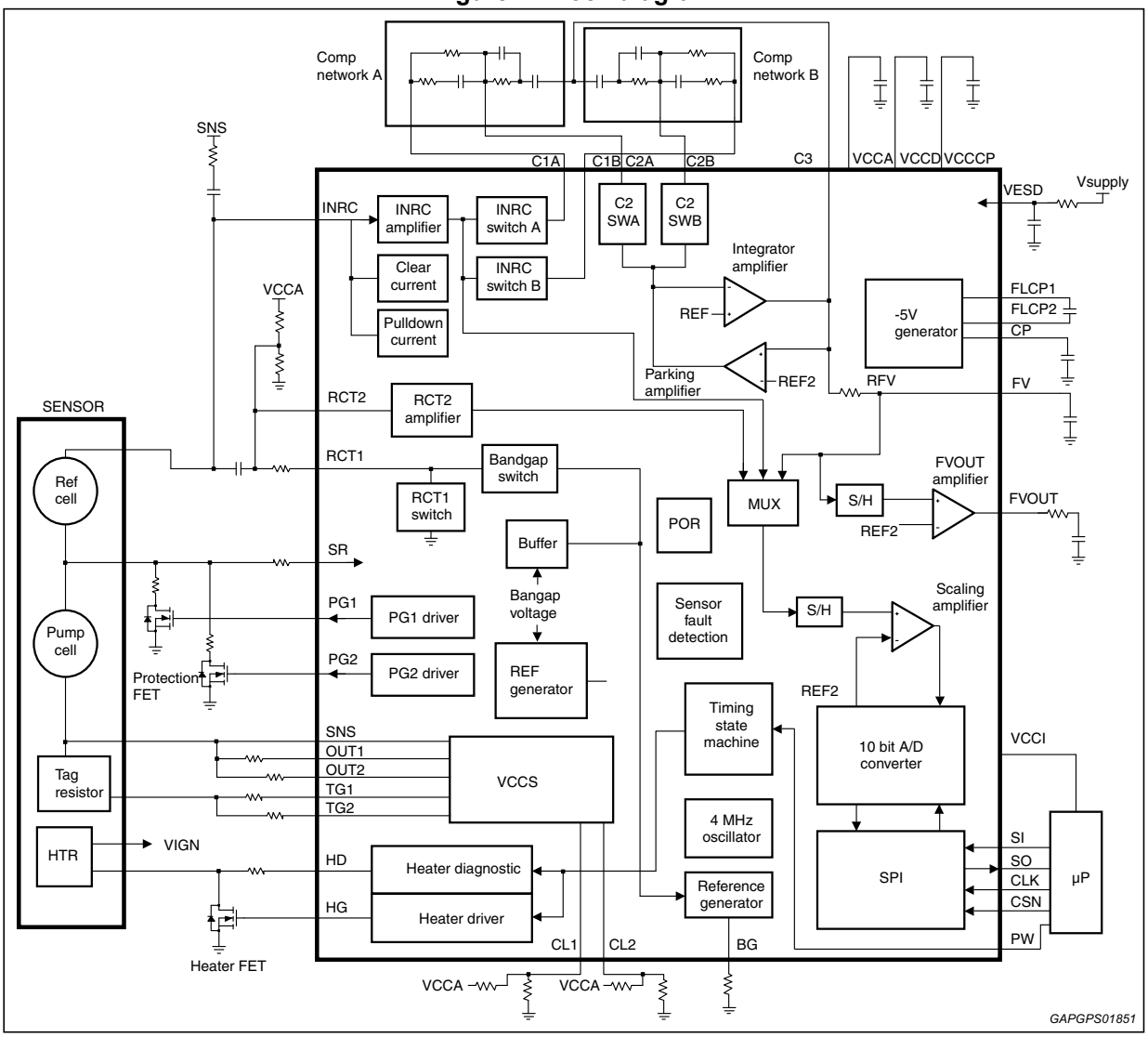
Table 5. Operating temperature range

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range	-40 to 125	°C

3 Block diagram

The following is L9780 block diagram; the description of each block and the definition of external components can be found in the next sections.

Figure 2. Block diagram



4 Main functionalities

4.1 Power supplies

4 different power supplies are present in the device: VCCA, VCCD, VCCCP, VCCI, respectively for analog part, digital part, charge pump, digital interfaces. Digital inputs are compatible with 2 different logic levels (5 V or 3.3 V, the possible levels for VCCI), and are converted to the range 0V-VCCD using internal level shifters connected to VCCD and VCCI. In the device a negative charge pump is also present and it is used to generate -5 V voltage level (on CP pin), to bias the substrate and to allow the excursion to the negative range to the output pins of VCCS. Charge pump clock frequency is 2 MHz.

3 different ground pins are also present in the device: GNDA, GNDD, GNDCP, respectively for analog, digital and charge pump circuitry.

Possible ranges for power supplies, currents consumption and input/output logic levels are specified in *Table 9*, *Table 12* and *Table 13*. External component values are specified in *Table 19*.

4.2 Pin protection

On the device a high ESD reference voltage pin (VESD) is available and is used as a protection for the pins externally connected to the sensor and for HD pin; this voltage must be the highest in the application and has to be always connected to the device, through the RC low pass filter shown in *Figure 12* (external component values are specified in *Table 19*). For pins compatible to negative voltages, the negative ESD reference voltage is the substrate (internally connected to CP pin, -5 V). All the other pins have a 5V positive ESD protection voltage level and GND as negative ESD protection voltage level.

4.3 Internal references

Into the device the following voltage references are present:

- a band-gap voltage (typical value 1.215 V) with 3 trimming bits dedicated;
- REF voltage; obtained as the band-gap multiplied by a factor of 1.555; typical value for this voltage is 1.89 V (possible range for this parameter is specified in *Table 10*.
- REF2 voltage; typical value is about VCCA/2 (possible range for this parameter is specified in *Table 11*).

All internal currents are generated from a reference current obtained by the band-gap (buffered on BG pin) applied on an external resistance; the possible BG pin voltage range is specified in *Table 9*, the value of external resistance is defined in *Table 19*.

All timing references are calculated as multiples of the period of the internal oscillator (TOSC); the typical oscillation frequency is 4 MHz, the possible range is specified in *Table 15*. Internal oscillator has 4 trimming bits dedicated.

4.4 Power on reset

A power on reset (POR) circuit is present into the device; this circuit monitors VCCA, VCCCP, VCCD, GNDA, GNDCP, GNDD voltage levels. If one of the supplies falls below (or one of the grounds exceeds) the defined POR threshold (defined in *Table 10*) all the outputs are driven in inactive state, all the registers are set at their default state and the time state machine and all the timers are fixed in the reset state. All these actions are applied after a typical filter time of 15 µs (possible range is defined in *Table 15*). When the supply that has caused POR condition reaches POR value plus hysteresis (or the ground decreases under POR threshold) all the outputs are re-enabled.

During reset condition an internal switch connects the charge pump output voltage (CP pin) to GNDA.

4.5 Pin INRC functionalities: INRC amplifier, clean currents, pull-down current

Pin INRC in the application is connected to the sensor reference cell; the voltage generated by this cell and applied on L9780 INRC pin is a function of the λ parameter of the sensor and gives information about how much the λ parameter is far from the target value. The final purpose is to obtain λ =1, that in terms of electrical parameters means to have 450 mV as output of the reference cell (and applied on INRC pin). In the device this pin is the input of an amplifier (INRC amplifier) with gain selectable via SPI (using bit INRCGAIN). The output of this amplifier is one of the multiplexed inputs of the A/D converter (in order to give the µP the estimation of the λ parameter of the sensor via SPI) and is also internally connected by a switch (INRC switch) to C1A or C1B pin and the external compensation network. The selection of channel A or B is possible using bit COMPSEL. Electrical parameters of INRC amplifier and INRC switches are specified in *Table 10*.

On INRC pin is present a diagnostic circuitry able to detect short to battery/ground conditions and communicate it via SPI (bits STBS2 and STGRC of SPI output register); short to battery detection is always enabled, while the short to ground detection is disabled by default; it can be enabled using bit STGINRC. INRC short to battery/ground thresholds typical values are 3.2 V and 200 mV (possible ranges are defined in *Table 13*). The consequences of the detection of each one of these faults are described in *Section 5.1* and *5.2*.

The INRC pin is connected to the clean current generator: it is a pull-up current source used to clean the air reference of the sensor; the generated current value is selectable via SPI (using bits CCS[3..0]). Possible clean current values are specified in *Table 10*.

On the same pin a 500 µA pull-down current source is also available, used in order to prevent the presence of false short to battery detection due to capacitive commutations. The activation of this current is selectable via SPI (bit INRCPD); pull-down current range is specified in *Table 10*.

A detailed bit description is present in *Section 6.3* and *6.4*.

4.6 Pin RCT1 – RCT2 functionalities: RCT2 amplifier, RCT1 switch, RCT1 band-gap switch

RCT2 pin is the input of an amplifier with typical gain 4.2 (electrical characteristics of RCT2 amplifier are specified in *Table 10*). The output of this amplifier is evaluated during the impedance test and converted in order to communicate its value via SPI to the µP: the value of RCT2 amplifier output, measured in 2 different conditions (with RCT1 switch open and closed), can in fact give a feedback about the impedance of the reference cell, and consequently about the temperature of the sensor.

RCT1 pin is connected through a switch (RCT1 switch) to ground and through another switch (RCT1 band-gap switch) to the band-gap voltage; both these functions are used during the reference cell impedance test, in particular the second one is used to restore the correct charge of the reference cell after the impedance test (charge balance mechanism). RCT1 switches resistance range and RCT1 voltage during charge balance are specified in *Table 10*. For the time diagram of the sequence and the related description see *Section 4.12*. Values of external components connected to pins RCT1 and RCT2 are specified in *Table 19*.

4.7 Pin C1A, C2A, C1B, C2B, C3 functionalities: compensation network connection

These pins are used to connect externally the compensation network to the device; via SPI (using COMPSEL bit) it is possible to select the desired channel (A or B) and connect the external network to the pins C1(A or B), C2(A or B) and C3. The pins of the non selected channel are in high impedance state. C1 is internally connected to the output of INRC amplifier through the INRC switch (driven by the logic during the impedance test, for details see *Section 4.12*), while C2 and C3 are internally connected to the inverting input and the output of an integrator amplifier (C3 is also the VCCS control voltage pin). The non inverting input of the amplifier is connected to REF voltage (typ 1.89 V). The integrator amplifier and the VCCS create a loop (with the external compensation network) of a PI controller. When the loop reaches a stable condition ($\lambda = 1$), on INRC pin there are 450 mV (if 4.2 gain for INRC amplifier is selected), while the inputs of integrator amplifier are both to 1.89 V (450 mV * 4.2). In this condition there is no output current from the VCCS cell (2.5 V on C3 pin).

The values of the external components that must be used in compensation network depend on the sensor that will be driven by the device.

Two examples of possible compensation networks (with defined external components values) are shown below.

Figure 3. Typical sensor D compensation network

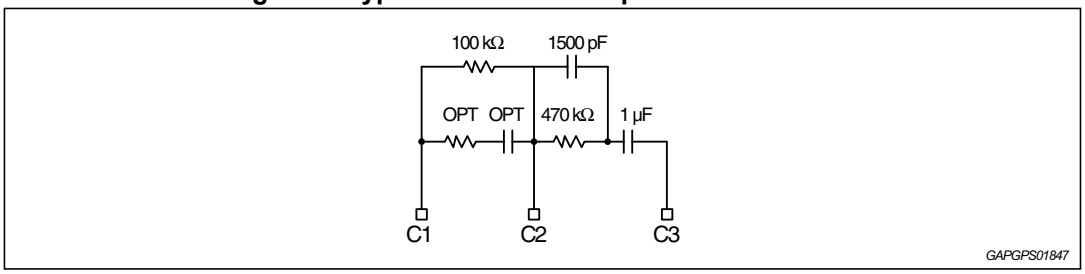


Figure 4. Typical sensor N compensation network

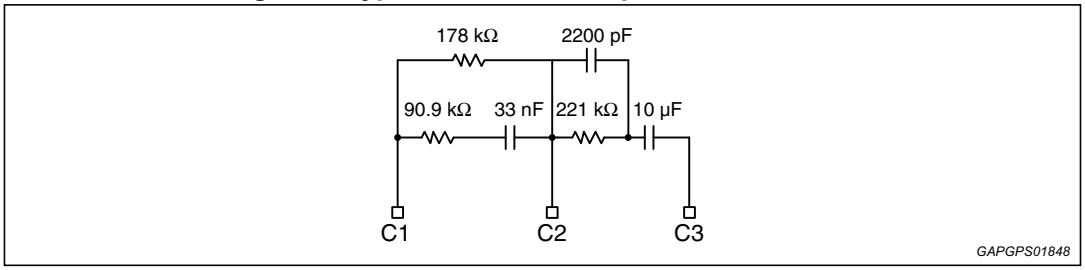
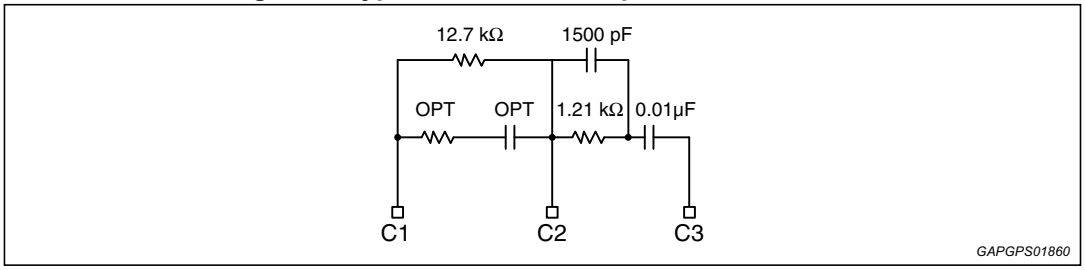


Figure 5. Typical sensor B compensation network



Typical ranges for integrator amplifier electrical parameters are specified in *Table 15*.

4.8 Pin FV, FVOUT functionalities: FVOUT amplifier

C3 pin voltage is the VCCS direct input control voltage. Thanks to the presence of the external capacitor on FV pin (CFV, specified in *Table 19*) and the internal resistance RFV (typical value 5 kΩ and possible range specified in *Table 11*), on FV pin the low pass filtered C3 voltage can be measured. FV voltage is the input of the FVOUT amplifier used to provide on FVOUT pin a signal range compatible with an external A/D converter, as follows:

$$FVOUT = REF2 + G * (FV – REF2)$$

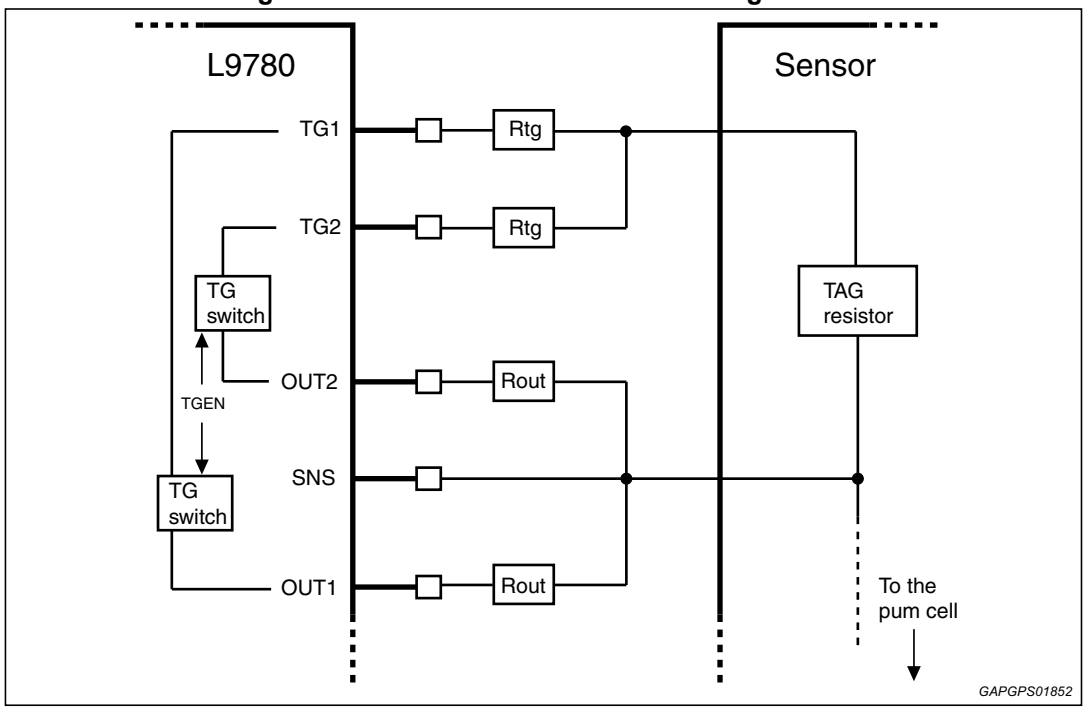
Where G is the gain of VOUT amplifier selectable via SPI (using bits SAMP[2..0]) among the following values: 1 - 1.5 - 2 - 3 - 4 - 6 - 8 – 12. A sample and hold circuitry and the offset compensation technique are used in the architecture of FVOUT amplifier; for this cell all the electrical parameters are specified in *Table 10* and *Table 15*.

4.9 Pin TG1, TG2, OUT1, OUT2, SNS functionalities: the VCCS

TG1, TG2, OUT1, OUT2, SNS are the interface pins between VCCS structure and the external pump cell. The pump cell allows to control the oxygen concentration by forcing an electric current through the cell itself; in other words it is possible to control the direction and the intensity of oxygen transport, because it is directly related to the direction and the intensity of the current. By controlling the amount of current through the pump cell, it is possible to control the amount of oxygen and consequently the λ parameter of the sensor; closing this mechanism into a loop, like in L9780, it is possible to regulate the pump cell current in order to obtain the target λ = 1. The best working condition for the sensor is the high temperature; in this condition the AC impedance of the pump cell can be assumed to be a large capacitance in series to with a resistor of about 20-30 Ω. When cold, the pump cell can be assumed to be an open circuit.

VCCS is a voltage controlled current source and is able to sink or source current from the pump cell, depending on its control voltage, that is the voltage present on C3 pin. Through TG and OUT pins there is the VCCS output current flow, while SNS is a sense pin. VCCS present in L9780 has 2 output channels (1 and 2), selectable via SPI (using bit VCCSOUT); TG and OUT pins of the non selected channel are in high impedance condition. In VCCS architecture there are 2 internal switches (TG switches) able to short OUT and TG pins of the selected channel (see *Figure 6*); the actuation of these switches can be selected via SPI (using bit TGEN).

Figure 6. VCCS external resistance configuration



If the switch is in off condition the TG pin of the selected channel is in high impedance state. If the TG switch is in on state the output current of VCCS structure can flow both through TG and OUT pins and can be described with the following expression:

$$I_{out} = - (C3 – REF2)/R_{tot}$$

where R_{tot} is the external total resistance, that can be obtained as a combination of all the external resistances connected to the VCCS pins. Referring to *Figure 6*, R_{tot} can be calculated as follows:

$$R_{tot} = R_{out} // (R_{tg} + \text{TAG resistor})$$

where R_{tg} and R_{out} are the series resistances of the VCCS pins related to the selected channel.

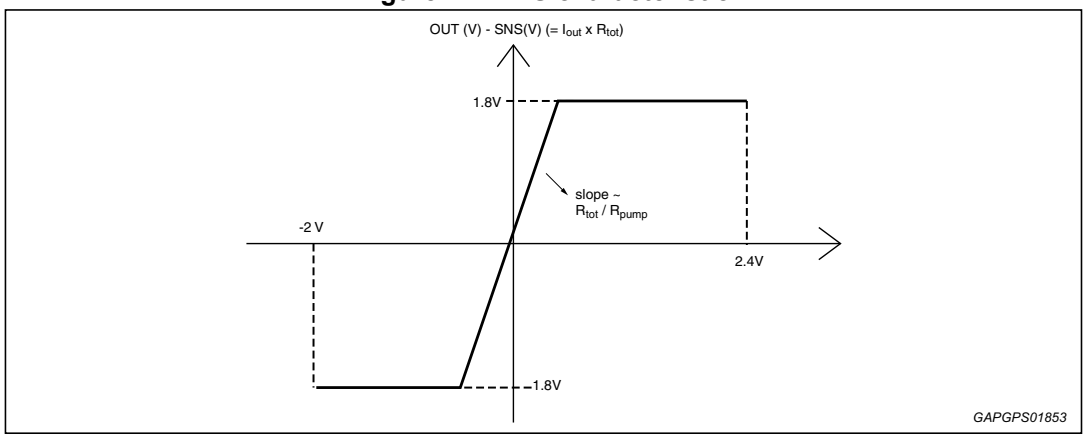
Otherwise, if TG switch is in off state, $R_{tot} = R_{out}$ and consequently the VCCS output current can be described with the following expression:

$$I_{out} = - (C3 – REF2)/R_{out}$$

The VCCS characteristic is shown in *Figure 7*. In this figure the relationship between SNS voltage and the voltage on R_{tot} resistance (that is equal to the difference between OUT voltage and SNS voltage) is defined; these two quantities are in agreement in sign as both

depend on the VCCS output current multiplied by a resistance value (the resistance of the pump cell in SNS voltage case and the R_{tot} resistance in the voltage drop case); from the same figure it is evident that the maximum SNS voltage dynamic range compatible with L9780 VCCS architecture is -2 V < SNS < 2.4 V and the maximum drop allowed on R_{tot} (or Rout if TG switch is off) is 1.8 V.

Figure 7. VCCS characteristic



At the startup of the device, VCCS structure is disabled by default, that means that all its pins are in high impedance condition and the “parking functionality” is active; in other words, the parking amplifier is switched on and a voltage similar to REF2 is present on C3 pin (see block diagram in *Figure 2*). Besides, a pull-down resistor is internally connected by default from OUT1 pin to GNDA; this is done to avoid that a leakage current can increase the voltage value of VCCS pins until the short to battery condition. When VCCS is enabled or a sensor short to battery condition is detected, the pull-down resistor is automatically disconnected from OUT1 pin; when VCCS is disabled and no fault conditions are present, VCCS pull-down resistor can be re enabled via SPI (using bit VCCSPD).

If no sensor short to battery condition is present, VCCS structure can be enabled and the output channel selected with an SPI frame (using bits VCCSEN and VCCSOUT); in this case the “parking functionality” is disabled. When VCCS is enabled, it is also possible to activate/deactivate clamp functionality via SPI (using bit CLAMPEN), in order to protect the sensor; when the clamp functionality is activated, a voltage control is enabled on SNS pin and, if its value is going to exceed the voltage range defined by the user, the clamp circuit intervenes in order to modify the VCCS output current and make SNS pin reenter the clamp limits. The clamp limit range can be symmetric or asymmetric; the desired kind of range can be defined via SPI (bit CLAMPSIM). In case of symmetric range, if VCL is the clamp voltage defined by the user, the consequent range allowed for SNS voltage is:

$$-VCL < SNS < +VCL, \text{ with } 0.75V<VCL<2V$$

In case of asymmetric range, if VCL is the clamp voltage defined by the user, the consequent range for SNS voltage is:

$$-0.8333*VCL < SNS < +VCL, \text{ with } 0.75\ V < VCL < 2.4\ V$$

If the clamp circuit is activated and intervenes while VCCS is working, it is visible also via SPI because CLAMP bit in SO register is kept = 1 until the clamp circuit is acting during VCCS activation. The clamp voltage VCL is defined by the user and is equal to the voltage applied on CL1 or CL2 pin; the input channel chosen to read the clamp voltage can be selected via SPI (bit CLAMPCL); the non selected pin can be left open.

On all VCCS pins a short to battery diagnostic is always active: a short to battery condition is detected if OUT or TG pins exceed VCCA voltage + 30 mV or if SNS pin exceed STBS3 threshold voltage (2.7 V typical value, possible range defined in). The consequences of a short to battery fault detection are specified in *Section 5.1*.

On SNS pin is also present a short to ground diagnostic circuitry, that is able to detect if SNS pin is into the range SNS_NTH < SNS < SNS_PTH (SNS_NTH and SNS_PTH are voltage thresholds specified in *Table 13*, their typical values are -200 mV and 200 mV). The consequences of a sensor short to ground detection are specified in *Section 5.3*.

VCCS is designed to respect specification of minimum bandwidth (100 kHz) for different R_{tot} values and is able to guarantee in all conditions a minimum phase margin of 60°. This is possible thanks to the programmability of the VCCS internal compensation capacitances (C_{int}). In SPI input frame, 6bit for capacitance configuration are present (VCCSCAP[5..0]); these bits allow to drive the connection of internal compensation capacitances, that in this way are selectable by the user. The higher is the value of capacitance selected and the higher is the phase margin of the structure, but the lower is the consequent bandwidth; with some simplifications the bandwidth of VCCS can be described with the following formula:

$$Ft = (Gm\_in * Gm\_outDC * R_{tot})/ (2\pi * C_{int})$$

where Gm_in * Gm_outDC is a constant parameter depending by on the structure used in the design; R_{tot} is the external total resistance and C_{int} the internal selectable capacitance.

In the following table it is shown that a wide range of possible R_{tot} can be driven obtaining the correct compromise between bandwidth and phase margin.

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
1	6	4
2	13	9
3	19	13
4	26	17
5	33	22
6	40	27
7	46	31
8	53	35
9	60	40
10	66	44
11	72	48
12	79	53
13	85	57
14	91	61
15	98	65
16	104	69
17	111	74

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth (continued)

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
18	117	78
19	123	82
20	129	86
21	135	90
22	141	94
23	148	99
24	154	103
25	160	107
26	166	111
27	172	115
28	178	119
29	184	123
30	190	127
31	196	131
32	202	135
33	208	139
34	214	143
35	220	147
36	226	151
37	231	154
38	237	158
39	243	162
40	249	166
41	255	170
42	261	174
43	267	178
44	272	181
45	278	185
46	284	189
47	290	193
48	295	197
49	301	201
50	306	204
51	312	208

Table 6. C_{int} vs. possible R_{tot} to guarantee phase margin and bandwidth (continued)

C_{int} (pF)	Maximum R_{tot} [Ω] value to guarantee a phase margin > 60°	Minimum R_{tot} [Ω] value to guarantee a bandwidth > 100 kHz
52	318	212
53	324	216
54	329	219
55	335	223
56	341	227
57	347	231
58	352	235
59	357	238
60	363	242
61	369	246
62	374	249
63	380	253
64	386	257

In the table above the list of selectable C_{int} is shown and for each C_{int} is specified maximum and minimum R_{tot} value that guarantee respectively a phase margin > 60° and a bandwidth > 100 kHz.

In order to avoid that during the activation of VCCS for a short time the output current can be out of control, the selection or the change of different functionalities of VCCS (like the change of output channel, of input clamp or of C_{int} capacitances) are possible only when VCCS is disabled. Well defined rules have to be respected in order to be able to drive correctly VCCS; these rules are specified in *Section 5.5.2*.

All VCCS electrical parameters ranges are specified in sections *Table 12* and *Table 15*. All the logic signals used to select VCCS functionalities are defined in detail in section 7.3.

4.10 Pin PG1, PG2, SR functionalities

The device is able to drive via SPI (through bits PG1EN, PG2EN) the gate of the external protection FET, that can be connected to PG1 or PG2 pin. This external FET acts as a switch that connects to ground the second terminal of the pump cell and completes the path for VCCS output current (see block diagram in *Figure 2*). In this condition SR pin voltage is expected to be low; if the voltage value exceeds STBS1 threshold (typical value of 200mV and possible range specified in *Table 13*), a sensor short to battery condition is detected. For the consequences of this detection see *Section 5.1*.

In order to avoid the possibility that the external FET switch on when the device is un-powered the FET driver has 100 kΩ (typ) pull down resistor permanently connected to PG1 and PG2 pins. Electrical parameters of PG driver are specified in *Table 12* and *Table 15*.

4.11 Analog to digital conversion

In the device a 10bit A/D converter is present. The analog voltages to be converted are multiplexed by the logic while the state machine is running and are: the output of RCT2 amplifier, the output of INRC amplifier and FV pin voltage (see block diagram in *Figure 2*). Between the analog inputs and the A/D converter a scaling amplifier is present; this cell is able to amplify the input signal according to the gain selected via SPI (using bit SAMP[2..0]) with the following relation:

$$OUTsa = REF2 + G * (Input\_voltage – REF2)$$

where G is the gain selectable via SPI among the following values: 1 - 1.5 - 2 - 3 - 4 - 6 - 8 – 12, and OUTsa is the output of the scaling amplifier (and the input of A/D converter). When the selected input of the scaling amplifier is the output of the INRC or RCT2 amplifier, G is fixed (=1), while when the input is FV voltage the gain G can be modified by the user. The multiplexing sequence at the input of the scaling amplifier when the state machine is running is shown in *Figure 8*.

The absolute conversion accuracy compared to an ideal transfer curve is ±2 counts. All the electrical parameters regarding the scaling amplifier and the A/D conversion are specified in *Table 11*.

The nominal conversion of the scaling amplifier output is defined in the following formula:

$$count\_SA = floor\left(\frac{OUTsa}{VCCA} \cdot 1024\right)$$

where:

count_SA is the result of the A/D conversion;

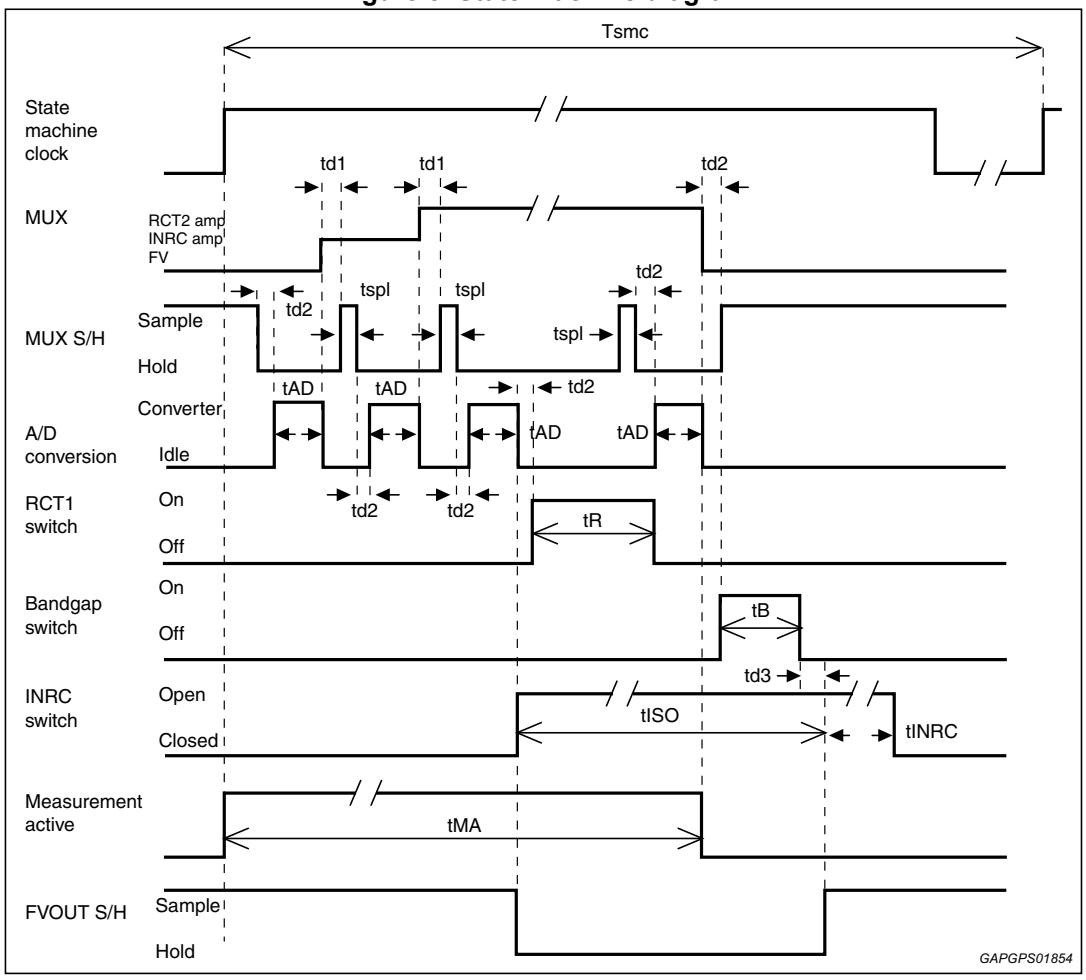
OUTsa is the output voltage of the scaling amplifier;

floor: a function that returns the greatest integer less than or equal to the argument.

4.12 Timing state machine

The internal temporization of A/D conversion and of the impedance test are defined by an internal state machine that acts as shown in *Figure 8*.

Figure 8. State machine diagram



The A/D conversion results give an indication about the λ parameter of the sensor (that is in relation with INRC pin voltage), about the VCCS output current (from FV voltage evaluation) and about the sensor temperature (from the double conversion of the output of RCT2 amplifier the external µP is able to evaluate the impedance of the reference cell and consequently the temperature).

All times are defined in *Table 16*; some of them (the state machine clock period (T_{smc}), the duration of RCT1 switch and band-gap switch pulses (t_R and t_B) and the second portion of INRC switch pulse (t_{INRC})) can be defined by SPI (using bits MCP[1..0], ITPT[6..0], CBT[6..0], ISPT[2..0]), while the first portion of INRC switch pulse is determined by the summation of different events. The SPI selectable variables can not change during the measurement; if any change occurs while a measurement is on going, the new values will be applied in the next measurement cycle.

In SO output frame, 3 bits are dedicated to the measurement cycle counter (COUNT[2..0]); the value measured by the counter is cleared after every power on reset, is automatically incremented by one at every falling edge of measurement clock and latched in SO output

register. When the counter reaches its maximum value, the count restarts from zero. The measurement is able to operate in free running or synchronized mode, according to SPI selection (bit SNC); if free running mode is selected, the timing state machine is continuously running, otherwise if synchronized mode is selected the measurement cycle starts for each rising edge on SY pin; if multiple rising edges are detected on SY pin during one measurement cycle, they will be ignored. For a more detailed description of the bits involved see *Section 6.3*.

When the INRC amplifier is selected by the MUX, the scaling amplifier gain is automatically set to 1, and the nominal transfer function from INRC pin to A/D output is:

$$count\_INRC = floor\left(Ginrc \cdot \frac{INRC}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$INRC = \frac{count\_INRC}{1024} \cdot \frac{1}{Ginrc} \cdot VCCA$$

where:

Ginrc is the gain of the INRC amplifier;

count_INRC is the result of the A/D conversion of INRC pin voltage;

INRC is the INRC pin voltage level.

INRC voltage resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±0.5%);

scaling amplifier offset (±300 µV);

INRC amplifier gain accuracy (±1%);

INRC amplifier output offset (±21 mV);

VCCA voltage precision.

When the RCT2 amplifier is selected by the MUX, the scaling amplifier gain is automatically set to 1, and the nominal transfer function from RCT2 pin to A/D output is:

$$count\_RCT2 = floor\left(Grtc2 \cdot \frac{RCT2}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$RCT2 = \frac{count\_RCT2}{1024} \cdot \frac{1}{Grtc2} \cdot VCCA$$

where:

Grct2 is the gain of the RCT2 amplifier;

count_RCT2 is the result of the A/D conversion of RCT2 pin voltage;

RCT2 is the RCT2 pin voltage level.

RCT2 voltage resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±.5%);

scaling amplifier offset (±300 µV);

RCT2 amplifier gain accuracy (±1%);

RCT2 amplifier output offset (±21 mV);

VCCA voltage precision.

When the VCCS filtered control voltage FV is selected by the MUX, the nominal transfer function from VCCS current (I_VCCS) to A/D output is:

$$count\_VCCS = floor\left(512 + \frac{Gsa \cdot (-I\_VCCS) \cdot Rtot}{VCCA} \cdot 1024\right)$$

and the nominal transfer function is:

$$I\_VCCS = -\left(\frac{count\_VCCS}{1024} - \frac{1}{2}\right) \cdot \frac{1}{Gsa \cdot Rtot} \cdot VCCA$$

where:

Gsa is the scaling amplifier gain;

I_VCCS is the VCCS output current;

count_VCCS is the result of the A/D conversion of FV pin voltage;

Rtot is the VCCS external resistance as defined in *Section 4.9*.

I_VCCS current resolution depends on different contributions:

A/D error conversion (±2 counts);

scaling amplifier gain accuracy (±0.5% if Gsa=1, ±1% if Gsa = 1.5-2-3-4, ±2% if Gsa=6-8-12);

scaling amplifier offset (±300 µV);

VCCS gain accuracy (±1.2%);

VCCS offset (±700 µV);

VCCA voltage precision;

Rtot precision.

4.13 Pin HD, HG functionalities: heater FET driver and diagnostic

As shown in the block diagram of *Figure 2*, HG pin is externally connected to the gate of the external heater FET (an NMOS in low-side configuration, with the drain directly connected to the heater element), while HD is connected to the drain through the external resistance RHD (possible range for this resistor is specified in *Table 19*).

The heater is necessary in order to make the sensor work at a correct temperature. The sensor can only operate in high temperature conditions, but as it is not able to reach the desired range of temperature passively, an active heater is usually incorporated into the sensor structure. This heater is normally composed by an ohmic resistor through which the heater FET current is forced. The µP is able to obtain information regarding the sensor temperature from the results of the impedance test performed into the device and communicated to the µP via SPI (the higher is the sensor temperature, the lower is its impedance); consequently, the µP can intervene on sensor temperature acting on PW pin. PW is a digital input pin of the device and can be driven with a PWM signal by the µP. PW pin signal is then internally inverted by the logic and the consequent signal is then applied on HG pin, conditioning the activation/deactivation of the external heater FET (and so the power consumption necessary to heat the sensor).

Capacitive coupling due to heater commutations can cause undesired signals on the reference cell; in order to avoid it, the logic freezes the current state of HG signal during the measurement cycle. HG status will be driven again by PW signal once the measurement cycle is completed.

In order to avoid that the external FET switches on when VIGN voltage is present but the device is un-powered, a 100 kΩ pull-down resistor is permanently connected to HG pin.

A diagnostic circuitry is also present into the heater driver, in order to detect open circuit, short to ground or short to battery fault conditions; the logic into the device can communicate via SPI to the µP the fault detection through OCH, STGH, STBH bit status. The actions related to the diagnostic fault detection are described in *Section 5.4*, while all the heater diagnostic thresholds are specified in *Table 13*. More details about the heater diagnostic bits can be found in *Section 6.4*.

The ranges of the electrical parameters of the heater FET driver are specified in *Table 12* and *Table 15*.

5 Diagnostic

5.1 Sensor short to battery

L9780 is able to detect and take actions when a short to battery condition happens on its sensor pins. In particular voltage levels on pins INRC, SNS, SR, OUT1/2 and TG1/2 are controlled. If INRC, SNS or SR pin exceeds the corresponding voltage threshold reported in *Table 13* (or one of TG/OUT pins exceeds VCCA + 30 mV), a possible sensor short to battery condition is detected. Sensor short to battery diagnostic on SR pin is not active when both PG1 and PG2 are OFF.

Possible sensor short to battery condition is confirmed by the logic (and reported in the SPI output register) and the failure countermeasures are applied in the device only if the duration of the fault is greater than a filter time defined as a multiple of the clock period (possible filter times ranges are defined in *Table 17*); in other words, when the possible sensor short to battery condition is detected, a logic counter starts and when the count reaches the value defined in *Table 17* the fault condition is considered validated. This counter is reset when the possible short to battery fault is cleared and after every power on reset.

As soon as a possible sensor short to battery condition is detected the VCCS pull-down resistor is disabled immediately, without waiting any filter time; the pull-down will be re enabled once the short to battery condition is removed and the SPI bits are cleared by the user.

Actions

Once the sensor short to battery fault is validated (the duration of possible fault is greater than the filter time) the following actions are taken:

1. Latch off PG1 and PG2;
2. Disable VCCS output current (all VCCS pins are in high impedance condition), impedance test and charge balance switches;
3. Set the STBS1/ STBS2/ STBS3 bit in the SPI output register, according to the pin where the fault has been detected (STBS3 in case of TG/OUT pins).

These actions remain valid until cleared by the user.

During short to battery condition, all pins compatible with this fault have to respect the leakage current consumption specified in *Table 14*.

When the short to battery condition is cleared, VCCS, impedance test and charge balance switches may be re enabled asynchronously from VCCS clock if their enable bits are =1. In order to avoid this situation these functions should be disabled via SPI when a short to battery fault is reported. When the fault is de asserted, these functions can be re enabled via SPI.

For more details about SPI bits see *Section 6.4*.

5.2 INRC pin short to ground

The device is able to detect and take actions when a short to ground condition happens on INRC pin. This detection is active only if STGINRC bit in SPI input register is set =1 and only if the impedance test switch is disabled.

If INRC pin is below the corresponding voltage threshold reported in *Table 13*, a possible short to ground condition is detected. Possible short to ground condition is confirmed by the logic (and reported in the SPI output register) only if the duration of the fault is greater than a filter time, defined as a multiple of the clock period; in other words, when the possible sensor short to ground condition is detected, a logic counter starts and when the count reaches the value defined in*Table 17*, the fault condition is considered validated. This counter is reset when the possible short to ground fault is cleared and after every power on reset.

Actions

Once the INRC short to ground fault is validated (the duration of possible fault is greater than the filter time) the following action is taken:

1. Set the STGRC bit in the SPI output register.

This action remains valid until cleared by the user.

5.3 SNS pin short to ground

The device is able to detect and take actions when a short to ground condition happens on SNS pin.

If SNS pin is in the range SNS_NTH < SNS < SNS_PTH (SNS_NTH, SNS_PTH thresholds values reported in *Table 13*), a possible short to ground condition is detected. Possible short to ground condition is confirmed by the logic (and reported in the SPI output register) only if the duration of the fault is greater than a filter time, defined as a multiple of the clock period; in other words, when the possible sensor short to ground condition is detected a logic counter starts and when the count reaches the value defined in *Table 17*, the fault condition is considered validated. This counter is reset when the possible short to ground fault is cleared and after every power on reset.

Actions

Once the SNS short to ground fault is validated (the duration of possible fault is greater than the filter time) the following action is taken:

1. Set the STGSNS bit in the SPI output register.

This action remains valid until cleared by the user.

Application note

When the regulation loop is approaching the condition λ =1, that in terms of electrical parameters means to have 450 mV as output of the reference cell (applied on INRC pin), the output current of the VCCS is very small so the voltage of SNS is near to GND. This does not flag a fault condition but the STGSNS bit in the SPI output register is expected to be set.

5.4 Heater diagnostic

The device is able to detect and take actions when a fault condition happens on external heater FET, connected to the device through HG and HD pins. Detected fault conditions are: heater short to battery, heater short to ground, heater open circuit.

From a design point of view, to HD pin are connected an 80 µA sink current generator (normally on, except for particular diagnostic conditions) and a 190 µA source current generator (normally off, except for particular diagnostic conditions); possible ranges for generated currents are specified in *Table 13*.

5.4.1 Heater short to battery

When the external heater is in “on” condition, the heater drain is expected to be low (the external heater is considered “on” when the HG voltage value is higher than a specific threshold, defined in *Table 13*, typical value 4V). If the heater drain voltage value is higher than the heater short to battery threshold (selectable via SPI using bit STBHTH, as defined in *Table 13*), a possible heater short to battery condition is detected. Possible heater short to battery condition is confirmed by the logic (and reported in the SPI output register) only if the duration of the fault is greater than a filter time, defined as a multiple of the clock period; in other words, when the possible heater short to battery condition is detected, a logic counter starts and when the count reaches the value defined in *Table 17* (and selectable via SPI using bit STBHFT[1..0]) the fault condition is considered validated. This counter is reset when the possible short to battery fault is cleared and after every power on reset.

Actions

Once the heater short to battery fault is validated (the duration of possible fault is greater than the filter time) the following actions are taken:

1. Latch HG off;
2. Set STBH bit in SPI output register.

These actions remain valid until cleared by the user.

5.4.2 Heater short to ground

When the external heater is in “off” condition, the heater drain is expected to be high. If the heater drain voltage value is lower than the heater short to ground threshold HSG (3.69 V typical value, possible range specified in *Table 13*), a possible heater short to ground condition is detected. Possible heater short to ground condition is confirmed only if the duration of the fault is greater than a filter time, defined as a multiple of the clock period; in other words, when the possible heater short to ground condition is detected a logic counter starts and when the count reaches the value defined in *Table 17* the fault condition is considered validated. This counter is reset when the possible short to ground fault is cleared and after every power on reset.

Actions

Once the heater short to ground fault is validated (the duration of possible fault is greater than the filter time) the following actions are taken:

1. Set the STGH bit in SPI output register;
2. Latch HG off;
3. Invoke a test of heater open circuit.

These actions remain valid until cleared by the user or modified after the open circuit test.

5.4.3 Heater open circuit

The device is able to distinguish between heater FET short to ground and open circuit conditions. Once the heater open circuit test is invoked, the following actions are taken:

1. Turn off HD sink current generator;
2. Turn on HD source current generator;
3. If HD voltage value > open circuit threshold (specified in *Table 13*) a possible heater open circuit is detected and immediately validated.

Actions

Once the heater open circuit fault is validated the following actions are taken:

1. Set the OCH bit in SPI output register;
2. Clear the STGH bit in SPI output register.

These actions remain valid until cleared by the user.

5.5 SPI diagnostic

Once a fault condition is reported in the SPI output register but the fault condition is removed from the device, the user is able to clear the register and restore the normal operative condition. This is possible using the CLEARFLT bit in the SPI input register. The effect of this bit is to clear all the latched fault conditions and re enable every previously disabled output; on HD pin sink and source currents are restored to their default condition. The bit is then internally cleared when the clear operation is completed.

5.5.1 SPI data fault

The device continuously monitors the data input on SPI register. Bits 14 and 15 (CB0, CB1) are the data confirmation bits and if one of their values is different from the expected (CB0=0, CB1=1) an SPI data fault is detected and immediately validated.

Actions

Once an SPI data fault is validated the following actions are taken:

1. Ignore the corrupted message;
2. Assert SPIF1 and de assert SPIF2 bits in the output register; these bits are latched until cleared by CLEARFLT;
3. Set REG bit to ‘0’.

5.5.2 SPI length fault

Receiving an SPI frame with a length different from [64 + (n*8)] bits is considered an SPI length fault, immediately detected and validated.

Actions

Once an SPI length fault is validated the following actions are taken:

1. Ignore the corrupted message;
2. Assert SPIF1 and de assert SPIF2 bits in the output register; these bits are latched until cleared by CLEARFLT;
3. Set REG bit to ‘0’.

5.5.3 SPI not valid command fault

Any of the following conditions is considered an SPI not valid command fault:

1. SPI frame with INRCPD = VCCSEN = 1;
2. SPI frame with VCCSPD = VCCSEN = 1;
3. When VCCS is enabled, the SPI frame modifies VCCSOUT, COMPSEL or VCCSCAP[5..0] bit status;
4. When VCCS and clamp are enabled, the SPI frame modifies CLAMPCL or CLAMPSIM bit status.

The fault is validated immediately.

Actions

Once an SPI not valid command fault is validated the following actions are taken:

1. Ignore the corrupted message;
2. Assert and latch SPIF1 and de assert SPIF2 bits in the output register; these bits are latched until cleared by CLEARFLT;
3. Set REG bit to ‘0’.

5.6 Loss of ground

L9780 has no loss of ground detection. If one of the grounds exceeds the power on reset voltage threshold, the device enters the reset condition. For detailed description see *Section 4.4*.

6 Digital interface description

L9780 contains a serial peripheral interface (SPI) composed by the serial clock (CLK), serial data out (SO), serial data in (SI), chip select (CSN) and is configured as an SPI slave. If CSN is asserted and the SPI master continues to issue CLK pulses after the SPI shift register is filled, the device shall shift the master's SI data out on SO output.

SPI can support a daisy chain configuration, so the external processor can send SPI commands to multiple devices without using additional chip select pins, as shown in *Figure 9* and *10*.

Figure 9. Daisy chain configuration

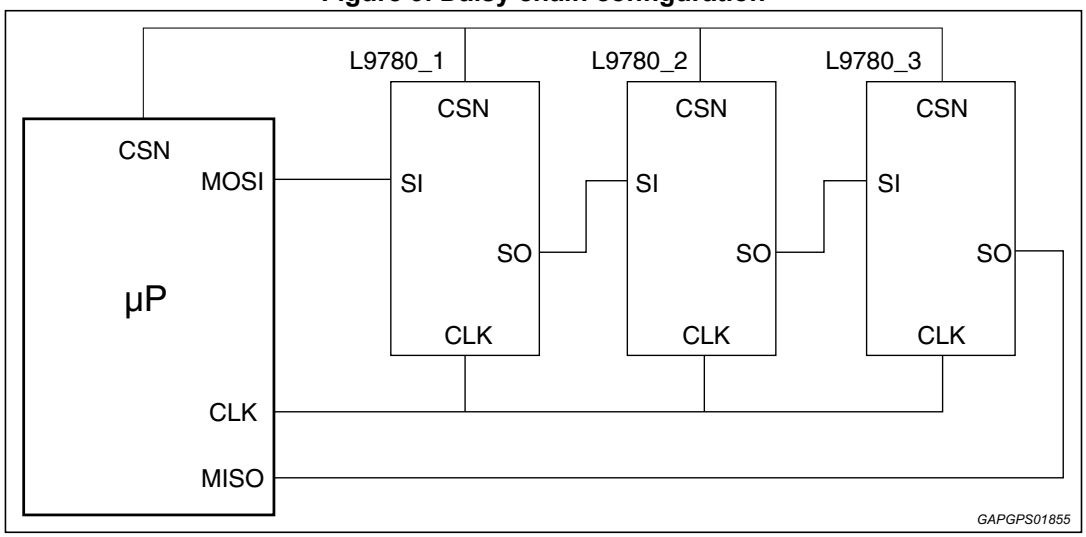
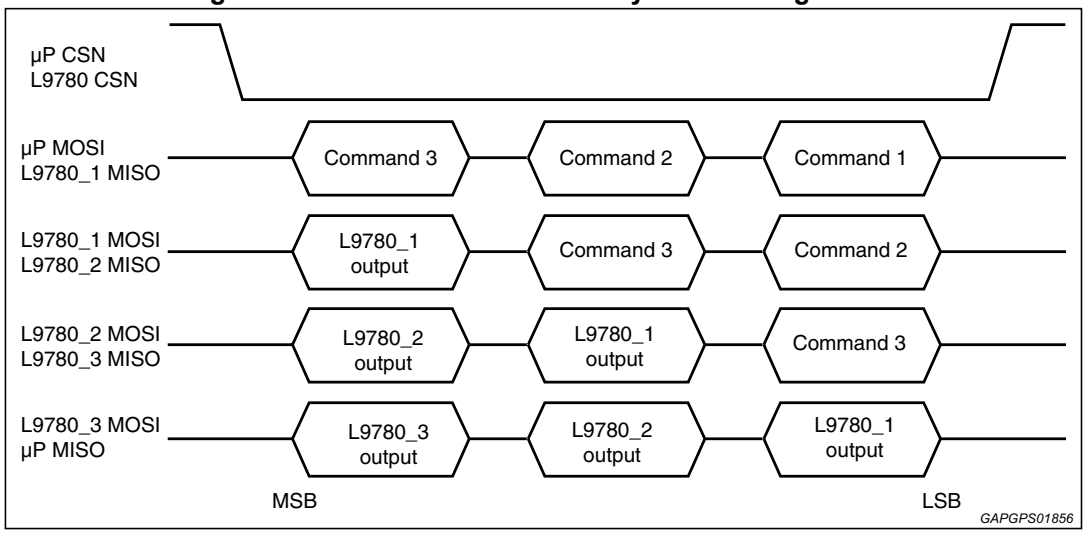


Figure 10. SPI transmission in Daisy chain configuration



The first 64 bit data coming out of SO are the output register bits; the subsequent bits are the SPI commands received through SI pin.

6.1 CSN

CSN pin is used to select the device for serial transfer. If CSN is asserted, SO pin exits its tri state condition and all status information is latched into SPI shift register; register data are shifted into SI pin and out from SO pin on each subsequent CLK. If CSN is negated, SO pin is in tri state condition and the fault register is reloaded (latched) with current filtered status bits. CSN is immune to spurious pulses of 50 ns or shorter (SO pin can exit tri state condition but no fault clear is applied and no status bit changes). An internal 30 µA pull-up current is present on CSN pin in order to force the negated condition if a pin open circuit is present.

6.2 CLK

CLK pin provides to the device the clock signal necessary for serial data transfer. When CSN is asserted the device latches input data and shall shift output data on CLK rising edge.

6.3 SI

SI pin is able to receive data from the master microprocessor while CSN is asserted. The MSB is the first bit and LSB is the last bit of the word received on SI. The input word consists of 64 bit; follows the description of the SPI input register.

6.3.1 SPI input register

63(MSB)	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
X	X	X	X	REG	INRCPD	STGINRC	INRCGAIN	TGEN	VCCSEN	VCCSOUT	VCCSPD	COMPSEL	CLAMPEN	CLAMPCL	CLAMPSIM	CLEARFLT	CCS3	CCS2	CCS1	CCS0	SAMP2	SAMP1	SAMP0	VCCSCAP5	VCCSCAP4	VCCSCAP3	VCCSCAP2	VCCSCAP1	VCCSCAP0	MCP1	MCP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0(LSB)
STBHITH	ITPT6	ITPT5	ITPT4	ITPT3	ITPT2	ITPT1	ITPT0	SNC	CBT6	CBT5	CBT4	CBT3	CBT2	CBT1	CBT0	CB1	CB0	X	STBHFT1	STBHFT0	ISPT2	ISPT1	ISPT0	PG2EN	PG1EN	X	X	X	X	X	X

Bit 63 – 60:

These bits are not used and their status is ignored.

Bit 59: REG

The meaning of this bit is to select a specific content for SO register. If REG='0', SO contains the status register, if REG='1' SO contains the input register. The device sends the requested information in the next SPI frame.

Default state for this bit after power on reset: 0.

Bit 58: INRCPD

This bit enables (INRCPD='1') or disables (INRCPD='0') INRC pull-down current.

If the device receives an SPI command in order to modify the status of this bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. The information reported in the output register is the configuration used in the last measurement cycle.

If the device receives an SPI command in order to modify INRCPD and VCCSEN bits at the same time, it will perform these two actions in sequence, with a delay between the two events. In particular if in the input frame INRCPD='0' and VCCSEN ='1', the device disables INRC pull-down before enabling VCCS, viceversa if in the input frame INRCPD='1' and VCCSEN ='0', the device disables VCCS before enabling INRC pull-down current.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0.

Bit 57: STGINRC

This bit enables (STGINRC='1') or disables (STGINRC='0') short to ground diagnostic on INRC pin.

Default state for this bit after power on reset: 0.

Bit 56: INRCGAIN

This bit selects the gain of INRC amplifier as follows:

INRCGAIN ='0' => selected 4.2 gain;

INRCGAIN ='1' => selected 2.1 gain.

Possible ranges for these gains are specified in section 8.1.2.1.

If the device receives an SPI command in order to modify the gain of INRC amplifier in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. The value of the gain reported in the output register is the gain used in the last measurement cycle.

Default state for this bit after power on reset: 0.

Bit 55: TGEN

This bit enables (TGEN='1') or disables (TGEN='0') VCCS TG switches between TG and OUT pins.

If the device receives an SPI command in order to modify TGEN bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. TGEN bit value reported in the output register is the value used in the last measurement cycle.

Default state for this bit after power on reset: 0.

Bit 54: VCCSEN

This bit enables (VCCSEN='1') or disables (VCCSEN='0') VCCS cell. When VCCSEN='0', VCCS is disabled and the "parking functionality" is active, that means that on C3 pin a voltage similar to REF2 is present (the range of this voltage is specified in *Table 11*).

If the device receives an SPI command in order to modify VCCSEN bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. VCCSEN bit value reported in the output register is the value used in the last measurement cycle.

Refer to INRCPD bit description to define VCCS and INRC pull-down current switch on sequence.

Refer to VCCSPD bit description to define VCCS and VCCS pull-down resistor switch on sequence.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0.

Bit 53: VCCSOUT

This bit selects VCCS output channel (and corresponding TG pin) as follows:

VCCSOUT='0' => selected channel 1;

VCCSOUT='1' => selected channel 2.

If the device receives an SPI command in order to modify VCCSOUT bit in the middle of a measurement cycle while VCCS is disabled, it stores the new information and applies it at the beginning of the new measurement cycle. VCCSOUT bit value reported in the output register is the value used in the last measurement cycle.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0.

Bit 52: VCCSPD

This bit enables (VCCSPD='1') or disables (VCCSPD='0') VCCS pull-down resistor on OUT1 pin.

If the device receives an SPI command in order to modify VCCSPD bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. VCCSPD bit value reported in the output register is the value used in the last measurement cycle.

If the device receives an SPI command in order to modify VCCSPD and VCCSEN bits at the same time, it will perform these two actions in sequence, with a delay between the two events. In particular if in the input frame VCCSPD='0' and VCCSEN ='1', the device disables VCCS pull-down before enabling VCCS, viceversa if in the input frame VCCSPD='1' and VCCSEN ='0', the device disables VCCS before enabling VCCS pull-down resistor.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 1.

Bit 51: COMPSEL

This bit selects the output compensation network as follows:

COMPSEL='0' => selected channel A;

COMPSEL='1' => selected channel B.

If the device receives an SPI command in order to modify COMPSEL bit in the middle of a measurement cycle while VCCS is disabled, it stores the new information and applies it at

the beginning of the new measurement cycle. COMPSEL bit value reported in the output register is the value used in the last measurement cycle.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0.

Bit 50: CLAMPEN

This bit enables (CLAMPEN='1') or disables (CLAMPEN='0') VCCS voltage clamp.

If the device receives an SPI command in order to modify CLAMPEN bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. CLAMPEN bit value reported in the output register is the value used in the last measurement cycle.

Default state for this bit after power on reset: 0.

Bit 49: CLAMPCL

This bit selects the clamp voltage input pin as follows:

CLAMPCL='0' => selected pin CL1;

CLAMPCL='1' => selected pin CL2.

If the device receives an SPI command in order to modify CLAMPCL bit in the middle of a measurement cycle while VCCS is disabled, it stores the new information and applies it at the beginning of the new measurement cycle. CLAMPCL bit value reported in the output register is the value used in the last measurement cycle.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0

Bit 48: CLAMPSIM

This bit selects symmetric or asymmetric voltage clamp limit range as follows:

CLAMPSIM='0' => symmetric clamp limit range;

CLAMPSIM='1' => asymmetric clamp limit range.

For the meaning of symmetric/asymmetric range refer to VCCS analog description in section 5.9.

If the device receives an SPI command in order to modify CLAMPSIM bit in the middle of a measurement cycle while VCCS is disabled, it stores the new information and applies it at the beginning of the new measurement cycle. CLAMPSIM bit value reported in the output register is the value used in the last measurement cycle.

For correct use of this bit, refer also to *Section 5.5.3*.

Default state for this bit after power on reset: 0

Bit 47: CLEARFLT

This bit is used to clear latched faults when the origin of the fault is removed, as follows:

CLEARFLT='0' => no action;

CLEARFLT='1' => clears faults after CSN bit returns to '1'.

Default state for this bit after power on reset: 0.

Bit 46 - 43: CCS[3..0]

These bits are used to select the clean current source on INRC pin, as specified in *Table 10*.

If the device receives an SPI command in order to modify CCS[3..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. CCS[3..0] bits reported in the output register are the values used in the last measurement cycle.

Default state for these bits after power on reset: 0000.

Bit 42 - 40: SAMP[2..0]

These bits are used to select the gain of the scaling and FVOUT amplifiers, as specified in *Table 11*.

If the device receives an SPI command in order to modify SAMP[2..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. SAMP[2..0] bits reported in the output register are the values used in the last measurement cycle.

Default state for these bits after power on reset: 000.

Bit 39 - 34: VCCSCAP[5..0]

These bits are used to set the compensation capacitance C_{int} into VCCS cell. 1pF is permanently connected as compensation capacitance; to this value the decimal conversion of VCCSCAP[5..0] sequence has to be added in order to obtain the total capacitance used as compensation, as follows:

VCCSCAP[5..0] = 000000 => 1 pF

VCCSCAP[5..0] = 111111 => 64 pF

The device is able to change compensation capacitance only when the VCCS is disabled.

The correct selection of C_{int} depends on the kind of the external resistive network that the VCCS has to drive; some rules for a correct selection of C_{int} capacitance are described in *Section 4.9*.

For correct use of these bits, refer also to *Section 5.5.3*.

Default state for these bits after power on reset: 111111.

Bit 33 - 32: MCP[1..0]

These bits are used to set the measurement clock period (Tsmc), as specified in *Table 16*.

If the device receives an SPI command in order to modify MCP[1..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. MCP[1..0] bits reported in the output register are the values used in the last measurement cycle.

When the device is configured in synchronous mode, MCP bit configuration is ignored and the status bits reported in SPI output register is 00.

For the description of the timing sequence refer to *Section 4.12*.

Default state for these bits after power on reset: 00.

Bit 31: STBHTH

This bit selects the heater short to battery threshold as follows:

STBHTH='0' => 250 mV;

STBHTH='1' => 425 mV;

The possible ranges of these thresholds are specified in *Table 13*.

If the device receives an SPI command in order to modify STBHTH bit in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. STBHTH bit value reported in the output register is the value used in the last measurement cycle.

Default state for this bit after power on reset: 0.

Bit 30 - 24: ITPT[6..0]

These bits are used to set the RCT1 switch time pulse duration (t_R), as specified in section *Table 16*.

If the device receives a configuration ITPT[6..0]='0011000' or less (except 0000000), the device considers this configuration as '0011001', and shall provide SO response with the configuration received from SI, even if is '0011000' or less.

If the device receives an SPI command in order to modify ITPT[6..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. ITPT[6..0] bits reported in the output register are the values used in the last measurement cycle.

For the description of the timing sequence refer to *Section 4.12*.

Default state for these bits after power on reset: 0000000 (corresponding to disable state).

Bit 23: SNC

This bit selects the synchronized mode for the device (when SNC='1') or the free running mode (when SNC='0').

If the device receives an SPI command in order to set SNC='1' bit in the middle of a measurement cycle, it terminates the measurement cycle and discards all the temporary conversions; then operates in idle configuration until a rising edge on SY pin is detected; this is the signal necessary to start a new measurement cycle and to clear the measurement counter.

Default state for this bit after power on reset: 0.

Bit 22 - 16: CBT[6..0]

These bits are used to set the RCT1 band-gap switch time pulse duration (t_B), as specified in *Table 16*.

If the device receives an SPI command in order to modify CBT[6..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. CBT[6..0] bits reported in the output register are the values used in the last measurement cycle.

For the description of the timing sequence refer to *Section 4.12*.

Default state for these bits after power on reset: 0000000.

Bit 15 - 14: CB[1..0]

These are confirmation bits.

CB1 => expected always = ‘1’; if it is not verified, a problem (short to ground or open) in SPI interface is present;

CB0 => expected always = ‘0’; if it is not verified, a problem (short to supply) in SPI interface is present.

Bit 13:

This bit is not used and its status is ignored.

Bit 12 - 11: STBHFT[1..0]

These bits are used to define the heater short to battery fault time duration, as specified in *Table 17*.

Default state for these bits after power on reset: 00.

Bit 10 - 8: ISPT[2..0]

These bits are used to define the INRC switch time pulse duration (t_{INRC}), as specified in *Table 16*.

If the device receives an SPI command in order to modify ISPT[2..0] bits in the middle of a measurement cycle, it stores the new information and applies it at the beginning of the new measurement cycle. ISPT[2..0] bits reported in the output register are the values used in the last measurement cycle.

For the description of the timing sequence refer to *Section 4.12*.

Default state for these bits after power on reset: 000.

Bit 7: PG2EN

This bit enables (PG2EN=’1’) or disables (PG2EN=’0’) protection FET on channel 2. If a sensor short to battery condition is detected, the PG driver remains off even if a frame with PG2EN=’1’ is sent; if

detailed description of the diagnostic fault detection refer to *Section 5.1*.

Default state for this bit after power on reset: 0.

Bit 6: PG1EN

This bit enables (PG1EN=’1’) or disables (PG1EN=’0’) protection FET on channel 1. If a sensor short to battery condition is detected, the PG driver remains off even if a frame with PG1EN=’1’ is sent; if the driver is in on state and a sensor short to battery condition is detected, it will be switched off. For a detailed description of the diagnostic fault detection refer to *Section 5.1*.

Default state for this bit after power on reset: 0.

Bit 5 – 0:

These bits are not used and their status is ignored.

6.4 SO

SO pin is in tri state condition when CSN is negated. When CSN is asserted the MSB is the first bit and LSB is the last bit of the word transmitted on SO.

SPI output register can be configured to report the configuration status of the device (with conversion and fault detection results) or can be configured to report an echo of the previous SPI input sequence. The first solution can be selected setting REG bit to ‘0’; the second solution can be selected setting REG bit to ‘1’. The output word consists of 64 bit. Here following the description of the SPI output register in both configurations.

6.4.1 SPI output register (status configuration)

63(MSB)	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
X	VER2	VER1	VER0	REG	X	RCAMP9	RCAMP8	RCAMP7	RCAMP6	RCAMP5	RCAMP4	RCAMP3	RCAMP2	RCAMP1	RCAMP0	COUNT2	COUNT1	COUNT0	STBS3	STBS2	STBS1	FV9	FV8	FV7	FV6	FV5	FV4	FV3	FV2	FV1	FV0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0(LSB)
CB1	CB0	SPIF1	SPIF2	X	X	RCIMP1_9	RCIMP1_8	RCIMP1_7	RCIMP1_6	RCIMP1_5	RCIMP1_4	RCIMP1_3	RCIMP1_2	RCIPM1_1	RCIMP1_0	STGSNS	CLAMP	OCH	STBH	STGH	STGRC	RCIMP2_9	RCIMP2_8	RCIMP2_7	RCIMP2_6	RCIMP2_5	RCIMP2_4	RCIMP2_3	RCIMP2_2	RCIMP2_1	RCIMP2_0

Bit 63:

Bit not used.

Bit 62 - 60: VER[2..0]

Silicon version bits. These bits are updated after every silicon revision as follows:

Table 7. Silicon version bits

VER2	VER1	VER0	Description
0	0	1	First silicon
0	1	0	Second silicon
0	1	1	Third silicon

Bit 59: REG

This bit represents the SO content, as follows:

REG=’0’ => SO status register;

REG=’1’ => SO input register.

Bit 58:

Bit not used.

Bit 57 - 48: RCAMP[9..0]

10 bit A/D conversion of the output of INRC amplifier. For detailed description of the timing sequence refer to *Section 4.12*.

Bit 47 - 45: COUNT[2..0]

3 bit measurement counter. For detailed description of the timing sequence refer to *Section 4.12*.

Bit 44 - 42: STBS[3..1]

These bits represent the sensor short to battery condition as follows:

STBS='0' => no fault;

STBS='1' => short to battery detected.

with the following association:

STBS1 => short to battery detected on SR pin;

STBS2 => short to battery detected on INRC pin;

STBS3 => short to battery detected on SNS, OUT or TG pins.

For detailed description of the fault detection refer to section *Section 5.1*.

Bit 41 - 32: FV[9..0]

10 bit A/D conversion of FV pin voltage. For detailed description of the timing sequence refer to *Section 4.12*.

Bit 31 - 30: CB[1..0]

These are confirmation bits and their values is fixed, CB1='1', CB0='0'; these bits can be used by the µP to detect SPI data faults.

Bit 29 - 28: SPIF[1..2]

These bits indicate the presence of an SPI data fault, as described in the following table:

Table 8. SPI data fault

SPIF1	SPIF2	Description
0	X	No fault
1	0	SPI fault: SPI length error / data fault (CB error)
	1	SPI fault: illegal SPI command

Bit 27 - 26:

Bits not used.

Bit 25 - 16: RCIMP1_[9..0]

10 bit A/D conversion of the output of RCT2 amplifier before the activation of RCT1 switch. For detailed description of the timing sequence refer to *Section 4.12*.

Bit 15: STGSNS

This bit represents the sensor short to ground condition on SNS pin as follows:

STGSNS='0' => no fault;

STGSNS=’1’ => short to ground detected.

For detailed description of the fault detection refer to *Section 5.2*.

Bit 14: CLAMP

This bit indicates the activation of VCCS clamp as follows:

CLAMP=’0’ => no activation;

CLAMP=’1’ => clamp activated.

For detailed description of the analog circuitry refer to *Section 4.9*.

Bit 13: OCH

This bit represents the heater open circuit condition as follows:

OCH=’0’ => no fault;

OCH=’1’ => heater open circuit.

If the device detects a heater open circuit and then a short to ground condition without any fault clear frame between these 2 events, both OCH and STGH bits can be =’1’ in SPI output frame.

For detailed description of the fault detection refer to *Section 5.4.3*.

Bit 12: STBH

This bit represents the heater short to battery condition as follows:

STBH=’0’ => no fault;

STBH=’1’ => heater short to battery.

For detailed description of the fault detection refer to s*Section 5.4.1*.

Bit 11: STGH

This bit represents the heater short to ground condition as follows:

STGH=’0’ => no fault;

STGH=’1’ => heater short to ground.

For detailed description of the fault detection refer to *Section 5.4.2*.

Bit 10: STGRC

This bit represents the sensor short to ground condition on INRC pin as follows:

STGRC=’0’ => no fault;

STGRC=’1’ => short to ground detected.

For detailed description of the fault detection refer to *Section 5.2*

Bit 9 - 0: RCIMP2_[9..0]

10 bit A/D conversion of the output of RCT2 amplifier while RCT1 switch is active. For detailed description of the timing sequence refer to *Section 4.12*.

6.4.2 SPI output register (input echo configuration)

63(MSB)	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
X	X	X	X	REG	INRCPD	STGINRC	INRCGAIN	TGEN	VCCSEN	VCCSOUT	VCCSPD	COMPSEL	CLAMPEN	CLAMPCL	CLAMPSIM	CLEARFLT	CCS3	CCS2	CCS1	CCS0	SAMP2	SAMP1	SAMP0	VCCSCAP5	VCCSCAP4	VCCSCAP3	VCCSCAP2	VCCSCAP1	VCCSCAP0	MCP1	MCP0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0(LSB)
STBHTH	ITPT6	ITPT5	ITPT4	ITPT3	ITPT2	ITPT1	ITPT0	SNC	CBT6	CBT5	CBT4	CBT3	CBT2	CBT1	CBT0	CB1	CB0	X	STBHFT1	STBHFT0	ISPT2	ISPT1	ISPT0	PG2EN	PG1EN	X	X	X	X	X	X

Bit 63 – 0:

Refer to *Section 6.3* for the description of these bits.

7 Electrical characteristics

7.1 DC characteristics

VCCD = VCCA = VCCCP = 4.9 V to 5.1 V, VCCI = 3.14 V to VCCD, R_{bg} = 12.1 kΩ ±1%, T_{amb} =-40°C to 125/150°C; unless otherwise specified.

Table 9. Supplies and control inputs

Parameter	Conditions	Min.	Max.	Unit
Power supplies				
VCCA + VCCD + VCCCP current	VCCS disabled	-	30	mA
	VCCS enabled, full load	-	40	mA
VESD pin leakage current	VESD voltage = 14.7V; T_j = 85 °C	-	5	µA
	VESD voltage = 40 V	-	20	µA
Negative supply voltage (CP pin)	CP current = 18 mA; OUT, TG current = 0 mA	-VCCCP	-4.3	V
Interface logic level supply current consumption (VCCI pin)	SO pin current = -800 µA	0	1	mA
POR (power on reset)				
VCCA POR threshold	Release reset above this voltage	-	4.6	V
	Issue reset below this voltage	4.1	4.45	V
VCCA POR hysteresis	-	100	300	mV
VCCD, VCCCP POR threshold	Release reset above this voltage	3.82	4.22	V
	Issue reset below this voltage	3.58	3.98	V
VCCD + VCCCP POR hysteresis	-	140	440	mV
GNDD, GNDCP loss detection	Referred to GNDA	175	225	mV
VCCA loss detection	VCCD - VCCA	165	215	mV
GNDA loss detection	GNDA - GNDD	165	215	mV
Current reference				
Reference pin voltage (BG pin)	-	1.178	1.252	V
Logic levels (SI, CLK, CSN, PW, SY pins)				
Input high voltage	-	-	0.7	VCCI
Input low voltage	-	0.3	-	
Input hysteresis	-	0.1	-	
SI, CLK input leakage current	Vin = VCCI	-	1	µA
	Vin = from 0V to input low voltage max	-1	-	
Input pull-up current (CSN, PW pins)	Vin = from GNDA to input high voltage min	-50	-10	
Input pull-down current (SY pin)	Vin = from input low voltage min to VCCI	10	50	

Table 9. Supplies and control inputs (continued)

Parameter	Conditions	Min.	Max.	Unit
Logic levels (SO pin)				
Output low voltage	SO current = 1.6 mA	-	0.4	V
Output high voltage	VCCI = 4.9 V, SO current = -800 µA	VCCI – 0.8V	-	
	VCCI = 3.13 V, SO current = -100 µA			
SO pin leakage current	Vin = VCCI or GNDA, tri state condition	-5	5	µA

Table 10. INRC, RCT2 and integrator amplifiers, RCT1, INRC and band-gap switches, clean currents

Parameter	Conditions	Min.	Max.	Unit
INRC amplifier				
Bias point (voltage measured on C1A/B pin)	INRC pin voltage = 450 mV	1.842	1.937	V
GAIN	INRCGAIN bit = 0	4.137	4.242	V/V
	INRCGAIN bit = 1	2.079	2.121	V/V
Output offset voltage	-	-26	26	mV
Output voltage swing	Maximum output voltage, C1 pin current = -500 µA	4.3	VCCA	V
	Minimum output voltage, C1 pin current = 500 µA	0	200	mV
INRC pull down current	INRCPD bit = 1	400	600	µA
RCT2 amplifier				
GAIN	INRCGAIN = 0	4.137	4.242	V/V
Output offset voltage	-	-26	26	mV
Output voltage swing	Maximum output voltage, output current = -500 µA	4.3	VCCA	V
	Minimum output voltage, output current = 500 µA	0	200	mV
RCT2 leakage current	Impedance test disabled	-1	1	µA
Integrator amplifier				
Input offset voltage	-	-8	8	mV
Open loop gain		100	-	dB
Reference voltage (REF)	-	1.848	1.932	V
Input bias current (C2 pin)	-	-0.2	0.2	µA
Output voltage swing	C3 current = -500 µA, C2 voltage < 0.9 * REF voltage	VCCA–0.3	VCCA	V
	C3 current = 500 µA, C2 voltage > 1.1 * REF voltage	0	300	mV

Table 10. INRC, RCT2 and integrator amplifiers, RCT1, INRC and band-gap switches, clean currents (continued)

Parameter	Conditions	Min.	Max.	Unit
Parking voltage	C3 voltage with VCCSEN bit = 0	REF2– 0.02	REF2+ 0.02	V
RCT1 switch				
On resistance	-	4	16	Ω
RCT1 bandgap switch				
On resistance	-	2	16	Ω
Output voltage (RCT1 pin)	Charge balance mechanism activated	1.154	1.275	V
INRC switch				
On resistance	-	2.5	20	Ω
Output leakage current in off state (C1 pin)	Charge balance mechanism activated	-1	1	µA
Clean currents				
Clean current	Bits CCS[3..0] = 0000, 0 < INRC < VCCA	-1	1	µA
	Bits CCS[3..0] = 0001, 0 < INRC < 2 V	-15.4	-12.6	
	Bits CCS[3..0] = 0010, 0 < INRC < 2 V	-22	-18	
	Bits CCS[3..0] = 0100, 0 < INRC < 2 V	-44	-36	
	Bits CCS[3..0] = 1000, 0 < INRC < 2 V	-88	-72	

Table 11. FVOUT, scaling amplifiers, A/D conversion, RFV resistor

Parameter	Conditions	Min.	Max.	Unit
RFV resistor				
RFV resistor value	-	3.75	6.25	kΩ
FVOUT amplifier				
GAIN	Bit SAMP[2..0] = 000; nominal gain = 1	0.995	1.005	V/V
	Bit SAMP[2..0] = 001; nominal gain = 1.5	1.485	1.515	
	Bit SAMP[2..0] = 010; nominal gain = 2	1.98	2.02	
	Bit SAMP[2..0] = 011; nominal gain = 3	2.955	3.015	
	Bit SAMP[2..0] = 100; nominal gain = 4	3.93	4.03	
	Bit SAMP[2..0] = 101; nominal gain = 6	5.88	6.12	

Table 11. FVOUT, scaling amplifiers, A/D conversion, RFV resistor (continued)

Parameter	Conditions	Min.	Max.	Unit
GAIN	Bit SAMP[2..0] = 110; nominal gain = 8	7.84	8.16	V/V
	Bit SAMP[2..0] = 111; nominal gain = 12	11.7	12.18	
Input offset voltage	-	-0.3	0.3	mV
Bias reference voltage (**REF2**)	-	0.498	0.502	VCCA
Output voltage swing	Maximum output voltage, output current = -500 µA	VCCA – 0.2	VCCA	V
	Minimum output voltage, output current = 500 µA	0	200	mV
Scaling amplifier				
GAIN	Bit SAMP[2..0] = 000; nominal gain = 1	0.995	1.005	V/V
	Bit SAMP[2..0] = 001; nominal gain = 1.5	1.485	1.515	
	Bit SAMP[2..0] = 010; nominal gain = 2	1.98	2.02	
	Bit SAMP[2..0] = 011; nominal gain = 3	2.97	3.03	
	Bit SAMP[2..0] = 100; nominal gain = 4	3.94	4.04	
	Bit SAMP[2..0] = 101; nominal gain = 6	5.88	6.12	
	Bit SAMP[2..0] = 110; nominal gain = 8	7.84	8.16	
	Bit SAMP[2..0] = 111; nominal gain = 12	11.76	12.24	
Input offset voltage	-	-0.3	0.3	mV
A/D conversion				
INRC amplifier	INRC pin voltage = 225 mV	180	207	cnts
	INRC pin voltage = 400 mV	324	364	
	INRC pin voltage = 500 mV	407	453	
VCCS current conversion	FV pin voltage = 4.3 V	863	898	
	FV pin voltage = 3.85 V	775	802	
	FV pin voltage = 2.5 V	508	515	
	FV pin voltage = 1.15 V	221	248	
	FV pin voltage = 700 mV	125	160	
ADC error conversion	Mean error after 8 A/D conversions	-4	4	
	Maximum error for each conversion	-2	2	

Table 12. VCCS, PG1 (PG2) driver, Heater Fet driver

Parameter	Conditions	Min.	Max.	Unit
VCCS				
SNS common mode range	Design information	-2	2.4	V

Table 12. VCCS, PG1 (PG2) driver, Heater Fet driver

Parameter	Conditions	Min.	Max.	Unit
RTOT maximum drop	|OUT voltage – SNS voltage|; design information	-	1.8	V
RTOT range	Design information	50	300	Ω
Gain	ΔI (OUT pin) / (ΔV (C3 pin) * RTOT)	0.988	1.012	V/V
Max VCCS current	C3 voltage = 0V, RTOT = 0Ω	12	20	mA
	C3 voltage = 5V, RTOT = 0Ω	-20	-12	
VCCS leakage current (evaluated on OUT1, OUT2, SNS pins)	Bit VCCSEN = 0, OUT1 = OUT2 = SNS = 0V, T = 150 °C	-5	5	µA
	Bit VCCSEN = 0, OUT1 = OUT2 = SNS = 5V, T = 150 °C	-	5	
Offset voltage	C3 voltage = REF2, VCCS offset voltage = OUT voltage – SNS voltage	-0.7	0.7	mV
Voltage clamp error, positive limit	CL1 (CL2) voltage – SNS voltage	-25	25	mV
Voltage clamp error, negative limit	CL1 (CL2) voltage – SNS voltage	-50	50	mV
Output impedance	-	100	-	kΩ
Common mode gain	C3 voltage fixed, SNS pin moved, Δ(OUT voltage – SNS voltage) / ΔSNS voltage	-2	2	mV/V
TG switch on resistance	Internal switch between TG and OUT pin	-	4	Ω
VCCS pull-down resistance	-	10	21	kΩ
OUT differential current	OUT current = 0mA; OUT current variation if SNS pin is moved from 0V to -2 V or to 2.4 V	-	7	µA
	OUT current = ±12 mA; RTOT = 120Ω; OUT current variation if SNS pin is moved from 0 V to -2 V (I=12 mA) or to 2.4 V (I=-12 mA)	-	40	
	OUT current = ±11 mA; RTOT = 97Ω; OUT current variation if SNS pin is moved from 0 V to -2 V (I=11 mA) or to 2.4 V (I=-11 mA)	-	20	
PG driver				
PG pin output voltage	PG current = -10 µA	VCCA -0.1	VCCA	V
	PG current = 10 µA	0	100	mV
Pull-down resistor	-	70	130	kΩ
Heater FET driver				
HG pin output voltage	PG current = -10 µA	VCCA -0.2	VCCA	V
	PG current = 10 µA	0	100	mV
Pull-down resistor	-	70	130	kΩ

Table 13. Diagnostic

Parameter	Conditions	Min.	Max.	Unit
Heater diagnostic				
HD diagnostic current	Source current, HD = 3 V	160	220	µA
HD diagnostic current	Sink current, HD = 3 V	68	92	µA
HG pin voltage threshold for on state of Heater FET	If HG voltage > specified value, Heater FET is considered on	3.88	4.12	V
Heater short to ground threshold **(HSG)**	-	0.715	0.76	VCCA
Heater short to battery threshold	Bit STBHTH = 0	225	275	mV
	Bit STBHTH = 1	400	450	mV
Heater open circuit threshold	-	HSG-0.45	HSG-0.01	V
INRC, SR, SNS diagnostic				
INRC short to ground threshold	-	175	225	mV
SNS short to ground threshold	SNS_PTH: positive threshold	175	225	mV
	SNS_NTH: negative threshold	-250	-150	mV
Sensor short to battery threshold	STBS1: SR pin	175	225	mV
	STBS2: INRC pin	0.62	0.66	VCCA
	STBS3: SNS pin	2.6	2.8	V

Table 14. Leakage currents

Parameter	Conditions	Min.	Max.	Unit
Short to battery compatible pins				
HD leakage current	HD voltage = 53 V	0	150	µA
SR + INRC sum of leakage currents	Applied voltage on pins under test = 0 V, 19 V, T = 150 °	-	3	
INRC + SR + SNS + TG1 + TG2 + OUT1 + OUT2 sum of leakage currents	Applied voltage on pins under test = 0 V, 19 V, 40 V, T = 150 °C	-	20	
RCT1 + RCT2 sum of leakage currents	Applied voltage on pins under test = 0 V, 19 V, T = 150 °C	-	3	

7.2 AC characteristics

VCCD = VCCA = VCCCP = 4.9 V to 5.1 V, VCCI = 3.14 V to VCCD, R_{bg} = 12.1 kΩ ±1%, T_{amb} =-40 °C to 125/150 °C. Timing is considered with respect to 20 % and 70 % of VCCA unless otherwise specified.

Table 15. AC parameters

Parameter	Conditions	Min.	Max.	Unit
Internal oscillator				
Clock frequency (**FOSC**)	TOSC = 1/FOSC	3.8	4.2	MHz
POR (power on reset)				
POR filter time	-	10	20	µs
INRC amplifier				
Bandwidth	-	200	-	kHz
Slew rate	-	1.5	-	V/µs
RCT2 amplifier				
Bandwidth	-	200	-	kHz
Slew rate	-	1.5	-	V/µs
Integrator amplifier				
Bandwidth	-	1	-	MHz
Slew rate	-	1.5	-	V/µs
FVOUT amplifier: S&H				
Time constant	Sample mode	-	1	µs
Voltage sag	Hold mode	0	0.5	mV/µs
Synchronization delay	-	0	16	µs
Scaling amplifier: S&H				
Time constant	Sample mode	-	1	µs
Voltage sag	Hold mode	0	0.5	mV/µs
VCCS				
Bandwidth	-	100	-	kHz
En/disable sequence delay	Hold mode	4		TOSC
Gate drivers				
HG transition time	Rise time, 5nF load	30	50	µs
	Fall time	30	50	µs
	Fall time, diagnostic shutoff	0	200	ns
PG transition time	Rise time, 5nF load	0	1.5	µs
	Fall time	0	200	ns

Table 16. Timing

Parameter	Conditions	Min.	Max.	Unit
Heater PWM frequency	Design information	0	600	Hz
State machine clock (T_{smc})	Bit MCP[1..0] = 00	40000		T_{OSC}
	Bit MCP[1..0] = 01	80000		
	Bit MCP[1..0] = 10	200000		
	Bit MCP[1..0] = 11	400000		
RCT1 switch time (t_R)	nitp: decimal conversion of ITPT[6..0]; lower value limited by hardware to nitp = 25. No pulse if set to 0.	0	2*nitp	
RCT1 band-gap switch time (t_B)	ncbt: decimal conversion of CBT[6..0]	2*ncbt		
INRC switch extension time (t_{INRC})	ninrc: decimal conversion of ISPT[2..0]	960*ninrc	1024*ninrc	
S&H settling time (t_{spl})	-	20		
A/D conversion time (t_{AD})	-	40		
Settling delay	td1	14		
	td2	16		
	td3	18		
SY assertion time	-	3	-	
SY de-assertion time	-	3	-	
Integrator settling time	Time from VCCSEN de assertion to parking functionality activation	-	1	ms

Table 17. Diagnostic filter times

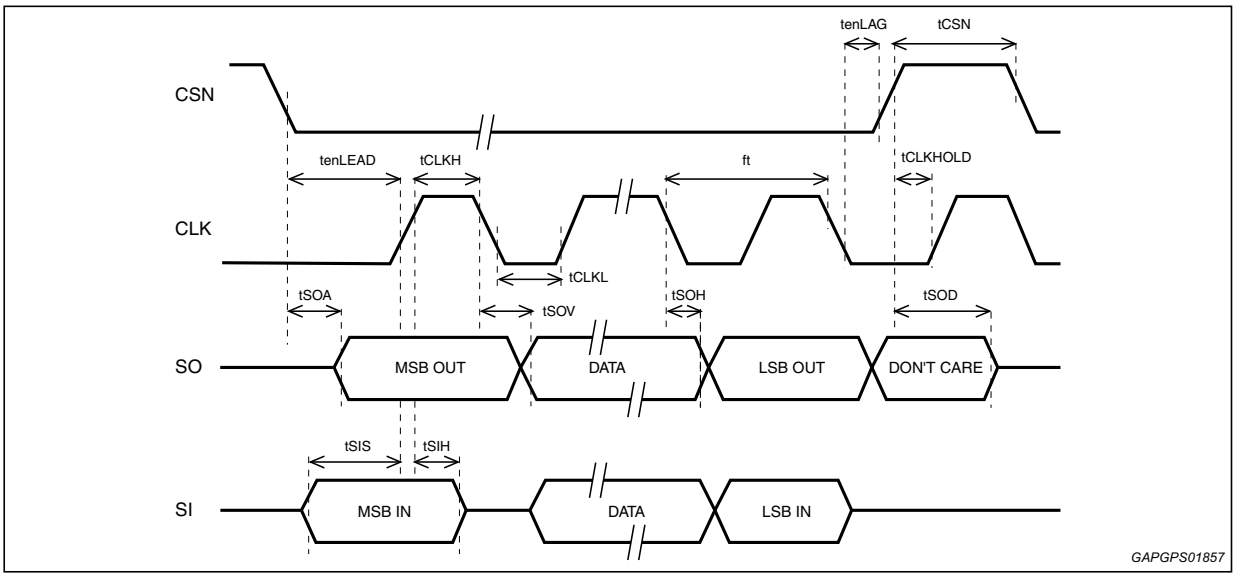
Parameter	Conditions	Min.	Max.	Unit
Heater short to ground filter time		960	1024	T_{OSC}
Heater short to battery filter time	STBHFT[1..0] = 00	80	81	
	STBHFT[1..0] = 01	60	61	
	STBHFT[1..0] = 10	40	41	
	STBHFT[1..0] = 11	20	21	
Sensor short to battery filter time	On SR, INRC, SNS pins	20	21	
Sensor short to ground filter time	On INRC, SNS pins	20	24	

SPI data shift happens on rising edges. Logic timing parameters are defined in *Figure 11*.

Table 18. Logic communications timing

Parameter	Conditions	Min.	Max.	Unit
Transfer frequency (f_t)	-	-	8	MHz
CLK period (t_{CLK})	-	125	-	ns
Enable lead time (t_{enLEAD})	-	375	-	
Enable lag time (t_{enLAG})	-	50	-	
CLK high time (t_{CLKH})	-	50	-	
CLK low time (t_{CLKL})	-	50	-	
SI input setup time (t_{SIS})	-	15	-	
SI input hold time (t_{SIH})	-	20		
SO access time (t_{SOA})	VCCI = 3.13 V; Cload = 50 pF	-	340	
	VCCI = 3.13 V; Cload = 100 pF			
	VCCI = 4.75 V; Cload = 50 pF			
	VCCI = 4.75 V; Cload = 100 pF			
SO disable time (t_{SOD})	-	-	100	
SO output valid time (t_{SOV})	VCCI = 3.13 V; Cload = 50 pF	-	60	
	VCCI = 3.13 V; Cload = 100 pF	-	160	
	VCCI = 4.75 V; Cload = 50 pF	-	40	
	VCCI = 4.75 V; Cload = 100 pF	-	80	
SO output hold time (t_{SOH})	-	20	-	
CLK hold time ($t_{CLKHOLD}$)	-	300	-	
CSN negated time (t_{CSN})	-	2	-	µs

Figure 11. SPI timing diagram



8 Application circuit

Figure 12. Application circuit

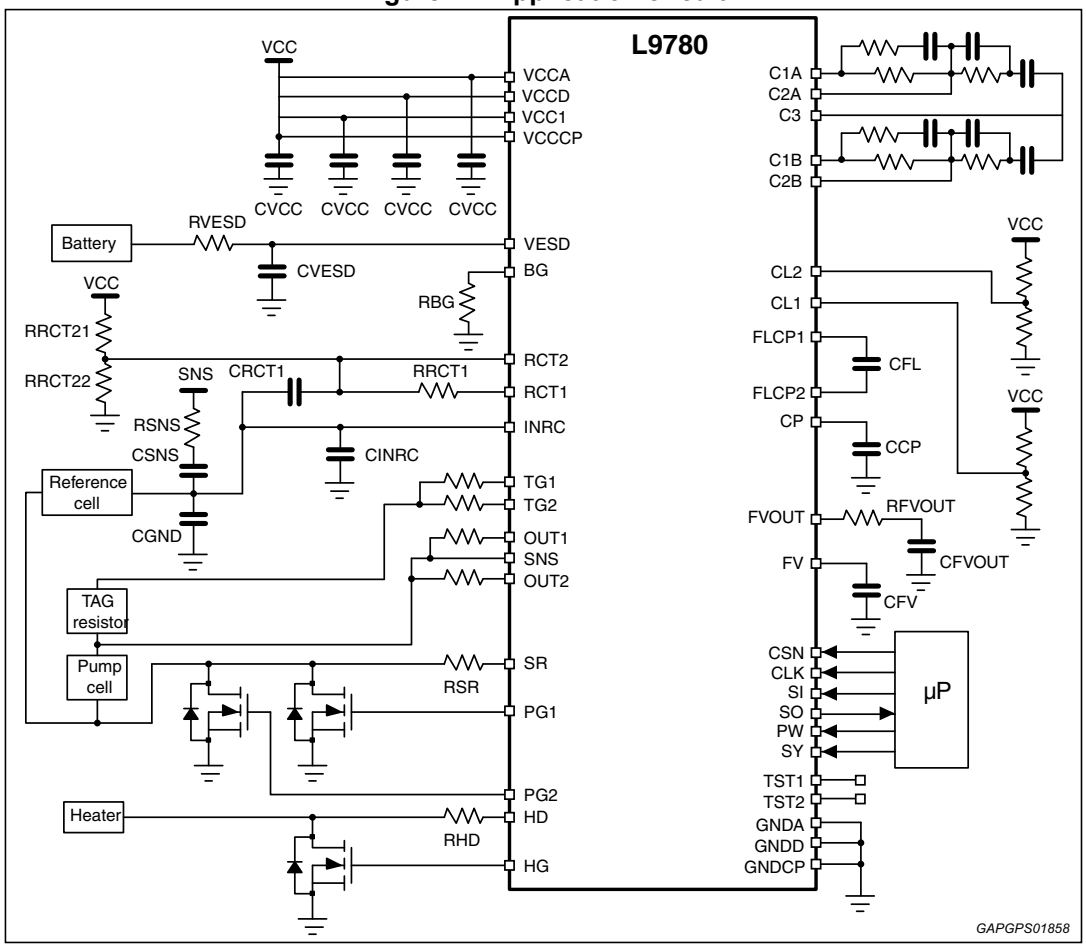


Table 19. External components value

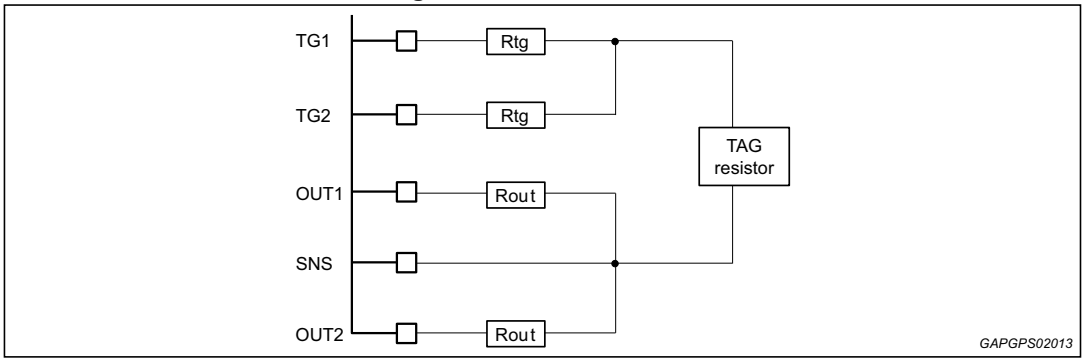
Parameter(1)	Min.	Typ.	Max.	Unit
CVCC*	-	100	-	nF
RVESD	-	1	-	kΩ
CVESD	-	10	-	nF
RBG	11.979	12.1	12.221	kΩ
RRCT1	-	442	-	Ω
CRCT1	-	1	-	µF
CINRC	-	2.2	-	nF
RSNS	-	10	-	kΩ
CSNS	-	1	-	µF
RRCT21	-	45.3	-	kΩ

Table 19. External components value (continued)

Parameter(1)	Min.	Typ.	Max.	Unit
RRCT22	-	11	-	kΩ
CGND	-	1	-	nF
RSR	-	10	-	kΩ
RHD	-	2	7.5	kΩ
CFL(2)	-	470	-	nF
CCP(2)	-	1	-	µF
CFVOUT	0.1	10	100	nF
RFVOUT	5	7.5	-	kΩ
CFV	-	4.7	-	µF

1. Not defined external components have values depending on the kind of sensor that has to be managed (as for compensation network components or VCCS external resistors) or depending on the value defined by the user (like for CL voltage dividers). TST pins have to be left open.
2. It is recommended to use ceramic capacitances and place them as close as possible to the part.

Figure 13. Sensor circuit



Sensors value:

Sensor D: Rout = 301 Ω typ, Rtg = 0 Ω, TAG resistor ≅ 596 Ω;

Sensor B: Rout = 61.9 Ω typ, Rtg = 0 Ω, TAG resistor ≅ 113 Ω;

Sensor N: Rout = 137 Ω typ, Rtg = 221 Ω typ, TAG resistor ≅ 408 Ω.

9 Package information

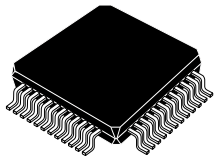
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 14. LQFP48 mechanical data and package dimensions

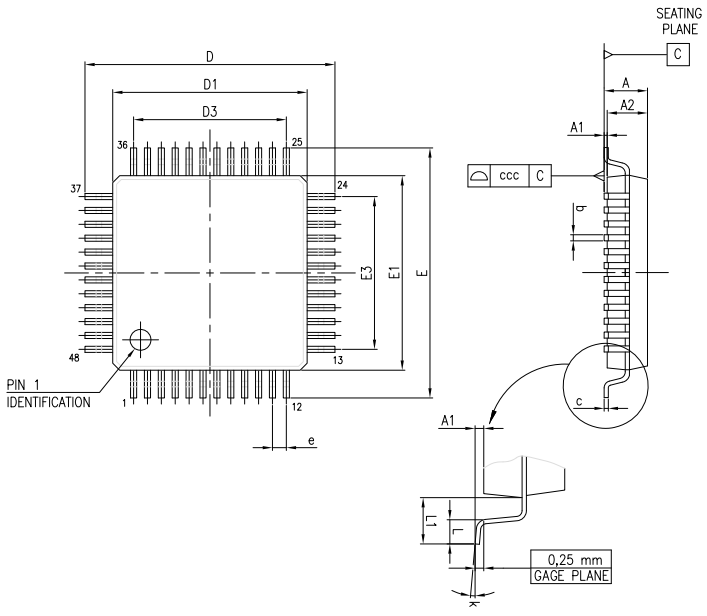
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D3		5.50			0.217	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E3		5.50			0.217	
e		0.50			0.019	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 7 x 7 x 1.4mm

LQFP48



GAPGPS01859

10 Revision history

Table 20. Document revision history

Date	Revision	Changes
15-May-2014	1	Initial release.
01-Oct-2014	2	Updated *Table 4: Absolute maximum ratings on page 9*.
27-Nov-2014	3	In the *Table 4: Absolute maximum ratings* added 'TGx, OUTx' at the Parameter 'SR, SNS' of V_{in},. Updated for the parameter |TGx - OUTx| the value from +20 V to +16 V.

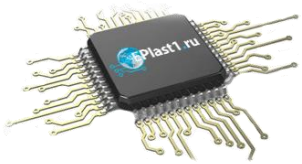
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.