XR21B1424

Enhanced 4-Ch Full-Speed USB UART

General Description

The XR21B1424 is an enhanced Universal Asynchronous Receiver and Transmitter (UART) bridge to USB interface. The USB interface is fully compliant to the USB 2.0 (Full-Speed) specification with 12 Mbps USB data transfer rate. The USB interface also supports USB suspend, resume and remote wakeup operations. The USB Vendor ID, Product ID, power mode, remote wakeup support, maximum power, and numerous other settings may be programmed in the on-chip OTP memory via the USB interface.

The XR21B1424 includes an internal oscillator and does not require an external crystal/oscillator. Any UART baud rate from 300 bps to 12 Mbps may be generated with this internal clock and the fractional baud rate generator.

The UART pins for each port may also be configured as GPIO; direction, state, output driver type and input pull-up or pull-down resistors are programmed either through on chip OTP, or on the fly via memory mapped registers.

Large 512-byte TX and RX FIFOs prevent buffer overflow errors and optimize data throughput. Automatic half-duplex direction control and optional multi drop (9-bit) mode simplify both hardware and software in half-duplex RS-485 applications. Wide mode allows for each individual received character to be monitored for errors.

The XR21B1424 uses the native OS CDC-ACM driver or a MaxLinear supplied custom driver. MaxLinear provides WHQL/HCK-certified software drivers for Windows 2000, XP, Vista, 7, 8, 8.1 and 10 as well as software drivers for Windows CE, Linux and Mac OS X. Full source code is available.

The XR21B1424 operates from a single 5V or 3.3V power supply. When powered with 5V input, a regulated 3.3V output is supplied.

FEATURES

- ±15kV ESD on USBD+/USBD-
- USB 2.0 Compliant, Full-Speed (12Mbps)
- Unique pre-programmed USB serial number
- Internally generated 48MHz core clock
- Enhanced UART features
  - Baud rates from 300 bps to 12 Mbps
  - Fractional Baud Rate Generator
  - 512-byte TX and 512-byte RX FIFOs
  - Auto Hardware / Software Flow Control
  - Multidrop and Half-Duplex Modes
  - Auto RS-485 Half-Duplex Control
  - Selectable GPIO or Modem I/O
- Up to 10 GPIOs per channel
- 5V tolerant GPIO inputs
- Suspend state GPIO configuration
- Configurable clock output
- 64-pin LQFP package
- Industrial -40°C to +85°C Temperature Range

APPLICATIONS

- Building Automation
- Security Systems
- Factory and Process Control
- ATM Terminals
- USB to Serial Controllers

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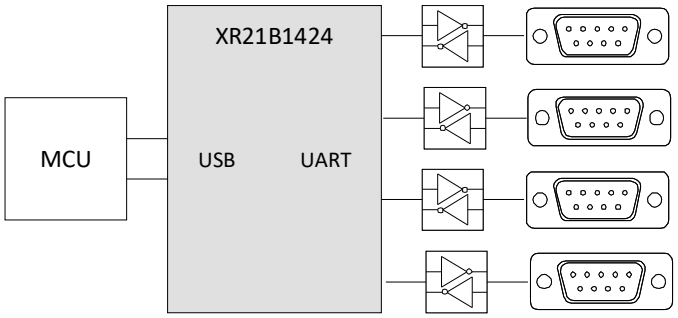
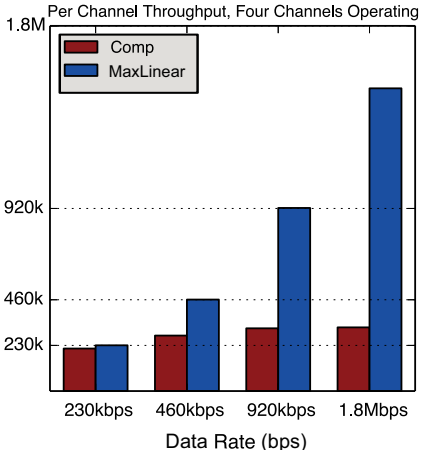
Typical Application





Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating may affect device reliability and lifetime.

Supply Voltage (VCC_REG).....+5.75V

Supply Voltage (VCC, VIO).....+4V

Input Voltage (VBUS_SENSE).....-0.3 to +5.75V

Input Voltage (All other pins).....-0.3 to +5.6V

Junction Temperature.....125°C

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

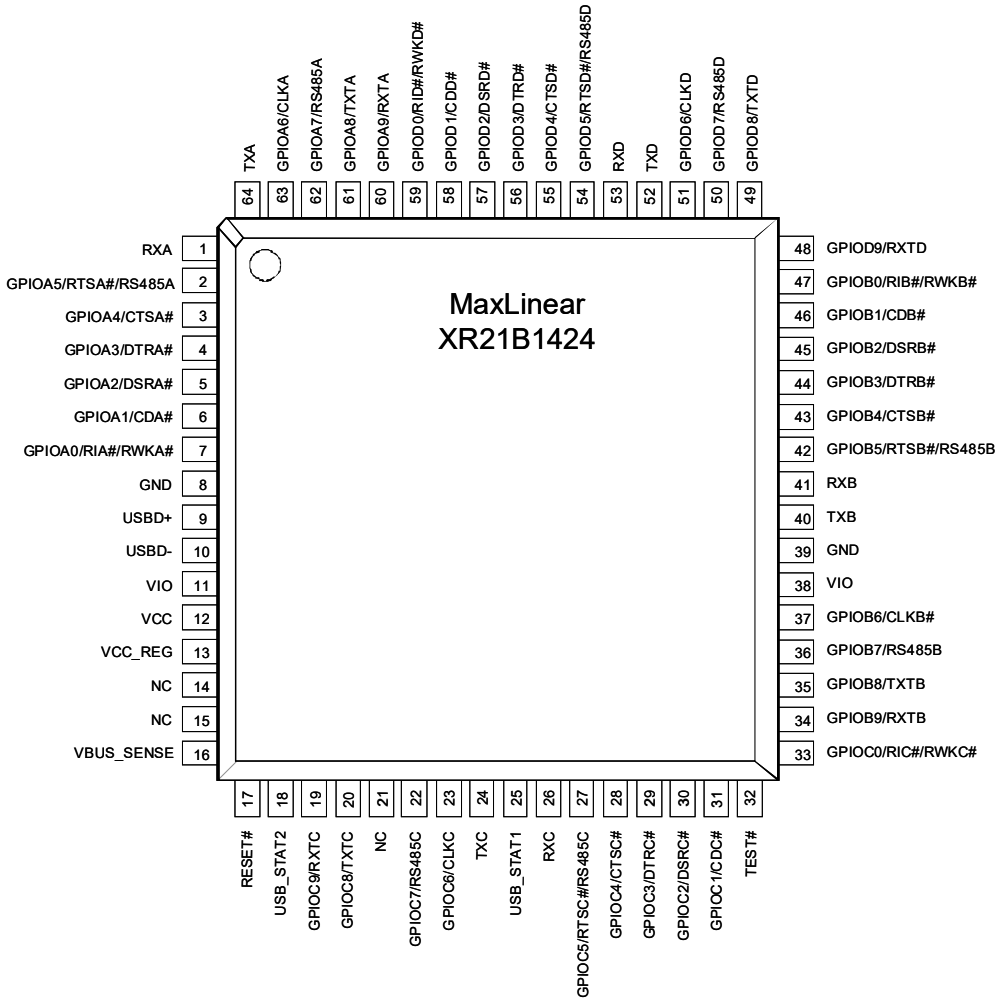
Electrical Characteristics

Unless otherwise noted: T_A = -40°C to +85°C, VCC_REG = +4.4V to +5.25V or +3.0V to +3.6V, VIO = +1.8V to +3.6V.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power							
I_{CC}	Power Supply Current	VCC_REG = +4.4V to +5.25V			15	23	mA
I_{SUSP}	Lowpower Mode Current				0.85	1.25	mA
V_{OUT}	Regulated Output Voltage (VCC pin)	VCC_REG = +4.4V to +5.25V. Maximum output current = 200 mA including the supply current of the XR21B1424.		3	3.3	3.6	V
UART, USB_STAT and GPIO Pins							
V_{IL}	Input Low Voltage			-0.3		0.25* VIO	V
V_{IH}	Input High Voltage			0.70* VIO		5.5	V
V_{OL}	Output Low Voltage	IOL = 1mA, VIO = +1.6V				0.3	V
		IOL = 4mA, VIO = +3.6V				0.5	V
V_{OH}	Output High Voltage	IOH = -400uA, VIO = +1.6V		1.3		VIO	V
		IOH = -1.5mA, VIO = +3.6V		2.8		VIO	V
I_{IL}	Input Low Leakage Current	VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = 0V				±10	µA
I_{IH}	Input High Leakage Current	VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = +3.3V				±10	µA
		VIO = +3V to +3.6V, VCC_REG = +4.4V to +5.25V, V_{INPUT} = +5.5V				±120	µA
C_{IN}	Input Pin Capacitance					5	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Units
USB I/O Pins							
V_{IL}	Input Low Voltage			-0.3		0.8	V
V_{IH}	Input High Voltage			2.0		5.5	V
V_{OL}	Output Low Voltage	External 15kΩ to GND on USBD+ and USBD- pins		0		0.3	V
V_{OH}	Output High Voltage	External 15kΩ to GND on USBD+ and USBD- pins		2.8		3.6	V
V_{DrvZ}	Driver Output Impedance			28		44	Ω

Pin Configuration



Top View

Pin Assignments

Pin No.	Pin Name	Type	Description
1	RXA	I	UART Receive Data.
2	GPIOA5/RTSA#/RS485A	I/O	General purpose I/O, or UART Request-to-Send output (active low), or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16 or "Multidrop mode with address matching" on page 18.
3	GPIOA4/CTSA#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16.
4	GPIOA3/DTRA#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
5	GPIOA2/DSRA#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
6	GPIOA1/CDA#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up resistor.
7	GPIOA0/RIA#/RWKA#	I/O	General purpose I/O, or UART Ring-Indicator input (active low), or Remote Wakeup input. Defaults to GPIO input with internal pull-up resistor. Wakeup signaling to the USB host is sent when a falling edge is detected. See "Remote Wakeup" on page 10.
8	GND	PWR	Power supply common, ground.
9	USBD+	I/O	USB port differential data positive. This pin has internal pull-up resistor compliant to the USB 2.0 specification. The ESD protection on this pin is ±15kV HBM.
10	USBD-	I/O	USB port differential data negative. The ESD protection on this pin is ±15kV HBM.
11	VIO	PWR	I/O voltage input to the UART/GPIO pins. Must be between 1.8 and 3.6V. May be connected to VCC (pin 12) if VCC_REG input voltage is 5V. See "USB Power Modes" on page 12.
12	VCC	PWR	3.3V power to the device, or 3.3V power output from the device when 5V power is supplied to VCC_REG pin. 3.3V output power can source up to 200 mA maximum (including the device) and should be decoupled by minimum of 4.7µF ceramic capacitor. See "USB Power Modes" on page 12.
13	VCC_REG	PWR	5V or 3.3V power to the device. In bus-powered mode, connect VBUS power from the USB host to this pin and to the VBUS_SENSE pin - see Figure 1. To conform to USB specifications, an inrush current limiting circuit is recommended. In self-powered mode, connect on-board 5V or 3.3V source to this pin and VBUS from the USB host to the VBUS_SENSE pin. See Figure 2 and Figure 3. USB specification requires a minimum of 1uF and a maximum of 10uF of decoupling on VBUS power.
14	NC	-	No Connect.
15	NC	-	No Connect.
16	VBUS_SENSE	I	Must be connected to VBUS power from the USB host PC. This pin is used to disable the internal pull-up resistor on the USBD+ signal when VBUS is not present. In bus-powered mode, connect VBUS (5V) power from the USB host to this pin and to the VCC_REG pin - see Figure 1. In self-powered mode, connect VBUS from the USB host to this pin. This pin must be decoupled by a 4.7 uF tantalum capacitor.
17	RESET#	I/O / OD	Active low open drain output. Asserted at power on or any time device is reset by either register or USB bus reset. As an input, must be asserted for at least 15µs to force a device reset. Reset pulse width input of shorter than 15µs will have unknown effects. A weak internal pull-up resistor provides noise immunity if left unconnected.

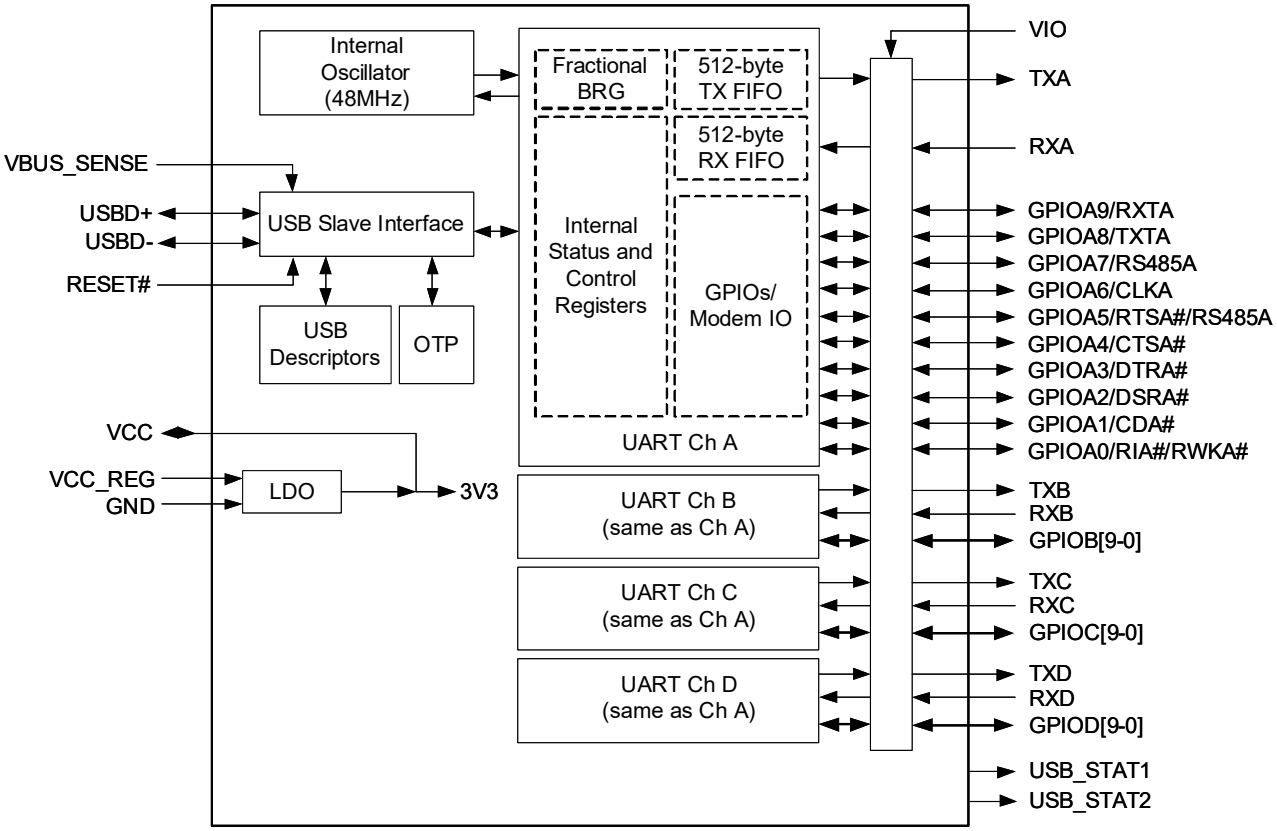
Pin No.	Pin Name	Type	Description
18	USB_STAT2	O / OD	This pin has the same functionality as the USB_STAT1 pin. However, the default output for this pin is active low polarity, asserted whenever the XR21B1424 is placed into a suspended state. This default may be changed via the PIN_CFG_USB_STAT2 register.
19	GPIOC9/RXTC	I/O	General purpose I/O, or UART receive data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as receive indicator, this pin will toggle at ~10Hz intervals while the UART is receiving data.
20	GPIOC8/TXTC	I/O	General purpose I/O, or UART transmit data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as transmit indicator, this pin will toggle at ~10Hz intervals while the UART is transmitting data.
21	NC	-	No Connect.
22	GPIOC7/RS485C	I/O	General purpose I/O, or RS-485 half-duplex enable output. Defaults to GPIO input with internal pull-up resistor.
23	GPIOC6/CLKC	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up resistor. See "Programmable Output Clock" on page 16.
24	TXC	O	UART Transmit Data.
25	USB_STAT1	O	The USB_STAT1 output pin may be used to indicate any of three USB status conditions: 1. USB_STAT1 is asserted when the USB host asserts USB reset. 2. USB_STAT1 is asserted when the USB host PC places the XR21B1424 device into the suspended state. 3. USB_STAT1 is asserted when it is not safe to draw the amount of current requested in the Device Maximum Power field of the Configuration Descriptor. a. For a low power device (<=1 unit load or 100mA, bMaxPower <= 0x32), USB_STAT1 will be asserted when the USB UART is in the suspended state. b. For a high power device (bMaxPower > 0x32), USB_STAT1 will be asserted when the USB UART is in the suspended state or when it is not yet configured. The assertion polarity and status condition are selectable via the PIN_CFG_STAT1 register. The USB_STAT pin will be de-asserted whenever the selected condition(s) is/are not met. The default output for this pin is active high polarity, asserted whenever the XR21B1424 is placed into a suspended state.
26	RXC	I	UART Receive Data.
27	GPIOC5/RTSC#/RS485C	I/O	General purpose I/O, or UART Request-to-Send output (active low), or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16 or "Multidrop mode with address matching" on page 18.
28	GPIOC4/CTSC#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16.
29	GPIOC3/DTRC#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
30	GPIOC2/DSRC#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
31	GPIOC1/CDC#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up resistor.
32	TEST#	I	Test mode. Must be left open or pulled high to VIO for normal operation.
33	GPIOC0/RIC#/RWKC#	I/O	General purpose I/O, or UART Ring-Indicator input (active low), or Remote Wakeup input. Defaults to GPIO input with internal pull-up resistor. Wakeup signaling to the USB host is sent when a falling edge is detected. See "Remote Wakeup" on page 10.
34	GPIOB9/RXTB	I/O	General purpose I/O, or UART receive data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as receive indicator, this pin will toggle at ~10Hz intervals while the UART is receiving data.

Pin No.	Pin Name	Type	Description
35	GPIOB8/TXTB	I/O	General purpose I/O, or UART transmit data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as transmit indicator, this pin will toggle at ~10Hz intervals while the UART is transmitting data.
36	GPIOB7/RS485B	I/O	General purpose I/O, or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor.
37	GPIOB6/CLKB	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up resistor. See "Programmable Output Clock" on page 16.
38	VIO	PWR	I/O voltage input to the UART/GPIO pins. Must be between 1.8 and 3.6V. May be connected to VCC (pin 12) if VCC_REG input voltage is 5V. See "USB Power Modes" on page 12.
39	GND	PWR	Power supply common, ground.
40	TXB	O	UART Transmit Data.
41	RXB	I	UART Receive Data.
42	GPIOB5/RTSB#/RS485B	I/O	General purpose I/O, or UART Request-to-Send output (active low), or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16 or "Multidrop mode with address matching" on page 18.
43	GPIOB4/CTSB#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16.
44	GPIOB3/DTRB#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
45	GPIOB2/DSRB#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic DTR/DSR Hardware Flow Control" on page 17.
46	GPIOB1/CDB#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up resistor.
47	GPIOB0/RIB#/RWKB#	I/O	General purpose I/O, or UART Ring-Indicator input (active low), or Remote Wakeup input. Defaults to GPIO input with internal pull-up resistor. Wakeup signaling to the USB host is sent when a falling edge is detected. See "Remote Wakeup" on page 10.
48	GPIOD9/RXTD	I/O	General purpose I/O, or UART receive data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as receive indicator, this pin will toggle at ~10Hz intervals while the UART is receiving data.
49	GPIOD8/TXTD	I/O	General purpose I/O, or UART transmit data indicator. Defaults to GPIO input with internal pull-up resistor. See "TXT and RXT Pins" on page 19. When configured as transmit indicator, this pin will toggle at ~10Hz intervals while the UART is transmitting data.
50	GPIOD7/RS485D	I/O	General purpose I/O, or RS-485 half-duplex enable output. Defaults to GPIO input with internal pull-up resistor.
51	GPIOD6/CLKD	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up resistor. See "Programmable Output Clock" on page 16.
52	TXD	O	UART Transmit Data.
53	RXD	I	UART Receive Data.
54	GPIOD5/RTSD#/RS485D	I/O	General purpose I/O, or UART Request-to-Send output (active low) or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16 or "Multidrop mode with address matching" on page 18.
55	GPIOD4/CTSD#	I/O	General purpose I/O, or UART Clear-to-Send input (active low). Defaults to GPIO input with internal pull-up resistor. See "Automatic RTS/CTS Hardware Flow Control" on page 16.

Pin No.	Pin Name	Type	Description
56	GPIOD3/DTRD#	I/O	General purpose I/O, or UART Data-Terminal-Ready push-pull output (active low). Defaults to GPIO input with internal pull-up resistor. See “Automatic DTR/DSR Hardware Flow Control” on page 17.
57	GPIOD2/DSRD#	I/O	General purpose I/O, or UART Data-Set-Ready input (active low). Defaults to GPIO input with internal pull-up resistor. See “Automatic DTR/DSR Hardware Flow Control” on page 17.
58	GPIOD1/CDD#	I/O	General purpose I/O, or UART Carrier-Detect input (active low). Defaults to GPIO input with internal pull-up resistor.
59	GPIOD0/RID#/RWKD#	I/O	General purpose I/O, or UART Ring-Indicator input (active low), or Remote Wakeup input. Defaults to GPIO input with internal pull-up resistor. Wakeup signaling to the USB host is sent when a falling edge is detected. See “Remote Wakeup” on page 10.
60	GPIOA9/RXTA	I/O	General purpose I/O, or UART receive data indicator. Defaults to GPIO input with internal pull-up resistor. See “TXT and RXT Pins” on page 19. When configured as receive indicator, this pin will toggle at ~10Hz intervals while the UART is receiving data.
61	GPIOA8/TXTA	I/O	General purpose I/O, or UART transmit data indicator. Defaults to GPIO input with internal pull-up resistor. See “TXT and RXT Pins” on page 19. When configured as transmit indicator, this pin will toggle at ~10Hz intervals while the UART is transmitting data.
62	GPIOA7/RS485A	I/O	General purpose I/O, or auto RS-485 half-duplex control. Defaults to GPIO input with internal pull-up resistor. See “Multidrop mode with address matching” on page 18.
63	GPIOA6/CLKA	I/O	General purpose I/O, or clock or pulse output. Defaults to GPIO input with internal pull-up resistor. See “Programmable Output Clock” on page 16.
64	TXA	O	UART Transmit Data.

Type: I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Functional Description

USB Interface

The USB interface of the XR21B1424 is compliant with the USB 2.0 Full-Speed Specifications.

The XR21B1424 uses the following set of parameters:

- 1 Control Endpoint
  - Endpoint 0 as outlined in the USB specifications
- 1 Configuration is supported
- 1 Interface for each UART channel
  - Bulk-in and bulk-out endpoints
  - Interrupt-in endpoint for notifications

USB Vendor and Product IDs

MaxLinear's USB Vendor ID is 0x04E2. This is the default Vendor ID that is used for the XR21B1424. Customers may obtain their own Vendor ID from USB.org. The default USB Product ID for the XR21B1424 is 0x1424. Upon request, MaxLinear will provide up to 8 PID values for use with MaxLinear's VID. The VID and PID can be changed using the VID and PID fields. Refer to Table 1.

USB Suspend

All USB peripheral devices must support the USB suspend mode. Per USB standard, the XR21B1424 device will begin to enter the suspend state if it does not detect any activity, (including Start of Frame or SOF packets) on its USB data lines for 3 ms. The peripheral device must then reduce power consumption from VBUS power within the next 7 ms to the allowed limit of 2.5 mA for the suspended state. Note that in this context, the "device" is all circuitry (including the XR21B1424) that draws power from the host VBUS.

Remote Wakeup

If the XR21B1424 device has been placed into the suspend state by the USB host, a high to low transition on the RI#/RWK# pins can be used to request that the host exit the suspended state. By default the XR21B1424 device reports in its USB device attributes that it supports remote wakeup, and the RI#/RWK# pins of each UART channel are enabled for remote wakeup signaling if their default configuration as an input pin has not been changed. The RI#/RWK# pins from each UART channel are logically ANDed, such that a logic '0' on any of the four pins will prevent the remote wakeup signaling. Additionally, the RX pins of each UART channel may also be enabled via OTP to support remote wakeup unless those UART channels have RX pin remote wakeup. Again all RX pins that are enabled to support remote wakeup signaling are also logically ANDed. Note that the CDC driver does not support remote wakeup.

USB Strings

USB specifies three character string descriptors that are provided to the USB host during enumeration in string descriptors: the manufacturer, product and serial strings. The default manufacturer and product strings for the XR21B1424 device are "Exar Corp." and, "Exar USB UART", respectively. The serial number string is a unique alpha-numeric string programmed into the device at the factory. All character strings use Unicode UTF-16LE format. The character string language ID is US English.

Table 1: USB String Descriptor Defaults

Descriptor	Value
Exar USB Vendor ID	0x04E2
Exar USB Product ID	0x1424
Manufacturer String	Exar Corp.
Product String	Exar USB UART

Device Driver

The XR21B1424 device may be used with either a standard CDC-ACM driver or a MaxLinear supplied custom driver. The CDC-ACM driver is native to the Operating System. In Linux, the CDC-ACM driver will automatically load for the XR21B1424, but in the Windows OS, an extra INF file is required to install the CDC-ACM driver. The custom drivers must also be installed, although for Windows 7 OS and newer with Internet access and Windows updates set to automatic, the latest Windows-Certified (WHQL/HCK) driver will be downloaded and installed automatically.

CDC-ACM Driver

Because the CDC-ACM driver has no ability to access the XR21B1424 internal device registers, the device is initialized to certain hardware defaults. By default the XR21B1424 enables hardware RTS/CTS flow control, GPIO7 is set as active high auto RS-485 half-duplex control, and RI, CD and DSR pins are enabled to be interrupt sensitive. These settings are listed in Table 2. Additionally, the low latency threshold in CDC mode is automatically set to 40,960 bps. Refer to "RX FIFO Low Latency" on page 16. This threshold may be modified in the OTP CDC_ACM_BAUD_THRESH locations.

Table 2: XR21B1424 Register Defaults with CDC-ACM Driver

Register	Value	Notes
FLOW_CONTROL	0x0001	Hardware flow control
GPIO_MODE	0x0339	RTS / CTS flow control, GPIO7 is used as RS-485 half-duplex enable (RS485) with active high polarity. GPIO6 is a GPIO input, RXT and TXT remain enabled.
GPIO_DIRECTION	0x0028	DTR / RTS are configured as outputs (TXT, RXT, CLK and RS485 are also special function outputs). All other GPIOs are configured as inputs.
GPIO_INT_MASK	0x03F0	RI, CD and DSR are interrupt sensitive, i.e. can cause a USB interrupt to be generated.

Custom MaxLinear Driver

Custom drivers for all major Operating Systems are available from MaxLinear. The custom driver allows software applications to make full use of the XR21B1424 register set and features.

Note that a custom driver must always immediately set CUSTOM_DRIVER bit-0 = 1. Once CUSTOM_DRIVER bit-0 is set, the custom driver can use standard CDC-ACM commands without the XR21B1424 automatically changing to the settings in the Table 2.

Character Format

Both CDC and custom drivers use the CDC command SET_LINE_CODING to set the character data size (5-9), parity (odd, even, mark, space, none), and stop bits (1 or 2 for 6-9 bit characters, 1 1/2 or 2 for 5 bit characters). A parity bit is not allowed when selecting 9 bit data.

USB Power Modes

The XR21B1424 device may be configured in any of the following power modes: bus-powered, self-powered 5V, or self-powered 3.3V. In all three modes, the VBUS power signal from the USB host must be connected to the VBUS_SENSE pin of the device.

The default power mode for the XR21B1424 is bus powered. In this mode, the USB device's maximum power requirement from the host must be specified. In this context, the USB device includes all components on the PCB that will draw power from the USB host VBUS power. The default maximum power for the XR21B1424 is 100mA. This may be changed using the Attributes field in the OTP.

Bus-Powered

In bus-powered mode, VBUS from the USB cable supplies 5V to the XR21B1424 device. The VCC pin will supply a 3.3V output. The VIO pins may be externally connected to VCC or to an alternate voltage source.

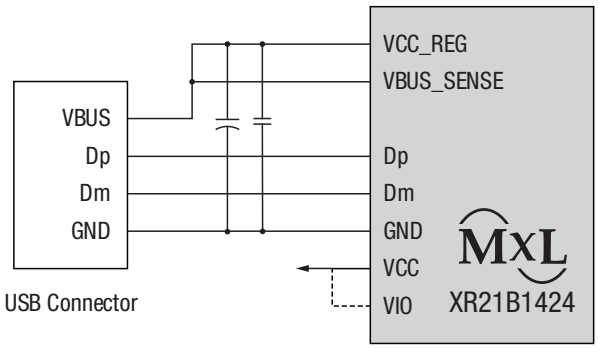


Figure 1: Bus-Powered Mode

Self-Powered 5V

In self-powered 5V mode, a local source provides 5V to the XR21B1424 device. The USB attributes should be changed in the OTP to correctly report self-powered mode. The VCC pin will supply a 3.3V output. VIO pins may be externally connected to VCC or to an alternate voltage source.

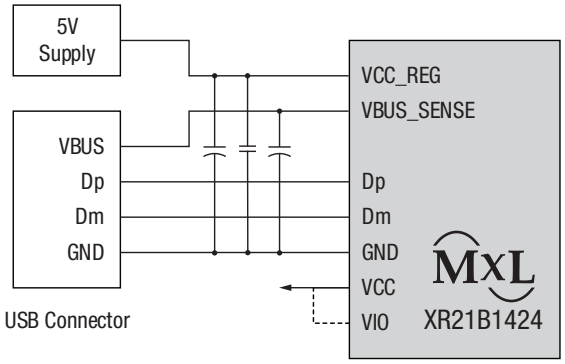


Figure 2: Self-Powered 5V Mode

Self-Powered 3.3V

In self-powered 3.3V mode, a local source provides 3.3V to both the VCC_REG and VCC pins of the XR21B1424 device. The USB attributes should be changed in the OTP to correctly report self-powered mode. VIO pins may be externally connected to VCC or to an alternate voltage source.

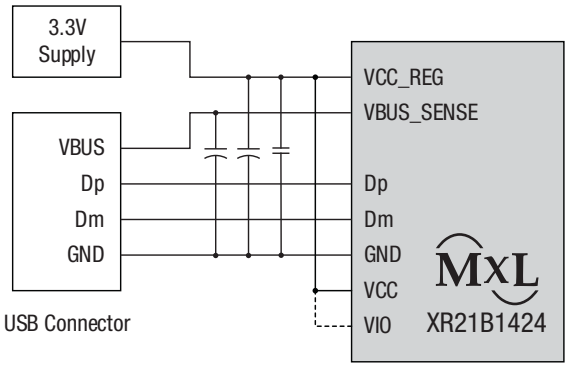


Figure 3: Self-Powered 3.3V Mode

Reset

The XR21B1424 has three different types of resets: power-on reset or POR, hardware reset, and USB bus reset. The results of each of the three types of resets are listed in Table 3.

Table 3: Device Resets

Reset Type	Device Actions
Power On Reset (POR)	Resets all registers and pins to default states including any OTP modifications. Locks OTP from further writes if Global Lock is set.
Hardware Reset	Resets all registers and pins to default states including any OTP modifications. Locks OTP from further writes if Global Lock is set.
USB Bus Reset	Resets USB Interface, re-enumerate device, reset all internal states, clear UART FIFOs. Does not reset registers or pin configurations.

UART

The UART may be configured via USB control transfers from the USB host. The UART transmitter and receiver sections are described separately in the following sections. At power-up, the XR21B1424 will default to 115.2 kbps, 8 data bits, no parity bit, 1 stop bit, and no flow control. If a standard CDC driver accesses the XR21B1424, these defaults will be changed. See "Device Driver" on page 11.

UART Wide mode allows for each character to be monitored for errors. Each received data character is accompanied by another byte containing error status for parity, framing and overrun errors as well as break condition. In 9 bit Wide mode, the 9th bit may be used for denoting address or data in multidrop applications.

Transmitter

The transmitter consists of a 512-byte TX FIFO and a Transmit Shift Register (TSR). Once a Set transmit data interrupt out or bulk-out packet has been received and the CRC has been validated, the data bytes in that packet are written into the TX FIFO. Data from the TX FIFO is transferred to the TSR when the TSR is idle or has completed sending the previous data byte. The TSR shifts the data out onto the TX output pin at the selected baud rate. The transmitter sends the start bit followed by the data bits (starting with the LSB), inserts the proper parity-bit if enabled, and adds the stop-bit(s). The transmitter may be configured for 5, 6, 7 or 8 data bits with or without parity or 9 data bits without parity. If 5, 6, 7 or 8 bit data with parity is selected, the TX FIFO contains 8 bits data and the parity bit is automatically generated and transmitted. If 9 bit data is selected, parity cannot be generated. The 9th bit will not be transmitted unless the wide mode is enabled.

Wide Mode Transmit

When both 9 bit data and wide mode are enabled, two bytes of data will be written into the TX FIFO. The first byte is the first 8 bits (data bits 7-0) of the 9-bit data. Bit-0 of the second byte is bit-8 of the 9-bit data. The data that is transmitted on the TX pin is as follows: start bit, 9-bit data, stop bit. Wide mode transmit may be enabled by the TX_WIDE_MODE register.

Receiver

The receiver consists of a 512-byte RX FIFO and a Receive Shift Register (RSR). Data that is received in the RSR via the RX pin is transferred into the RX FIFO. Data from the RX FIFO is sent to the USB host by in response to a bulk-in request. Depending on the mode, error / status information for that data character may or may not be stored in the RX FIFO with the data.

Normal receive operation with 5, 6, 7 or 8-bit data

Received data is stored in the RX FIFO. Any parity, framing or overrun error or break status information related to the data is discarded. The receive data format is shown in Figure 4.

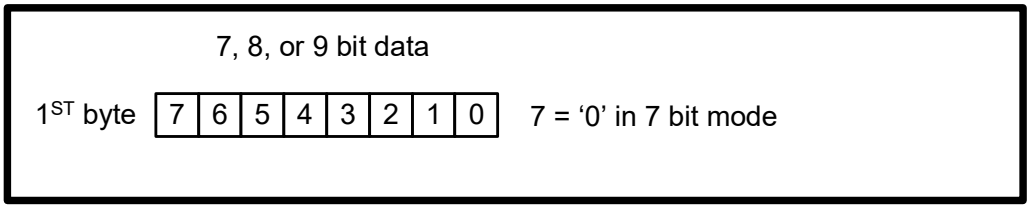


Figure 4: Receive Data Format

Normal receive operation with 9-bit data

The first 8 bits of data received is stored in the RX FIFO. The 9th bit as well as any parity, framing or overrun error or break status information related to the data is discarded.

Wide mode receive operation with 5, 6, 7 or 8-bit data

Two bytes of data are loaded into the RX FIFO for each byte of data received. The first byte is the received data. The second byte consists of the error bits and break status. Wide mode receive may be enabled by the RX_WIDE_MODE register. Wide mode receive data format is shown in Figure 5.

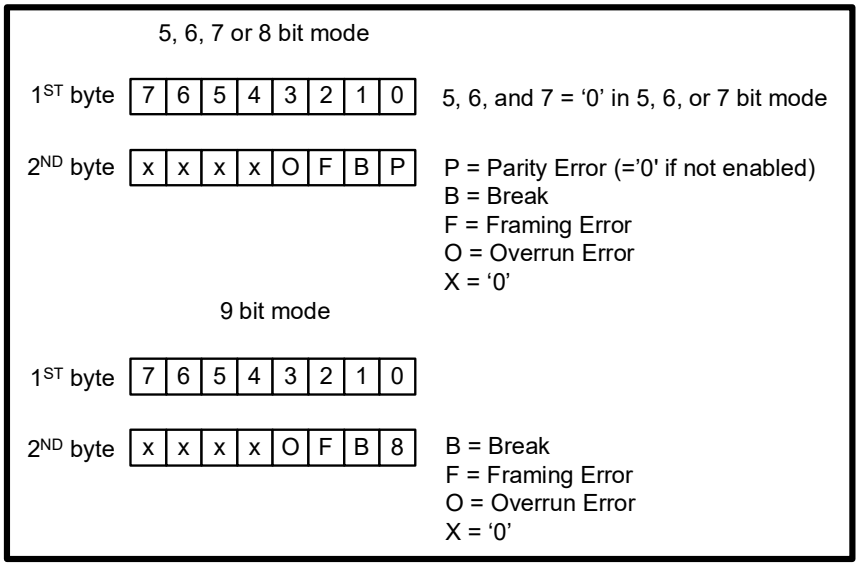


Figure 5: Wide Mode Receive Data Format

Wide mode receive operation with 9-bit data

In 9 bit wide mode, the Parity bit is replaced by the 9th data bit. The framing and overrun errors and break condition remain as shown in Figure 5.

Error flags are also available from the ERROR_STATUS register and the interrupt packet, however these flags are historical flags indicating that an error has occurred since the previous request.

RX FIFO Low Latency

In normal operation all bulk-in transfers will be of maxPacketSize (64) bytes to improve throughput and to minimize host processing. When there are 64 bytes of data in the RX FIFO, the XR21B1424 will acknowledge a bulk-in request from the host and transfer the data packet. If there are less than 64 bytes in the RX FIFO, the XR21B1424 may respond to the bulk-in request with a NAK indicating that data is not ready to transfer at that time. However, if there are less than 64 bytes in the RX FIFO and no data has been received for more than 3 character times, the XR21B1424 will acknowledge the bulk-in request and transfer any data in the RX FIFO to the USB host.

In some cases, especially when the baud rate is low, this behavior may increase latency unacceptably. The XR21B1424 has a low latency register bit that will enable the XR21B1424 to immediately transfer any received data in the RX FIFO to the USB host without waiting for 3 character times. The custom driver may be used to automatically set the RX_FIFO_LOW_LATENCY register to enable low latency mode, or the user may manually set it. With the CDC-ACM driver, the low latency mode is automatically set whenever the baud rate is set to a value of less than 40960 bps using the CDC_ACM_IF_SET_LINE_CODING command.

GPIO

Each UART has 10 GPIO pins in addition to the TX and RX pins. Each GPIO pin may also be configured for one or more special functions. All GPIO pins as well as USB_STAT1 and USB_STAT2 may be configured for a variety of pin type options using the GPIO_MODE register or by writing the OTP using XR_SET_OTP. All enabled pull-up and pull-down resistors are maintained during the USB suspend state. Pin configurations set using XR_SET_OTP are enabled following the next power-up reset and are permanent. During USB bus reset, resistors are disabled and are re-enabled after bus reset is de-asserted. Pin configurations set using the GPIO_MODE register will be lost after POR or USB bus reset.

Programmable Output Clock

The GPIO6/CLK pin may be enabled as a clock output using the GPIO_MODE register. The OUTCLK register can be used to program the output frequency of the clock from 24 MHz down to approximately 47 KHz. The duty cycle can also be programmed from 50/50 to a single low or high going pulse. The default values of zero for both DIV_HI and DIV_LO in the OUTCLK register will result in a frequency of 24 MHz. For any non-zero values for DIV_HI and DIV_LO, the clock frequency is determined by the formula:

FREQ = 24 MHz / (DIV_HI + DIV_LO). The duty cycle is determined by the ratio of DIV_HI to DIV_LO.

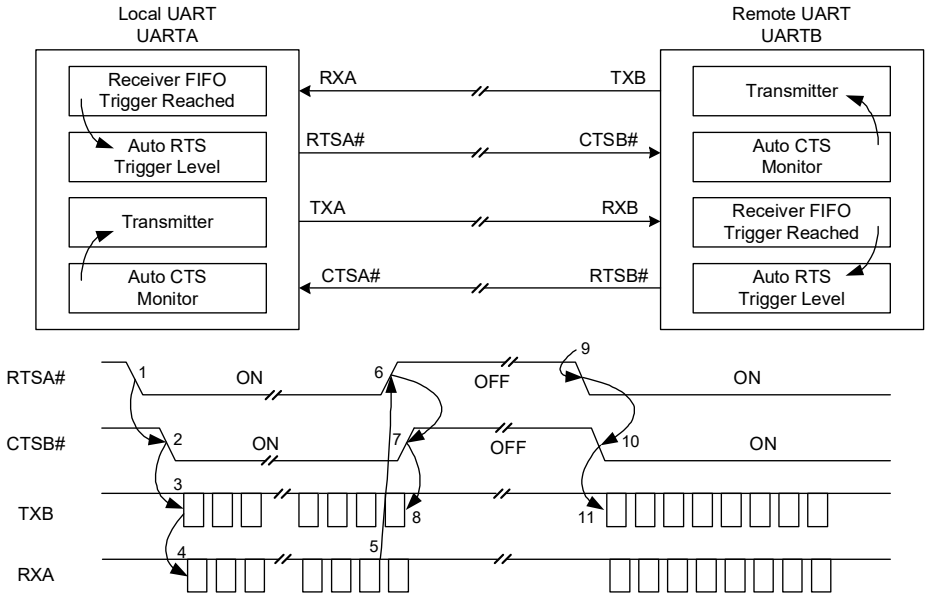
Flow Control

The XR21B1424 is able to perform both hardware and software flow control. Both hardware and software flow control modes are configured via the GPIO_MODE and FLOW_CONTROL registers. In both modes, flow control is asserted when the bytes in the RX FIFO reach the watermark set in the RX_THRESHOLD register.

Hardware flow control can either be RTS/CTS or DTR/DSR controlled. Note that although the default pin configuration for GPIO5/RTS#/RS485 and GPIO4/CTS# are for RTS output and CTS input respectively, the hardware RTS/CTS flow control mode must be set in the FLOW_CONTROL register in order to utilize the flow control functionality.

Automatic RTS/CTS Hardware Flow Control

Automatic RTS flow control is used to prevent data overrun errors in the local RX FIFO using the RTS signal to the remote UART. The RTS signal will be asserted (low) when there are less than 450 bytes in the receive FIFO. When the RX FIFO reaches the 450 byte threshold, the RTS pin will be de-asserted. The CTS# input is monitored by the remote UART to suspend/restart the local transmitter. Refer to Figure 6. Conversely, when the remote UART reaches its receive FIFO threshold, its RTS will be de-asserted, and the B1424 CTS input will cause the device to suspend data transmission.



1) COM port opened, RX FIFO empty, RTSA# output is asserted
2) Signal propagated to CTSB# input
3) Data bytes enter TX FIFO, begin transmitting on TXB
4) Data propagates to Receiving device RXA
5) RX FIFO reaches threshold
6) RTSA# de-asserts
7) Signal propagates to CTSB# input
8) Transmission stops on TXB
9) USB Bulk-In empties RX FIFO below threshold, RTSA# is asserted
10) Signal propagated to CTSB# input
11) Data bytes resume transmitting on TXB

Figure 6: Auto RTS and CTS Flow Control Operation

Automatic DTR/DSR Hardware Flow Control

Auto DTR/DSR hardware flow control behaves the same as the Auto RTS/CTS hardware flow control described above except that it uses the DTR# and DSR# signals. GPIO2 and GPIO3 become DSR# and DTR#, respectively, when the GPIO_MODE register is configured for DTR/DSR hardware flow control.

Automatic XON/XOFF Software Flow Control

When software flow control is enabled, the XR21B1424 compares the receive data characters with the programmed XON or XOFF characters. If the received character matches the programmed XOFF character, the XR21B1424 will halt transmission as soon as the current character has completed transmission. Data transmission is resumed when a received character matches the XON character.

In the receive data direction, the XOFF character will be sent when there are 450 bytes in the receive FIFO. When there are again less than 450 bytes in the RX FIFO, the XON character will be sent. This threshold may be changed using the RX_THRESHOLD register.

Software flow control is enabled / disabled by the FLOW_CONTROL register. Additionally, the XON_CHAR and XOFF_CHAR registers may be used to configure the start (XON) and stop (XOFF) characters.

Multidrop mode with address matching

The XR21B1424 device has two address matching modes which are set by the FLOW_CONTROL and GPIO_MODE registers. These modes are intended for use in a multi-drop network application. Address matching may be used with any size data character, as well as with and without parity. An address match occurs when the last (most significant) received data bit or the parity bit, if there is one, is a '1' and the address matches the value stored in either the XON_CHAR or XOFF_CHAR register. To send an address byte use 5, 6, 7, 8 or 9 bit data with either the most significant data bit a '1' or if parity is used, set mark parity. To send data bytes, the most significant data bit must be a '0' or use space parity.

Receiver

If an address match occurs in either of the address matching modes, the address byte and all subsequent data bytes will be loaded into the RX FIFO. The UART Receiver will automatically be disabled when an address byte is received that does not match the values in the XON_CHAR or XOFF_CHAR characters.

Transmitter

In flow control mode 3, the UART transmitter will transmit irrespective of the RX address match. In flow control mode 4, the UART will only transmit following an RX address match.

Programmable Turn-Around Delay

By default, the selected RS-485 half-duplex enable pin (either GPIO7/RS485 or GPIO5/RTS#/RS485) will be de-asserted immediately after the stop bit of the last byte has been shifted. However, this may not be ideal for systems where the signal needs to propagate over long cables. Therefore, the de-assertion of the RS-485 half-duplex enable can be delayed from 1 to 15 bit times via the XCVR_EN_DELAY register to allow for the data to reach distant UARTs.

UART Half-Duplex Mode

In UART half-duplex mode, the UART will ignore any data on the RX input when the UART is transmitting data. The half-duplex mode can be configured using the FLOW_CONTROL register.

IR Mode

The XR21B1424 supports IR mode at a maximum baud rate of 2.5 Mbaud with transmit pulses of 3/16th or 4/16th of a bit period and centered in the bit period. Receive data may be inverted to conform to some manufacturer's non-standard devices. IR mode is disabled by default but may be enabled by the IR_MODE register.

USB_STAT Pins

The XR21B1424 has two USB_STAT output pins that may be used to indicate 3 different statuses in either positive or negative polarity. The SUSPEND status indicates that the XR21B1424 device has been placed into a suspended state by the USB host. This output can then be used by external circuitry, for example, to power down devices in order to meet USB requirements for suspend mode. The LOW_POWER status is similar to the SUSPEND status, but LOW_POWER is also asserted for high power devices (any device that consumes more than 100 mA of VBUS power from the USB host), before the device is configured during enumeration by the USB host. For low power devices (devices that consume 100 mA or less of VBUS power), SUSPEND and LOW_POWER status outputs are functionally the same. Lastly, the BUS_RST output status is asserted any time the XR21B1424 device is being reset by the USB host. This status output could be used, for example, by an FPGA or other logic device to synchronize this external logic with the XR21B1424 device.

Suspend Mode Settings

The USE_SUSPEND bit controls the GPIO pins when the XR21B1424 device is suspended by the USB host. If USE_SUSPEND is cleared to '0', the GPIO pins retain their output states when the device is suspended. When USE_SUSPEND is set to '1', the GPIO pin's behavior is defined by the SUSPEND_STATE and SUSPEND_MODE registers, with the following exceptions: GPIO0/CLK when configured as an output clock will always be driven low, i.e the clock output will stop, and GPIO1/RTS#/RS485 or GPIO3/RS485 when configured as auto. RS-485 half-duplex enable will always be de-asserted.

Note that USE_SUSPEND does not affect the UART RX and TX pins. During suspend state, RX and TX will always idle to a logic ’1’ state.

The SUSPEND_STATE field will set or clear the GPIO pins and the SUSPEND_MODE field will configure GPIO outputs as either open drain or push-pull outputs. SUSPEND_STATE and SUSPEND_MODE may be configured through registers or OTP. As opposed to OTP configuration, register configurations are not retained if the power is lost or the bus is reset.

TXT and RXT Pins

The Transmit toggle and Receive toggle pins "toggle" at a rate of approximately 10 Hz whenever the UART transmit and receive pins (respectively) are active.

OTP

The OTP is an on-chip non-volatile memory, that is incrementally one-time programmable via the USB interface. Some bits are pre-programmed at the factory and caution must be taken not to program any locations except those user defined addresses given in this data sheet. Once a specific portion of the OTP is programmed, the PROG bit for that section of the OTP must be set and further changes to that section will not be allowed.

USB Control Commands

The following table shows all of the USB Control Commands that are supported by the XR21B1424. Commands include standard USB commands, CDC-ACM commands and MaxLinear vendor specific commands. The device internal registers are accessed using the vendor specific XR_GET_REG and XR_SET_REG, XR_GET_REVISION, XR_GET_USB_STAT and XR_SET_USB_STAT vendor specific commands.

Table 4: Supported USB Control Commands

Name	Request Type	Request	Value		Index		Length		Description
			LSB	MSB	LSB	MSB	LSB	MSB	
DEV GET_STATUS	0x80	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Device: remote wake-up + self-powered
IF GET_STATUS	0x81	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Interface: zero
EP GET_STATUS	0x82	0x0	0x0	0x0	0x0,0x4, 0x84	0x0	0x2	0x0	Endpoint: halted
DEV CLEAR_FEATURE	0x00	0x1	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP CLEAR_FEATURE	0x02	0x1	0x0	0x0	0x0,0x4, 0x84	0x0	0x0	0x0	Endpoint halt
DEV SET_FEATURE	0x00	0x3	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP SET_FEATURE	0x02	0x3	0x0	0x0	0x0,0x4, 0x84	0x0	0x0	0x0	Endpoint halt
SET_ADDRESS	0x00	0x5	addr	0x0	0x0	0x0	0x0	0x0	addr = 1 to 127
GET_DESCRIPTOR	0x80	0x6	0x0	0x1	0x0	0x0	len MSB	len MSB	Device descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x2	LangID	LangID	len MSB	len MSB	Configuration descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x3	0x0	0x0	len MSB	len MSB	String descriptor
GET_CONFIGURATION	0x80	0x8	0x0	0x0	0x0	0x0	0x1	0x0	
SET_CONFIGURATION	0x00	0x9	n	0x0	0x0	0x0	0x0	0x0	n = 0, 1
GET_INTERFACE	0x81	0x10	0x0	0x0	0x0	0x0	0x1	0x0	
CDC_ACM_IF SET_LINE_CODING	0x21	0x20	0x0	0x0	Chan #	0x0	0x7	0x0	Set the UART baud rate, parity, stop bits, etc. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.
CDC_ACM_IF GET_LINE_CODING	0xA1	0x21	0x0	0x0	Chan #	0x0	0x7	0x0	Get the UART baud rate, parity, stop bits, etc. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.
CDC_ACM_IF SET_CONTROL_ LINE_STATE	0x21	0x22	0x0	0x0	Chan #	0x0	0x7	0x0	Set/Clear DTR in CDC-ACM mode. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.

Table 4: Supported USB Control Commands

Name	Request Type	Request	Value		Index		Length		Description
			LSB	MSB	LSB	MSB	LSB	MSB	
CDC_ACM_IF SEND_BREAK	0x21	0x23	val LSB	val MSB	Chan #	0x0	0x0	0x0	Send a break for the specified duration. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.
XR_GET_CHIP_ID	0xC0	0xFF	0x0	0x0	0x0	0x0	0x6	0x0	Get MaxLinear VID (2 bytes), PID (2 bytes) and bcdDevice (2 bytes)
XR_SET_REG See Table 5	0x41	0x0	write-data LSB	write-data MSB	write addr	Chan #	0x0	0x0	Vendor specific register access. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.
XR_GET_REG See Table 5	0xC1	0x0	0x0	0x0	read addr	Chan #	0x2	0x0	Vendor specific register access. Channel #0, 2, 4, 6 for channel A, B, C, D, respectively.
XR_GET_REVISION See Table 5	0xC0	0x0	0x0	0x0	0x60	0x02	0x2	0x0	Vendor specific register access.
XR_GET_USB_STAT See Table 5	0x40	0x0	write-data LSB	write-data MSB	0x62	0x02	0x0	0x0	Vendor specific register access.
XR_SET_USB_STAT See Table 5	0xC0	0x0	0x0	0x0	0x62	0x02	0x2	0x0	Vendor specific register access.

Register Set Description

The internal register set of the XR21B1424 controls the UART channel functionality, basic functionality of the FIFOs, OTP controls, as well as registers associated with the processing of driver commands. All registers are accessible via the USB interface using the XR_SET_REG and XR_GET_REG USB commands, except for the REVISION_ID and USB_STAT registers which are accessible with the XR_GET_REVISION and XR_GET/SET_USB_STAT commands respectively. Note that the UART_ENABLE register should be used to disable the UART prior to any register write and re-enable the UART following any single or sequence of register writes except for the GPIO_SET, GPIO_CLEAR, TX_BREAK and ERROR_STATUS registers.

All registers are 16 bits wide. The upper byte of single byte registers as well as bit locations with field label of '0' in Table 5 are reserved. All reserved bits must be written as zeroes when modifying register contents.

Table 5: XR21B1424 Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x000	UART_ENABLE	0	0	0	0	0	0	RX	TX
0x006	FLOW_CONTROL	0	0	0	0	Half-Duplex	Flow Control Mode Select		
0x007	XON_CHAR	VALUE							
0x008	XOFF_CHAR	VALUE							
0x009	ERROR_STATUS	Break Status	Overrun Error	Parity Error	Framing Error	Break Error	0	0	0
0x00A	TX_BREAK[15:8]	VALUE (MSB)							
	TX_BREAK[7:0]	VALUE (LSB)							
0x00B	XCVR_EN_DELAY	0	0	0	0	Delay			
0x00C	GPIO_MODE[15:8]	0	0	0	0			RXT_EN	TXT_EN
	GPIO_MODE[7:0]	CLK_EN	RS485_SEL		XCVR Enable Pin	XCVR Enable Polarity	Mode Select		
0x00D	GPIO_DIRECTION[15:8]	0	0	0	0	0	0	GPIO9	GPIO8
	GPIO_DIRECTION[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x00E	GPIO_SET[15:8]	0	0	0	0	0	0	GPIO9	GPIO8
	GPIO_SET[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x00F	GPIO_CLEAR[15:8]	0	0	0	0	0	0	GPIO9	GPIO8
	GPIO_CLEAR[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x010	GPIO_STATE[15:8]	0	0	0	0	TX	RX	GPIO9	GPIO8
	GPIO_STATE[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x011	GPIO_INT_MASK[15:8]	0	0	0	0	0	RX	GPIO9	GPIO8
	GPIO_INT_MASK[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x012	CUSTOMIZED_INT	0	0	0	0	0	0	INT_ BREAK_ NEG	EN

Table 5: XR21B1424 Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x013	PIN_OPEN_DRAIN[15:8]	0	0	0	0	TX	0	GPIO9	GPIO8
	PIN_OPEN_DRAIN[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x014	PIN_PULLUP_EN[15:8]	0	0	0	0	0	RX	GPIO9	GPIO8
	PIN_PULLUP_EN[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x015	PIN_PULLDOWN_EN[15:8]	0	0	0	0	0	RX	GPIO9	GPIO8
	PIN_PULLDOWN_EN[7:0]	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x016	LOOPBACK	0	0	0	0	0	DTR_ DSR	RTS_ CTS	TX_ RX
0x017	IR_MODE	0	0	0	0	0	TX_- PULSE	RX_I NVERT	EN
0x018	OUTCLK[15:8]	DIV_HI							
	OUTCLK[7:0]	DIV_LO							
0x01F	REMOTE_WAKE	0	0	0	0	RX_EN	RI_EN	0	0
0x040	TX_FIFO_FLUSH	0	0	0	0	0	AUTO_- CLOSE	AUTO_ OPEN	RESET
0x041	TX_FIFO_COUNT[15:8]	0	0	0	0	0	0	COUNT[9:8]	
	TX_FIFO_COUNT[7:0]	COUNT[7:0]							
0x042	TX_WIDE_MODE	0	0	0	0	0	0	0	EN
0x043	RX_FIFO_FLUSH	0	0	0	0	0	AUTO_- CLOSE	AUTO_ OPEN	RESET
0x044	RX_FIFO_COUNT[15:8]	0	0	0	0	0	0	COUNT[9:8]	
	RX_FIFO_COUNT[7:0]	COUNT[7:0]							
0x045	RX_WIDE_MODE	0	0	0	0	0	0	0	EN
0x046	LOW_LATENCY	0	0	0	0	0	0	0	EN
0x047	RX_THRESHOLD[15:8]	0	0	0	0	0	0	COUNT[9:8]	
	RX_THRESHOLD[7:0]	COUNT[7:0]							
0x060	CUSTOM_DRIVER	0	0	0	0	0	0	0	ACTIVE
0x06A	SUSPEND_STATE[15:8]	0	0	DSR	DTR	RI	CD	0	0
	SUSPEND_STATE[7:0]	RXT	TXT	0	0	RS485	CTS	RTS	CLK
0x06B	SUSPEND_MODE[15:8]	USE_- SUS- PEND	0	DSR	DTR	RI	CD	0	0
	SUSPEND_MODE[7:0]	RXT	TXT	0	0	RS485	CTS	RTS	CLK
0x260	REVISION_ID[a]	VALUE							

Table 5: XR21B1424 Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x262	USB_STATUS[15:8][b]	0	0	STATE1	SEL1			CTRL1	
	USB_STATUS[7:0]	0	0	STATE0	SEL0			CTRL0	

a. The REVISION_ID register is accessed using XR_GET_REVISION.
b. The USB_STATUS registers are accessed using XR_SET_USB_STAT and XR_GET_USB_STAT.

XR21B1424 Register Descriptions

UART_ENABLE (0x000) - Read/Write

The UART transmitter and receiver must be disabled before writing to any other UART registers except for the GPIO_SET, GPIO_CLEAR, TX_BREAK and ERROR_STATUS registers.

Bit	Default	Description
15:2	0	**Reserved** These bits are reserved and should be written as '0'.
1	0	**Enable UART RX** 0: UART RX disabled 1: UART RX enabled
0	0	**Enable UART TX** 0: UART TX disabled 1: UART TX enabled

FLOW_CONTROL (0x006) - Read/Write

This register selects the flow control mode. This register should only be written to when the UART is disabled. Writing to the FLOW_CONTROL register when the UART is enabled will result in undefined behavior.

Bit	Default	Description
15:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**UART Half-Duplex Mode** 0: Normal (full-duplex) mode. The UART can transmit and receive data at the same time. 1: UART Half-Duplex Mode. In half-duplex mode, any data on the RX pin is ignored when the UART is transmitting data.
2:0	0	**Mode** 000: Mode 0. No flow control, no address matching. 001: Mode 1. HW flow control enabled. Auto RTS/CTS or DTR/DSR must be selected by GPIO_MODE. 010: Mode 2. SW flow control enabled. 011: Mode 3. Multidrop mode - RX only after address match, TX independent. (Typically used with GPIO_MODE 3). 100: Mode 4. Multidrop mode - RX/TX only after address match. (Typically used with GPIO_MODE 4). 101 to 111: Reserved

XON_CHAR (0x007) - Read/Write

The XON_CHAR stores the 5 through 8 bit XON character that is used for Automatic Software Flow control. In 9 bit mode, only bits 7 through 0 are used, i.e. bit 8 is always a '0'. Alternately, this register holds the unicast address for multi-drop applications with address matching mode.

Bit	Default	Description
15:8	0	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x11	**XON Character** In Automatic Software Flow control mode, the UART will suspend data transmission when the XON character has been received. For behavior in the address match mode, see "Multidrop mode with address matching" on page 18.

XOFF_CHAR (0x008) - Read/Write

The XOFF_CHAR stores the 5 through 8 bit XOFF character that is used for Automatic Software Flow control. In 9 bit mode, only bits 7 through 0 are used, i.e. bit 8 is always a '0'. Alternately, this register holds the multicast address for multi-drop applications with address matching mode.

Bit	Default	Description
15:8	0	**Reserved** These bits are reserved and should be written as '0'.
7:0	0x13	**XOFF Character** In Automatic Software Flow control mode, the UART will suspend data transmission when the XOFF character has been received. For behavior in the address match mode, see "Multidrop mode with address matching" on page 18.

ERROR_STATUS (0x009) - Read-Clear

This register reports any historical break status, or framing, parity and overrun errors since the last time this register was read. As such, it does not indicate which character(s) the error(s) were associated with. For diagnostic purposes, WIDE_MODE may be enabled such that errors are directly associated with the current byte.

Bit	Default	Description
15:8	0	**Reserved** These bits are reserved and should be written as '0'.
7	0	**Break Status (Read-Only)** 0: Break condition is not present. 1: Break condition is currently being detected.
6	0	**Overrun Error** 0: No overrun error. 1: An overrun error has been detected (clears after read). An overrun error occurs when the RX FIFO is full and another byte of data is received.
5	0	**Parity Error** 0: No parity error. 1: A parity error has been detected (clears after read).

Bit	Default	Description
4	0	**Framing Error** 0: No framing error. 1: A framing error has been detected (clears after read). A framing error occurs when a stop bit is not present when it is expected.
3	0	**Break Error** 0: No break condition. 1: A break condition has been detected (clears after read).
2:0	0	**Reserved** These bits are reserved and should be written as '0'.

TX_BREAK (0x00A) - Read/Write

This register controls UART TX break signaling.

Bit	Default	Description
15:0	0	**Value** For value TX_BREAK value of N: If N == 0xFFFF, the UART TX outputs a continuous break signal. If 0x0000 < N < 0xFFFF (a maximum of 64,534 ms), the UART TX outputs a break signal that lasts N ms, and the register serves as a counter, counting down to 0, decrementing by 1 every millisecond. If N == 0x0000, the UART TX stops sending the break signal. When the user writes to this register, any previous process is terminated, and the new command takes effect. If data is being shifted out of the TX pin, the data will be completely shifted out before the break condition is generated. NOTE: After this register is programmed from 0x0000 to a non-zero value, the UART TX may take up to, but no more than 1 ms, before sending out the break condition. In addition, after the break counter decrements to zero, the UART TX may take up to, but no more than 2 UART characters, based on the current UART configuration, before stopping the break. Thus, the actual break length may be slightly longer than the programmed value, by up to, but no more than (1ms + 2x UART-character-length).

XCVR_EN_DELAY (0x00B) - Read/Write

Bit	Default	Description
15:4	0	**Reserved** These bits are reserved and should be written as '0'.
3:0	0	**Turn-around delay** Turn-around delay controls the number of bit times (0-15) to wait before changing the direction of the RS-485 half-duplex from transmit to receive when auto RS-485 half-duplex control is enabled. This allows for propagation of characters to complete across lengthy mediums.

GPIO_MODE (0x00C) - Read/Write

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be written as '0'.
9	1	**Receive Toggle** 0: GPIO9 is used for general purpose I/O 1: GPIO9 is used to receive toggle output (default).
8	1	**Transmit Toggle** 0: GPIO8 is used for general purpose I/O. 1: GPIO8 is used to transmit toggle output (default).
7	0	**Clock Enable** 0: GPIO6 is used for general purpose I/O 1: GPIO6 is used to output a clock. See "OUTCLK (0x018) - Read/Write" on page 35.
6:5	0	**Auto RS-485 Half-Duplex Select** 00: GPIO. GPIO7/RS485 is used for general purpose I/O 01: RS485_EN_ACT. GPIO7/RS485 is used for auto RS-485 half-duplex enable. Asserted whenever the UART is transmitting 10: RS485_EN_FLOW. GPIO7/RS485 is used for auto RS-485 half-duplex enable. Asserted for the duration of the address match 11: RESERVED. Reserved value, do not use
4	0	**Auto RS-485 Half-Duplex Pin** 0: GPIO5/RTS#/RS485 function is selected by GPIO_MODE[2:0]. GPIO7/RS485 function is GPIO. 1: GPIO7/RS485 function is selected by GPIO_MODE[6:5]. GPIO5/RTS#/RS485 function must be any function other than that selected for GPIO7/RS485.
3	0	**Auto RS-485 Half-Duplex Polarity** 0: Active low auto. RS-485 half-duplex enable 1: Active high auto. RS-485 half-duplex enable
2:0	0	GPIO Mode Select 000: GPIO. RTS/CTS and DTR/DSR are used for general purpose I/O. 001: RTS_CTS. GPIO4 and GPIO5 used for Auto RTS/CTS HW Flow Control 010: DTR_DSR. GPIO2 and GPIO3 used for Auto DTR/DSR HW Flow Control 011: RS485_EN_ACT. GPIO5/RTS#/RS485 pin used for auto .RS-485 half-duplex enable during Transmit 100: RS485_EN_FLOW. GPIO5/RTS#/RS485 pin used for auto RS-485 half-duplex enable after address match. 101 to 111: Reserved. Reserved value, do not use.

GPIO_DIRECTION (0x00D) - Read/Write

This register controls the direction of pins that are configured as GPIO. Pins that are configured for alternate functions via the GPIO_MODE register are not controlled by this register.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be '0'.
9:0	0	**GPIO Direction of GPIO[9:0]** 0: GPIOx is an input. 1: GPIOx is an output.

GPIO_SET (0x00E) - Write-Only

This register controls pins configured as GPIO outputs. Pins configured for alternate functions via the GPIO_MODE register are not controlled by this register. Writing a ’1’ to a bit position in this register sets the corresponding GPIO output high. Writing a ’0’ to a bit has no effect. For GPIO pins configured as inputs via the GPIO_DIRECTION register, this register has no effect.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be ‘0’.
9:0	0	**GPIO Set of GPIO[9:0]** 0: No effect on GPIOx pin. 1: GPIOx output is set to a ’1’.

GPIO_CLEAR (0x00F) - Write-Only

This register controls pins configured as GPIO outputs. Pins configured for alternate functions via the GPIO_MODE register are not controlled by this register. Writing a ’1’ to a bit position in this register clears the corresponding GPIO output low. Writing a ’0’ to a bit has no effect. For GPIO pins configured as inputs via the GPIO_DIRECTION register, this register has no effect.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be ‘0’.
9:0	0	**GPIO Set of GPIO[9:0]** 0: No effect on GPIOx pin. 1: GPIOx output is cleared to a ’0’.

GPIO_STATE (0x010) - Read/Write

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be ‘0’.
9:0	0	**GPIO State of GPIO[9:0]** Read returns state of all pins, whether GPIO or alternate function, input or output 0: Write clears the respective GPIO output to a ’0’ 1: Write sets the respective GPIO output to a ’1’

GPIO_INT_MASK (0x011) - Read/Write

This register is used to configure whether a change in pin state causes the device to generate a USB interrupt packet. Note that the GPIO status register will still report the GPIO pin state when read, and if an interrupt packet is formed due to other interrupt trigger, the interrupt packet will contain the current state of the pin. This register applies to all inputs pins irrespective of if they are configured as GPIO or alternate functions.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be written as '0'.
9:0	0x100	**GPIO Interrupt Mask of GPIO[9:0]** 0: A change in the input pin's state causes the device to generate an interrupt packet 1: A change in the input pin's state does not cause the device to generate an interrupt packet

CUSTOMIZED_INT (0x012) - Read/Write

This register enables the customized interrupt packet format that will report all GPIO pin status in the interrupt packet.

Bit	Default	Description
15:2	0	**Reserved** These bits are reserved and should be written as '0'.
1	0	**Break Interrupt Enable** 0: No interrupt is generated when break character is received. 1: Interrupt is generated when break character is received.
0	0	**Enable** 0: Use standard interrupt packet. See Table 6. 1: Use customized interrupt packet. See Table 8.

Table 6: Standard Interrupt Packet Format

Offset	Field	Size (Bytes)	Value	Description
0	bmRequestType	1	8'b10100001	D7 = Device-to-host direction D6:5 = Class Type D4:0 = Interface Recipient
1	bNotification	1	8'h20	Defined encoding for SERIAL_STATE
2	wValue	2	16'h0000	
4	wIndex	2	16'h0000	D15:8 = Reserved (0) D7:0 = Interface number, 8'h00 for the CDC Command Interface
6	wLength	2	16'h0002	2 bytes of transferred data
8	Data	2	Standard int_status See Table 7	D15-7 = Reserved (0) D6 = bOverRun D5 = bParity D4 = bFraming D3 = bRingSignal (RI) D2 = bBreak D1 = bTxCarrier (DSR) D0 = bRxCarrier (CD)

Table 7: Data Field of Standard Interrupt Packet

Bit	Field	Description
D15:7		Reserved (future use)
D6	bOverRun	Received data has been discarded due to overrun in the device.
D5	bParity	A parity error has occurred.
D4	bFraming	A framing error has occurred.
D3	bRingSignal	State of ring signal detection of the device.
D2	bBreak	State of break detection mechanism of the device.
D1	bTxCarrier	State of transmission carrier. This signal corresponds to V.24 signal 106 and RS-232 signal DSR.
D0	bRxCarrier	State of receiver carrier detection mechanism of device. This signal corresponds to V.24 signal 109 and RS-232 signal DCD.

If the MaxLinear vendor specific packet mapping is enabled then the interrupt packet format is as shown in Table 8.

Table 8: Customized Interrupt Packet Format

Offset	Field	Size (Bytes)	Value	Description
0	GPIO_STATE	2		Byte 0: GPIO_STATE[7:0] Byte 1: GPIO_STATE[9:8]
2	GPIO_INT	2		Byte 2: GPIO_INT[7:0] Byte 3: GPIO_INT[9:8]
4	Data	1		D15:4 = Reserved (0) D3 = Overrun Error D2 = Parity Error D1 = Frame Error D0 = Break Status

PIN_OPEN_DRAIN (0x013) - Read/Write

This register controls all pins configured as outputs irrespective of if they are configured as GPIO or alternate functions.

Bit	Default	Description
15:12	0	**Reserved** These bits are reserved and should be written as '0'.
11	0	**UART TX** 0: TX Pin is push-pull output 1: TX Pin pin is open drain output
10	0	**Reserved** These bits are reserved and should be written as '0'.
9:8	0	**Pin Open Drain on GPIO[9:8]** 0: Pin configured as output is push-pull output 1: Pin configured as output is open drain output
7	1	**Pin Open Drain on GPIO7/RS485** 0: Pin configured as output is push-pull output 1: Pin configured as output is open drain output
6:0	0	**Pin Open Drain on GPIO[6:0]** 0: Pin configured as output is push-pull output 1: Pin configured as output is open drain output

PIN_PULLUP_EN (0x014) - Read/Write

This register controls all pins configured as inputs irrespective of if they are configured as GPIO or alternate functions.

Bit	Default	Description
15:11	0	**Reserved** These bits are reserved and should be written as '0'.
10	1	**RX** 0: Disable pull-up on the RX pin 1: Enable pull-up on the RX pin. If both pull-up and pull-down resistors are selected, only the pull-up will be enabled.
9:0	0x3FF	**Pin Pull-up Enable on GPIO[9:0]** 0: Disable pull-up on the corresponding input pin 1: Enable pull-up on the corresponding input pin. If both pull-up and pull-down resistors are selected for a given GPIO, only the pull-up will be enabled.

PIN_PULLDOWN_EN (0x015) - Read/Write

This register controls all pins configured as inputs irrespective of if they are configured as GPIO or alternate functions.

Bit	Default	Description
15:11	0	**Reserved** These bits are reserved and should be written as '0'.
10	0	**RX** 0: Disable pull-down on the RX pin 1: Enable pull-down on the RX pin. If both pull-up and pull-down resistors are selected, only the pull-up will be enabled.
9:0	0	**Pin Pull-down Enable on GPIO[9:0]** 0: Disable pull-down on the corresponding input pin 1: Enable pull-down on the corresponding input pin. If both pull-up and pull-down resistors are selected for a given GPIO, only the pull-up will be enabled.

LOOPBACK (0x016) - Read/Write

This register is used to configure the internal UART loopback.

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as '0'.
2	0	**DTR_DSR** When this bit is set, DTR is looped back to DSR. 0: Disable loopback. 1: Enable loopback.
1	0	**RTS_CTS** When this bit is set, RTS is looped back to CTS. 0: Disable loopback. 1: Enable loopback.
0	0	**TX_RX** When this bit is set, all transmitted UART data is internally looped back to the UART receiver. Note that when internal loop-back is enabled, external TX data will be disabled and RX data will be ignored. 0: Disable loopback. 1: Enable loopback.

IR_MODE (0x017) - Read/Write

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as '0'.
2	0	**TX_PULSE** This bit controls the pulse width of the TX data 0: TX pulse width is 3/16th of the bit period 1: TX pulse width is 4/16th of the bit period
1	0	**RX_INVERT** This bit inverts the RX data for IR devices that do not conform to standard. 0: RX data is not inverted 1: RX data is inverted
0	0	**EN** This register bit is used to enable the infrared (IR) mode. 0: Disable IR mode. 1: Enable IR mode.

OUTCLK (0x018) - Read/Write

This register is used to set the output clock frequency and duty cycle.

Bit	Default	Description
15:8	0	**DIV_HI** Sets the high period of the clock in intervals of 41.67 ns.
7:0	0	**DIV_LO** Sets the low period of the clock in intervals of 41.67 ns.

REMOTE_WAKE (0x01F) - Read/Write

This register is used to configure the remote wakeup feature.

Bit	Default	Description
15:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**RX_EN** 0: The XR21B1424 device is not sensitive to RX pin for remote wakeup 1: A high to low transition on the RX pin signals a remote wakeup event to the XR21B1424 device if the RX pin is configured as an input.
2	1	**RI_EN** 0: The XR21B1424 device is not sensitive to the RI#/RWK# pin for remote wakeup. 1: A high to low transition on the RI#/RWK# pin signals a remote wakeup event to the XR21B1424 device if the RI#/RWK# pin is configured as an input.
1:0	0	**Reserved** These bits are reserved and should be written as '0'.

TX_FIFO_FLUSH (0x040) - Write Only

This register is used to flush the transmit FIFO.

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as '0'.
2	0	**AUTO_CLOSE** 0: No effect on the TX FIFO when the UART port TX is disabled 1: The TX FIFO is automatically flushed when the UART port TX is disabled
1	1	**AUTO_OPEN** 0: No effect on the TX FIFO when the UART port TX is enabled 1: The TX FIFO is automatically flushed when the UART port TX is enabled
0	0	**Reset** 0: No effect on the TX FIFO 1: Resets the TX FIFO, self-clearing

TX_FIFO_COUNT (0x041) - Read Only

This register is used to read the number of bytes currently in the transmit FIFO.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be written as '0'.
9:0	0	**Count** Reports the number of bytes currently in the TX FIFO.

TX_WIDE_MODE (0x042) - Read/Write

This register is used to enable the Wide Mode for the Transmitter.

Bit	Default	Description
15:1	0	**Reserved** These bits are reserved and should be written as '0'.
0	0	**Enable** 0: Normal (5, 6, 7, 8 or 9 bit data) mode 1: Wide mode

RX_FIFO_FLUSH (0x043) - Write Only

This register is used to flush the receive FIFO.

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as '0'.
2	0	**AUTO_CLOSE** 0: No effect on the RX FIFO when the UART port RX is disabled 1: The RX FIFO is automatically flushed when the UART port RX is disabled
1	1	**AUTO_OPEN** 0: No effect on the RX FIFO when the UART port RX is enabled 1: The RX FIFO is automatically flushed when the UART port RX is enabled
0	0	**Reset** 0: No effect on the RX FIFO 1: Resets the RX FIFO, self-clearing

RX_FIFO_COUNT (0x044) - Read Only

This register is used to read the number of bytes currently in the receive FIFO.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be written as '0'.
9:0	0	**Count** Reports the number of bytes currently in the RX FIFO.

RX_WIDE_MODE (0x045) - Read/Write

This register is used to enable the Wide Mode for the Receiver.

Bit	Default	Description
15:1	0	**Reserved** These bits are reserved and should be written as '0'.
0	0	**EN** 0: Normal (5, 6, 7, 8 or 9 bit data) mode 1: Wide mode. See "Wide Mode Transmit" on page 14, "Wide mode receive operation with 5, 6, 7 or 8-bit data" on page 15 and "Wide mode receive operation with 9-bit data" on page 15.

LOW_LATENCY (0x046) - Read/Write

This register is automatically set to logic '1' for baud rates below 40,960 bps when using the CDC-ACM driver. A custom driver can also automatically enable low latency mode based upon the selected baud or the user may manually enable it by writing to this register.

Bit	Default	Description
15:1	0	**Reserved** These bits are reserved and should be written as '0'.
0	0	**EN** 0: Data from the RX FIFO is not immediately forwarded to the USB host following the bulk-in request until bMaxPacketSize (normally 64 bytes) bytes have been received or a timeout period (of 3 character times) has been reached. (Note: When the CDC-ACM driver is used, bMaxPacketSize is 63 bytes.) 1: Receive data is forwarded from RX FIFO immediately following the bulk-in request.

RX_THRESHOLD (0x047) - Read/Write

This register sets the threshold for asserting flow control when enabled in the UART. This register applies to both hardware and software flow control.

Bit	Default	Description
15:10	0	**Reserved** These bits are reserved and should be written as '0'.
9:0	0x1C2	**Count** Hardware or software flow control is asserted when the RX_FIFO reaches the threshold count set in this register. Default value for this register is 450 or 0x1C2.

CUSTOM_DRIVER (0x060) - Write Only

This register determines which device driver is used (custom or CDC driver). For proper operation, a custom driver must set the ACTIVE bit prior to sending any of the 4 CDC_ACM commands supported by the XR21B1424.

Bit	Default	Description
15:1	0	**Reserved** These bits are reserved and should be written as '0'.
0	0	**Active** 0: Informs the XR21B1424 that the standard CDC_ACM driver is being used. 1: Informs the XR21B1424 that a custom driver is being used.

SUSPEND_STATE (0x6A) - Read/Write

This register is used to set the state of GPIO pins based on the setting of the USE_SUSPEND bit in the SUSPEND_MODE register.

Bit	Default	Description
15:14	0	**Reserved** These bits are reserved and should be written as '0'.
13	0	**DSR** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
12	0	**DTR** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
11	0	**RI** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1"
10	0	**CD** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1"
9:8	0	**Reserved** These bits are reserved and should be written as '0'.

Bit	Default	Description
7	0	**RXT** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
6	0	**TXT** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
5:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**RS485** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
2	0	**CTS** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
1	0	**RTS** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'
0	0	**CLK** 0: When USE_SUSPEND is '1', clear this bit to a '0' 1: When USE_SUSPEND is '1', set this bit to a '1'

SUSPEND_MODE (0x06B) - Read/Write

Bit	Default	Description
15	0	**USE_SUSPEND** 0: GPIO pins will retain output state when device is suspended' 1: GPIO pins will assert state defined in SUSPEND_STATE and mode defined in SUSPEND_MODE when device is suspended.
14	0	**Reserved** This bit is reserved and should be written as '0'.
13	0	**DSR** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
12	0	**DTR** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
11	0	**RI** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
10	0	**CD** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
9:8	0	**Reserved** These bits are reserved and should be written as '0'.

Bit	Default	Description
7	0	**RXT** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
6	0	**TXT** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
5:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**RS485** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
2	0	**CTS** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
1	0	**RTS** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain
0	0	**CLK** 0: When USE_SUSPEND is '1', output will be actively driven 1: When USE_SUSPEND is '1', output will be open drain

REVISION_ID (0x260) - Read-Only

Bit	Default	Description
15:0	0	Revision ID

USB_STATUS (0x262) - Read-Write (except as noted)

Bit	Default	Description
15:14	0	**Reserved** These bits are reserved and should be written as '0'.
13	0	**STATE1 - Read only** Returns the current state of the USB_STAT2 pin.
12:10	0	**SEL1** 000: USB_STAT2 asserted high when in suspended state or when USB bus reset is asserted 001: USB_STAT2 asserted high when in suspended state 010: For low power device (<= 100 mA) USB_STAT2 asserted high when in suspended state. For high power device (101-500 mA) asserted high when in suspended state or when not yet configured. 011: USB_STAT2 asserted high when USB bus reset is asserted 100: USB_STAT2 asserted high when in suspended state or when USB bus reset is asserted 101: USB_STAT2 asserted low when in suspended state 110: For low power device (<= 100 mA) USB_STAT2 asserted low when in suspended state. For high power device (101-500 mA) asserted low when in suspended state or when not yet configured. 111: USB_STAT2 asserted low when USB bus reset is asserted

Bit	Default	Description
9:8	0x2	**CTRL1** 00: Invalid 01: USB_STAT2 open drain 10: USB_STAT2 actively driven 11: Invalid
7:6	0	**Reserved** These bits are reserved and should be written as '0'.
5	0	**STATE0 - Read only** Returns the current state of the USB_STAT1 pin.
4:2	0	**SEL0** 000: USB_STAT1 asserted low when in suspended state or when USB bus reset is asserted 001: USB_STAT1 asserted high when in suspended state 010: For low power device (<= 100 mA) USB_STAT1 asserted high when in suspended state. For high power device (101-500 mA) asserted high when in suspended state or when not yet configured. 011: USB_STAT1 asserted high when USB bus reset is asserted 100: USB_STAT1 asserted low when in suspended state or when USB bus reset is asserted 101: USB_STAT1 asserted low when in suspended state 110: For low power device (<= 100 mA) USB_STAT1 asserted low when in suspended state. For high power device (101-500 mA) asserted low when in suspended state or when not yet configured. 111: USB_STAT1 asserted low when USB bus reset is asserted
1:0	0x2	**CTRL0** 00: Invalid 01: USB_STAT1 open drain 10: USB_STAT1 actively driven 11: Invalid

OTP Map

Note that all OTP memory locations are 8 bits wide.

Table 9: XR21B1424 OTP Memory

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x000	HW_CONFIG	0	GLBL_ LOCK	Reserved					
0x007	CDC_ACM_OVERRIDES	0	0	0	BAUD_ THRESH	GPIO_ INT_ MASK	GPIO_ DIR	GPIO_ MODE	FLOW
0x008	CDC_ACM_FLOW	0	0	0	0	Half-Duplex	Mode Select		
0x009	CDC_ACM_MODE_LSB	CLK_EN	RS485_SEL		RS485_ PIN	RS485_ POL	Mode Select		
0x00A	CDC_ACM_MODE_MSB	0	0	0	0	0	0	RX_ TOG	TX_TOG
0x00B	CDC_ACM_GPIO_DIR_LSB	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x00C	CDC_ACM_GPIO_DIR_MSB	0	0	0	0	0	0	GPIO9	GPIO8
0x00D	CDC_ACM_GPI-O_INT_MASK_LSB	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x00E	CDC_ACM_GPI-O_INT_MASK_MSB	0	0	0	0	0	RX	GPIO9	GPIO8
0x00F	CDC_ACM_BAUD_THRESH_0	THRESH[7:0]							
0x010	CDC_ACM_BAUD_THRESH_1	THRESH[15:8]							
0x011	CDC_ACM_BAUD_THRESH_2	THRESH[23:16]							
0x012	VID_LSB	VALUE[7:0]							
0x013	VID_MSB	VALUE[15:8]							
0x014	PID_LSB	VALUE[7:0]							
0x015	PID_MSB	VALUE[15:8]							
0x016	USB_MAX_POWER	VALUE							
0x017	USB_ATTRIBUTES	0	0	0	0	RMT_ WAKE_ EN	RMT_ WAKE_ VALID	PWR_MODE	
0x018	RELEASE_MAJOR	VALUE							
0x019	RELEASE_MINOR	VALUE							
0x01A	AUTO_FLUSH	0	0	0	RX_ CLOSE	RX_ OPEN	TX_ CLOSE	TX_ OPEN	0
0x01D	PROG_BYTE_0	LANG_ ID	PIN_ CONFIG _UART3	PIN_ CONFIG _UART2	PIN_ CONFIG _UART1	PIN_ CONFIG _UART0	SER_ STRG	PROD_ STRG2	PROD_ STRG1
0x01E	PROG_BYTE_1	VEN_ STRNG2	VEN_ STRNG1	FLUSH	REL	USB_AT TRIB	MAX_ POWER	PID	VID

Table 9: XR21B1424 OTP Memory

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01F	PIN_CFG_USB_STAT1	0	0	0	SEL			CTRL	
0x020	PIN_CFG_USB_STAT2	0	0	0	SEL			CTRL	
0x024 /0x037 /0x04A /0x05D	PIN_CFG_CLK	PULLUP	PULL_ DOWN	0	0	0		CTRL	
0x025 /0x038 /0x04B /0x05E	PIN_CFG_RTS	PULLUP	PULL_ DOWN	0	0	0	CTRL		
0x026 /0x039 /0x04C /0x05F	PIN_CFG_CTS	PULLUP	PULL_ DOWN	0	0	0	0	CTRL	
0x027 /0x03A /0x04D /0x060	PIN_CFG_RS485	PULLUP	PULL_ DOWN	0	0	0	0	CTRL	
0x028 /0x03B /0x04E /0x061	PIN_CFG_TXT	PULLUP	PULL_ DOWN	0	0	0	0	CTRL	
0x029 /0x03C /0x04F 0x062	PIN_CFG_RXT	PULLUP	PULL_ DOWN	0	0	0	0	CTRL	
0x02A /0x03D /0x050 /0x063	PIN_CFG_CD	PULLUP	PULL_ DOWN	0	0	0	0	CTRL	
0x02B /0x03E /0x051 /0x064	PIN_CFG_RI	PULLUP	PULL_ DOWN	REM_ WAKE	0	0	0	CTRL	
0x02C /0x03F /0x052 /0x065	PIN_CFG_DTR	PULLUP	PULL_ DOWN	0	0	0	CTRL		
0x02D /0x040 /0x053 0x066	PIN_CFG_DSR	PULLUP	PULL_ DOWN		0	0	0	CTRL	
0x02E /0x041 /0x054 /0x067	PIN_CFG_DATA_PINS	PULLUP	PULL_ DOWN	RX_ REM_ WAKE	0	0	0	0	CTRL

Table 9: XR21B1424 OTP Memory

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F /0x042 /0x055 /0x068	SUSPEND_STATE (MSB)	0	0	DSR	DTR	RI	CD	0	0
0x030 /0x043 /0x056 /0x069	SUSPEND_STATE (LSB)	RXT	TXT	0	0	RS485	CTS	RTS	CLK
0x031 /0x044 /0x057 /0x06A	SUSPEND_MODE (MSB)	0	0	DSR	DTR	RI	CD	0	0
0x032 /0x045 /0x058 /0x06B	SUSPEND_MODE (LSB)	RXT	TXT	0	0	RS485	CTS	RTS	CLK
0x033 /0x046 /0x059 /0x06C	PIN_CFG_RS485_POL								POL
0x034 /0x047 /0x05A /0x06D	CLK_DIV	VALUE							

OTP Memory Descriptions

Some OTP locations will be pre-programmed at the factory. All OTP reset default values are ’0’ indicating that these bits have not been programmed. Conversely a ’1’ in any bit position indicates that bit has been previously programmed.

NOTE: If the Global Lock bit is set, all OTP programming will be disallowed. The contents of all fields, except the CDC_ACM overrides fields will not take effect unless the corresponding bit in the PROG_BYTE_LSB or PROG_BYTE_MSB registers have been set. Once that bit has been set, no further changes can be made to that field. CAUTION: Do not set the PROG bit for any field that has not had desired data entered, otherwise, the field will be programmed with all ’0’s. Programming of OTP memory locations will be reflected after power-up into respective registers.

HW_CONFIG (0x000) - Read/Write OTP

Bit	Default	Description
7	0	**Reserved** This bit is reserved and should remain ‘0’.
6	0	**Global Lock** 0: Global lock is not set 1: Global lock is set. All further writes to the OTP will be disallowed. Before setting the Global Lock bit, user must first set register 0x1898 to 0x10. Note that global lock does not take effect until the next hardware or power on reset.
5:0	0	**Reserved** Factory programmed - overwriting these bits may cause functional damage to the XR21B1424 device

CDC_ACM_OVERRIDES (0x007) - Read/Write OTP

CDC_ACM override registers 0x008 - 0x00E are not described here as the bit definitions are the same as in the equivalent register in Table 5.

Bit	Default	Description
7:5	0	**Reserved** These bits are reserved and should be written as ‘0’.
4	0	**BAUD_THRESHOLD** 0: Use default CDC-ACM 1: Override CDC-ACM baud rate threshold defaults with the values in the CDC_ACM_BAUD_THRESH registers
3	0	**GPIO_INT_MASK** 0: Use default CDC-ACM 1: Override CDC-ACM GPIO interrupt mask defaults with the values in the CDC_ACM_GPIO_INT_MASK register
2	0	**GPIO_DIRECTION** 0: Use default CDC-ACM 1: Override CDC-ACM GPIO direction defaults with the values in the CDC_ACM_DIR register
1	0	**GPIO_MODE** 0: Use default CDC-ACM 1: Override CDC-ACM GPIO mode defaults with the values in the CDC_ACM_GPIO_MODE register
0	0	**Flow** 0: Use default CDC-ACM flow control 1: Override CDC-ACM flow control defaults with the values in the CDC_ACM_FLOW register

CDC_ACM_FLOW (0x008) - Read/Write OTP

Bit	Default	Description
15:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**UART Half-Duplex Mode** 0: Normal (full-duplex) mode. The UART can transmit and receive data at the same time. 1: UART Half-Duplex Mode. In half-duplex mode, any data on the RX pin is ignored when the UART is transmitting data.
2:0	0	**Mode** 000: Mode 0. No flow control, no address matching. 001: Mode 1. HW flow control enabled. Auto RTS/CTS or DTR/DSR must be selected by GPIO_MODE. 010: Mode 2. SW flow control enabled. 011: Mode 3. Multidrop mode - RX only after address match, TX independent. (Typically used with GPIO_MODE 3). 100: Mode 4. Multidrop mode - RX/TX only after address match. (Typically used with GPIO_MODE 4). 101 to 111: Reserved

CDC_ACM_MODE_LSB (0x009) - Read/Write OTP

Bit	Default	Description
7	0	**Clock Enable** 0: GPIO6 is used for general purpose I/O 1: GPIO6 is used to output a clock.
6:5	0	**Auto RS-485 Half-Duplex Select** 00: GPIO. GPIO7/RS485 is used for general purpose I/O 01: RS485_EN_ACT. GPIO7/RS485 is used for auto RS-485 half-duplex enable. Asserted whenever the UART is transmitting 10: RS485_EN_FLOW. GPIO7/RS485 is used for auto RS-485 half-duplex enable. Asserted for the duration of the address match 11: RESERVED. Reserved value, do not use
4	0	**Auto RS-485 Half-Duplex Pin** 0: GPIO5/RTS#/RS485 function is selected by GPIO_MODE[2:0]. GPIO7/RS485 function is GPIO. 1: GPIO7/RS485 function is selected by GPIO_MODE[6:5]. GPIO5/RTS#/RS485 function must be any function other than that selected for GPIO7/RS485.
3	0	**Auto RS-485 Half-Duplex Polarity** 0: GPIO5/RTS#/RS485 function is selected by GPIO_MODE[2:0]. GPIO7/RS485 function is GPIO. 1: GPIO7/RS485 function is selected by GPIO_MODE[6:5]. GPIO5/RTS#/RS485 function must be any function other than that selected for GPIO7/RS485.
2:0	0	GPIO Mode Select 000: GPIO. RTS/CTS and DTR/DSR are used for general purpose I/O. 001: RTS_CTS. GPIO4 and GPIO5 used for Auto RTS/CTS HW Flow Control 010: DTR_DSR. GPIO2 and GPIO3 used for Auto DTR/DSR HW Flow Control 011: RS485_EN_ACT. GPIO5/RTS#/RS485 pin used for auto .RS-485 half-duplex enable during Transmit 100: RS485_EN_FLOW. GPIO5/RTS#/RS485 pin used for auto RS-485 half-duplex enable after address match. 101 to 111: Reserved. Reserved value, do not use.

CDC_ACM_MODE_MSB (0x00A) - Read/Write OTP

Bit	Default	Description
7:2	0	**Reserved** These bits are reserved and should be written as '0'.
1	1	**Receive Toggle** 0: GPIO9 is used for general purpose I/O 1: GPIO9 is used to receive toggle output (default).
0	1	**Transmit Toggle** 0: GPIO8 is used for general purpose I/O. 1: GPIO8 is used to transmit toggle output (default).

CDC_ACM_GPIO_DIR_LSB (0x00B) - Read/Write OTP

Bit	Default	Description
7:0	0	**GPIO Direction of GPIO[7:0]** 0: GPIOx is an input. 1: GPIOx is an output.

CDC_ACM_GPIO_DIR_MSB (0x00C) - Read/Write OTP

Bit	Default	Description
7:2	0	**Reserved** These bits are reserved and should be '0'.
1:0	0	**GPIO Direction of GPIO[9:8]** 0: GPIOx is an input. 1: GPIOx is an output.

CDC_ACM_GPIO_INT_MASK_LSB (0x00D) - Read/Write OTP

Bit	Default	Description
7:0	0x0	**GPIO Interrupt Mask of GPIO[7:0]** 0: A change in the input pin's state causes the device to generate an interrupt packet 1: A change in the input pin's state does not cause the device to generate an interrupt packet

CDC_ACM_GPIO_INT_MASK_MSB (0x00E) - Read/Write OTP

Bit	Default	Description
7:2	0	**Reserved** These bits are reserved and should be written as '0'.
1:0	0	**GPIO Interrupt Mask of GPIO[9:8]** 0: A change in the input pin's state causes the device to generate an interrupt packet 1: A change in the input pin's state does not cause the device to generate an interrupt packet

CDC_ACM_BAUD_THRES_0 (0x00F) - Read/Write OTP

Bit	Default	Description
7:0	0	**CDC_ACM_BAUD_THRES[7:0]** Least significant byte of the CDC_ACM baud rate threshold override for low latency mode.

CDC_ACM_BAUD_THRES_1 (0x010) - Read/Write OTP

Bit	Default	Description
7:0	0	**CDC_ACM_BAUD_THRES[15:8]** Second least significant byte of the CDC_ACM baud rate threshold override for low latency mode.

CDC_ACM_BAUD_THRES_2 (0x011) - Read/Write OTP

Bit	Default	Description
7:0	0	**CDC_ACM_BAUD_THRES[23:16]** Most significant byte of the CDC_ACM baud rate threshold override for low latency mode.

VID_LSB (0x012) - Read/Write OTP

Bit	Default	Description
7:0	0	**Vendor ID[7:0]** Least significant byte of the Vendor ID.

VID_MSB (0x013) - Read/Write OTP

Bit	Default	Description
7:0	0	**Vendor ID[15:8]** Most significant byte of the Vendor ID.

PID_LSB (0x014) - Read/Write OTP

Bit	Default	Description
7:0	0	**Product ID[7:0]** Least significant byte of the Product ID.

PID_MSB (0x015) - Read/Write OTP

Bit	Default	Description
7:0	0	**Product ID[15:8]** Most significant byte of the Product ID.

USB_MAX_POWER (0x016) - Read/Write OTP

Bit	Default	Description
7:0	0	**USB Max Power** The bMaxPower field of the device descriptor. Maximum device power consumption from VBUS power. Values from 0x01 (2 mA) to 0xFA (500 mA).

USB_ATTRIBUTES (0x017) - Read/Write OTP

Bit	Default	Description
7:4	0	**Reserved** These bits are reserved and should be written as '0'.
3	0	**REMOTE_WAKE_EN** This bit advertises if remote wakeup is enabled or disabled in D5 of bmAttributes field of the configuration descriptor if the REMOTE_WAKE_VALID bit is set. 0: Remote wakeup is disabled 1: Remote wakeup is enabled
2	0	**REMOTE_WAKE_VALID** This bit allows the remote wakeup setting in REMOTE_WAKE_EN to be advertised in D5 of the bmAttributes field of the configuration descriptor. 0: Do not advertise remote wakeup setting in REMOTE_WAKE_EN 1: Advertise remote wakeup setting in REMOTE_WAKE_EN
1:0	0	**POWER_MODE** This field determines power mode as reported in the configuration descriptor. 00: Bus powered mode 01: Self powered mode 10: Self powered mode 11: Invalid

RELEASE_MAJOR (0x018) - Read/Write OTP

Bit	Default	Description
7:0	0	Major Release

RELEASE_MINOR (0x019) - Read/Write OTP

Bit	Default	Description
7:0	0	Minor Release

AUTO_FLUSH (0x01A) - Read/Write OTP

This register controls whether the FIFO buffers are flushed on open and/or close events.

Bit	Default	Description
7:5	0	**Reserved** These bits are reserved and should be written as '0'.
4	0	**RX_CLOSE** 0: Do not automatically flush the RX FIFO 1: Automatically flush the RX FIFO when the COM port is closed

Bit	Default	Description
3	0	**RX_OPEN** 0: Do not automatically flush the RX FIFO 1: Automatically flush the RX FIFO when the COM port is opened
2	0	**TX_CLOSE** 0: Do not automatically flush the TX FIFO 1: Automatically flush the TX FIFO when the COM port is closed
1	0	**TX_OPEN** 0: Do not automatically flush the TX FIFO 1: Automatically flush the TX FIFO when the COM port is opened
0	0	**Reserved** This bit is reserved and should be written as '0'.

PROG_BYTE_0 (0x01D) - Read/Write OTP

Each bit field in the PROG_BYTE_0 register must be set by the user to indicate the corresponding field has been programmed. Any field that has been programmed can not be programmed again.

CAUTION: Do not set the PROG bit for any field that has not had the entire data field entered, otherwise, the empty field or any portion thereof will be programmed (all '0's) into the OTP.

For definitions of the individual fields, refer to the corresponding register definition in "XR21B1424 Register Map" on page 21.

Bit	Default	Description
7	0	**LANG_ID** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
6	0	**PIN_CFG_UART3** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
5	0	**PIN_CFG_UART2** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
4	0	**PIN_CFG_UART1** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
3	0	**PIN_CFG_UART0** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
2	0	**SERIAL_STRING** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
1	0	**PROD_STRING_2** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
0	0	**PROD_STRING_1** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.

PROG_BYTE_1 (0x01E) - Read/Write OTP

Each bit field in the PROG_BYTE_1 register must be set by the user to indicate the corresponding field has been programmed. Any field that has been programmed can not be programmed again.

CAUTION: Do not set the PROG bit for any field that has not had the entire data field entered, otherwise, the empty field or any portion thereof will be programmed (all '0's) into the OTP.

For definitions of the individual fields, refer to the corresponding register definition in "XR21B1424 Register Map" on page 21.

Bit	Default	Description
7	0	**VEND_STRING2** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
6	0	**VEND_STRING1** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
5	0	**FLUSH** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
4	0	**RELEASE** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
3	0	**USB_ATTRIBUTES** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
2	0	**MAX_POWER** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
1	0	**PID** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.
0	0	**VID** 0: Corresponding field has not been programmed. Values will not be read from OTP. 1: Corresponding field has been programmed. Values will be read from OTP.

PIN_CFG_USB_STAT1 (0x01F) - Read/Write OTP

Controls the configuration of the USB_STAT1 pin during suspend state

Bit	Default	Description
7:5	0	**Reserved** These bits are reserved and should be written as '0'.
4:2	0	**SEL** 000: Assert logic '1' during SUSPEND or USB BUS_RESET else logic '0' 001: Assert logic '1' during SUSPEND else logic '0' 010: Assert logic '1' during LOW_PWR else logic '0' 011: Assert logic '1' during USB BUS_RESET else logic '0' 100: Assert logic '1' during SUSPEND or USB BUS_RESET else logic '0' 101: Assert logic '0' during SUSPEND else logic '1' 110: Assert logic '0' during LOW_PWR else logic '1' 111: Assert logic '0' during USB BUS_RESET else logic '1'
1:0	0	**CTRL** 00: Invalid, do not use 01: Output, open drain 10: Output, push-pull 11: Invalid, do not use

PIN_CFG_USB_STAT2 (0x020) - Read/Write OTP

Controls the configuration of the USB_STAT2 pin during suspend state

Bit	Default	Description
7:5	0	**Reserved** These bits are reserved and should be written as '0'.
4:2	0	**SEL** 000: Assert logic '0' during SUSPEND or USB BUS_RESET else logic '1' 001: Assert logic '1' during SUSPEND else logic '0' 010: Assert logic '1' during LOW_PWR else logic '0' 011: Assert logic '1' during USB BUS_RESET else logic '0' 100: Assert logic '0' during SUSPEND or USB BUS_RESET else logic '1' 101: Assert logic '0' during SUSPEND else logic '1' 110: Assert logic '0' during LOW_PWR else logic '1' 111: Assert logic '0' during USB BUS_RESET else logic '1'
1:0	0	**CTRL** 00: Invalid, do not use 01: Output, open drain 10: Output, push-pull 11: Invalid, do not use

PIN_CFG_CLK (UART0: 0x024; UART1: 0x037; UART2: 0x04A; UART3: 0x05D) - Read/Write OTP

This register configures the functionality of the GPIO6/CLK pin.

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO6/CLK is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO6/CLK is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 00: GPIO6/CLK is configured as a GPIO input 01: GPIO6/CLK is configured as a GPIO open drain output 10: GPIO6/CLK is configured as a GPIO push-pull output 11: GPIO6/CLK is configured as a push-pull CLK output

PIN_CFG_RTS (UART0: 0x025; UART1: 0x038; UART2: 0x04B; UART3: 0x05E) - Read/Write OTP

This register configures the functionality of the GPIO5/RTS#/RS485 pin.

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO5/RTS#/RS485 is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO5/RTS#/RS485 is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:3	0	**RESERVED** These bits are reserved and should be written as '0'.
2:0	0	**CTRL** Note: If configured as RTS output, GPIO4/CTS# must be configured as CTS input and GPIO2/DSR# and GPIO3/DTR# must be configured as GPIOs. 000: GPIO5/RTS#/RS485 is configured as a GPIO input 001: GPIO5/RTS#/RS485 is configured as a GPIO open drain output 010: GPIO5/RTS#/RS485 is configured as a GPIO push-pull output 011: GPIO5/RTS#/RS485 is configured as a open drain RTS output 100: GPIO5/RTS#/RS485 is configured as a push-pull RTS output 101 to 111: invalid, do not use

PIN_CFG_CTS (UART0: 0x026; UART1: 0x039; UART2: 0x04C; UART3: 0x05F) - Read/Write OTP

This register configures the functionality of the GPIO4/CTS# pin.

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO4/CTS# is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO4/CTS# is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** Note: If configured as CTS input, GPIO5/RTS# must be configured as RTS# output and GPIO2/DSR# and GPIO3/DTR# must be configured as GPIOs. 00: GPIO4/CTS# is configured as a GPIO input 01: GPIO4/CTS# is configured as a GPIO open drain output 10: GPIO4/CTS# is configured as a GPIO push-pull output 11: GPIO4/CTS# is configured as a open drain CTS input

PIN_CFG_RS485 (UART0: 0x027; UART1: 0x03A; UART2: 0x04D; UART3: 0x060) - Read/Write OTP

This register configures the functionality of the GPIO7/RS485 pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO7/RS485 is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO7/RS485 is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 00: GPIO7/RS485 is configured as a GPIO input 01: GPIO7/RS485 is configured as a GPIO open drain output 10: GPIO7/RS485 is configured as a GPIO push-pull output 11: GPIO7/RS485 is configured as a push-pull auto. RS-485 half-duplex enable output

PIN_CFG_TXT (UART0: 0x028; UART1: 0x03B; UART2: 0x04E; UART3: 0x061) - Read/Write OTP

This register configures the functionality of the GPIO8/TXT pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO8/TXT is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO8/TXT is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 00: GPIO8/TXT is configured as a GPIO input 01: GPIO8/TXT is configured as a GPIO open drain output 10: GPIO8/TXT is configured as a GPIO push-pull output 11: GPIO8/TXT is configured as a push-pull TX toggle output

PIN_CFG_RXT (UART0: 0x029; UART1: 0x03C; UART2: 0x04F; UART3: 0x062) - Read/Write OTP

This register configures the functionality of the GPIO9/RXT pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO9/RXT is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO9/RXT is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 000: GPIO9/RXT is configured as a GPIO input 001: GPIO9/RXT is configured as a GPIO open drain output 010: GPIO9/RXT is configured as a GPIO push-pull output 011: GPIO9/RXT is configured as a push-pull RX toggle output

PIN_CFG_CD (UART0: 0x02A; UART1: 0x03D; UART2: 0x050; UART3: 0x063) - Read/Write OTP

This register configures the functionality of the GPIO1/CD# pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO1/CD# is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO1/CD# is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 00: GPIO1/CD# is configured as a GPIO input 01: GPIO1/CD# is configured as a GPIO open drain output 10: GPIO1/CD# is configured as a GPIO push-pull output 11: Invalid, do not use

PIN_CFG_RI (UART0: 0x02B; UART1: 0x03E; UART2: 0x051; UART3: 0x064) - Read/Write OTP

This register configures the functionality of the GPIO0/RI#/RWK# pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO0/RI#/RWK# is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO0/RI#/RWK# is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5	0	**REMOTE_WAKE_DIS** This register bit disables remote wakeup capability on the RI pin. 0: RI pin is enabled for remote wakeup if global remote wakeup is enabled 1: RI pin is not enabled for remote wakeup
4:2	0	**RESERVED** These bits are reserved and should be written as '0'.
1:0	0	**CTRL** 00: GPIO0/RI#/RWK# is configured as a GPIO input 01: GPIO0/RI#/RWK# is configured as a GPIO open drain output 10: GPIO0/RI#/RWK# is configured as a GPIO push-pull output 11: Invalid, do not use

PIN_CFG_DTR (UART0: 0x02C; UART1: 0x03F; UART2: 0x052; UART3: 0x065) - Read/Write OTP

This register configures the functionality of the GPIO3/DTR# pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO3/DTR# is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO3/DTR# is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:3	0	**RESERVED** These bits are reserved and should be written as '0'.
2:0	0	**CTRL** Note: If configured as DTR output, GPIO2/DSR# must be configured as DSR input and GPIO5/RTS#/RS485 and GPIO4/CTS# must be configured as GPIOs. 000: GPIO3/DTR is configured as a GPIO input 001: GPIO3/DTR is configured as a GPIO open drain output 010: GPIO3/DTR is configured as a GPIO push-pull output 011: GPIO3/DTR is configured as a open drain DTR output 100: GPIO3/DTR is configured as a push-pull DTR output 101 to 111: Invalid, do not use

PIN_CFG_DSR (UART0: 0x02D; UART1: 0x040; UART2: 0x053; UART3: 0x066) - Read/Write OTP

This register configures the functionality of the GPIO2/DSR# pin

Bit	Default	Description
7	0	**PULLUP_DIS** This register bit is used to disable the internal pull-up resistor. This setting will be ignored if GPIO2/DSR# is configured as an output. 0: Enable internal pull-up 1: Disable internal pull-up
6	0	**PULLDOWN_EN** This register bit is used to enable the internal pull-down resistor. This setting will be ignored if GPIO2/DSR# is configured as an output. 0: Do not enable internal pull-down 1: Enable internal pull-down (will not be enabled if Pull up is enabled)
5:2	0	**RESERVED** These bits are reserved and should be written as '0'.

Bit	Default	Description
1:0	0	**CTRL** Note: If configured as DSR input, GPIO3/DTR# must be configured as DTR output and GPIO5/RTS#/RS485 and GPIO4/CTS# must be configured as GPIOs. 00: GPIO2/DSR# is configured as a GPIO input 01: GPIO2/DSR# is configured as a GPIO open drain output 10: GPIO2/DSR# is configured as a GPIO push-pull output 11: GPIO2/DSR# is configured as an open drain DSR input

PIN_CFG_DATA_PINS (UART0: 0x02E; UART1: 0x041; UART2: 0x054; UART3: 0x067) - Read/Write OTP

This register configures the functionality of the RX and TX data pins

Bit	Default	Description
7	0	**RX_PULLUP_DIS** This register bit is used to disabled the internal pull-up on the RX pin 0: Enable internal pull-up on RX pin 1: Disable internal pull-up on RX pin
6	0	**RX_PULLDOWN_EN** This register bit is used to enabled the internal pull-down on the RX pin 0: Do not enable internal pull-down on RX pin 1: Enable internal pull-down on RX pin (will not be enabled if pull-up is enabled)
5	0	**RX_REMOTE_WAKE_EN** This register bit enables remote wakeup capability on the RX pin 0: RX pin is not enabled for remote wakeup 1: RX pin is enabled for remote wakeup if global remote wakeup is enabled
4:1	0	**RESERVED** These bits are reserved and should be written as '0'.
0	0	**TX_CTRL** 0: TX push-pull output 1: TX open drain output

SUSPEND_STATE_MSB (UART0: 0x02F; UART1: 0x042; UART2: 0x055; UART3: 0x068) - Read/Write OTP

This register configures the state of the GPIO pins during suspend state. Note that RX and TX data pins are not controlled by SUSPEND_STATE. USE_SUSPEND is not a physical pin, but instead acts as the control for pins in the suspended state and is in the most significant bit position of SUSPEND_MODE_MSB.

Bit	Default	Description
7	0	**GPIO9/RXT** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
6	0	**GPIO8/TXT** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
5:4	0	**Not used**

Bit	Default	Description
3	0	**GPIO7/RS485** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
2	0	**GPIO4/CTS#** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
1	0	**GPIO5/RTS#/RS485** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
0	0	**GPIO6/CLK** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'

SUSPEND_STATE_LSB (UART0: 0x030; UART1: 0x043; UART2: 0x056; UART3: 0x069) - Read/Write OTP

This register configures the state of the GPIO pins during suspend state.

Bit	Default	Description
7:6	0	**Not used**
5	0	**GPIO2/DSR#** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
4	0	**GPIO3/DTR#** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
3	0	**GPIO0/RI#** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
2	0	**GPIO1/CD#** 0: Corresponding bit set to logic '0' during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
1:0	0	**Not used**

SUSPEND_MODE_MSB (UART0: 0x031; UART1: 0x044; UART2: 0x057; UART3: 0x06A) - Read/Write OTP

This register configures the mode of the GPIO pins during suspend state. Note that RX and TX data pins are not controlled by SUSPEND_STATE. USE_SUSPEND is not a physical pin, but instead acts as the control for pins in the suspended state and is in the most significant bit position of SUSPEND_MODE_MSB.

Bit	Default	Description
7	0	**GPIO9/RXT** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
6	0	**GPIO8/TXT** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'

Bit	Default	Description
5:4	0	**Not used**
3	0	**GPIO7/RS485** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
2	0	**GPIO4/CTS#** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
1	0	**GPIO5/RTS#/RS485** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
0	0	**GPIO6/CLK** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'

SUSPEND_MODE_LSB (UART0: 0x032; UART1: 0x045; UART2: 0x058; UART3: 0x06B) - Read/Write OTP

This register configures the state of the GPIO pins during suspend state.

Bit	Default	Description
7	0	**USE_SUSPEND** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
6	0	**Not used**
5	0	**GPIO2/DSR#** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
4	0	**GPIO3/DTR#** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
3	0	**GPIO0/RI#** 0: Corresponding GPIO is push-pull output during suspend if USE_SUSPEND = '1' 1: Corresponding GPIO is open-drain output during suspend if USE_SUSPEND = '1'
2	0	**GPIO1/CD#** 0: Corresponding GPIO is push-pull outupt during suspend if USE_SUSPEND = '1' 1: Corresponding bit set to logic '1' during suspend if USE_SUSPEND = '1'
1:0	0	**Not used**

PIN_CFG_RS485_POL (UART0: 0x033; UART1: 0x046; UART2: 0x059; UART3: 0x06C) - Read/Write OTP

This register configures the polarity of the selected auto RS-485 half-duplex control pin.

Bit	Default	Description
7:1	0	**Reserved** These bits are reserved and should be written as '0'.
0	0	**POL** 0: Active low auto. RS-485 half-duplex enable 1: Active high auto. RS-485 half-duplex enable

CLK_DIV (UART0: 0x034; UART1: 0x047; UART2: 0x05A; UART3: 0x06D) - Read/Write OTP

This register sets the default clock divisor for the CLK output.

Bit	Default	Description
7:0	0	**VALUE** Output clock frequency will be determined by the formula: FREQ = 24 MHz / 2 * (VALUE). If VALUE = 0, FREQ = 24 MHz

Application Circuits

The GPIO inputs are 5V tolerant. However, when GPIO input voltage levels exceed VIO, an external clamp circuit is required to prevent VIO from increasing. Two examples of different application circuits are shown in Figure 7.

VIO Clamp Circuits

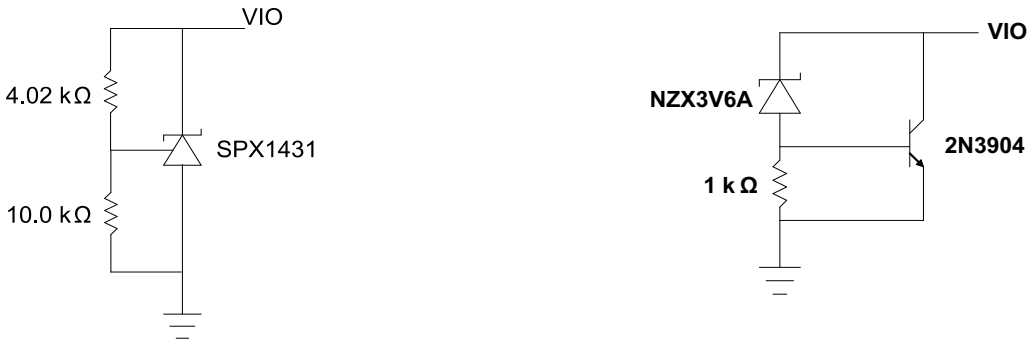
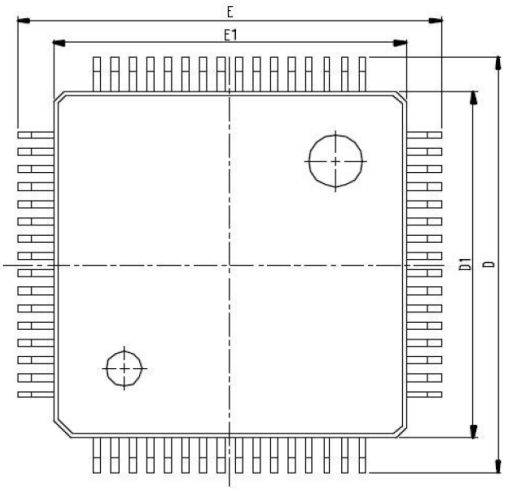


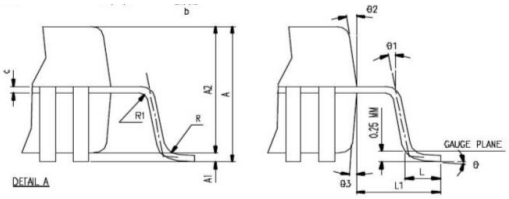
Figure 7: VIO Clamp Circuits

Mechanical Dimensions

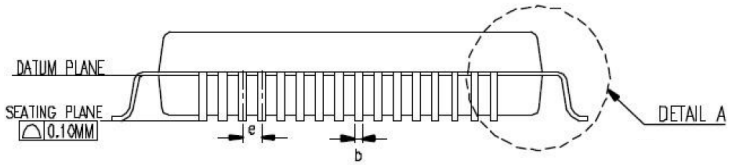
64-Pin LQFP



TOP VIEW



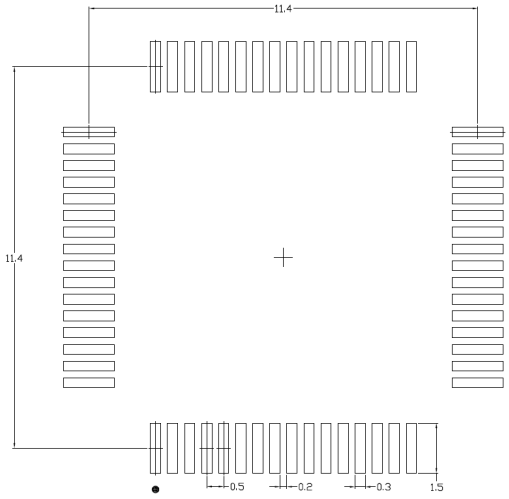
DETAIL A



SIDE VIEW

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

TERMINAL DIMENSION



TYPICAL RECOMMENDED LAND PATTERN

1. Control dimensions are in Millimeters
2. Dimensions and tolerance per Jedec MS-026

Drawing No. : POD - 00000092

Revision: A

Ordering Information[1]

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR21B1424IV64-F	-40°C to +85°C	Yes[2]	64-pin LQFP	Tray
XR21B1424IV64TR-F				Reel
XR21B1424IV64-0A-EVB	Evaluation Board for XR21B1424			

NOTE:

1. Refer to www.exar.com/XR21B1424 for most up-to-date Ordering Information
2. Visit www.exar.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	April 2014	Initial release [ECN1416-06 l 04/15/2014]
1B	November 2014	Corrected Request value for 4 CDC-ACM USB control commands. Corrected marking specification in Ordering Information table [ECN 1446-10 Nov 12 2014]
1C	August 2017	Updated to MaxLinear logo. Updated format and ordering information table. Added Character Format section. Updated USB_STAT, VCC_REG, VBUS_SENSE and RI#/RWK# pin descriptions. Updated OTP Memory intro paragraph and Remote Wake-up section. Changed LOCK_BYTE to PROG_BYTE in OTP Map and Descriptions. Clarified minimum baud rate of 300 bps in General Description and Features. Updated Read/Write of USB_STATUS register and updated bits 0 and 1. Updated USB Strings section. Corrected GET_USB_STAT typo in USB Control Commands. Corrected typos in registers 0x00B, 0x00C and 0x00E.
1D	September 2018	Removed incorrect connection from VCC_REG to VCC in Figure 2. Mechanical dimensions drawing updated to reflect 64 pins.
1E	January 2019	Updated registers: TX_FIFO_FLUSH (0x040) bit 0; bits 6-7 of PIN_CFG_CLK (0x024), PIN_CFG_RTS (0x025), PIN_CFG_CTS (0x026), PIN_CFG_RS485 (0x027), PIN_CFG_TXT (0x028), PIN_CFG_RXT (0x029), PIN_CFG_CD (0x02A), PIN_CFG_RI (0x02B), PIN_CFG_DTR (0x02C), PIN_CFG_DSR (0x02D); bits 0-1 of PIN_CFG_DSR (0x02D); bits 0 and 7 of PIN_CFG_DATA_PINS (0x02E); bits 0-1 of PROG_BYTE_0 (0x01D); bits 0-2 of PIN_CFG_RTS; bits 0-1 of PIN_CFG_RS485 (0x027); bits 0-1 of PIN_CFG_RI. Added remote wakeup to register 0x02B bit 5. Added UART1, UART2 and UART3 register addresses to Table 9 Address column and register descriptions. Corrected pin name of PIN_CFG_CD (0x02A), PIN_CFG_RI (0x02B), PIN_CFG_DTR (0x02C), PIN_CFG_DSR (0x02D).

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- Консультации по применению компонента;
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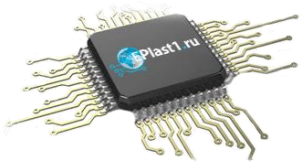
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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