ZXGD3105N8

SYNCHRONOUS MOSFET CONTROLLER IN SO-8

Description

ZXGD3105N8 synchronous controller is designed for driving a MOSFET as an ideal rectifier. This is to replace a diode for increasing the power transfer efficiency.

Proportional Gate drive control monitors the reverse voltage of the MOSFET such that if body diode conduction occurs a positive voltage is applied to the MOSFET's Gate pin. Once the positive voltage is applied to the Gate the MOSFET switches on allowing reverse current flow. The controllers' output voltage is then proportional to the MOSFET Drain-Source voltage and this is applied to the Gate via the driver. This action minimizes body diode conduction whilst enabling a rapid MOSFET turn off as Drain current decays to zero.

Applications

Flyback Converters in:

- Low Voltage AC / DC Adaptors
- Set Top Box
- PoE power devices

Resonant Converters in:

- Telecoms PSU
- Laptop Adaptors
- Computing Power Supplies - ATX and Server PSU

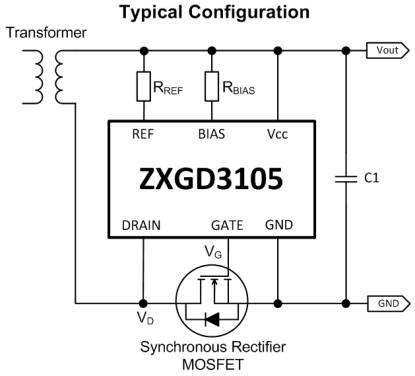
Features

- Proportional gate drive to minimize body diode conduction
- Low standby power with quiescent supply current < 1mA
- 4.5V operation enables low voltage supply
- 25V V_{CC} rating
- 100V Drain voltage rating
- Operation up to 500kHz
- Critical Conduction Mode (CrCM) & Continuous Mode (CCM)
- Compliant with Eco-design directive
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

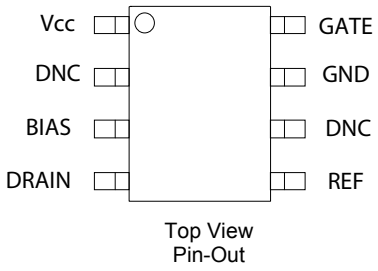
Mechanical Data

- Case: SO-8
- Case material: molded plastic. "Green" molding compound.
- UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

Typical Configuration



SO-8



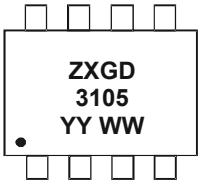
Top View
Pin-Out

Ordering Information (Note 4)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXGD3105N8TC	ZXGD3105	13	12	2500

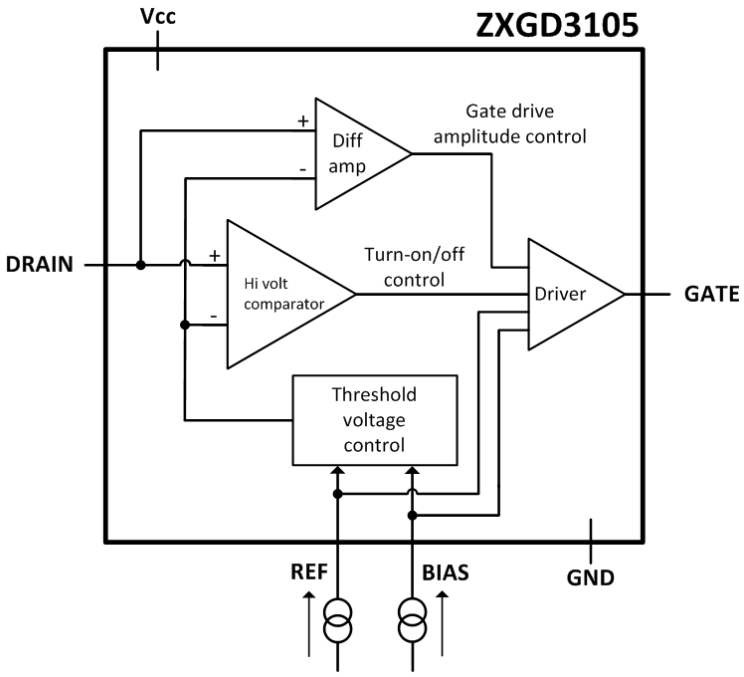
Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen and Antimony free,"Green" and Lead-Free.
3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com

Marking Information



ZXGD = Product Type Marking Code, Line 1
3105 = Product Type Marking Code, Line 2
YY = Year (ex: 11 = 2011)
WW = Week (01 - 53)

Functional Block Diagram



Pin Number	Pin Name	Pin Function and Description
1	V_{CC}	**Power supply** This supply pin should be closely decoupled to ground with a ceramic capacitor.
2	DNC	**Do not connect** Leave pin floating.
3	BIAS	**Bias** Connect this pin to V_{CC} via R_{BIAS} resistor. Select R_{BIAS} to source 0.54mA into this pin. Refer to Table 1 and 2, in Application Information section.
4	DRAIN	**Drain sense** Connect directly to the synchronous MOSFET drain terminal.
5	REF	**Reference** Connect this pin to V_{CC} via R_{REF} resistor. Select R_{REF} to source 1.02mA into this pin. Refer to Table 1 and 2, in Application Information section.
6	DNC	**Do not connect** Leave pin floating.
7	GND	**Ground** Connect this pin to the synchronous MOSFET source terminal and ground reference point.
8	GATE	**Gate drive** This pin sinks and sources the I_{SINK} and I_{SOURCE} current to the synchronous MOSFET gate.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Supply voltage, relative to GND	V_{CC}	25	V
Drain pin voltage	V_D	-3 to +100	V
Gate output voltage	V_G	-3 to V_{CC} +3	V
Gate Driver peak source current	I_{SOURCE}	4	A
Gate Driver peak sink current	I_{SINK}	9	A
Reference voltage	V_{REF}	V_{CC}	V
Reference current	I_{REF}	25	mA
Bias voltage	V_{BIAS}	V_{CC}	V
Bias current	I_{BIAS}	100	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

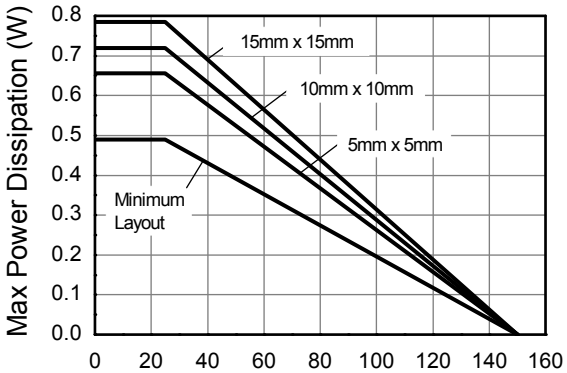
Characteristic		Symbol	Value	Unit
Power Dissipation Linear derating factor	(Note 5)	P_D	490 3.92	mW mW/°C
	(Note 6)		655 5.24	
	(Note 7)		720 5.76	
	(Note 8)		785 6.28	
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	255	°C /W
	(Note 6)		191	
	(Note 7)		173	
	(Note 8)		159	
Thermal Resistance, Junction to Lead	(Note 9)	$R_{\theta JL}$	135	°C /W
Operating Temperature Range		T_J	-40 to +150	°C
Storage Temperature Range		T_{STG}	-50 to +150	

ESD Ratings (Note 10)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	200	V	B

Notes:
5. For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as note (5), except pin 1 (V_{CC}) and pin 7 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
7. Same as note (6), except both heatsinks are 10mm x 10mm.
8. Same as note (6), except both heatsinks are 15mm x 15mm.
9. Thermal resistance from junction to solder-point at the end of each lead on pin 1 (V_{CC}) and pin 7 (GND).
10. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

Thermal Derating Curve



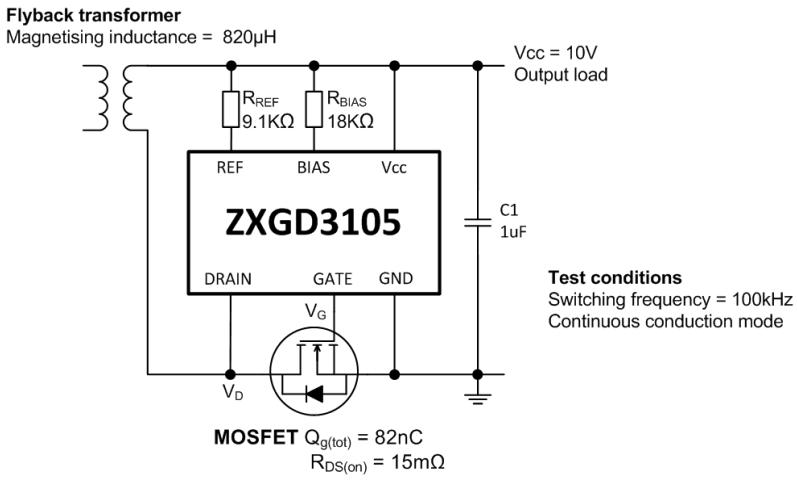
Derating Curve

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

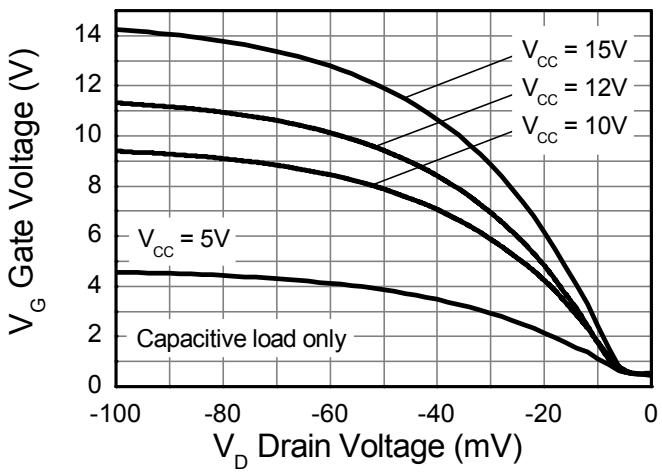
V_{CC} = 10V; R_{BIAS} = 18kΩ (I_{BIAS} = 0.54mA); R_{REF} = 9.1kΩ (I_{REF} = 1.02mA)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Input Supply						
Quiescent current	I_Q	—	1.56	—	mA	V_{DRAIN} ≥ 0mV
Gate Driver						
Gate peak source current	I_{SOURCE}	—	2	—	A	Capacitive load: C_L = 20nF
Gate peak sink current	I_{SINK}	—	7	—		
Detector under DC condition						
Turn-off Threshold Voltage	V_T	-20	-10	0	mV	V_G = 1V
Gate output voltage	$V_{G(off)}$	—	0.2	0.6	V	V_{DRAIN} ≥ 1V
	V_G	5.0	7.8	—		V_{DRAIN} = -50mV
		8.0	9.4	—		V_{DRAIN} = -100mV
Switching Performance						
Turn-on propagation delay	$t_{d(rise)}$	—	70	—	ns	Rise and fall measured 10% to 90% Refer to application test circuit below
Gate rise time	t_r	—	175	—		
Turn-off propagation delay	$t_{d(fall)}$	—	15	—		
Gate fall time	t_f	—	20	—		

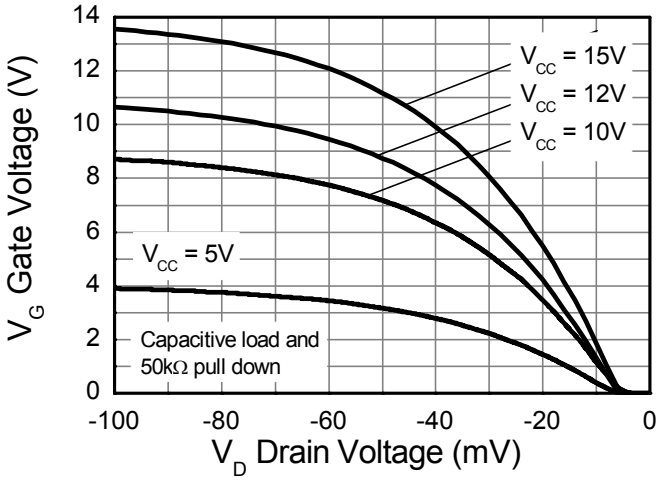
Test Circuit for Switching Performance



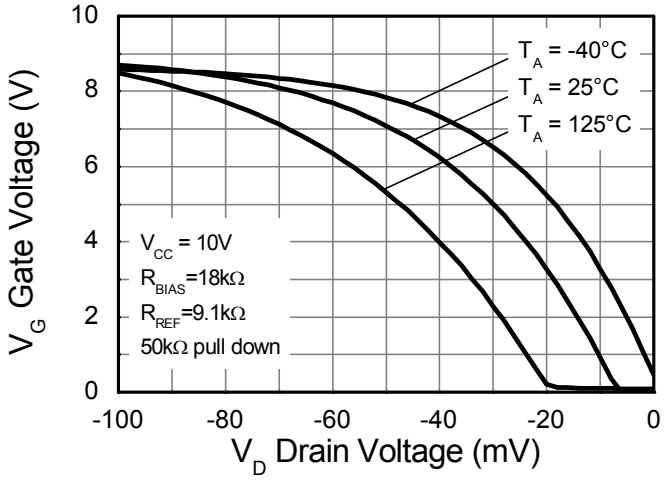
Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



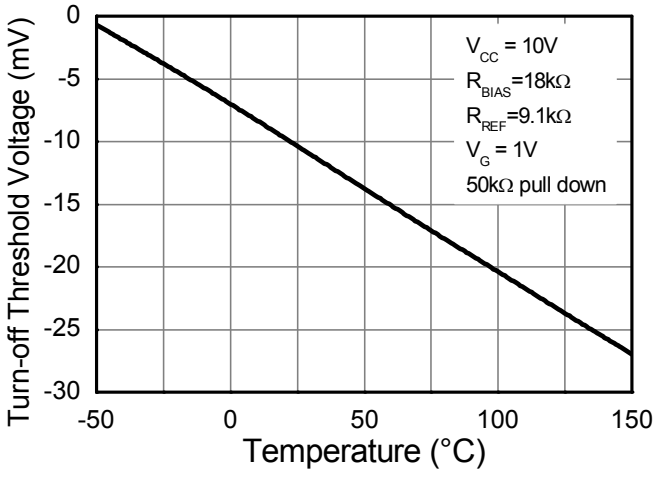
Transfer Characteristic



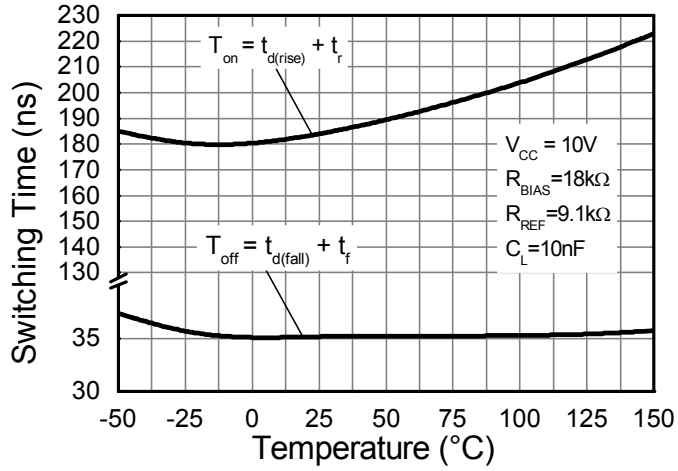
Transfer Characteristic



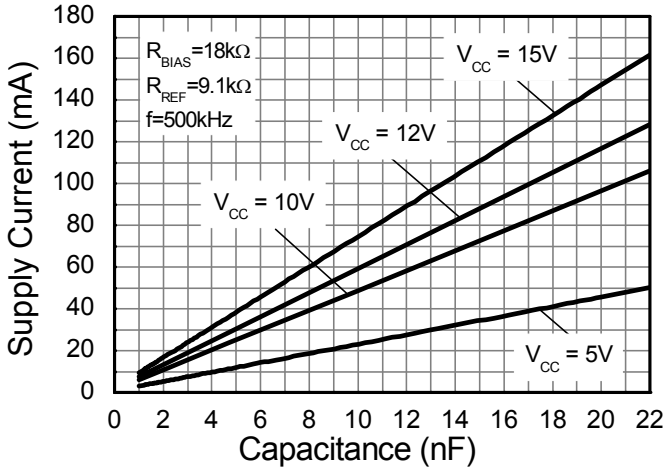
Transfer Characteristic



Turn-off Threshold Voltage vs Temperature

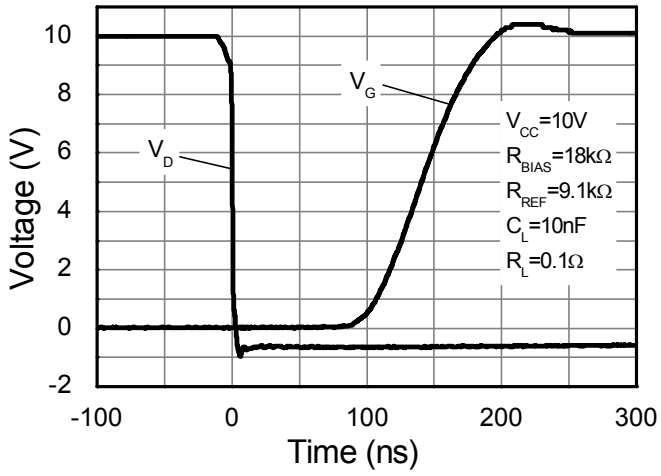


Switching vs Temperature

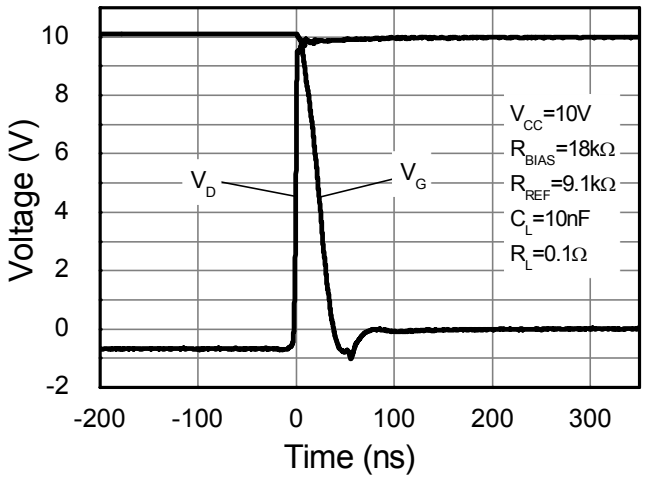


Supply Current vs Capacitive Load

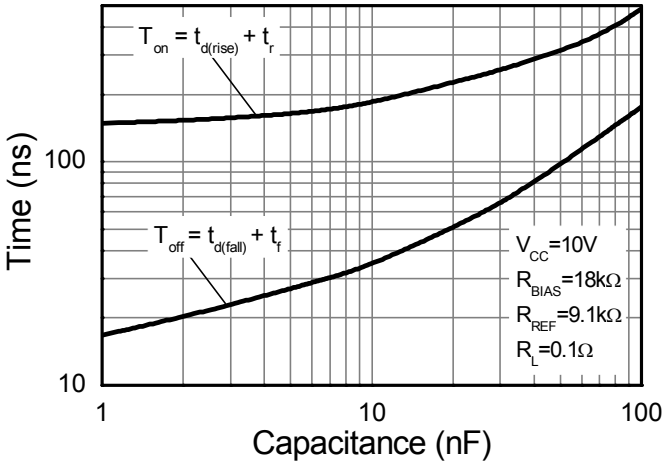
Typical Electrical Characteristics (cont.) (@T_A = +25°C, unless otherwise specified.)



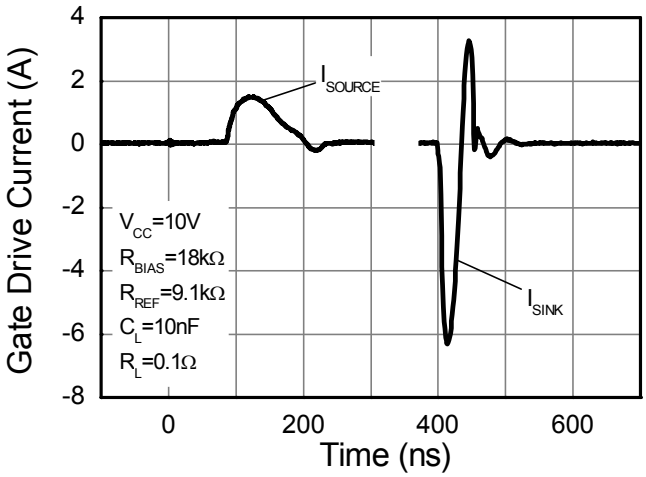
Switch On Speed



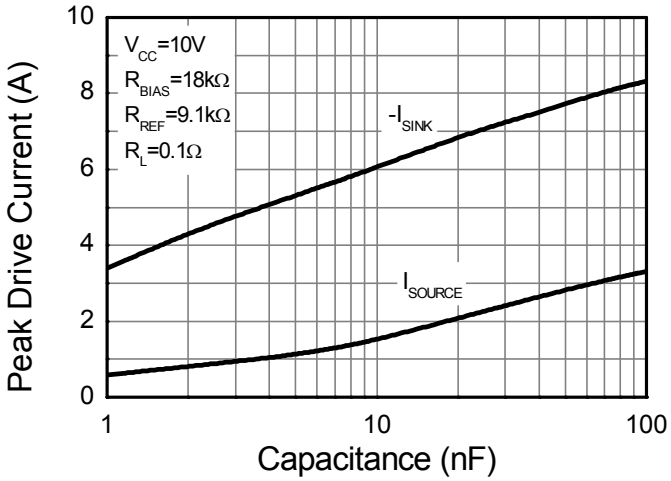
Switch Off Speed



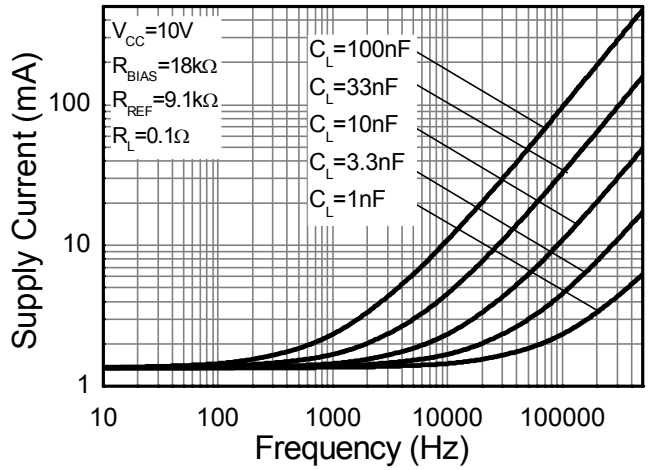
Switching vs Capacitive Load



Gate Drive Current



Gate Current vs Capacitive Load



Supply Current vs Frequency

Application Information

The purpose of the ZXGD3105 is to drive a MOSFET as a low-V_F Schottky diode replacement in isolated AC/DC converter. When combined with a low $R_{DS(ON)}$ MOSFET, the controller can yield significant power efficiency improvement, whilst maintaining design simplicity and incurring minimal component count. Figure 1 shows the typical configuration of ZXGD3105 for synchronous rectification in a low output voltage Flyback converter.

A typical circuit configuration of synchronous rectification with ZXGD3105 for use in resonant converter is shown in Figure 2. Two ZXGD3105 together with two synchronous MOSFETs should be used on the secondary side of the center tapped transformer winding.

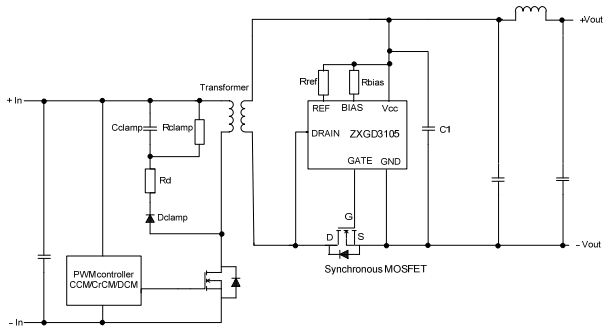


Figure 1. Typical Flyback application schematic

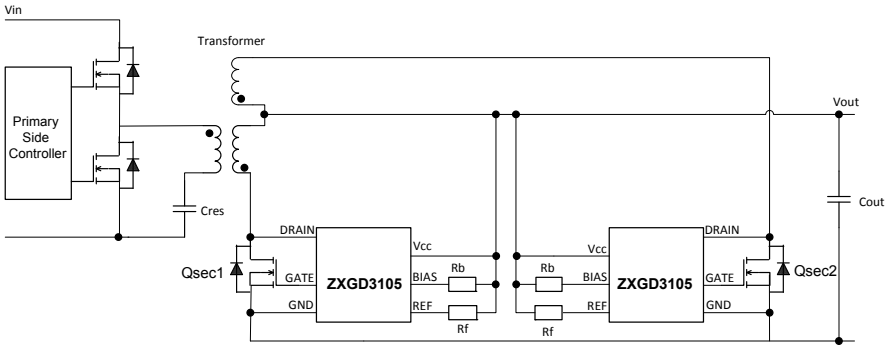


Figure 2. Synchronous rectification in resonant converter

Threshold Voltage and Resistor Setting

Proper selection of external resistors R_{REF} and R_{BIAS} is important for optimum device operation. R_{REF} and R_{BIAS} supply fixed current into the I_{REF} and I_{BIAS} pin of the controller. I_{REF} and I_{BIAS} combines to set the turn-off threshold voltage level, V_T. In order to set V_T to -10mV, the recommended I_{REF} and I_{BIAS} are 1.02mA and 0.54mA respectively.

The values for R_{REF} and R_{BIAS} are selected based on the V_{CC} voltage. If the V_{CC} pin is connected to the power converter's output, the resistors should be selected based on the nominal converter's output voltage. Table 1 provides the recommended resistor values for different Vcc voltages.

Supply, V_{CC}	Bias Resistor, R_{BIAS}	Reference Resistor, R_{REF}
5 V	9.6 kΩ	4.3 kΩ
10V	18 kΩ	9.1 kΩ
12V	24 kΩ	11 kΩ
15V	30 kΩ	15 kΩ

Table 1. Recommended resistor values for different V_{CC} voltages

Functional Descriptions for Flyback Converter

The operation of the device is described step-by-step with reference to the timing diagram in Figure 3.

1. The detector stage monitors the MOSFET Drain-Source voltage.
2. When, due to transformer action, the MOSFET body diode is forced to conduct there is a negative voltage on the Drain pin due to the body diode forward voltage.
3. When the negative Drain voltage crosses the turn-off Threshold voltage V_T, the detector stage outputs a positive voltage with respect to ground after the turn-on delay time $t_{d(fall)}$. This voltage is then fed to the MOSFET driver stage and current is sourced out of the GATE pin.
4. The controller goes into proportional gate drive control — the GATE output voltage is proportional to the MOSFET on-resistance-induced Drain-Source voltage. Proportional gate drive ensures that MOSFET conducts during the majority of the conduction cycle to minimize power loss in the body diode.
5. As the Drain current decays linearly toward zero, proportional gate drive control reduces the Gate voltage so the MOSFET can be turned off rapidly at zero current crossing. The GATE voltage falls to 1V when the Drain-Source voltage crosses the detection threshold voltage to minimize reverse current flow.
6. At zero Drain current, the controller GATE output voltage is pulled low to $V_{G(off)}$ to ensure that the MOSFET is off.

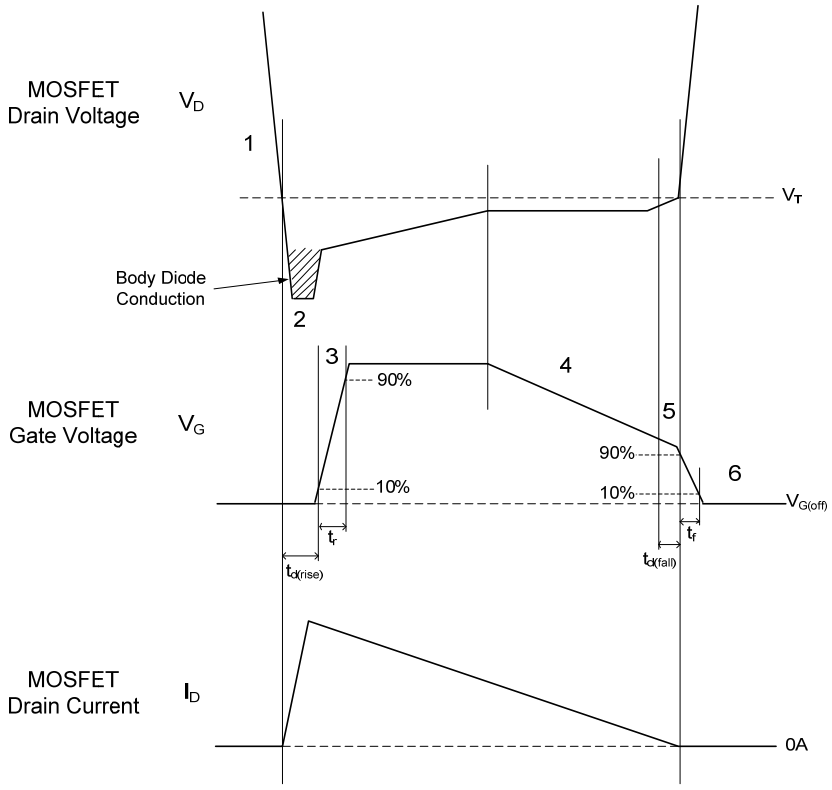


Figure 3. Timing diagram for a critical conduction mode Flyback converter

Functional Descriptions for Resonant Converter

The operation of the ZXGD3105 in resonant converter is described with reference to Figure 4.

1. The detector stage monitors the MOSFET Drain-GND voltage.

2. When, due to transformer action, the MOSFET body diode is forced to conduct there is a negative voltage on the Drain pin due to the body diode forward voltage.

3. When the negative Drain voltage crosses the Threshold voltage V_T, the detector stage outputs a positive voltage with respect to ground after the turn-on delay time $t_{d(rise)}$. This voltage is then fed to the MOSFET driver stage and current is sourced out of the GATE pin.

4. The controller goes into Proportional Gate Drive control. The GATE voltage now varies according to the MOSFET's Drain-GND voltage. During this phase, the relationship of V_G vs. V_D is shown by the transfer characteristic curve in page xx of this datasheet. As the Drain current decays linearly, the Gate voltage reduces so the MOSFET can be turned off rapidly at zero current crossing.
   Proportional Gate Drive also ensures that gate voltage is supplied to the MOSFET gate until the Drain current is virtually zero. This eliminates any parasitic diode conduction after the MOSFET switches off.

5. The GATE voltage falls to 1V when the Drain-GND voltage reaches V_T. The MOSFET is turned off precisely when the sinusoidal current goes to zero, with little or no reverse current. Threshold voltage V_T is defined as the Drain voltage V_D level at which Gate voltage V_G is 1V (refer to electrical characteristic section in page 4).

6. At zero Drain current, the GATE voltage is pulled low to $V_{G(off)}$ to ensure that the MOSFET is off.

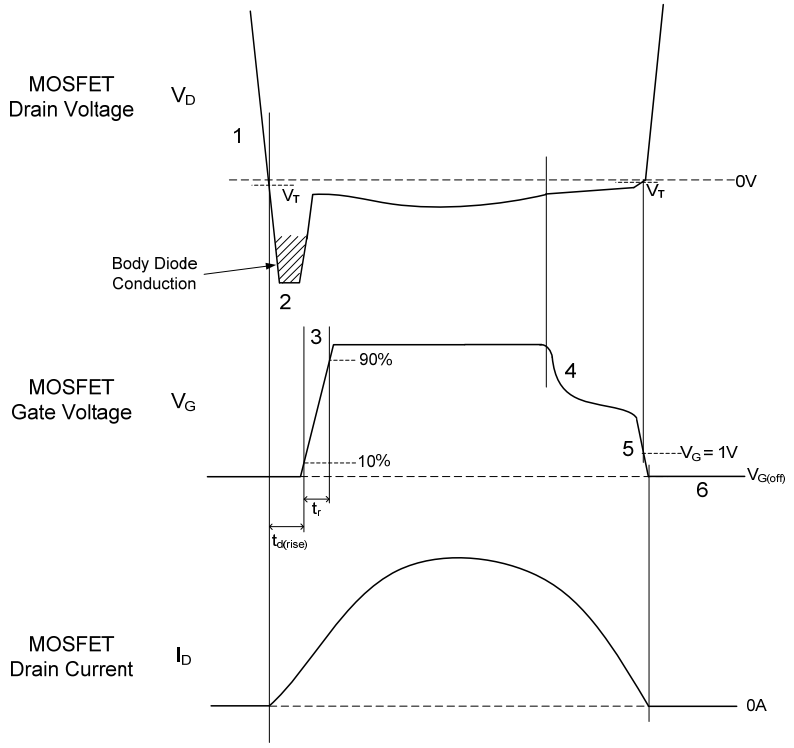
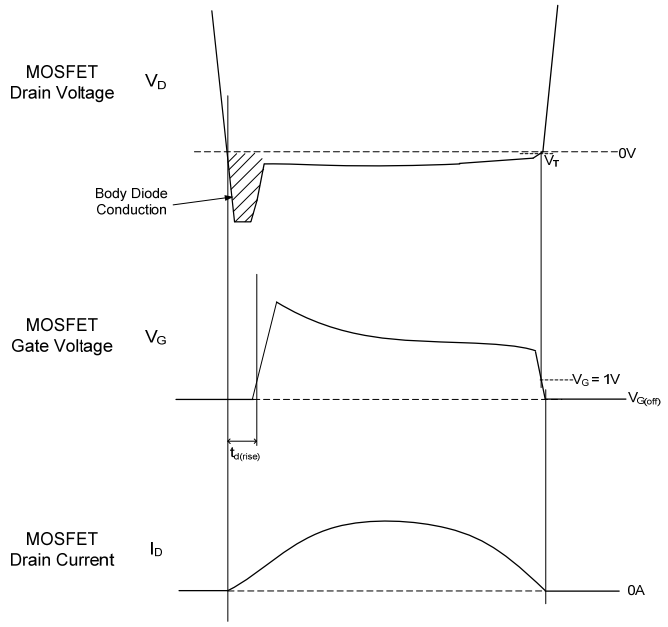


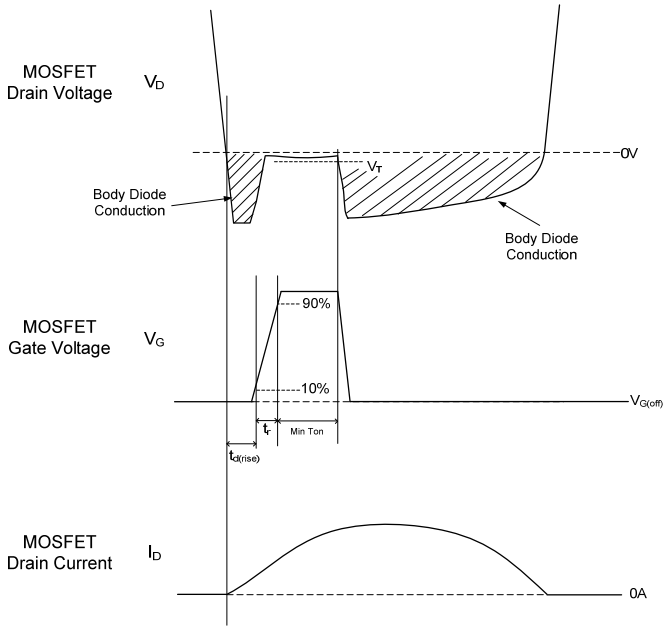
Figure 4. Timing diagram of synchronous rectification in the resonant converter

Besides that, Proportional Gate Drive improves the rectifier efficiency even at light to medium load condition by ensuring that the MOSFETs conduct during majority of the conduction cycle as shown in Figure 5a.

At reduced load condition, early termination of the gate drive voltage is likely for digital level gate drive due to the low current, which means that the threshold V_T is breached. With the early termination of the gate drive voltage, MOSFET turns off and the body diode conducts, see Figure 5. This is shown by an increase in Drain-GND voltage for the remaining time of the current waveform. With the current flowing through the body diode there will be an increase in power developed within the MOSFET. The efficiency impact due to early termination of digital level gate driver increases with lower $R_{DS(on)}$ MOSFET and/or higher operating frequency.



(a)



(b)

Figure 5. Timing diagram of synchronous rectification in the resonant converter (a) Proportional Gate Drive and (b) Digital Level Gate Drive

Gate Driver

The controller is provided with single channel high current gate drive output, capable of driving one or more N-channel power MOSFETs. The controller can operate from Vcc of 4.5V to drive both standard MOSFETs and logic level MOSFETs.

The Gate pins should be as close to the MOSFET's gate as possible. A resistor in series with GATE pin helps to control the rise time and decrease switching losses due to gate voltage oscillation. A diode in parallel to the resistor is typically used to maintain fast discharge of the MOSFET's gate.

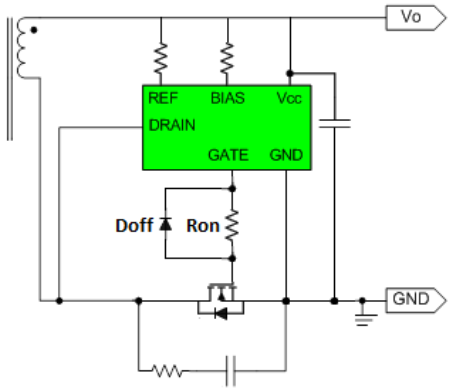


Figure 6. Typical connection of the ZXGD3105 to the synchronous MOSFET

Quiescent Current Consumption

The quiescent current consumption of the controller is the sum of I_{REF} and I_{BIAS}. For an application that requires ultra-low standby power consumption, I_{REF} and I_{BIAS} can be further reduced by increasing the value of resistor R_{REF} and R_{BIAS}.

Bias Current I_{BIAS}	Ref Current I_{REF}	Bias Resistor R_{BIAS}	Ref Resistor R_{REF}	Quiescent Current I_Q
0.25mA	0.61mA	39.2KΩ	15.4KΩ	0.86mA
0.35mA	0.81mA	28.0KΩ	11.5KΩ	1.16mA
0.46mA	0.99mA	21.5KΩ	9.3KΩ	1.45mA
0.50mA	1.00mA	19.6KΩ	8.9KΩ	1.50mA
0.55mA	1.13mA	17.8KΩ	8.1KΩ	1.68mA
0.80mA	1.66mA	12.1KΩ	5.6KΩ	2.46mA

Table 2. Quiescent current consumption for different resistor values at Vcc=10V

I_{REF} also controls the gate driver peak sink current whilst I_{BIAS} controls the peak source current. At the default current value of I_{REF} and I_{BIAS} of 1.02mA and 0.54mA, the gate driver is able to provide 2A source and 6A sink current. The gate current decreases if I_{REF} and I_{BIAS} are reduced. Care must be taken in reducing the controller quiescent current so that sufficient drive current is still delivered to the MOSFET particularly for high switching frequency application.

Layout Guidelines

When laying out the PCB, care must be taken in decoupling the ZXGD3105 closely to V_{CC} and ground with 1µF low-ESR, low-ESL X7R type ceramic bypass capacitor. If the converter's output voltage is higher than 20V, a 12V zener diode should be connected from the bias pin to GND to clamp the Gate voltage and protect the synchronous MOSFET. Figure 7 shows the typical connection diagram.

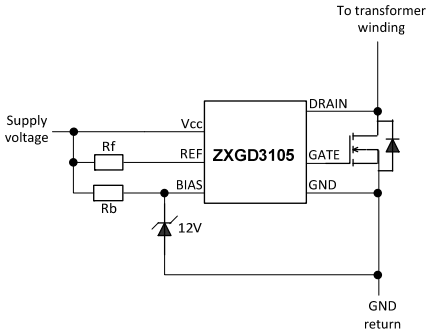


Figure 7. Zener Voltage Clamp Arrangement

GND is the ground reference for the internal high voltage amplifier as well as the current return for the gate driver. So the ground return loop should be as short as possible. Sufficient PCB copper area should be allocated to the Vcc and GND pin for heat dissipation especially for high switching frequency application.

Any stray inductance involved by the load current may cause distortion of the drain-to-source voltage waveform, leading to premature turn-off of the synchronous MOSFET. In order to avoid this issue, drain voltage sensing should be done as physically close to the drain terminals as possible. The PCB track length between the controller Drain pin and the MOSFET's terminal should be kept less than 10mm. MOSFET packages with low internal wire bond inductance are preferred for high switching frequency power conversion to minimize body diode conduction.

After the primary MOSFET turns off, its Drain voltage oscillates due to reverse recovery of the snubber diode. These high frequency oscillations are reflected across the transformer to the Drain terminal of the synchronous MOSFET. The synchronous controller senses the Drain voltage ringing, causing its gate output voltage to oscillate. The synchronous MOSFET cannot be fully enhanced until the Drain voltage stabilizes.

In order to prevent this issue, the oscillations on the primary MOSFET can be damped with either a series resistor Rd to the snubber diode or an R-C network across the diode (refer Figure 8). Both methods reduce the oscillations by softening the snubber diode's reverse recovery characteristic.

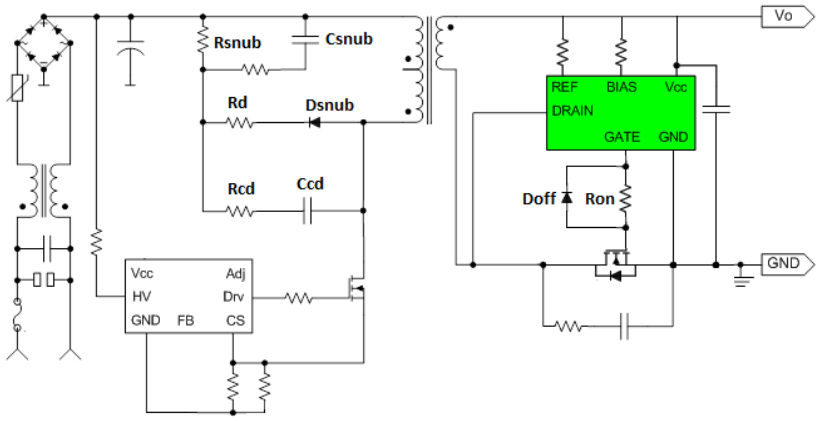
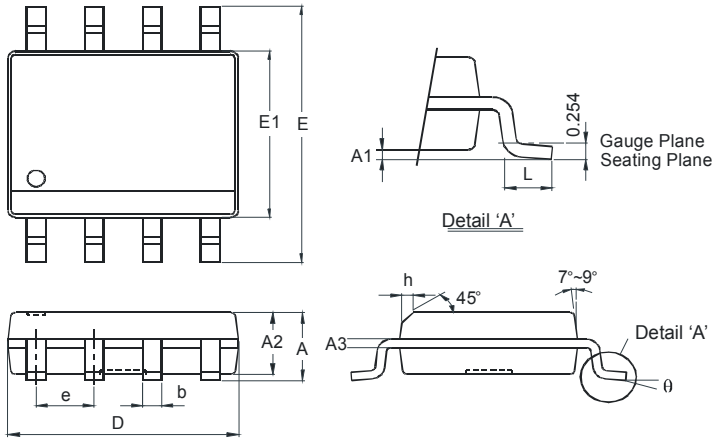


Figure 8. Primary Side Snubber Network to Reduce Drain Voltage Oscillations

Package Outline Dimensions

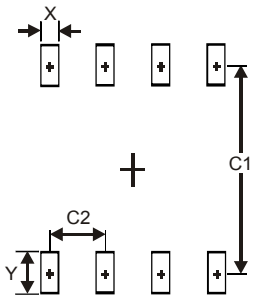
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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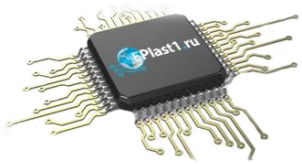
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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