Using the TPS84410EVM-001, TPS84210EVM-002, TPS84610EVM-003

User's Guide

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TPS84410EVM-001/TPS84210EVM-002/TPS84610EVM-003, 2-A to 6-A Integrated Power Solution

1 Introduction

The TPS84410EVM-001, TPS84210EVM-002, TPS84610EVM-003 Evaluation Module (TPS84x10EVM-00x) is designed as an easy to use platform that facilitates an extensive evaluation of the features and performance of the Integrated Power Solution (IPS) devices. The EVM PCB may be configured with one of three IPS devices (see Table 1).

Table 1. TPS84x10EVM-00x Device Configuration

DEVICE	TITLE
TPS84210	6-V input, 2-A output sync. step-down converter with PWM
TPS84410	6-V input, 4-A output sync. step-down converter with PWM
TPS84610	6-V input, 6-A output sync. step-down converter with PWM

This user guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

2 Description

The EVM features a TPS84x10 synchronous buck IPS device configured for operation with typical 3.3-V and 5-V input bus applications. The output voltage can be set to one of five popular values by using a simple configuration jumper. In similar fashion, the switching frequency can be set to one of four values by use of a jumper. The full 4-A rated output current can be supplied by the EVM. A minimal amount of input and output capacitance is used on the board. Component pads are provided for additional input and output capacitors if desired. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Control test points are provided for use of the PWRGD, Inhibit/UVLO, synchronization, and slow-start/tracking features of the IPS device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

3 Getting Started

Figure 1 highlights the user interface items associated with the EVM. The polarized V_{IN} Power terminal block is used for connection to the host input supply and the polarized V_{OUT} Power terminal block is used for connection to the load. The terminal blocks can except up to 16 AWG wire.

The V_{IN} monitor and V_{OUT} monitor test points located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure V_{IN} and V_{OUT}. The voltmeter references should be connected to any of the four V_{IN}/V_{OUT} monitor grounds test points located between the power terminal blocks. Do not use these V_{IN} and V_{OUT} monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

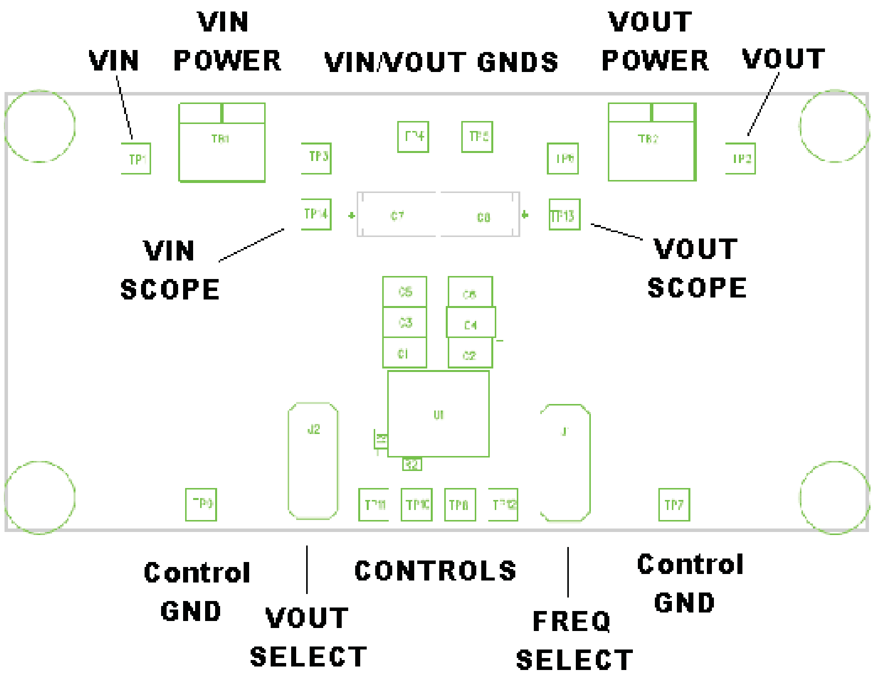

Figure 1. TPS84x10EVM-00x User Interface

The V_{IN} scope and V_{OUT} scope test points can be used to monitor V_{IN} and V_{OUT} waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes. The scope probe tip should be connected to the socket labeled VIN or VOUT, and the scope ground barrel should lean against to the test point labeled GND. The GND TP may need to be cut or bent slightly to hold the probe barrel.

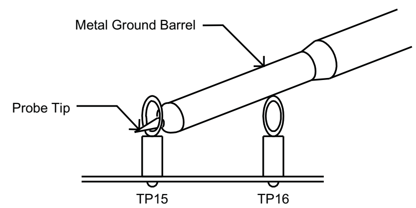

Figure 2. Tip and Barrel Measurement

The control test points located directly below the TPS84x10 IPS device are made available to test the features of the device. Any external connections made to these test points should be referenced to either of the two control ground test points located along the bottom of the EVM. Refer to Section 4 of this user guide for more information on the individual control test points.

The V_{OUT}-select and F_{SW}-select configuration jumpers are provided for selecting the desired output voltage and appropriate switching frequency. Before applying power to the EVM, ensure that the jumpers are present and properly positioned for the intended output voltage. Refer to Table 2 for the recommended jumper settings. Always remove input power before changing the jumper settings.

Once the jumper settings have been confirmed, configure the host input supply to apply the appropriate bus voltage listed in Table 2 and confirm that the selected output voltage is obtained.

Table 2. Output Voltage and Switching Frequency Jumper Settings

V_{OUT} SELECT	TPS84210, F_{SW} SELECT	TPS84410, F_{SW} SELECT	TPS84610, F_{SW} SELECT	V_{IN} BUS VOLTAGE
3.3 V	1.5 MHz	1 MHz	-	5 V
2.5 V	1.5 MHz	1 MHz	-	5 V
1.8 V	1 MHz	1 MHz	-	5 V or 3.3 V
1.2 V	750 kHz	750 kHz	-	5 V or 3.3 V
0.8 V	650 kHz	650 kHz	-	5 V or 3.3 V

4 Test Point Descriptions

Fourteen wire-loop test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the IPS device. A via labled PH is available near U1 to scope on the switching frequency. A description of each test point is listed in Table 3

Table 3. Test Point Descriptions

TEST POINT	DESCRIPTION
VIN	Input voltage monitor. Connect DVM to this point for measuring efficiency.
VOUT	Output voltage monitor. Connect DVM to this point for measuring efficiency, line regulation, and load regulation.
GND	Input and output voltage monitor grounds (located between terminal blocks). Reference the above DVMs to any of these four ground points.
VIN (scope)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT (scope)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
PWRGD	Monitors the power good signal of the IPS device. This is an open drain signal that requires an external pull-up resistor to V_{IN} if monitoring is desired. A 10-kΩ to 100-kΩ pull-up resistor is recommended. PWRGD is high if the output voltage is within 92% to 106% of its nominal value.
INH/UVLO	Connect this point to control ground to inhibit the IPS device. Allow this point to float to enable the device. Do not use a pull-up resistor. An external resistor can be connected from this point to control ground to increase the under-voltage lockout (UVLO) of the device.
RT/CLK	Connects to the RT/CLK pin of the IPS device. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.
SS/TR	Connects to the internal slow-start capacitor of the IPS device. An external capacitor can be connected from this point to control ground to increase the slow-start time of the device. This point can also be used as an input for tracking applications.
GND	Control grounds (located along bottom of EVM). Reference any signals associated with the control test points to either of these two ground points.

5 Operation Notes

The UVLO threshold of the factory-stock EVM is approximately 3.05 V with 0.3 V of hysteresis. The input voltage must be above the UVLO threshold in order to startup the IPS device. The UVLO threshold can be increased by adding a resistor to the INH/UVLO test point as described above. After startup, the minimum input voltage to the IPS device must be at least 2.95 V or (V_{OUT} + 1.1 V), whichever is greater, in order to produce a regulated output. The maximum operating input voltage for the IPS device is 6 V. Refer to the TPS84410 datasheet for further information on the input voltage range and UVLO operation.

After application of the proper input voltage, the output voltage of the IPS device will ramp to its final value in approximately 1 ms. If desired, this soft-start time can be increased by adding a capacitor to the SS/TR test point as described above. Refer to the TPS84410 datasheet for further information on adjusting the soft-start time.

Table 1 lists the recommended switching frequencies for each of the V_{OUT} selections. These recommendations cover operation over a wide range of input voltage and output load conditions. Several factors such as duty cycle, minimum on-time, minimum off-time, and current limit influence selection of the appropriate switching frequency. In some applications, other switching frequencies might be used for particular output voltages, depending on the above factors. Refer to the TPS84410 datasheet for further information on switching frequency selection, including synchronization.

6 TPS84x10EVM-00x Schematic

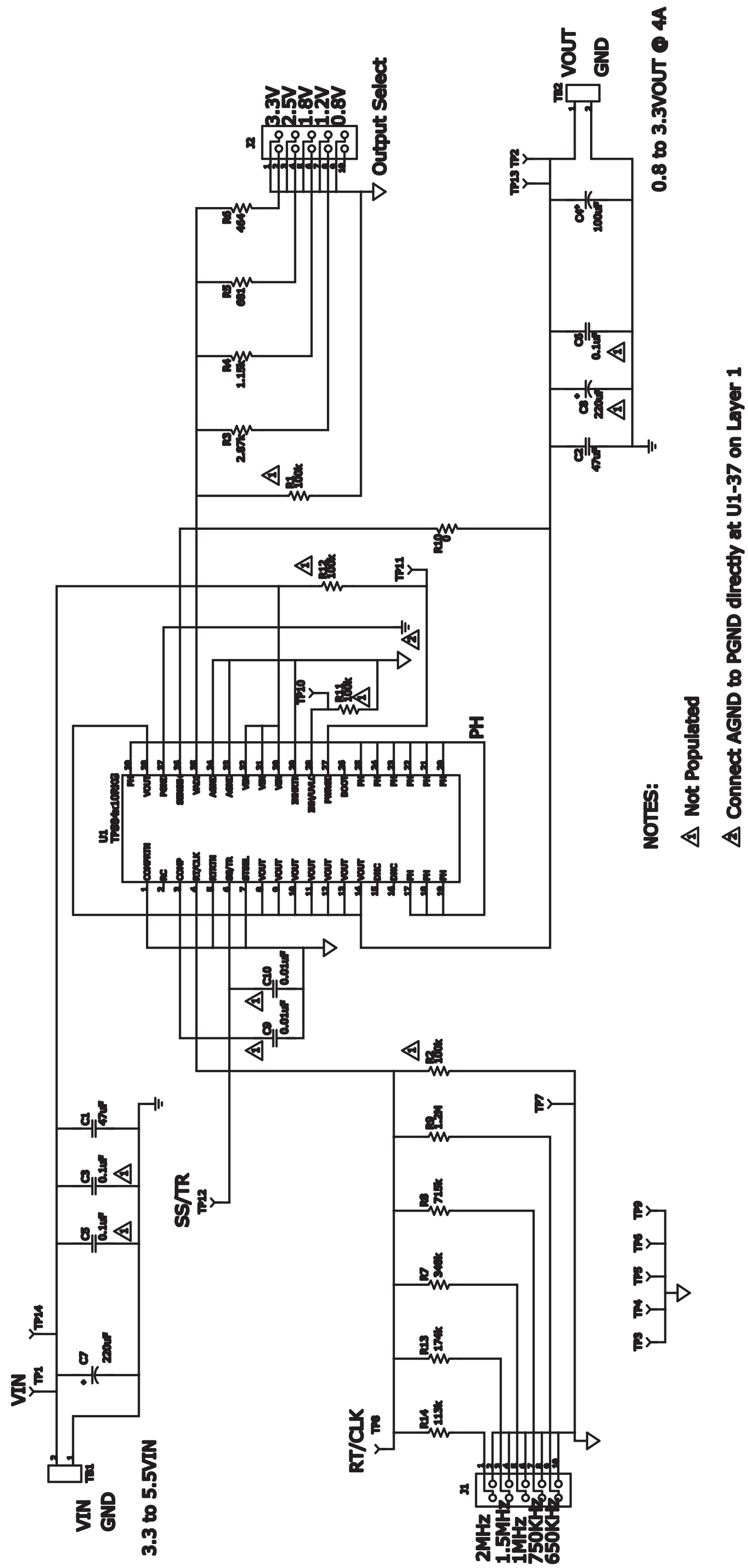

Figure 3. TPS84x10EVM-00x Schematic

7 PCB Layouts

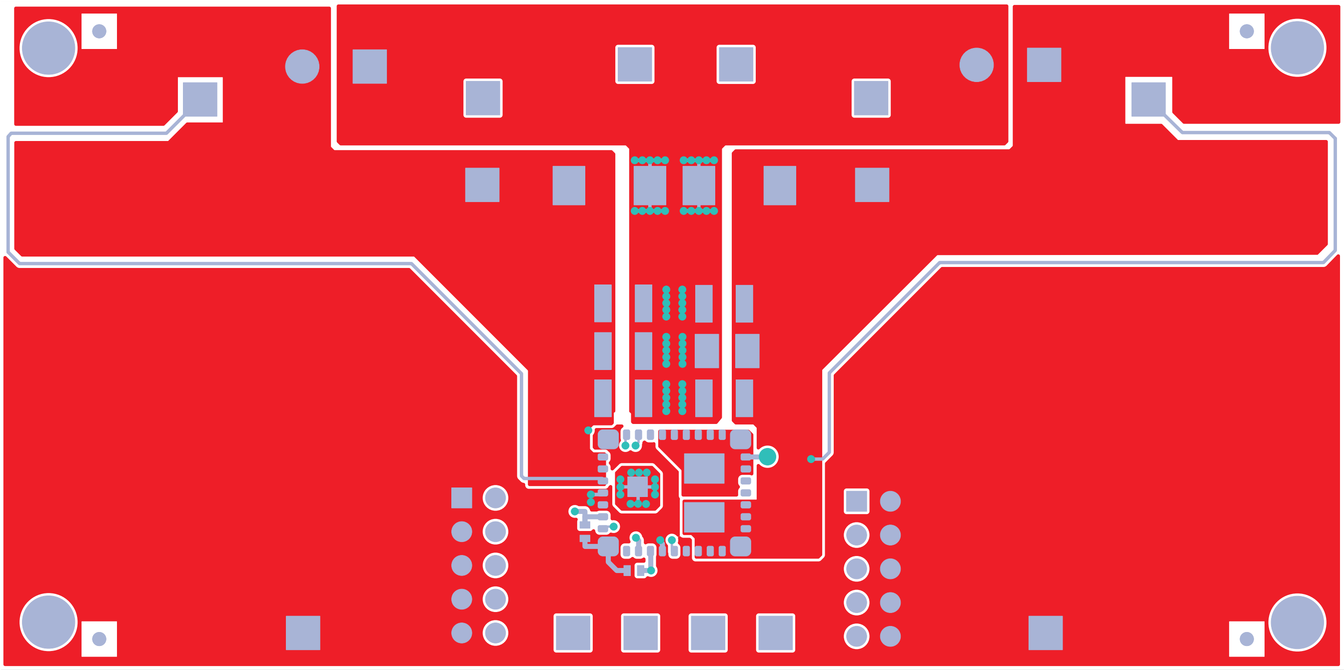

Figure 4. Top Layer

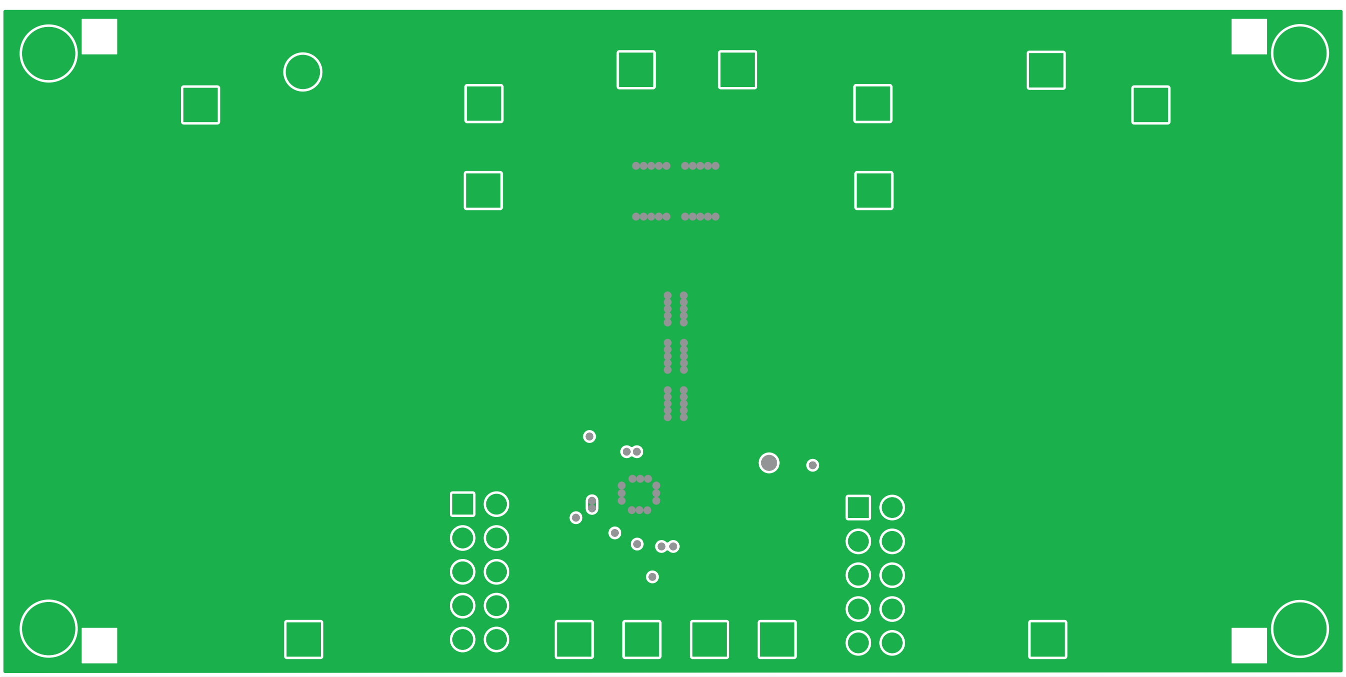

Figure 5. Internal 1 Layer

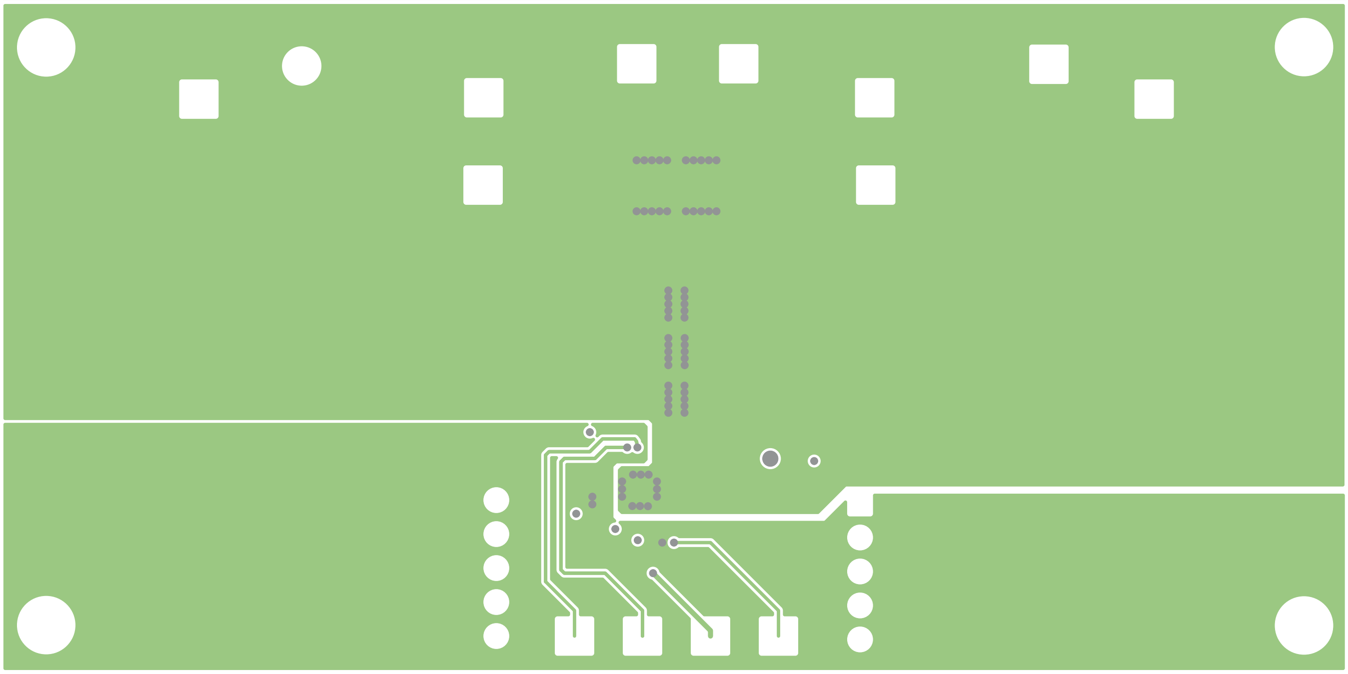

Figure 6. Internal 2 Layer

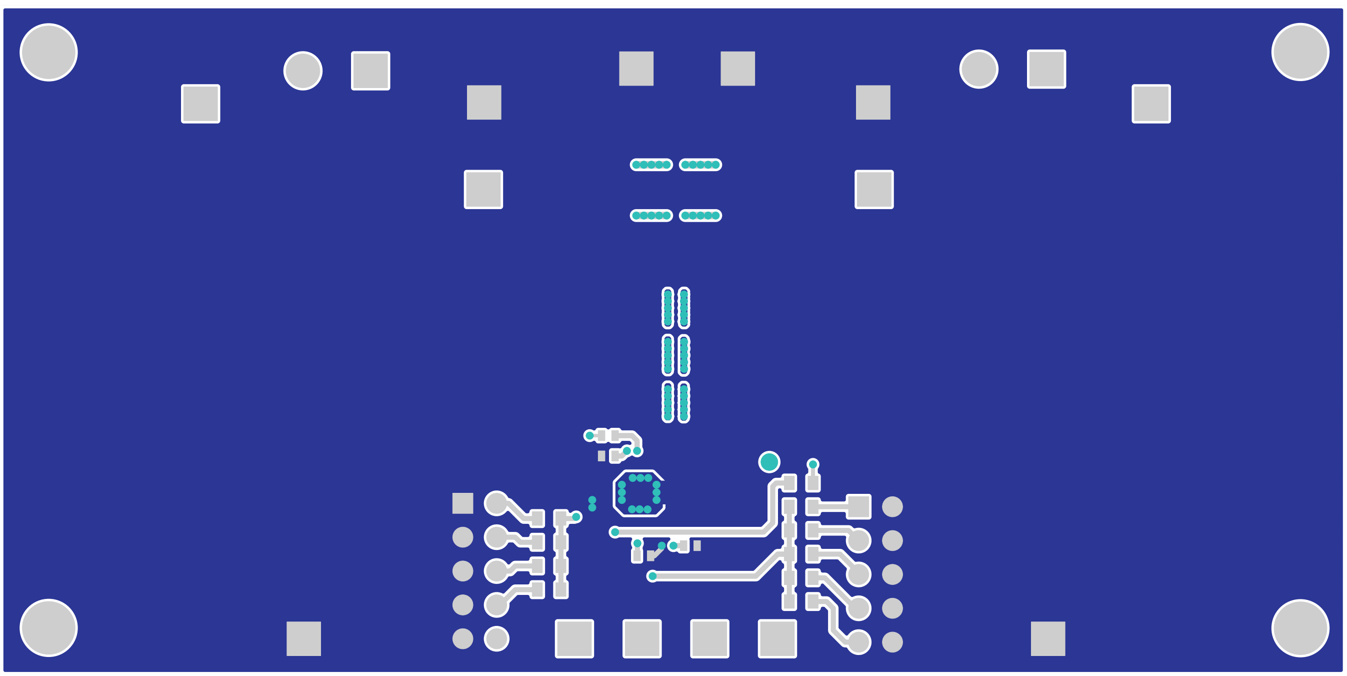

Figure 7. Bottom Layer

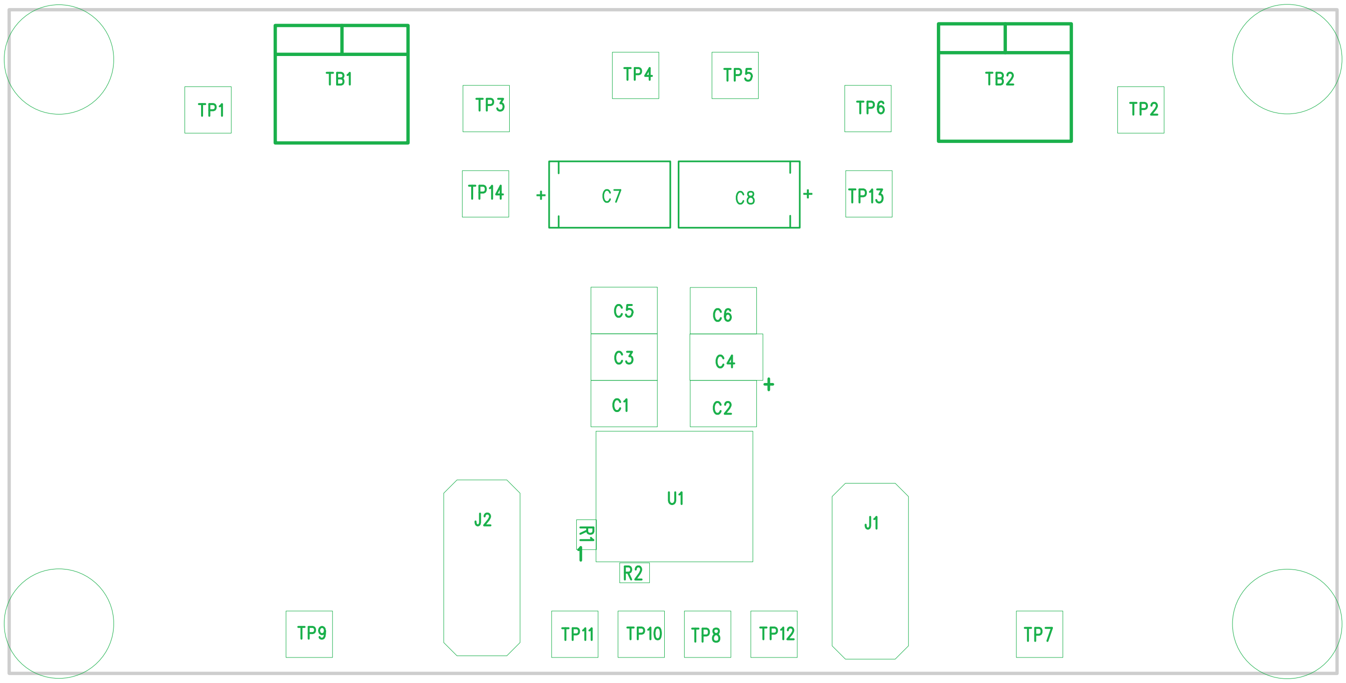

Figure 8. Top Assembly

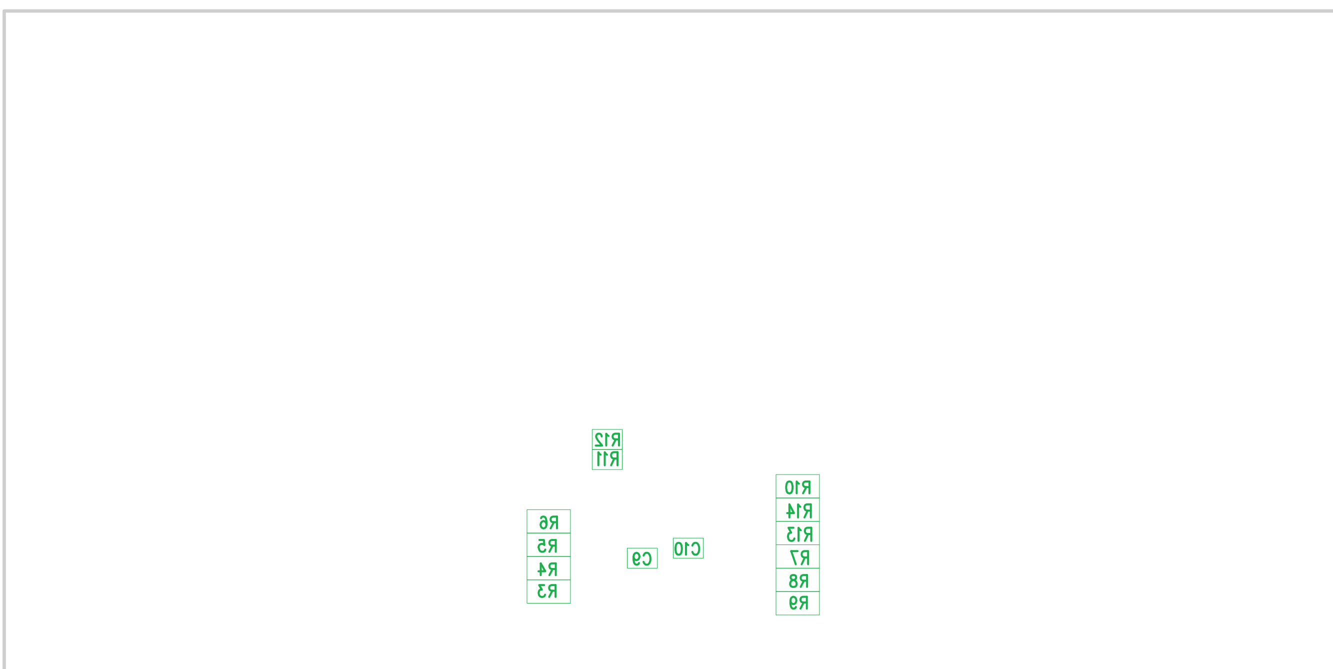

Figure 9. Bottom Layer

8 List of Material

Table 4. TPS84x10EVM-00x List of Material[(1)][(2)][(3)][(4)][(5)]

-003	-002	-001	REF DES	DESCRIPTION	Part Number	MFR
1	1	1	C1	Capacitor, ceramic, 10 V, x5R, 10%, 47 µF, 1210	GRM32ER61A476K	Murata
1	1	1	C2	Capacitor, ceramic, 6.3 V, x5R, 20%, 47 µF, 1210	GRM32ER60J476M	Murata
1	1	1	C7	Capacitor, polymer, 10 V, 20%, 220 µF, D3L	10TPE220ML	Sanyo
0	0	0	C8	Capacitor, polymer, 10 V, 20%, 220 µF, D3L	10TPE220ML	Sanyo
1	1	1	C4	Capacitor, polymer, 6.3 V, 20%, 100 µF, B2	6TPE100MPB	Sanyo
0	0	0	C3, C5, C6	Capacitor, ceramic, 0.1 µF, 1210	Std	STD
0	0	0	10	Capacitor, ceramic, 0.01 µF, 0402	STD	STD
2	2	2	J1-2	Header, male 2 x 5 pin, 100-mil spacing, 0.100 inch x 5 inch x 2 inch	PEC05DAAN	Sullins
1	1	1	R3	Resistor, chip, 1/16 W, 1%, 2.87 kΩ, 0603	STD	STD
1	1	1	R4	Resistor, chip, 1/16 W, 1%, 1.15 kΩ, 0603	STD	STD
1	1	1	R5	Resistor, chip, 1/16 W, 1%, 681 Ω, 0603	STD	STD
1	1	1	R6	Resistor, chip, 1/16 W, 1%, 464 Ω, 0603	STD	STD
1	1	1	R7	Resistor, chip, 1/16 W, 1%, 348 kΩ, 0603	STD	STD
1	1	1	R8	Resistor, chip, 1/16 W, 1%, 715 kΩ, 0603	STD	STD
1	1	1	R9	Resistor, chip, 1/16 W, 1%, 1.2 MΩ, 0603	STD	STD
1	1	1	R10	Resistor, chip, 1/16 W, 5%, 0 Ω, 0603	STD	STD
1	1	1	R13	Resistor, chip, 1/16 W, 1%, 174 kΩ, 0603	STD	STD
1	1	1	R14	Resistor, chip, 1/16 W, 1%, 113 kΩ, 0603	STD	STD
0	0	0	R1, R2, R11, R12	Resistor, chip, 1/16 W, 1%, 100 kΩ, 0402	Std	Std

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's component.
(5) Install label after final wash. Text shall be 8 pt font. Text shall be per Table 5.

Table 4. TPS84x10EVM-00x List of Material[(1)(2)(3)(4)(5)] (continued)

-003	-002	-001	REF DES	DESCRIPTION	Part Number	MFR
2	2	2	TB1-2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 inch x 0.35 inch	ED120/2DS	OST
8	8	8	TP1, TP2 TP8 TP10- TP14	Test point, white, thru hole, 5012, 0.125 inch x 0.125 inch	5012	Keystone
6	6	6	TP3-7 TP9	Test point, black, thru hole, 5011, 0.125 inch x 0.125 inch	5011	Keystone
0	0	1	U1	6-V input, 4-A Output Sync. Step-Down Converter with PWM, QFN	TPS84410RKG	TI
0	1	0	U1	6-V input, 2-A Output Sync. Step-Down Converter with PWM, QFN	TPS84210RKG	TI
1	0	0	U1	6-V input, 6-A Output Sync. Step-Down Converter with PWM, QFN	TPS84610RKG	TI
1	1	1		PCB, 0.063 inch H x 1.9 inch L x 3.9 inch W	PWR059	ANY
2	2	2		Conn jumper shorting gold flash	SPC02SYAN	Sullins
4	4	4		Bumpon hemisphere 0.44 inch x 0.20 inch clear, 0.440 inch Dia x 0.200 inch H	SJ-5303	3M

Table 5. Labeling

ASSEMBLY NUMBER	TExT
PWR059-001	TPS84410EVM-001
PWR059-002	TPS84210EVM-002
PWR059-003	TPS84610EVM-003

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 3 V to 6 V and the output voltage range of 0.8 V to 3.6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 40° C. The EVM is designed to operate properly with certain components above 80° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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