



## L6788A

### 3-phase controller with embedded drivers for the next GPU generation

#### Features

- 1, 2 or 3 selectable phase operation
- Phases self detection
- High current internal drivers
- Versatile solution: serial and parallel VID for output voltage setting
- Serial BUS interface for power manager and monitoring
- Automatic startup phase procedure
- Advanced IC and VRM thermal management to assure robust design and safe operation
- 5 V LDO regulator output to increases design flexibility.
- Adjustable and precise output voltage
- Full differential current sense across inductor
- Differential remote voltage sensing
- LSLess startup to manage pre-biased output
- Programmable overcurrent protection
- Adjustable switching frequency
- Enable signal
- VPQFN40 6x6 mm package with exposed pad

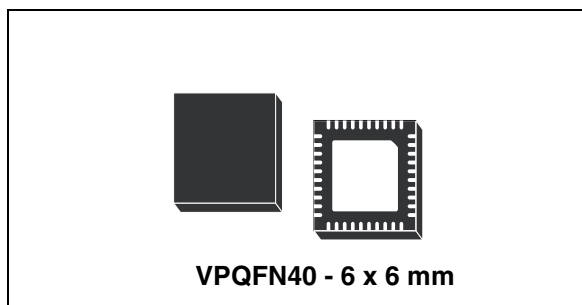
#### Applications

- Graphic card GPU supply
- High current DC-DC converters

#### Description

The device implements a one-to-three phases step-down controller with three integrated high current drivers in a compact 6x6 mm body package with exposed pad.

Output voltage can be selected trough serial and parallel VID up to 1.3500 V and managing D-VID with  $\pm 2\%$  output voltage accuracy.



The device manages serial BUS communication to program power management functionalities as well as monitoring.

The device features automatic startup phase procedure and phases self detection for safe operation.

The controller embeds 5 V LDO regulator increasing design flexibility.

Advanced IC and VRM thermal management to assure robust design and safe operation.

The controller assures fast protection against load overcurrent and under / overvoltage.

L6788A is available in VPQFN 6 x 6 mm package.

**Table 1. Device summary**

| Order code | Package | Packing       |
|------------|---------|---------------|
| L6788A     | VPQFN40 | Tray          |
| L6788ATR   | VPQFN40 | Tape and reel |

# Contents

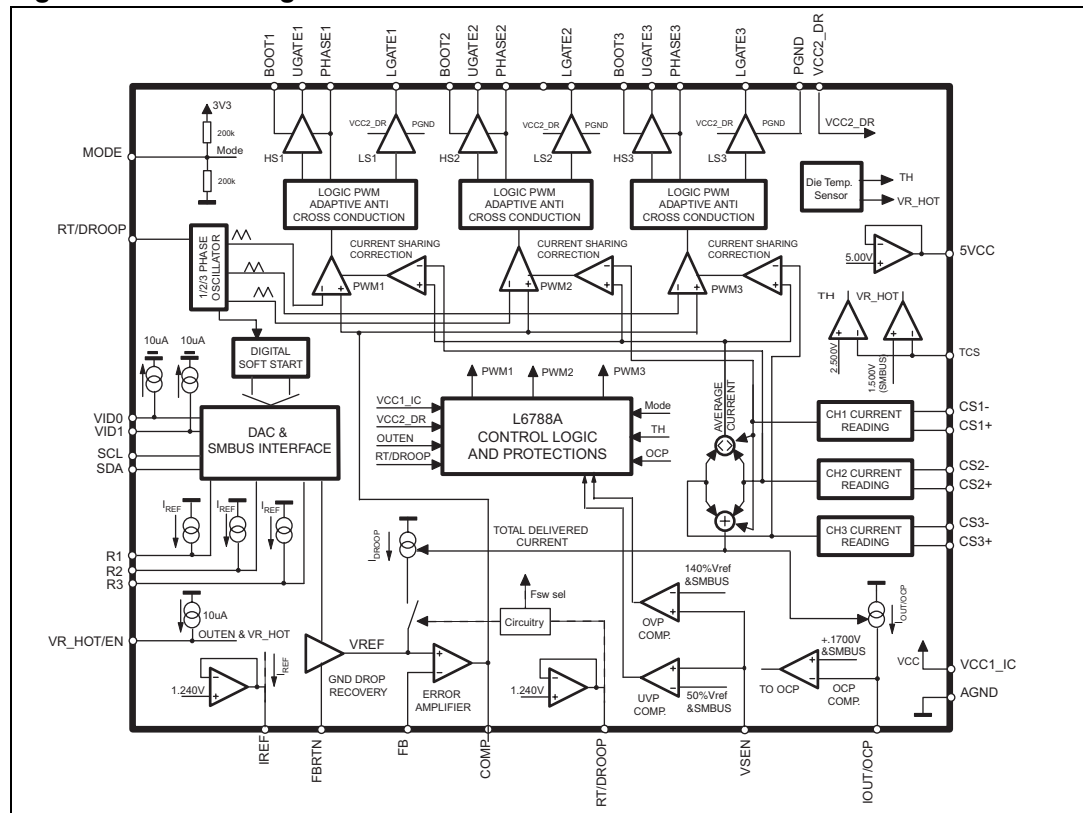
|          |  |           |
|----------|--|-----------|
| <b>1</b> | <b>Application circuit and block diagram</b>   | <b>3</b>  |
| 1.1      | Principle application circuit                  | 3         |
| 1.2      | Block diagram                                  | 4         |
| <b>2</b> | <b>Pins description and connection diagram</b> | <b>5</b>  |
| 2.1      | Pin description                                | 5         |
| <b>3</b> | <b>Maximum ratings</b>                         | <b>10</b> |
| 3.1      | Thermal data                                   | 10        |
| 3.2      | Absolute maximum ratings                       | 10        |
| <b>4</b> | <b>Electrical specifications</b>               | <b>11</b> |
| 4.1      | Electrical characteristics                     | 11        |
| <b>5</b> | <b>Mechanical data and package dimensions</b>  | <b>16</b> |
| <b>6</b> | <b>Revision history</b>                        | <b>17</b> |

### 1.1 Principle application circuit

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## 1.2 Block diagram

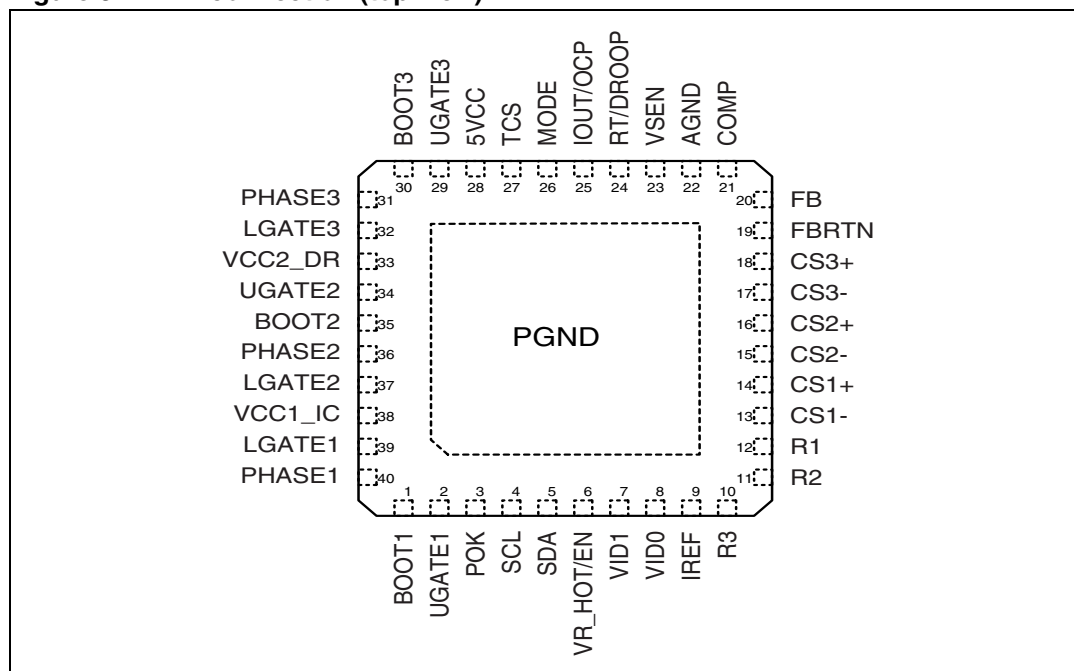
Figure 2. Block diagram



a. Refer to the application note for the reference schematic

## 2 Pins description and connection diagram

Figure 3. Pin connection (top view)



### 2.1 Pin description

Table 2. Pin description

| Pin n° | Name   | Description  |
|--------|--------|--|
| 1      | BOOT1  | Channel 1 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE1<br>Needed external bootstrap diode.<br>The device implements Vin detections through this pin. See “vin detection” section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see reference schematic). |
| 2      | UGATE1 | Channel 1 HS driver output. It must be connected to the HS1 MOSFET gate.<br>A small series resistors helps in reducing device-dissipated power.  |
| 3      | POK    | Power OK<br>Open drain output sets free after soft start has finished and pulled low when triggering any latched protection (OVP, UVP, OCP average).<br>Pull up to a voltage lower than 3.3 V (typ), if not used it can be left floating.  |
| 4      | SCL    | Serial BUS clock input.  |
| 5      | SDA    | Serial BUS data input.   |

Table 2. Pin description (continued)

| Pin n° | Name          | Description   |
|--------|---------------|---|
| 6      | VR_HOT/<br>EN | <p>Voltage regulator HOT / enable pin. Internally pulled up by 10 <math>\mu</math>A (typ) to 3.3 V. Multifunction pin to enable/disable the system (input-signal) and to provide the information about the warning temperature (output-signal).</p> <p>Forced low, the device stops operations with all MOSFETs OFF: all the latched protections are disabled. Removing the short on VR_HOT/EN pin, the device starts-up implementing soft-start and the voltage at the pin is clamped by the device at 1.5 V (typ). When a warning temperature is detected the device leaves the pin floating.</p> <p>Thermal monitoring enabled if <math>V_{CC} &gt; UVLOVCC</math> (See "thermal monitoring" section for details).</p> <p>VR_HOT/EN pin is set free when:</p> <ul style="list-style-type: none"> <li>• Either TCS pin voltage overcomes the warning threshold voltage (see TCS pin for details).</li> <li>• Or <math>T_{j\_IC}</math> Die temperature overcomes the die warning temperature (<math>T_{HOT}</math>) Where <math>T_{HOT} = T_{Shutdown} - T_{Delta}</math></li> </ul> <p>Use a pull-up resistor in the range of 10 k<math>\Omega</math>–30 k<math>\Omega</math> when VR_HOT/EN pin is directly pulled up to 3.3 V. (see VR_HOT/EN pin voltage Electrical Characteristic table).</p> <p>Cycle this pin to recover latch from protections.</p> |
| 7      | VID1          | <p>Voltage identification pins. Internally pulled low by 10 <math>\mu</math>A.</p> <p>They allow programming output voltage from the 4-level "power play table" in PVID mode.</p>   |
| 8      | VID0          |   |
| 9      | IREF          | <p>Current reference pin.</p> <p>Internally fixed at 1.240 V, connecting a <math>R_{IREF} = 12.4 \text{ k}\Omega</math> (+/-0.1%) resistor vs. AGND allows setting 100 <math>\mu</math>A current that is mirrored into R1, R2, R3 pins in order to program the three power play table levels voltage. See "power play table level" section for details.</p>   |
| 10     | R3            | <p>Default "power play table" voltage setting pins.</p> <p>The device sources from each Rx pin the same constant current sourced from the IREF pin ( Internally mirrored). As a consequence the Voltage between Rx pin and AGND is given by the following relationship: <math>V_{Rx} = I_{REF} \cdot R_x = 100 \mu\text{A} \cdot R_x</math>, where IREF is the current programmed on IREF pin (100 <math>\mu</math>A). As soon as the ENABLE is released the device reads the Rx pin voltage and it stores these value. As a consequence if the power play table is re-written by serial BUS the analog values can not be recovered (voltage fixed by Rx resistor). See "power play table level" section for details.</p>   |
| 11     | R2            |   |
| 12     | R1            |   |
| 13     | CS1-          | <p>Channel 1 current sense negative input.</p> <p>Connect through a <math>R_g</math> resistor to the output-side of the channel 1 inductor.</p>   |
| 14     | CS1+          | <p>Channel 1 current sense positive input.</p> <p>Connect through an R-C filter to the phase-side of the channel 1 inductor.</p>  |
| 15     | CS2-          | <p>Channel 2 current sense negative input.</p> <p>Connect through a <math>R_g</math> resistor to the output-side of the channel 2 inductor. Still connect to <math>V_{OUT}</math> through <math>R_g</math> resistor when using 1-phase operation.</p>   |

**Table 2. Pin description (continued)**

| Pin n° | Name         | Description  |
|--------|--------------|--|
| 16     | CS2+         | Channel 2 current sense positive input.<br>Connect through an R-C filter to the phase-side of the channel 2 inductor.<br>Short to V <sub>OUT</sub> when using 1-Phase operation.   |
| 17     | CS3-         | Channel 3 current sense negative input.<br>Connect through a R <sub>g</sub> resistor to the output-side of the channel 3 inductor.<br>Still connect to V <sub>OUT</sub> through R <sub>g</sub> resistor when using 1 or 2-phase operation.   |
| 18     | CS3+         | Channel 3 current sense positive input.<br>Connect through an R-C filter to the phase-side of the channel 3 inductor.<br>Short to V <sub>OUT</sub> when using 1 or 2-phase operation.  |
| 19     | FBRN         | Feedback return.<br>This pin is the ground return for remote sensing the output voltage.<br>Connect directly to the point where the output voltage is to be regulated.   |
| 20     | FB           | Error amplifier inverting input pin.<br>Connect with a resistor R <sub>FB</sub> vs. V <sub>SEN</sub> and with an RF - CF//CP vs. COMP pin.<br>See reference schematic for more details.<br>A current proportional to the load current can be sourced (in according to RT/DROOP pin status) from this pin in order to implement the droop effect.<br>See “droop function” section for details.  |
| 21     | COMP         | Error amplifier output. Connect with an RF - CF//CP vs. FB pin.  |
| 22     | AGND         | Signal ground pin. All the internal references are referred to this pin.<br>Connect it to the PCB signal ground (AGND).  |
| 23     | VSEN         | Output voltage monitor, manages OVP/UVP protections.<br>Connect to the positive side of the load to perform remote sense.<br>See “output voltage protections” section for more details.  |
| 24     | RT/<br>DROOP | Operation frequency setting.<br>Internally fixed at 1.240 V it allows programming the switching frequency F <sub>SW</sub> of each channel.<br>Frequency is programmed according to the R <sub>osc</sub> resistor connected from the pin vs. AGND with a gain of 9 kHz/μA. Leaving the pin floating programs a switching frequency of 200 kHz per phase.<br>The device uses this pin also to enable/disable the droop function.<br>See “droop function” section for details.  |
| 25     | IOUT/OCP     | Output current indication and over current protection setting.<br>The device sources from this pin a current proportional to the load current [(DCR/R <sub>g</sub> )*I <sub>OUT</sub> ].<br>Connect a resistor from this pin to AGND to program the over current protection level.<br>This pin is also used as output current indication. Voltage measured at this pin is proportional to the output current. External NTC can be used for temperature compensation of OCP and IOUT readings. See “over current protection” section for details. |

**Table 2. Pin description (continued)**

| Pin n° | Name    | Description  |
|--------|---------|--|
| 26     | MODE    | Phase Number selection pin. The maximum voltage on mode pin has to be limited to 3.6 V.<br>The voltage on MODE pin is used to select the number of phase used during normal operation. The device has an internal resistor divider in order to have 1.7 V on MODE pin when it is left floating. See "phase number selection" section for more details.       |
| 27     | TCS     | Temperature sense input pin.<br>Connecting the PTC network between 5 VCC and AGND in order to generate on TCS pin a voltage proportional to the temperature.<br>The device reads the TCS pin voltage and compare it with two thresholds in order to implements the warning and shutdown temperature action.<br>See "thermal monitoring" section for details. |
| 28     | 5VCC    | 5 VCC pin. The pin output is 5 V voltage with a minimum of 20 mAdc.<br>The device supply the 5 VCC if VCC1_IC pin voltage is higher than 8 (typ).<br>Filter the 5 VCC pin with a capacitor (470 nFMIN - 2.2 $\mu$ F MAX) versus PGND.  |
| 29     | UGATE3  | Channel 3 HS driver output. It must be connected to the HS3 MOSFET gate. A small series resistors helps in reducing device-dissipated power.   |
| 30     | BOOT3   | Channel 3 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE3<br>Needed external bootstrap diode.<br>The device implements Vin detections through this pin. see "vin detection" section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see reference schematic).                   |
| 31     | PHASE3  | Channel 3 HS driver return path. Connected to the HS3 MOSFET source and provides return path for the HS driver of channel 3.   |
| 32     | LGATE3  | Channel 3 LS driver output. Driver can support 12 V bus voltage. A small series resistor helps in reducing device-dissipated power.  |
| 33     | VCC2_DR | LS driver supply. Driver can support 12 V bus voltage.<br>Connect to 12 V_BUS and filter with RC network.<br>(Suggested value: R = 2.2 /0805 size; C=2x1 $\mu$ F MLCC capacitor vs. PGND).   |
| 34     | UGATE2  | Channel 2 HS driver output. It must be connected to the HS2 MOSFET gate. A small series resistors helps in reducing device-dissipated power.   |
| 35     | BOOT2   | Channel 2 HS driver supply. Connect through a capacitor (100 nF typ.) to PHASE2<br>Needed external bootstrap diode.<br>The device implements Vin detections through this pin. See "vin detection" section for details. A small resistor in series to the boot diode helps in reducing Boot capacitor overcharge (see Reference schematic).                   |
| 36     | PHASE2  | Channel 2 HS driver return path. Connected to the HS2 MOSFET source and provides return path for the HS driver of channel 2.   |
| 37     | LGATE2  | Channel 2 LS driver output. Driver can support 12 V bus voltage. A small series resistor helps in reducing device-dissipated power.  |



**Table 2. Pin description (continued)**

| Pin n° | Name    | Description  |
|--------|---------|--|
| 38     | VCC1_IC | Device supply voltage pin. The operative supply voltage is 12 V $\pm$ 10%.<br>Connect to 12 V_BUS and filter with RC network (R = 2.2 /0603 size, and C=1x1 $\mu$ F MLCC capacitor vs. PGND).  |
| 39     | LGATE1  | Channel 1 LS driver output. Driver can support 12 V bus voltage.<br>A small series resistor helps in reducing device-dissipated power.   |
| 40     | PHASE1  | Channel 1 HS driver return path. Connected to the HS1 MOSFET source and provides return path for the HS driver of channel 1.   |
| 41     | PGND    | Power ground pin (LS drivers return path). Connect to power ground plane.<br>Exposed pad connects also the silicon substrate. As a consequence it makes a good thermal contact with the PCB to dissipate the power necessary to drive the external MOSFETs. Connect it to the power ground plane using 4.2x4.2 mm square area on the PCB and with sixteen vias to improve electrical and thermal conductivity. |

## 3 Maximum ratings

### 3.1 Thermal data

**Table 3. Thermal data**

| Symbol     | Parameter  | Value      | Unit   |
|------------|--|------------|--------|
| $R_{thJA}$ | Thermal resistance junction to ambient<br>(Device soldered on 2s2p PC board) | 35         | °C / W |
| $R_{thJC}$ | Thermal resistance junction to case  | 1          | °C / W |
| $T_{MAX}$  | Maximum junction temperature   | 150        | °C     |
| $T_{stg}$  | Storage temperature range  | -40 to 150 | °C     |
| $T_J$      | Junction temperature range   | 0 to 125   | °C     |

### 3.2 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol                     | Parameter  | Value                | Unit |
|----------------------------|--|----------------------|------|
| $V_{CC1\_IC}, V_{CC2\_DR}$ | To PGNDx   | 15                   | V    |
| $V_{BOOTx}-V_{PHASEx}$     | Boot voltage   | 15                   | V    |
| $V_{UGATEx}-V_{PHASEx}$    |  | 15                   | V    |
|                            | LGATEx to PGND   | -0.3 to $V_{CC}+0.3$ | V    |
|                            | 5VCC to PGND   | -0.3 to 7            | V    |
|                            | SCL, SDA to PGND   | -0.3 to 5.5          | V    |
|                            | All other pins to PGND   | -0.3 to 3.6          | V    |
| $V_{PHASEx}$               | Negative peak voltage to PGND; $T < 400$ ns<br>$V_{CC1\_IC} = V_{CC2\_DR} = 12$ V; $V_{BOOTx} = 8.5$ V | -8                   | V    |
|                            | Positive peak voltage to PGND;<br>$V_{CC1\_IC} = V_{CC2\_DR} = 15$ V; $V_{BOOTx} = 41$ V               | 26                   | V    |

## 4 Electrical specifications

### 4.1 Electrical characteristics

$V_{CC} = 12\text{ V} \pm 15\%$ ,  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 5. Electrical characteristics**

| Symbol   | Parameter  | Test condition   | Min. | Typ. | Max. | Unit          |
|--|--|--|------|------|------|---------------|
| <b>Supply voltages operating conditions</b>    |  |  |      |      |      |               |
| $V_{CC1\_IC}$                                  | Device supply voltage                            |  | 10.8 | 12   | 13.2 | V             |
| $V_{CC2\_DR}$                                  | LS driver supply voltage                         |  | 10.8 | 12   | 13.2 | V             |
| $V_{sources}$ (VIN)                            | Conversion input voltage                         | $V_{source1} = V_{source2}$  | 10.8 |      | 13.2 | V             |
| $V_{source1} - V_{source2}$                    | BOOTx supply current                             | Max difference between conversion input voltages (static condition)                                    |      |      | 2.4  | V             |
| <b>Supply current and power-on</b>             |  |  |      |      |      |               |
| $I_{CC1\_IC}$                                  | VCC1_IC supply current                           | UGATEx and LGATEx OPEN;<br>$V_{CC1\_IC} = V_{CC2\_DR} = V_{BOOTx} = 12\text{ V}$                       |      | 25   |      | mA            |
| $I_{CC2\_DR}$                                  | VCC2_DR supply current                           | LGATEx = OPEN;<br>$V_{CC1\_IC} = V_{CC2\_DR} = 12\text{ V}$  |      | 6    |      | mA            |
| $I_{BOOTx}$                                    | BOOTx supply current                             | UGATEx = OPEN; PHASEx to PGND;<br>$V_{CC1\_IC} = V_{CC2\_DR} = V_{BOOTx} = 12\text{ V}$                |      | 2    |      | mA            |
| $UVLO_{VCC\_IC}$                               | VCC1_IC turn-ON threshold                        | VCC1_IC rising;<br>$V_{CC2\_DR} = V_{CC1\_IC}$   |      | 7    |      | V             |
|  | VCC1_IC turn-OFF threshold                       | VCC1_IC falling;<br>$V_{CC2\_DR} = V_{CC1\_IC}$  |      | 5.8  |      | V             |
| $UVLO_{5VCC}$                                  | 5VCC turn-ON threshold                           | 5 VCC rising; $V_{CC1\_IC} = V_{CC2\_DR} > 7$  |      | 3    |      | V             |
|  | 5VCC turn-OFF threshold                          | 5 VCC falling; $V_{CC1\_IC} = V_{CC2\_DR} > 7$   |      | 1    |      | V             |
| <b>Oscillator, soft start time and inhibit</b> |  |  |      |      |      |               |
| $F_{OSC}$                                      | Default value                                    | RT = OPEN  |      | 200  |      | kHz           |
|  | Programmability range                            | RT connected to AGND   | 200  |      | 800  | kHz           |
| $T_{rp}$                                       | Soft start time                                  | $V_{CC1\_IC} = 12\text{ V}$ ; $5VCC = 5\text{ V}$ ;<br>$V_{OUT} = 1.350\text{ V}$ ; EN rising.         |      | 3    | 5    | ms            |
| $VR\_HOT/EN$                                   | ENABLE threshold                                 | Input low  |      |      | 0.7  | V             |
|  |  | Input high   | 1.3  |      |      | V             |
|  | Pull-Up current                                  | $VR\_HOT/EN$ to AGND   |      | 10   |      | $\mu\text{A}$ |
|  | Voltage at VR_HOT/EN pin during normal operation | $I_{VR\_HOT\_EN} = 50\text{ }\mu\text{A}$ to $150\text{ }\mu\text{A}$ ;<br>(current sunk by VR_HOT/EN) |      | 1.5  |      | V             |
| $\Delta V_{osc}$                               | Ramp amplitude                                   |  |      | 1.5  |      | V             |
| FAULT  | Voltage at pin RT pin                            | OVP, UVP and OCP avg and thermal shutdown active   |      | 3.3  |      | V             |

Table 5. Electrical characteristics (continued)

| Symbol                          | Parameter                                      | Test condition  | Min. | Typ.  | Max. | Unit |
|---------------------------------|--|---|------|-------|------|------|
| <b>Reference and DAC</b>        |  |   |      |       |      |      |
| V <sub>OUT</sub>                | Output voltage accuracy                        | V <sub>OUT</sub> > 0.800 V; R <sub>IREF</sub> =12.4 kΩ                    | -2   | -     | 2    | %    |
| I <sub>RX</sub>                 | R <sub>X</sub> source current                  | R <sub>IREF</sub> = 12.4 kΩ resistor to AGND.                             |      | 100   |      | μA   |
| V <sub>IREF</sub>               | IREF pin voltage                               | R <sub>IREF</sub> = 12.4 kΩ resistor to AGND.                             |      | 1.240 |      | V    |
| 5VCC                            | Accuracy                                       | I <sub>5VCC</sub> = 2 mA to 20 mA; C = 1 μF to PGND.                      | -2.5 |       | 2.5  | %    |
|                                 | Maximum output current                         | C = 1 μF to PGND.   | 25   |       |      | mA   |
| VID                             | VID threshold; PVID mode                       | Input low   |      |       | 0.7  | V    |
|                                 |  | Input high  | 1.3  |       |      | V    |
|                                 | Pull-down current                              | VIDx to 3.3 V   |      | 10    |      | μA   |
| <b>Protections</b>              |  |   |      |       |      |      |
| OCP <sub>AVG</sub>              | Over current threshold on total output current | I <sub>OUT</sub> /OCP rising  |      | 1.700 |      | V    |
| I <sub>OCTH</sub>               | Over current threshold for each phase          | I <sub>CSX</sub> rising;<br>R <sub>IREF</sub> = 12.4 kΩ resistor to AGND. |      | 33    |      | μA   |
| OVP                             | Over voltage threshold                         | VSEN rising;<br>% programmed reference voltage                            |      | 140   |      | %    |
| UVP                             | Under voltage threshold                        | VSEN falling;<br>% programmed reference voltage                           |      | 50    |      | %    |
| <b>Thermal monitor</b>          |  |   |      |       |      |      |
| V <sub>TCS</sub>                | OT warning                                     | TCS rising  |      | 1.500 |      | V    |
|                                 | OT shut down                                   | TCS rising  |      | 2.500 |      | V    |
| <b>Soft-start end indicator</b> |  |   |      |       |      |      |
| V <sub>POK</sub>                | POK low voltage                                | I = -4 mA   |      |       | 0.4  | V    |
| <b>Error amplifier</b>          |  |   |      |       |      |      |
| A <sub>O</sub>                  |  |   |      | 100   |      | dB   |
| GBWP                            | Gain bandwidth product                         |   |      | 15    |      | MHz  |
| SR                              | Slew rate                                      | COMP = 10 pF to AGND  |      | 2     |      | V/μs |
| <b>Gate drivers</b>             |  |   |      |       |      |      |
| I <sub>UGATEx</sub>             | High side source current                       | BOOTx-PHASEx = 12 V;<br>C <sub>UGATEx</sub> to PHASEx = 3.3 nF            |      | 1.5   |      | A    |
| R <sub>UGATEx</sub>             | High side sink resistance                      | BOOTx-PHASEx = 12 V;  |      | 2     |      | Ω    |
| I <sub>LGATEx</sub>             | Low side source current                        | VCC1_IC=VCC2_DR = 12 V;<br>C <sub>LGATEx</sub> to PGND = 5.6 nF           |      | 2     |      | A    |
| R <sub>LGATEx</sub>             | Low side sink resistance                       | VCC1_IC = VCC2_DR = 12 V;   |      | 1     |      | Ω    |

**Table 6. GPU table for SVID mode**

| STEP | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VREF   |
|------|------|------|------|------|------|------|--------|
| 1    | 0    | 0    | 0    | 0    | 0    | 0    | 1.3500 |
| 2    | 0    | 0    | 0    | 0    | 0    | 1    | 1.3375 |
| 3    | 0    | 0    | 0    | 0    | 1    | 0    | 1.3250 |
| 4    | 0    | 0    | 0    | 0    | 1    | 1    | 1.3125 |
| 5    | 0    | 0    | 0    | 1    | 0    | 0    | 1.3000 |
| 6    | 0    | 0    | 0    | 1    | 0    | 1    | 1.2875 |
| 7    | 0    | 0    | 0    | 1    | 1    | 0    | 1.2750 |
| 8    | 0    | 0    | 0    | 1    | 1    | 1    | 1.2650 |
| 9    | 0    | 0    | 1    | 0    | 0    | 0    | 1.2500 |
| 10   | 0    | 0    | 1    | 0    | 0    | 1    | 1.2375 |
| 11   | 0    | 0    | 1    | 0    | 1    | 0    | 1.2250 |
| 12   | 0    | 0    | 1    | 0    | 1    | 1    | 1.2125 |
| 13   | 0    | 0    | 1    | 1    | 0    | 0    | 1.2000 |
| 14   | 0    | 0    | 1    | 1    | 0    | 1    | 1.1875 |
| 15   | 0    | 0    | 1    | 1    | 1    | 0    | 1.1750 |
| 16   | 0    | 0    | 1    | 1    | 1    | 1    | 1.1650 |
| 17   | 0    | 1    | 0    | 0    | 0    | 0    | 1.1500 |
| 18   | 0    | 1    | 0    | 0    | 0    | 1    | 1.1375 |
| 19   | 0    | 1    | 0    | 0    | 1    | 0    | 1.1250 |
| 20   | 0    | 1    | 0    | 0    | 1    | 1    | 1.1125 |
| 21   | 0    | 1    | 0    | 1    | 0    | 0    | 1.1000 |
| 22   | 0    | 1    | 0    | 1    | 0    | 1    | 1.0875 |
| 23   | 0    | 1    | 0    | 1    | 1    | 0    | 1.0750 |
| 24   | 0    | 1    | 0    | 1    | 1    | 1    | 1.0650 |
| 25   | 0    | 1    | 1    | 0    | 0    | 0    | 1.0500 |
| 26   | 0    | 1    | 1    | 0    | 0    | 1    | 1.0375 |
| 27   | 0    | 1    | 1    | 0    | 1    | 0    | 1.0250 |
| 28   | 0    | 1    | 1    | 0    | 1    | 1    | 1.0125 |
| 29   | 0    | 1    | 1    | 1    | 0    | 0    | 1.0000 |
| 30   | 0    | 1    | 1    | 1    | 0    | 1    | 0.9875 |
| 31   | 0    | 1    | 1    | 1    | 1    | 0    | 0.9750 |
| 32   | 0    | 1    | 1    | 1    | 1    | 1    | 0.9650 |
| 33   | 1    | 0    | 0    | 0    | 0    | 0    | 0.9500 |

**Table 6. GPU table for SVID mode (continued)**

| STEP | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | VREF   |
|------|------|------|------|------|------|------|--------|
| 34   | 1    | 0    | 0    | 0    | 0    | 1    | 0.9375 |
| 35   | 1    | 0    | 0    | 0    | 1    | 0    | 0.9250 |
| 36   | 1    | 0    | 0    | 0    | 1    | 1    | 0.9125 |
| 37   | 1    | 0    | 0    | 1    | 0    | 0    | 0.9000 |
| 38   | 1    | 0    | 0    | 1    | 0    | 1    | 0.8875 |
| 39   | 1    | 0    | 0    | 1    | 1    | 0    | 0.8750 |
| 40   | 1    | 0    | 0    | 1    | 1    | 1    | 0.8650 |
| 41   | 1    | 0    | 1    | 0    | 0    | 0    | 0.8500 |
| 42   | 1    | 0    | 1    | 0    | 0    | 1    | 0.8375 |
| 43   | 1    | 0    | 1    | 0    | 1    | 0    | 0.8250 |
| 44   | 1    | 0    | 1    | 0    | 1    | 1    | 0.8125 |
| 45   | 1    | 0    | 1    | 1    | 0    | 0    | 0.8000 |
| 46   | 1    | 0    | 1    | 1    | 0    | 1    | 0.7875 |
| 47   | 1    | 0    | 1    | 1    | 1    | 0    | 0.7750 |
| 48   | 1    | 0    | 1    | 1    | 1    | 1    | 0.7650 |
| 49   | 1    | 1    | 0    | 0    | 0    | 0    | 0.7500 |
| 50   | 1    | 1    | 0    | 0    | 0    | 1    | 0.7375 |
| 51   | 1    | 1    | 0    | 0    | 1    | 0    | 0.7250 |
| 52   | 1    | 1    | 0    | 0    | 1    | 1    | 0.7125 |
| 53   | 1    | 1    | 0    | 1    | 0    | 0    | 0.7000 |
| 54   | 1    | 1    | 0    | 1    | 0    | 1    | 0.6875 |
| 55   | 1    | 1    | 0    | 1    | 1    | 0    | 0.6750 |
| 56   | 1    | 1    | 0    | 1    | 1    | 1    | 0.6650 |
| 57   | 1    | 1    | 1    | 0    | 0    | 0    | 0.6500 |
| 58   | 1    | 1    | 1    | 0    | 0    | 1    | 0.6375 |
| 59   | 1    | 1    | 1    | 0    | 1    | 0    | 0.6250 |
| 60   | 1    | 1    | 1    | 0    | 1    | 1    | 0.6125 |
| 61   | 1    | 1    | 1    | 1    | 0    | 0    | 0.6000 |
| 62   | 1    | 1    | 1    | 1    | 0    | 1    | 0.5875 |
| 63   | 1    | 1    | 1    | 1    | 1    | 0    | 0.5750 |
| 64   | 1    | 1    | 1    | 1    | 1    | 1    | 0.5625 |

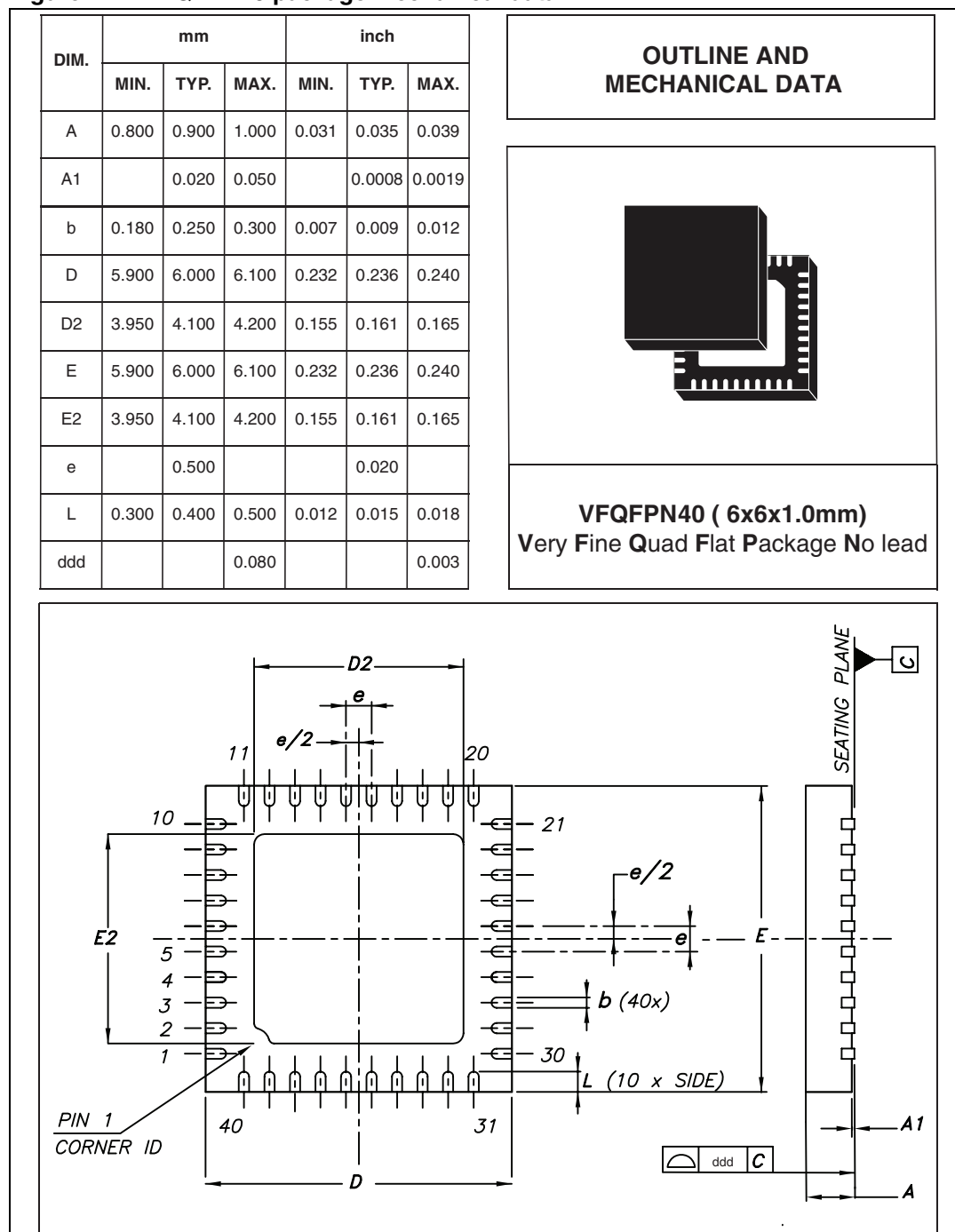
**Table 7. PVID mode table**

| VID1 (pin) | VID0 (pin) | Selected dynamic voltage table (DVT) level | Resistor strap |
|------------|------------|--|----------------|
| 0          | 0          | Level 1                                    | R1             |
| 0          | 1          | Level 2                                    | R2             |
| 1          | 0          | Level 3                                    | R3             |
| 1          | 1          | Level 4                                    | R3             |

## 5 Mechanical data and package dimensions

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**Figure 4. VFQFPN40 package mechanical data**





## 6 Revision history

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**Table 8. Document revision history**

| Date        | Revision | Changes                                    |
|-------------|----------|--|
| 27-Jan-2009 | 1        | Initial release                            |
| 22-Jul-2009 | 2        | Updated <a href="#">Figure 2 on page 4</a> |

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