

## Low Phase Noise VCXO with multipliers (for 100-200MHz Fund Xtal)

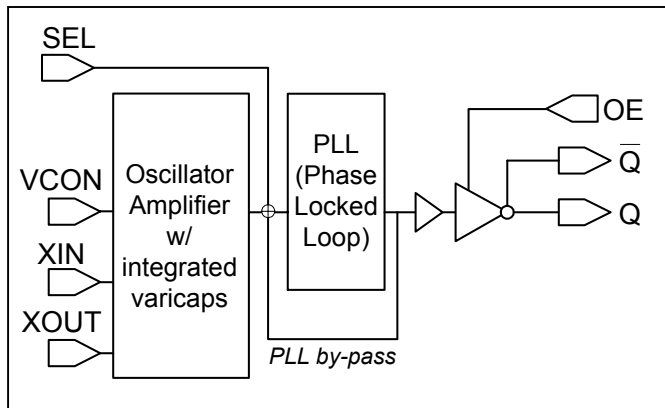
### FEATURES

- 100MHz to 200MHz Fundamental Mode Crystal.
- Output range: 100 – 200MHz (no multiplication), 200 – 400MHz (2x multiplier), 400 – 800MHz (4x multiplier), or 800MHz – 1GHz (PLL520-09 TSSOP only, 8x multiplier).
- High yield design supports up to 2pF stray capacitance at 200MHz.
- CMOS (Standard drive PLL520-07 or Selectable Drive PLL520-06), PECL (Enable low PLL520-08 or Enable high PLL520-05) or LVDS output (PLL520-09).
- Integrated variable capacitors.
- Supports 3.3V-Power Supply.
- Available in 16-Pin (TSSOP or 3x3mm QFN)  
Note: PLL520-06 only available in 3x3mm.  
Note: PLL520-07 only available in TSSOP.

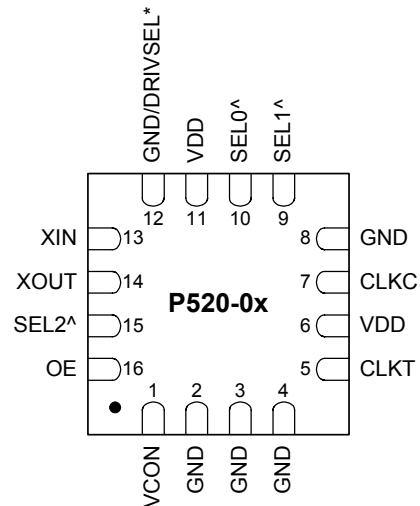
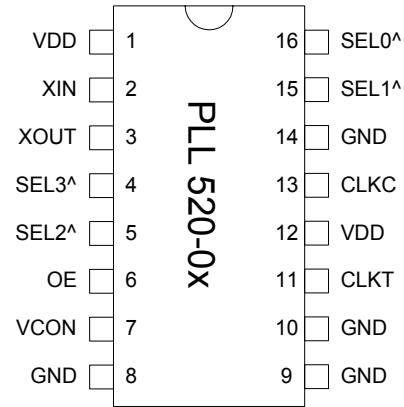
### DESCRIPTION

The PLL520-05/-06/-07/-08/-09 is a family of VCXO ICs specifically designed to pull high frequency fundamental crystals. Their design was optimized to tolerate higher limits of interelectrode capacitance and bonding capacitance to improve yield. They achieve very low current into the crystal resulting in better overall stability. Their internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

### BLOCK DIAGRAM



### PIN CONFIGURATION (Top View)



^: Internal pull-up

\*: PLL520-06 pin 12 is output drive select (DRIVSEL)  
(0 for High Drive CMOS, 1 for Standard Drive CMOS)

### OUTPUT ENABLE LOGICAL LEVELS

| Part #   | OE          | State          |
|--|-------------|----------------|
| PLL520-08  | 0 (Default) | Output enabled |
|  | 1           | Tri-state      |
| PLL520-05<br>PLL520-06<br>PLL520-07<br>PLL520-09 | 0           | Tri-state      |
|  | 1 (Default) | Output enabled |

OE input: Logical states defined by PECL levels for PLL520-08  
Logical states defined by CMOS levels for PLL520-05/-06/-07/-09

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### PIN DESCRIPTIONS

| Name      | TSSOP*<br>Pin number | 3x3mm QFN*<br>Pin number | Type | Description  |
|-----------|----------------------|--------------------------|------|--|
| XIN       | 2                    | 13                       | I    | Crystal in connector.  |
| XOUT      | 3                    | 14                       | I    | Crystal out connector.   |
| OE        | 6                    | 16                       | I    | Output enable pin.   |
| VCON      | 7                    | 1                        | I    | Frequency control input (0.3V to 3.0V)   |
| GND       | 8,9, 10, 14          | 2,3,4,8,12               | P    | Ground (except pin 12 on PLL520-06: DRIVSEL see below).  |
| DRIVSEL** | -                    | 12                       | I    | PLL520-06 only: Drive Select Input. This pin has an internal pull-up that will default DRIVSEL to '1' when not connect to GND. CMOS output of PLL520-06 will be high drive CMOS when DRIVSEL is set to '0', and will be standard CMOS otherwise. |
| CLKT      | 11                   | 5                        | O    | True output PECL (PLL520-08) or LVDS (PLL520-09) (N/C for PLL520-07)   |
| CLKC      | 13                   | 7                        | O    | Complementary output PECL (PLL520-08) or LVDS (PLL520-09) (CMOS out for PLL520-07).  |
| SEL0      | 16                   | 10                       | I    | Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.  |
| SEL1      | 15                   | 9                        | I    |  |
| SEL2      | 5                    | 15                       | I    |  |
| SEL3      | 4                    | Not available            | I    |  |
| VDD       | 1, 12                | 6,11                     | P    | +3.3V power supply.  |

\* Note: PLL520-06 only available in 3x3mm QFN, PLL520-07 only available in TSSOP.

\*\* Note: DRIVSEL on pin 12 on PLL520-06 only.

### FREQUENCY SELECTION TABLE

| SEL3* | SEL2 | SEL1 | SEL0 | Selected Multiplier               |
|-------|------|------|------|-----------------------------------|
| 0*    | 0    | 1    | 1    | Fin x 8 (PLL520-09 in TSSOP only) |
| 1*    | 0    | 1    | 1    | Fin x 4                           |
| 1*    | 1    | 1    | 0    | Fin x 2                           |
| 1*    | 1    | 1    | 1    | No multiplication                 |

**Note** \*: SEL3 is not available (always "1") in 3x3mm package

All pins have internal pull-ups (default value is 1). Connect to GND to set to 0.

## Low Phase Noise VCXO with multipliers (for 100-200MHz Fund Xtal)

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

| PARAMETERS                        | SYMBOL          | MIN. | MAX.                 | UNITS |
|-----------------------------------|-----------------|------|----------------------|-------|
| Supply Voltage                    | V <sub>DD</sub> |      | 4.6                  | V     |
| Input Voltage, dc                 | V <sub>I</sub>  | -0.5 | V <sub>DD</sub> +0.5 | V     |
| Output Voltage, dc                | V <sub>O</sub>  | -0.5 | V <sub>DD</sub> +0.5 | V     |
| Storage Temperature               | T <sub>S</sub>  | -65  | 150                  | °C    |
| Ambient Operating Temperature*    | T <sub>A</sub>  | -40  | 85                   | °C    |
| Junction Temperature              | T <sub>J</sub>  |      | 125                  | °C    |
| Lead Temperature (soldering, 10s) |                 |      | 260                  | °C    |
| ESD Protection, Human Body Model  |                 |      | 2                    | kV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

#### 2. Crystal Specifications

| PARAMETERS                  | SYMBOL                                | CONDITIONS                | MIN. | MAX. | UNITS |
|-----------------------------|---------------------------------------|---------------------------|------|------|-------|
| Crystal Resonator Frequency | F <sub>XIN</sub>                      | Parallel Fundamental Mode | 100  | 200  | MHz   |
| Crystal Loading Rating      | C <sub>L (xtal)</sub>                 | Die at VCON = 1.65V       |      | 4    | pF    |
| Interelectrode Capacitance  | C <sub>0</sub>                        |                           |      | 3.5  | pF    |
| Crystal Pullability         | C <sub>0</sub> /C <sub>1 (xtal)</sub> | AT cut                    |      | 250  | -     |
| Recommended ESR             | R <sub>E</sub>                        | AT cut                    |      | 30   | Ω     |

#### 3. Voltage Controlled Crystal Oscillator

| PARAMETERS                     | SYMBOL               | CONDITIONS  | MIN.  | TYP.    | MAX. | UNITS |
|--------------------------------|----------------------|---|-------|---------|------|-------|
| VCXO Stabilization Time *      | T <sub>VCXOSTB</sub> | From power valid  |       |         | 10   | ms    |
| VCXO Tuning Range              |                      | F <sub>XIN</sub> = 100 – 200MHz;<br>XTAL C <sub>0</sub> /C <sub>1</sub> < 250<br>0V ≤ VCON ≤ 3.3V |       | 200*    |      | ppm   |
| CLK output pullability         |                      | VCON=1.65V, ±1.65V  | ±100* |         |      | ppm   |
| On-chip Varicaps control range |                      | VCON = 0 to 3.3V  |       | 4 – 18* |      | pF    |
| Linearity                      |                      |   |       |         | 10*  | %     |
| VCXO Tuning Characteristic     |                      |   |       | 65      |      | ppm/V |
| VCON input impedance           |                      |   |       | 60      |      | kΩ    |
| VCON modulation BW             |                      | 0V ≤ VCON ≤ 3.3V, -3dB  | 25    |         |      | kHz   |

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

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### 4. General Electrical Specifications

| PARAMETERS                      | SYMBOL          | CONDITIONS                      | MIN. | TYP. | MAX.      | UNITS |
|---------------------------------|-----------------|---------------------------------|------|------|-----------|-------|
| Supply Current (Loaded Outputs) | I <sub>DD</sub> | PECL/LVDS/CMOS                  |      |      | 100/80/40 | mA    |
| Operating Voltage               | V <sub>DD</sub> |                                 | 2.97 |      | 3.63      | V     |
| Output Clock Duty Cycle         |                 | @ 50% V <sub>DD</sub> (CMOS)    | 45   | 50   | 55        | %     |
|                                 |                 | @ 1.25V (LVDS)                  | 45   | 50   | 55        |       |
|                                 |                 | @ V <sub>DD</sub> - 1.3V (PECL) | 45   | 50   | 55        |       |
| Short Circuit Current           |                 |                                 |      | ±50  |           | mA    |

### 5. Jitter Specifications

| PARAMETERS                      | CONDITIONS   | MIN. | TYP. | MAX. | UNITS |
|---------------------------------|--|------|------|------|-------|
| Period jitter RMS               | At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles     |      | 2.5  |      | ps    |
| Period jitter peak-to-peak      |  |      | 18.5 | 20   |       |
| Accumulated jitter RMS          | At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles. |      | 2.5  |      | ps    |
| Accumulated jitter peak-to-peak |  |      | 24   | 27   |       |
| Random Jitter                   | "RJ" measured on Wavecrest SIA 3000  |      | 2.5  |      | ps    |
| Integrated jitter RMS at 155MHz | Integrated 12 kHz to 20 MHz  |      | 0.3  | 0.4  | ps    |
| Period jitter RMS               | At 622.08MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles     |      | 11   |      | ps    |
| Period jitter peak-to-peak      |  |      | 45   | 49   |       |
| Accumulated jitter RMS          | At 622.08MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles. |      | 11   |      | ps    |
| Accumulated jitter peak-to-peak |  |      | 24   | 27   |       |
| Random Jitter                   | "RJ" measured on Wavecrest SIA 3000  |      | 3    |      | ps    |
| Integrated jitter RMS at 622MHz | Integrated 12 kHz to 20 MHz  |      | 1.6  | 1.8  | ps    |

Measured on Wavecrest SIA 3000

### 6. Phase Noise Specifications

| PARAMETERS                      | FREQUENCY | @10Hz | @100Hz | @1kHz | @10kHz | @100kHz | UNITS  |
|---------------------------------|-----------|-------|--------|-------|--------|---------|--------|
| Phase Noise relative to carrier | 155.52MHz | -75   | -95    | -125  | -140   | -145    | dBc/Hz |
|                                 | 622.08MHz | -75   | -95    | -110  | -125   | -120    |        |

Note: Phase Noise measured at VCON = 0V

### 7. CMOS Electrical Specifications

| PARAMETERS                                   | SYMBOL          | CONDITIONS   | MIN. | TYP. | MAX. | UNITS |
|--|-----------------|--|------|------|------|-------|
| Output drive current (High Drive)            | I <sub>OH</sub> | V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V | 30   |      |      | mA    |
|  | I <sub>OL</sub> | V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V                 | 30   |      |      | mA    |
| Output drive current (Standard Drive)        | I <sub>OH</sub> | V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V | 10   |      |      | mA    |
|  | I <sub>OL</sub> | V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V                 | 10   |      |      | mA    |
| Output Clock Rise/Fall Time (Standard Drive) |                 | 0.3V ~ 3.0V with 15 pF load                                    |      | 2.4  |      | ns    |
| Output Clock Rise/Fall Time (High Drive)     |                 | 0.3V ~ 3.0V with 15 pF load                                    |      | 1.2  |      |       |

\* Note: High Drive CMOS is available on PLL520-06 through DRIVSEL selector input on pin 12.

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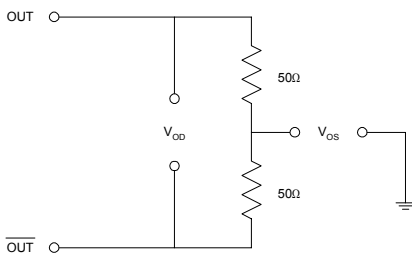
**8. LVDS Electrical Characteristics**

| PARAMETERS                   | SYMBOL          | CONDITIONS                                 | MIN.  | TYP.    | MAX.     | UNITS   |
|------------------------------|-----------------|--|-------|---------|----------|---------|
| Output Differential Voltage  | $V_{OD}$        | $R_L = 100 \Omega$<br>(see figure)         | 247   | 355     | 454      | mV      |
| $V_{DD}$ Magnitude Change    | $\Delta V_{OD}$ |  | -50   |         | 50       | mV      |
| Output High Voltage          | $V_{OH}$        |  |       | 1.4     | 1.6      | V       |
| Output Low Voltage           | $V_{OL}$        |  | 0.9   | 1.1     |          | V       |
| Offset Voltage               | $V_{OS}$        |  | 1.125 | 1.2     | 1.375    | V       |
| Offset Magnitude Change      | $\Delta V_{OS}$ |  | 0     | 3       | 25       | mV      |
| Power-off Leakage            | $I_{OXD}$       | $V_{out} = V_{DD}$ or GND<br>$V_{DD} = 0V$ |       | $\pm 1$ | $\pm 10$ | $\mu A$ |
| Output Short Circuit Current | $I_{OSD}$       |  |       | -5.7    | -8       | mA      |

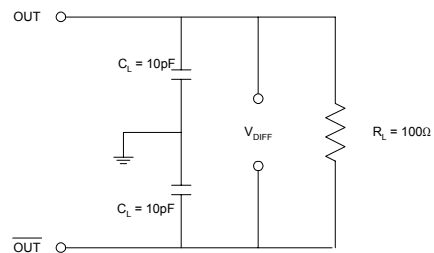
**9. LVDS Switching Characteristics**

| PARAMETERS                   | SYMBOL | CONDITIONS  | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------|---|------|------|------|-------|
| Differential Clock Rise Time | $t_r$  | $R_L = 100 \Omega$<br>$C_L = 10 \text{ pF}$<br>(see figure) | 0.2  | 0.7  | 1.0  | ns    |
| Differential Clock Fall Time | $t_f$  |   | 0.2  | 0.7  | 1.0  | ns    |

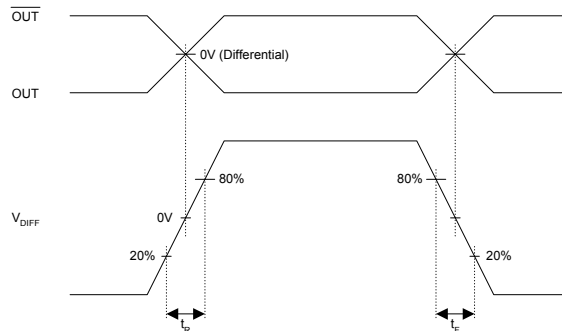
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



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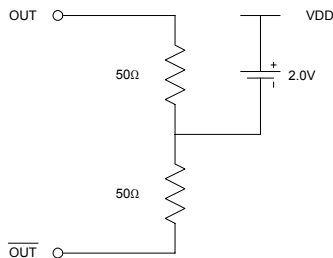
**10. PECL Electrical Characteristics**

| PARAMETERS          | SYMBOL   | CONDITIONS   | MIN.             | MAX.             | UNITS |
|---------------------|----------|--|------------------|------------------|-------|
| Output High Voltage | $V_{OH}$ | $R_L = 50 \Omega$ to $(V_{DD} - 2V)$<br>(see figure) | $V_{DD} - 1.025$ |                  | V     |
| Output Low Voltage  | $V_{OL}$ |  |                  | $V_{DD} - 1.620$ | V     |

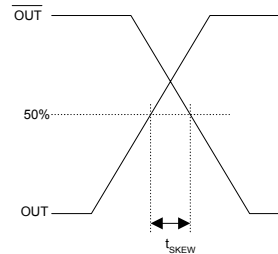
**11. PECL Switching Characteristics**

| PARAMETERS      | SYMBOL | CONDITIONS     | MIN. | TYP. | MAX. | UNITS |
|-----------------|--------|----------------|------|------|------|-------|
| Clock Rise Time | $t_r$  | @20/80% - PECL |      | 0.6  | 1.5  | ns    |
| Clock Fall Time | $t_f$  | @80/20% - PECL |      | 0.5  | 1.5  | ns    |

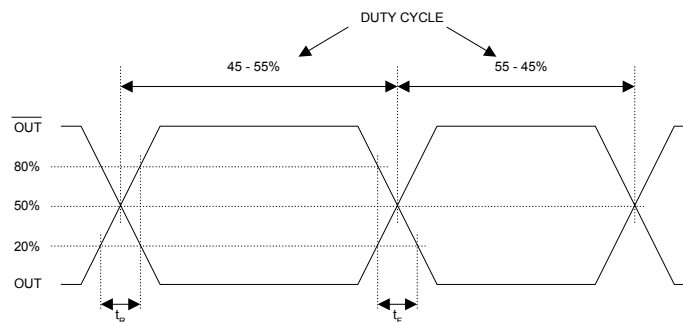
PECL Levels Test Circuit



PECL Output Skew

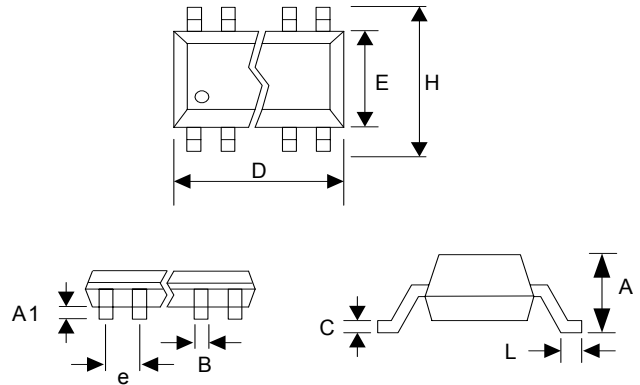


PECL Transition Time Waveform



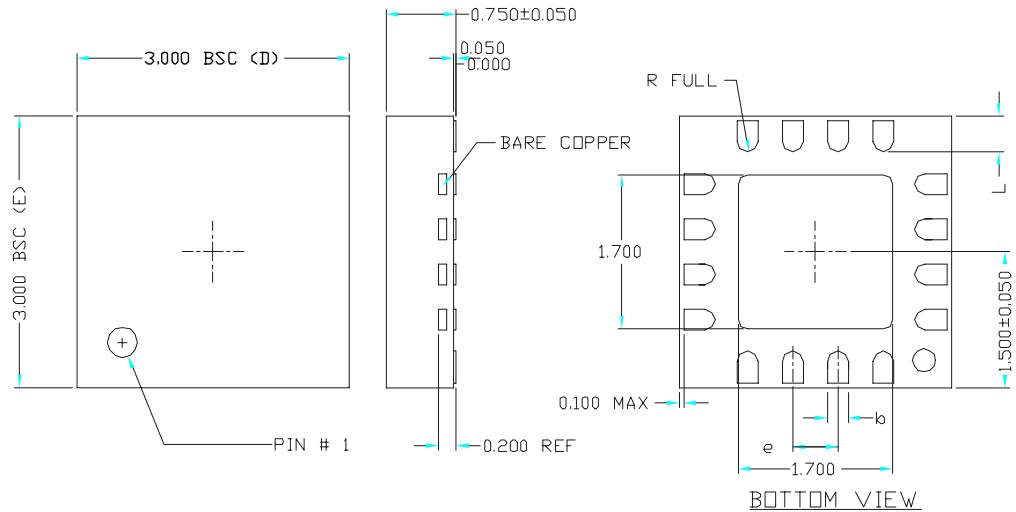
**PACKAGE INFORMATION**

| 16 PIN TSSOP ( mm ) |          |      |
|---------------------|----------|------|
| Symbol              | Min.     | Max. |
| A                   | -        | 1.20 |
| A1                  | 0.05     | 0.15 |
| B                   | 0.19     | 0.30 |
| C                   | 0.09     | 0.20 |
| D                   | 4.90     | 5.10 |
| E                   | 4.30     | 4.50 |
| H                   | 6.40 BSC |      |
| L                   | 0.45     | 0.75 |
| e                   | 0.65 BSC |      |



VARIATIONS:

| SYMBOL | 16 LD    |      |      |
|--------|----------|------|------|
|        | MIN      | NOM  | MAX  |
| e      | 0.50 BSC |      |      |
| b      | 0.18     | 0.23 | 0.30 |
| L      | 0.30     | 0.40 | 0.50 |
| ND     | 4        |      |      |
| NE     | 4        |      |      |



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**ORDERING INFORMATION**

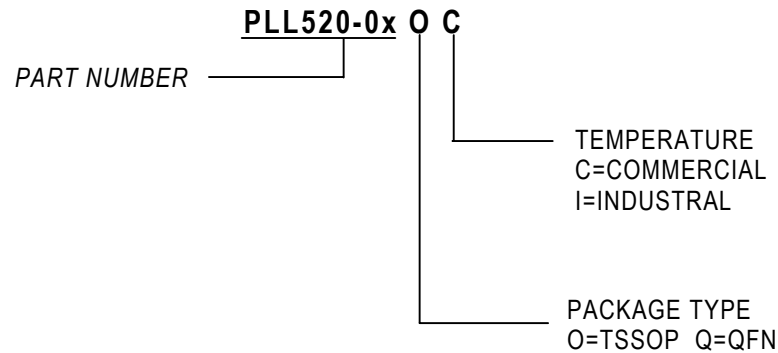
**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range



| <u>Order Number</u> | <u>Marking</u> | <u>Package Option</u>          |
|---------------------|----------------|--------------------------------|
| PLL520-05OC         | P520-05OC      | 16-Pin TSSOP (Tube)            |
| PLL520-05OC-R       | P520-05OC      | 16-Pin TSSOP (Tape and Reel)   |
| PLL520-05QC         | P520-05QC      | 16-Pin 3x3 QFN (Tube)          |
| PLL520-05QC-R       | P520-05QC      | 16-Pin 3x3 QFN (Tape and Reel) |
| PLL520-06QC         | P520-06QC      | 16-Pin 3x3 QFN (Tube)          |
| PLL520-06QC-R       | P520-06QC      | 16-Pin 3x3 QFN (Tape and Reel) |
| PLL520-07OC         | P520-07OC      | 16-Pin TSSOP (Tube)            |
| PLL520-07OC-R       | P520-07OC      | 16-Pin TSSOP (Tape and Reel)   |
| PLL520-08OC         | P520-08OC      | 16-Pin TSSOP (Tube)            |
| PLL520-08OC-R       | P520-08OC      | 16-Pin TSSOP (Tape and Reel)   |
| PLL520-08QC         | P520-08QC      | 16-Pin 3x3 QFN (Tube)          |
| PLL520-08QC-R       | P520-08QC      | 16-Pin 3x3 QFN (Tape and Reel) |
| PLL520-09OC         | P520-09OC      | 16-Pin TSSOP (Tube)            |
| PLL520-09OC-R       | P520-09OC      | 16-Pin TSSOP (Tape and Reel)   |
| PLL520-09QC         | P520-09QC      | 16-Pin 3x3 QFN (Tube)          |
| PLL520-09QC-R       | P520-09QC      | 16-Pin 3x3 QFN (Tape and Reel) |

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- Защита от снятия компонента с производства.



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