

# 32-Bit

Microcontroller

# TC1782

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.4.1 2014-05

Microcontrollers

**Edition 2014-05**

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## 1 Summary of Features

The **SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).



---

## Summary of Features

- One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of  $f_{FADC}$  clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

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  - 128 Kbyte Data Memory (LDRAM)
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  - 16 Kbyte BootROM (BROM)
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  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

---

## Summary of Features

The **SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 2 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
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  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

---

## Summary of Features

The **SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 160 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 160 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 128 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
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  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
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  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

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  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
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  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

**Summary of Features**
**Ordering Information**

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1782 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

This document describes the derivatives of the device. The **Table 1** enumerates these derivatives and summarizes the differences.

**Table 1 TC1782 Derivative Synopsis**

<b>Derivative</b>	<b>Ambient Temperature Range</b>	<b>Package</b>
SAK-TC1782F-320F180HR	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-20
SAK-TC1782F-320F180HL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-10
SAK-TC1782N-320F180HR	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-20
SAK-TC1782N-320F180HL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-10
SAK-TC1782N-256F133HR	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-20
SAK-TC1782N-256F133HL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-10
SAK-TC1782F-320F160HR	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-20
SAK-TC1782F-320F160HL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-10
SAK-TC1782N-320F160HR	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-20
SAK-TC1782N-320F160HL	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	PG-LQFP-176-10

## **2 System Overview of the TC1782**

The TC1782 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1782 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1782 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1782 ports are reserved for these peripheral units to communicate with the external world.

System Overview of the TC1782 Block Diagrams

2.1 Block Diagrams

Figure 1 shows the block diagram of the SAK-TC1782-320F180HR / SAK-TC1782-320F180HL / SAK-TC1782-320F160HR / SAK-TC1782-320F160HL.

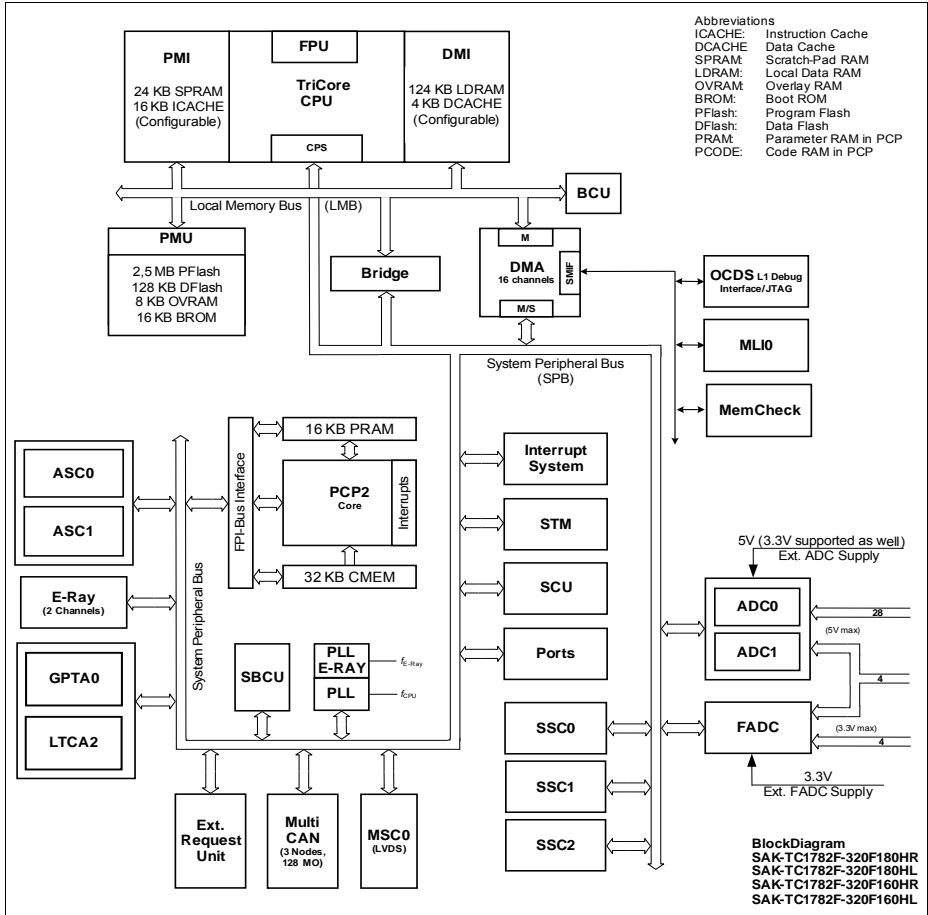


Figure 1 SAK-TC1782-320F180HR / SAK-TC1782-320F180HL / SAK-TC1782-320F160HR / SAK-TC1782-320F160HL Block Diagram

System Overview of the TC1782 Block Diagrams

Figure 2 shows the block diagram of the SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL.

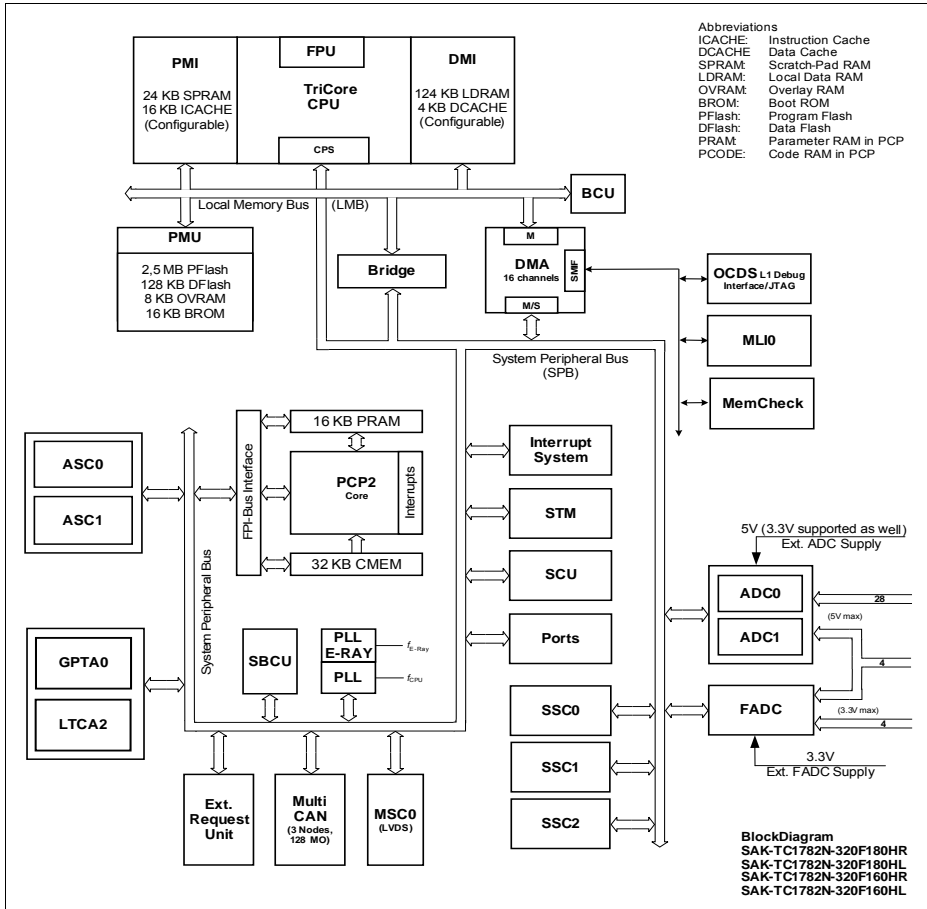


Figure 2 SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / Block Diagram

System Overview of the TC1782 Block Diagrams

Figure 3 shows the block diagram of the SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL.

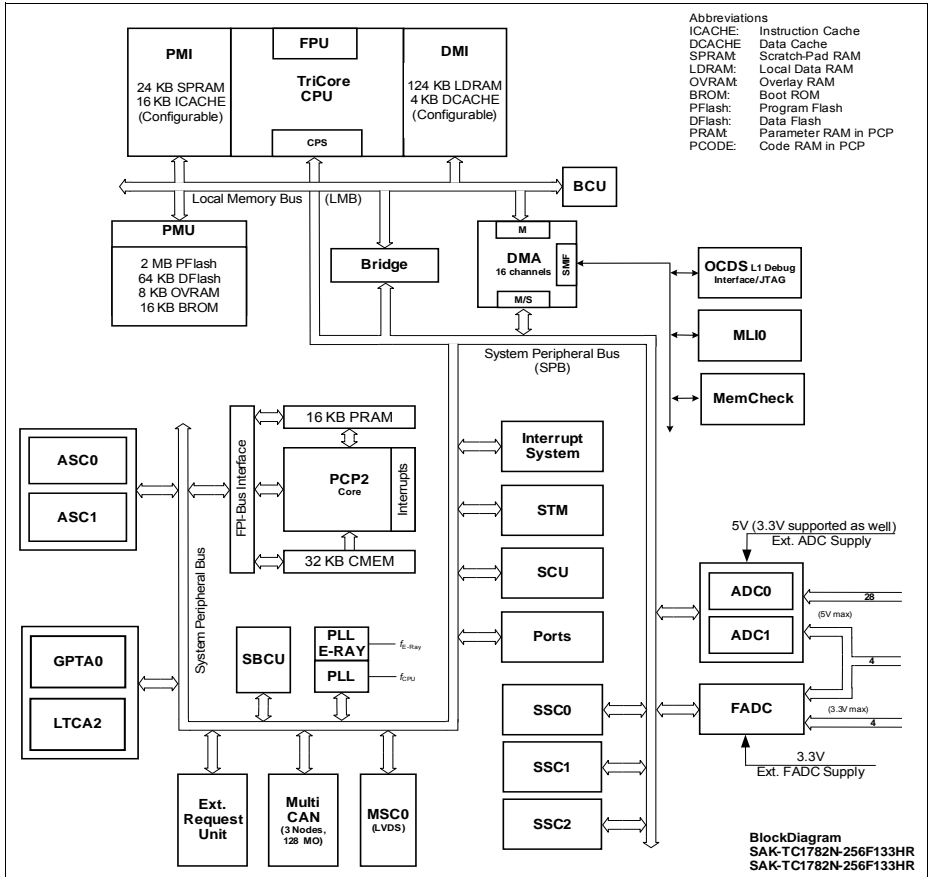


Figure 3 SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL Block Diagram

### 3 Pinning

Figure 4 is showing the TC1782 Logic Symbol.

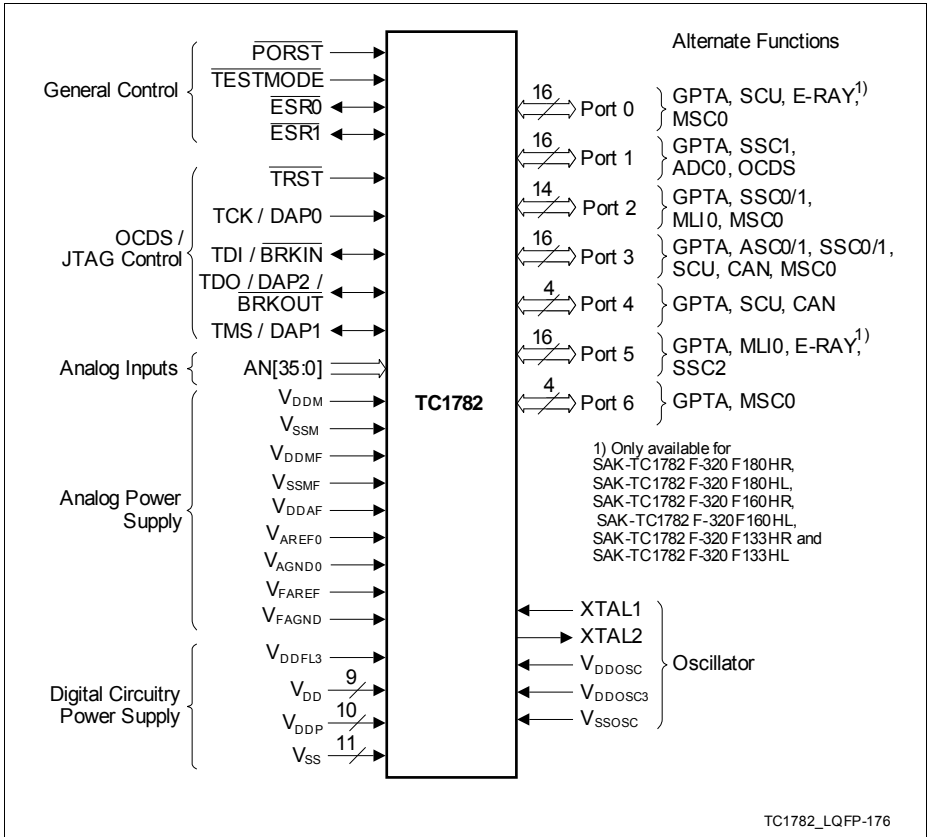
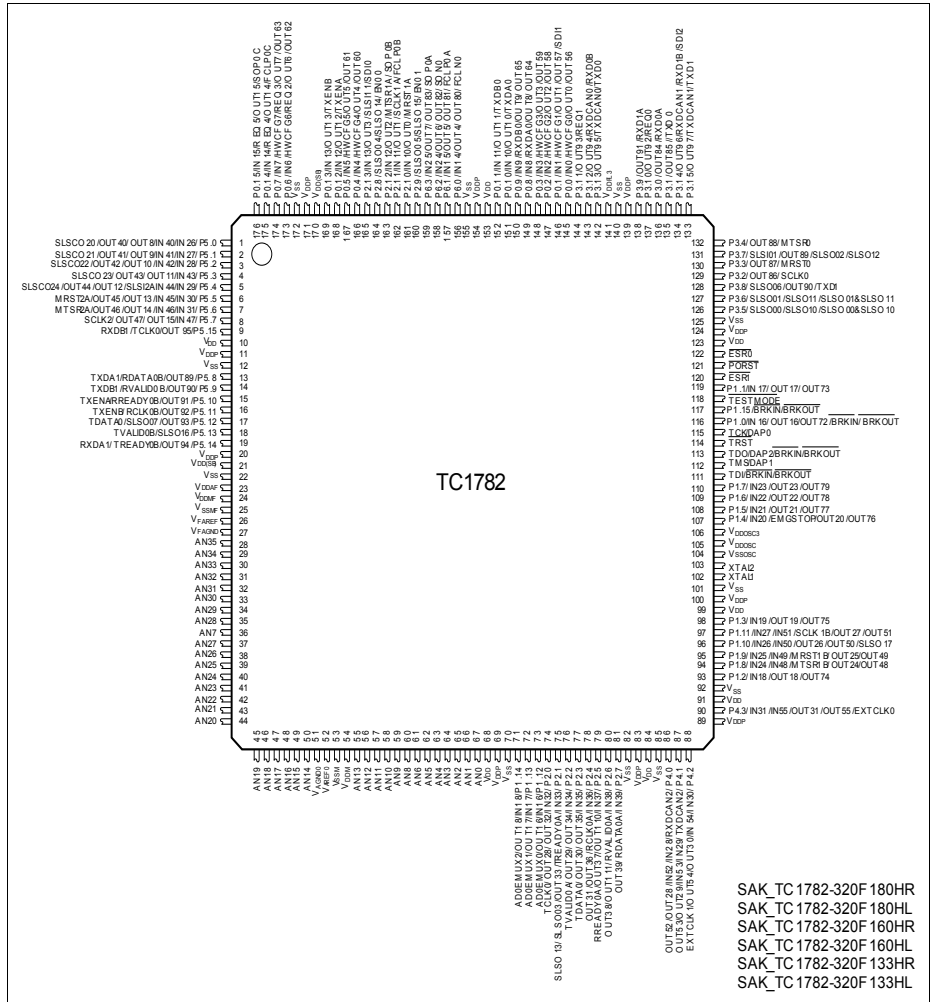


Figure 4 TC1782 Logic Symbol

**PinningTC1782 Pin Configuration****3.1 TC1782 Pin Configuration**

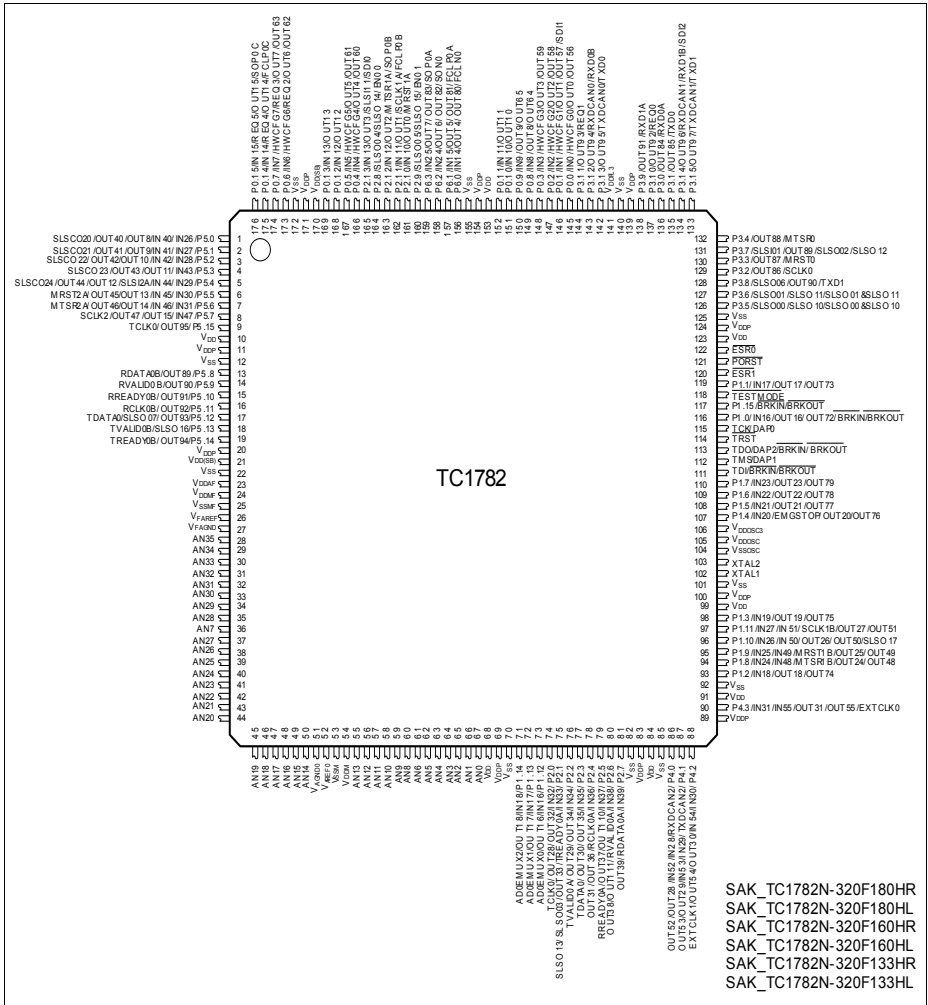
This chapter shows the pin configuration of the TC1782 package PG-LQFP-176-10 / PG-LQFP-176-20.



**Figure 5 SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL Pinning**



Pinning TC1782 Pin Configuration



**Figure 6** SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL / Pinning

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package)**

Pin	Symbol	Ctrl.	Type	Function
<b>Port 0</b>				
145	P0.0	I/O0	A1/ PU	<b>Port 0 General Purpose I/O Line 0</b>
	IN0	I		<b>GPTA0 Input 0</b>
	IN0	I		<b>LTCA2 Input 0</b>
	HWCFG0	I		<b>Hardware Configuration Input 0</b>
	OUT0	O1		<b>GPTA0 Output 0</b>
	OUT56	O2		<b>GPTA0 Output 56</b>
	OUT0	O3		<b>LTCA2 Output 0</b>
146	P0.1	I/O0	A1/ PU	<b>Port 0 General Purpose I/O Line 1</b>
	IN1	I		<b>GPTA0 Input 1</b>
	IN1	I		<b>LTCA2 Input 1</b>
	SDI1	I		<b>MSC0 Serial Data Input 1</b>
	HWCFG1	I		<b>Hardware Configuration Input 1</b>
	OUT1	O1		<b>GPTA0 Output 1</b>
	OUT57	O2		<b>GPTA0 Output 57</b>
	OUT1	O3		<b>LTCA2 Output 1</b>
147	P0.2	I/O0	A1/ PU	<b>Port 0 General Purpose I/O Line 2</b>
	IN2	I		<b>GPTA0 Input 2</b>
	IN2	I		<b>LTCA2 Input 2</b>
	HWCFG2	I		<b>Hardware Configuration Input 2</b>
	OUT2	O1		<b>GPTA0 Output 2</b>
	OUT58	O2		<b>GPTA0 Output 58</b>
	OUT2	O3		<b>LTCA2 Output 2</b>

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
148	P0.3	I/O0	A1+/PU	Port 0 General Purpose I/O Line 3
	IN3	I		GPTA0 Input 3
	IN3	I		LTCA2 Input 3
	HWCFG3	I		Hardware Configuration Input 3
	OUT3	O1		GPTA0 Output 3
	OUT59	O2		GPTA0 Output 59
	OUT3	O3		LTCA2 Output 3
166	P0.4	I/O0	A1/PU	Port 0 General Purpose I/O Line 4
	IN4	I		GPTA0 Input 4
	IN4	I		LTCA2 Input 4
	HWCFG4	I		Hardware Configuration Input 4
	OUT4	O1		GPTA0 Output 4
	OUT60	O2		GPTA0 Output 60
	OUT4	O3		LTCA2 Output 4
167	P0.5	I/O0	A1/PU	Port 0 General Purpose I/O Line 5
	IN5	I		GPTA0 Input 5
	IN5	I		LTCA2 Input 5
	HWCFG5	I		Hardware Configuration Input 5
	OUT5	O1		GPTA0 Output 5
	OUT61	O2		GPTA0 Output 61
	OUT5	O3		LTCA2 Output 5
173	P0.6	I/O0	A1/PU	Port 0 General Purpose I/O Line 6
	IN6	I		GPTA0 Input 6
	IN6	I		LTCA2 Input 6
	HWCFG6	I		Hardware Configuration Input 6
	REQ2	I		External Request Input 2
	OUT6	O1		GPTA0 Output 6
	OUT62	O2		GPTA0 Output 62
OUT6	O3	LTCA2 Output 6		

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
174	P0.7	I/O0	A1/ PU	Port 0 General Purpose I/O Line 7
	IN7	I		GPTA0 Input 7
	IN7	I		LTCA2 Input 7
	HWCFG7	I		Hardware Configuration Input 7
	REQ3	I		External Request Input 3
	OUT7	O1		GPTA0 Output 7
	OUT63	O2		GPTA0 Output 63
	OUT7	O3		LTCA2 Output 7
149	P0.8	I/O0	A1/ PU	Port 0 General Purpose I/O Line 8
	IN8	I		GPTA0 Input 8
	IN8	I		LTCA2 Input 8
	RXDA0	I		E-Ray Channel A Receive Data Input 0 <sup>1)</sup>
	OUT8	O1		GPTA0 Output 8
	OUT64	O2		GPTA0 Output 64
	OUT8	O3		LTCA2 Output 8
150	P0.9	I/O0	A1/ PU	Port 0 General Purpose I/O Line 9
	IN9	I		GPTA0 Input 9
	IN9	I		LTCA2 Input 9
	RXDB0	I		E-Ray Channel B Receive Data Input 0 <sup>1)</sup>
	OUT9	O1		GPTA0 Output 9
	OUT65	O2		GPTA0 Output 65
	OUT9	O3		LTCA2 Output 9
151	P0.10	I/O0	A2/ PU	Port 0 General Purpose I/O Line 10
	IN10	I		GPTA0 Input 10
	OUT10	O1		GPTA0 Output 10
	TXDA0	O2		E-Ray Channel A transmit Data Output <sup>1)</sup>
	OUT10	O3		LTCA2 Output 10

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
152	P0.11	I/O0	A2/ PU	Port 0 General Purpose I/O Line 11
	IN11	I		GPTA0 Input 11
	OUT11	O1		GPTA0 Output 11
	TXDB0	O2		E-Ray Channel B transmit Data Output <sup>1)</sup>
	OUT11	O3		LTCA2 Output 11
168	P0.12	I/O0	A2/ PU	Port 0 General Purpose I/O Line 12
	IN12	I		GPTA0 Input 12
	OUT12	O1		GPTA0 Output 12
	TXENA	O2		E-Ray Channel A transmit Data Output enable <sup>1)</sup>
	OUT12	O3		LTCA2 Output 12
169	P0.13	I/O0	A2/ PU	Port 0 General Purpose I/O Line 13
	IN13	I		GPTA0 Input 13
	OUT13	O1		GPTA0 Output 13
	TXENB	O2		E-Ray Channel B transmit Data Output enable <sup>1)</sup>
	OUT13	O3		LTCA2 Output 13
175	P0.14	I/O0	A1+/ PU	Port 0 General Purpose I/O Line 14
	IN14	I		GPTA0 Input 14
	REQ4	I		External Request Input 4
	OUT14	O1		GPTA0 Output 14
	FCLP0C	O2		MSC0 Clock Output Positive C
	OUT14	O3		LTCA2 Output 14
176	P0.15	I/O0	A1+/ PU	Port 0 General Purpose I/O Line 15
	IN15	I		GPTA0 Input 15
	REQ5	I		External Request Input 5
	OUT15	O1		GPTA0 Output 15
	SOP0C	O2		MSC0 Serial Data Output Positive C
	OUT15	O3		LTCA2 Output 15

**Port 1**

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
116	P1.0	I/O0	A2/ PU	Port 1 General Purpose I/O Line 0
	IN16	I		GPTA0 Input 16
	BRKIN	I		Break Input
	OUT16	O1		GPTA0 Output 16
	OUT72	O2		GPTA0 Output 72
	OUT16	O3		LTCA2 Output 16
	BRKOUT	O		Break Output (controlled by OCDS module)
119	P1.1	I/O0	A1/ PU	Port 1 General Purpose I/O Line 1
	IN17	I		GPTA0 Input 17
	OUT17	O1		GPTA0 Output 17
	OUT73	O2		GPTA0 Output 73
	OUT17	O3		LTCA2 Output 17
93	P1.2	I/O0	A1/ PU	Port 1 General Purpose I/O Line 2
	IN18	I		GPTA0 Input 18
	OUT18	O1		GPTA0 Output 18
	OUT74	O2		GPTA0 Output 74
	OUT18	O3		LTCA2 Output 18
98	P1.3	I/O0	A1/ PU	Port 1 General Purpose I/O Line 3
	IN19	I		GPTA0 Input 19
	IN19	I		LTCA2 Input 19
	OUT19	O1		GPTA0 Output 19
	OUT75	O2		GPTA0 Output 75
	OUT19	O3		LTCA2 Output 19
107	P1.4	I/O0	A1/ PU	Port 1 General Purpose I/O Line 4
	IN20	I		GPTA0 Input 20
	IN20	I		LTCA2 Input 20
	EMGSTOP	I		Emergency Stop Input
	OUT20	O1		GPTA0 Output 20
	OUT76	O2		GPTA0 Output 76
	OUT20	O3		LTCA2 Output 20

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
108	P1.5	I/O0	A1/ PU	<b>Port 1 General Purpose I/O Line 35</b>
	IN21	I		<b>GPTA0 Input 21</b>
	IN21	I		<b>LTCA2 Input 21</b>
	OUT21	O1		<b>GPTA0 Output 21</b>
	OUT77	O2		<b>GPTA0 Output 77</b>
	OUT21	O3		<b>LTCA2 Output 21</b>
109	P1.6	I/O0	A1/ PU	<b>Port 1 General Purpose I/O Line 6</b>
	IN22	I		<b>GPTA0 Input 22</b>
	IN22	I		<b>LTCA2 Input 22</b>
	OUT22	O1		<b>GPTA0 Output 22</b>
	OUT78	O2		<b>GPTA0 Output 78</b>
	OUT22	O3		<b>LTCA2 Output 22</b>
110	P1.7	I/O0	A1/ PU	<b>Port 1 General Purpose I/O Line 7</b>
	IN23	I		<b>GPTA0 Input 23</b>
	IN23	I		<b>LTCA2 Input 23</b>
	OUT23	O1		<b>GPTA0 Output 23</b>
	OUT79	O2		<b>GPTA0 Output 79</b>
	OUT23	O3		<b>LTCA2 Output 23</b>
94	P1.8	I/O0	A1+/ PU	<b>Port 1 General Purpose I/O Line 8</b>
	IN24	I		<b>GPTA0 Input 24</b>
	IN48	I		<b>GPTA0 Input 48</b>
	MTR1B	I		<b>SSC1 Slave Receive Input B (Slave Mode)</b>
	OUT24	O1		<b>GPTA0 Output 24</b>
	OUT48	O2		<b>GPTA0 Output 48</b>
	MTR1B	O3		<b>SSC1 Master Transmit Output B (Master Mode)</b>

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
95	P1.9	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 9
	IN25	I		GPTA0 Input 25
	IN49	I		GPTA0 Input 49
	MRST1B	I		SSC1 Master Receive Input B (Master Mode)
	OUT25	O1		GPTA0 Output 25
	OUT49	O2		GPTA0 Output 49
	MRST1B	O3		SSC1 Slave Transmit Output B (Slave Mode)
96	P1.10	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 10
	IN26	I		GPTA0 Input 26
	IN50	I		GPTA0 Input 50
	OUT26	O1		GPTA0 Output 26
	OUT50	O2		GPTA0 Output 50
	SLSO17	O3		SSC1 Slave Select Output 7
97	P1.11	I/O0	A1+/ PU	Port 1 General Purpose I/O Line 11
	IN27	I		GPTA0 Input 27
	IN51	I		GPTA0 Input 51
	SCLK1B	I		SSC1 Clock Input B
	OUT27	O1		GPTA0 Output 27
	OUT51	O2		GPTA0 Output 51
	SCLK1B	O3		SSC1 Clock Output B
73	P1.12	I/O0	A1/ PU	Port 1 General Purpose I/O Line 12
	IN16	I		LTCA2 Input 16
	AD0EMUX0	O1		ADC0 External Multiplexer Control Output 0
	AD0EMUX0	O2		ADC0 External Multiplexer Control Output 0
	OUT16	O3		LTCA2 Output 16
72	P1.13	I/O0	A1/ PU	Port 1 General Purpose I/O Line 13
	IN17	I		LTCA2 Input 17
	AD0EMUX1	O1		ADC0 External Multiplexer Control Output 1
	AD0EMUX1	O2		ADC0 External Multiplexer Control Output 1
	OUT17	O3		LTCA2 Output 17



## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
71	P1.14	I/O0	A1/ PU	Port 1 General Purpose I/O Line 14
	IN18	I		LTCA2 Input 18
	AD0EMUX2	O1		ADC0 External Multiplexer Control Output 2
	AD0EMUX2	O2		ADC0 External Multiplexer Control Output 2
	OUT18	O3		LTCA2 Output 18
117	P1.15	I/O0	A2/ PU	Port 1 General Purpose I/O Line 15
	BRKIN	I		Break Input
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BRKOUT	O		Break Output (controlled by OCDS module)
<b>Port 2</b>				
74	P2.0	I/O0	A2/ PU	Port 2 General Purpose I/O Line 0
	IN32	I		GPTA0 Input 32
	OUT32	O1		GPTA0 Output 32
	TCLK0	O2		MLI0 Transmitter Clock Output 0
	OUT28	O3		LTCA2 Output 28
75	P2.1	I/O0	A2/ PU	Port 2 General Purpose I/O Line 1
	IN33	I		GPTA0 Input 33
	TREADY0A	I		MLI0 Transmitter Ready Input A
	OUT33	O1		GPTA0 Output 33
	SLSO03	O2		SSC0 Slave Select Output Line 3
	SLSO13	O3		SSC1 Slave Select Output Line 3
76	P2.2	I/O0	A2/ PU	Port 2 General Purpose I/O Line 2
	IN34	I		GPTA0 Input 34
	OUT34	O1		GPTA0 Output 34
	TVALID0	O2		MLI0 Transmitter Valid Output
	OUT29	O3		LTCA2 Output 29

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
77	P2.3	I/O0	A2/ PU	Port 2 General Purpose I/O Line 3
	IN35	I		GPTA0 Input 35
	OUT35	O1		GPTA0 Output 35
	TDATA0	O2		MLI0 Transmitter Data Output
	OUT30	O3		LTCA2 Output 30
78	P2.4	I/O0	A2/ PU	Port 2 General Purpose I/O Line 4
	IN36	I		GPTA0 Input 36
	RCLK0A	I		MLI Receiver Clock Input A
	OUT36	O1		GPTA0 Output 36
	OUT36	O2		GPTA0 Output 36
	OUT31	O3		LTCA2 Output 31
79	P2.5	I/O0	A2/ PU	Port 2 General Purpose I/O Line 5
	IN37	I		GPTA0 Input 37
	OUT37	O1		GPTA0 Output 37
	RREADY0A	O2		MLI0 Receiver Ready Output A
	OUT110	O3		LTCA2 Output 110
80	P2.6	I/O0	A2/ PU	Port 2 General Purpose I/O Line 6
	IN38	I		GPTA0 Input 38
	RVALID0A	I		MLI Receiver Valid Input A
	OUT38	O1		GPTA0 Output 38
	OUT38	O2		GPTA0 Output 38
	OUT111	O3		LTCA2 Output 111
81	P2.7	I/O0	A2/ PU	Port 2 General Purpose I/O Line 7
	IN39	I		GPTA0 Input 39
	RDATA0A	I		MLI Receiver Data Input A
	OUT39	O1		GPTA0 Output 39
	OUT39	O2		GPTA0 Output 39
	Reserved	O3		-

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
164	P2.8	I/O0	A2/ PU	Port 2 General Purpose I/O Line 8
	SLSO04	O1		SSC0 Slave Select Output 4
	SLSO14	O2		SSC1 Slave Select Output 4
	EN00	O3		MSC0 Enable Output 0
160	P2.9	I/O0	A2/ PU	Port 2 General Purpose I/O Line 9
	SLSO05	O1		SSC0 Slave Select Output 5
	SLSO15	O2		SSC1 Slave Select Output 5
	EN01	O3		MSC0 Enable Output 1
161	P2.10	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 10
	MRST1A	I		SSC1 Master Receive Input A
	IN10	I		LTCA2 Input 10
	MRST1A	O1		SSC1 Slave Transmit Output
	OUT0	O2		LTCA2 Output 0
	Reserved	O3		-
162	P2.11	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 11
	SCLK1A	I		SSC1 Clock Input A
	IN11	I		LTCA2 Input 11
	SCLK1A	O1		SSC1 Clock Output A
	OUT1	O2		LTCA2 Output 1
	FCLP0B	O3		MSC0 Clock Output Positive B
163	P2.12	I/O0	A1+/ PU	Port 2 General Purpose I/O Line 12
	MTR1A	I		SSC1 Slave Receive Input A
	IN12	I		LTCA2 Input 12
	MTR1A	O1		SSC1 Master Transmit Output A
	OUT2	O2		LTCA2 Output 2
	SOP0B	O3		MSC0 Serial Data Output Positive B

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
165	P2.13	I/O0	A1/ PU	Port 2 General Purpose I/O Line 13
	SLSI11	I		SSC1 Slave Select Input 1
	SDI0	I		MSC0 Serial Data Input 0
	IN13	I		LTCA2 Input 13
	OUT3	O1		LTCA2 Output 3
	Reserved	O2		-
	Reserved	O3		-
<b>Port 3</b>				
136	P3.0	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 0
	RXD0A	I		ASC0 Receiver Input A (Async. & Sync. Mode)
	RXD0A	O1		ASC0 Output (Sync. Mode)
	RXD0A	O2		ASC0 Output (Sync. Mode)
	OUT84	O3		GPTA0 Output 84
135	P3.1	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 1
	TXD0	O1		ASC0 Output
	TXD0	O2		ASC0 Output
	OUT85	O3		GPTA0 Output 85
129	P3.2	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 2
	SCLK0	I		SSC0 Clock Input (Slave Mode)
	SCLK0	O1		SSC0 Clock Output (Master Mode)
	SCLK0	O2		SSC0 Clock Output (Master Mode)
	OUT86	O3		GPTA0 Output 86
130	P3.3	I/O0	A1+/ PU	Port 3 General Purpose I/O Line 3
	MRST0	I		SSC0 Master Receive Input (Master Mode)
	MRST0	O1		SSC0 Slave Transmit Output (Slave Mode)
	MRST0	O2		SSC0 Slave Transmit Output (Slave Mode)
	OUT87	O3		GPTA0 Output 87

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
132	P3.4	I/O0	A2/ PU	<b>Port 3 General Purpose I/O Line 4</b>
	MTSR0	I		<b>SSC0 Slave Receive Input (Slave Mode)</b>
	MTSR0	O1		<b>SSC0 Master Transmit Output (Master Mode)</b>
	MTSR0	O2		<b>SSC0 Master Transmit Output (Master Mode)</b>
	OUT88	O3		<b>GPTA0 Output 88</b>
126	P3.5	I/O0	A1+/ PU	<b>Port 3 General Purpose I/O Line 5</b>
	SLSO00	O1		<b>SSC0 Slave Select Output 0</b>
	SLSO10	O2		<b>SSC1 Slave Select Output 0</b>
	SLSOANDO0	O3		<b>SSC0 AND SSC1 Slave Select Output 0</b>
127	P3.6	I/O0	A1+/ PU	<b>Port 3 General Purpose I/O Line 6</b>
	SLSO01	O1		<b>SSC0 Slave Select Output 1</b>
	SLSO11	O2		<b>SSC1 Slave Select Output 1</b>
	SLSOANDO1	O3		<b>SSC0 AND SSC1 Slave Select Output 1</b>
131	P3.7	I/O0	A2/ PU	<b>Port 3 General Purpose I/O Line 7</b>
	SLSI01	I		<b>SSC0 Slave Select Input 1</b>
	SLSO02	O1		<b>SSC0 Slave Select Output 2</b>
	SLSO12	O2		<b>SSC1 Slave Select Output 2</b>
	OUT89	O3		<b>GPTA0 Output 89</b>
128	P3.8	I/O0	A2/ PU	<b>Port 3 General Purpose I/O Line 8</b>
	SLSO06	O1		<b>SSC0 Slave Select Output 6</b>
	TXD1	O2		<b>ASC1 Transmit Output</b>
	OUT90	O3		<b>GPTA0 Output 90</b>
138	P3.9	I/O0	A1/ PU	<b>Port 3 General Purpose I/O Line 9</b>
	RXD1A	I		<b>ASC1 Receiver Input A</b>
	RXD1A	O1		<b>ASC1 Receiver Output A (Synchronous Mode)</b>
	RXD1A	O2		<b>ASC1 Receiver Output A (Synchronous Mode)</b>
	OUT91	O3		<b>GPTA0 Output 91</b>

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
137	P3.10	I/O0	A1/ PU	<b>Port 3 General Purpose I/O Line 10</b>
	REQ0	I		<b>External Request Input 0</b>
	Reserved	O1		-
	Reserved	O2		-
	OUT92	O3		<b>GPTA0 Output 92</b>
144	P3.11	I/O0	A1/ PU	<b>Port 3 General Purpose I/O Line 11</b>
	REQ1	I		<b>External Request Input 1</b>
	Reserved	O1		-
	Reserved	O2		-
	OUT93	O3		<b>GPTA0 Output 93</b>
143	P3.12	I/O0	A1/ PU	<b>Port 3 General Purpose I/O Line 12</b>
	RXDCAN0	I		<b>CAN Node 0 Receiver Input</b>
	RXD0B	I		<b>ASC0 Receiver Input B</b>
	RXD0B	O1		<b>ASC0 Receiver Output B (Synchronous Mode)</b>
	RXD0B	O2		<b>ASC0 Receiver Output B (Synchronous Mode)</b>
	OUT94	O3		<b>GPTA0 Output 94</b>
142	P3.13	I/O0	A2/ PU	<b>Port 3 General Purpose I/O Line 13</b>
	TXDCAN0	O1		<b>CAN Node 0 Transmitter Output</b>
	TXD0	O2		<b>ASC0 Transmit Output</b>
	OUT95	O3		<b>GPTA0 Output 95</b>
134	P3.14	I/O0	A1/ PU	<b>Port 3 General Purpose I/O Line 14</b>
	RXDCAN1	I		<b>CAN Node 1 Receiver Input</b>
	RXD1B	I		<b>ASC1 Receiver Input B</b>
	SDI2	I		<b>MSC0 Serial Data Input 2</b>
	RXD1B	O1		<b>ASC1 Receiver Output B (Synchronous Mode)</b>
	RXD1B	O2		<b>ASC1 Receiver Output B (Synchronous Mode)</b>
	OUT96	O3		<b>GPTA0 Output 96</b>

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
133	P3.15	I/O0	A2/ PU	<b>Port 3 General Purpose I/O Line 15</b>
	TXDCAN1	O1		<b>CAN Node 1 Transmitter Output</b>
	TXD1	O2		<b>ASC1 Transmit Output</b>
	OUT97	O3		<b>GPTA0 Output 97</b>
<b>Port 4</b>				
86	P4.0	I/O0	A1+/ PU	<b>Port 4 General Purpose I/O Line 0</b>
	IN28	I		<b>GPTA0 Input 28</b>
	IN52	I		<b>GPTA0 Input 52</b>
	RXDCAN2	I		<b>CAN Node 2 Receiver Input</b>
	OUT28	O1		<b>GPTA0 Output 28</b>
	OUT52	O2		<b>GPTA0 Output 52</b>
	Reserved	O3		-
87	P4.1	I/O0	A1+/ PU	<b>Port 4 General Purpose I/O Line 1</b>
	IN29	I		<b>GPTA0 Input 29</b>
	IN53	I		<b>GPTA0 Input 53</b>
	OUT29	O1		<b>GPTA0 Output 29</b>
	OUT53	O2		<b>GPTA0 Output 53</b>
	TXDCAN2	O3		<b>CAN Node 2 Transmitter Output</b>
88	P4.2	I/O0	A2/ PU	<b>Port 4 General Purpose I/O Line 2</b>
	IN30	I		<b>GPTA0 Input 30</b>
	IN54	I		<b>GPTA0 Input 54</b>
	OUT30	O1		<b>GPTA0 Output 30</b>
	OUT54	O2		<b>GPTA0 Output 54</b>
	EXTCLK1	O3		<b>External Clock 1 Output</b>
90	P4.3	I/O0	A2/ PU	<b>Port 4 General Purpose I/O Line 3</b>
	IN31	I		<b>GPTA0 Input 31</b>
	IN55	I		<b>GPTA0 Input 55</b>
	OUT31	O1		<b>GPTA0 Output 31</b>
	OUT55	O2		<b>GPTA0 Output 55</b>
	EXTCLK0	O3		<b>External Clock 0 Output</b>

## PinningTC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
<b>Port 5</b>				
1	P5.0	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 0</b>
	IN40	I		<b>GPTA0 Input 40</b>
	IN26	I		<b>LTCA2 Input 26</b>
	OUT40	O1		<b>GPTA0 Output 40</b>
	OUT8	O2		<b>LTCA2 Output 8</b>
	SLSO20	O3		<b>SSC2 Slave Select Output 0</b>
2	P5.1	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 1</b>
	IN41	I		<b>GPTA0 Input 41</b>
	IN27	I		<b>LTCA2 Input 27</b>
	OUT41	O1		<b>GPTA0 Output 41</b>
	OUT9	O2		<b>LTCA2 Output 9</b>
	SLSO21	O3		<b>SSC2 Slave Select Output 1</b>
3	P5.2	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 2</b>
	IN42	I		<b>GPTA0 Input 42</b>
	IN28	I		<b>LTCA2 Input 28</b>
	OUT42	O1		<b>GPTA0 Output 42</b>
	OUT10	O2		<b>LTCA2 Output 10</b>
	SLSO22	O3		<b>SSC2 Slave Select Output 2</b>
4	P5.3	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 3</b>
	IN43	I		<b>GPTA0 Input 43</b>
	OUT43	O1		<b>GPTA0 Output 43</b>
	OUT11	O2		<b>LTCA2 Output 11</b>
	SLSO23	O3		<b>SSC2 Slave Select Output 3</b>



## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
5	P5.4	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 4
	IN44	I		GPTA0 Input 44
	IN29	I		LTCA2 Input 29
	SLSI2A	I		SSC2 Slave Select Input A
	OUT44	O1		GPTA0 Output 44
	OUT12	O2		LTCA2 Output 12
	SLSO24	O3		SSC2 Slave Select Output 4
6	P5.5	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 5
	IN45	I		GPTA0 Input 45
	IN30	I		LTCA2 Input 30
	MRST2A	I		SSC2 Master Receive Input (Master Mode)
	OUT45	O1		GPTA0 Output 45
	OUT13	O2		LTCA2 Output 13
	MRST2	O3		SSC2 Master Transmit Input (Slave Mode)
7	P5.6	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 6
	IN46	I		GPTA0 Input 46
	IN31	I		LTCA2 Input 31
	MTR2A	I		SSC2 Slave Receive Input (Slave Mode)
	OUT46	O1		GPTA0 Output 46
	OUT14	O2		LTCA2 Output 14
	MTR2	O3		SSC2 Master Transmit Output (Master Mode)
8	P5.7	I/O0	A1+/ PU	Port 5 General Purpose I/O Line 7
	IN47	I		GPTA0 Input 47
	SCLK2A	I		SSC2 Clock Input (Slave Mode)
	OUT47	O1		GPTA0 Output 47
	OUT15	O2		LTCA2 Output 15
	SCLK2	O3		SSC2 Clock Output (Master Mode)

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
13	P5.8	I/O0	A2/ PU	<b>Port 5 General Purpose I/O Line 8</b>
	RDATA0B	I		<b>MLI0 Receiver Data Input B</b>
	Reserved	O1		-
	TXDA1	O2		<b>E-Ray Channel A transmit Data Output <sup>1)</sup></b>
	OUT89	O3		<b>LTCA2 Output 89</b>
14	P5.9	I/O0	A2/ PU	<b>Port 5 General Purpose I/O Line 9</b>
	RVALID0B	I		<b>MLI0 Receiver Data Valid Input B</b>
	Reserved	O1		-
	TXDB1	O2		<b>E-Ray Channel B transmit Data Output <sup>1)</sup></b>
	OUT90	O3		<b>LTCA2 Output 90</b>
15	P5.10	I/O0	A2/ PU	<b>Port 5 General Purpose I/O Line 10</b>
	RREADY0B	O1		<b>MLI0 Receiver Ready Input B</b>
	TXENA	O2		<b>E-Ray Channel A transmit Data Output enable <sup>1)</sup></b>
	OUT91	O3		<b>LTCA2 Output 91</b>
16	P5.11	I/O0	A2/ PU	<b>Port 5 General Purpose I/O Line 11</b>
	RCLK0B	I		<b>MLI0 Receiver Clock Input B</b>
	Reserved	O1		-
	TXENB	O2		<b>E-Ray Channel B transmit Data Output enable <sup>1)</sup></b>
	OUT92	O3		<b>LTCA2 Output 92</b>
17	P5.12	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 12</b>
	TDATA0	O1		<b>MLI0 Transmitter Data Output</b>
	SLSO07	O2		<b>SSC0 Slave Select Output 7</b>
	OUT93	O3		<b>LTCA2 Output 93</b>
18	P5.13	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 13</b>
	TVALID0B	O1		<b>MLI0 Transmitter Valid Input B</b>
	SLSO16	O2		<b>SSC1 Slave Select Output 6</b>
	Reserved	O3		-

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
19	P5.14	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 14</b>
	TREADY0B	I		<b>MLI0 Transmitter Ready Input B</b>
	RXDA1	I		<b>E-Ray Channel A Receive Data Input 1 <sup>1)</sup></b>
	Reserved	O1		-
	Reserved	O2		-
	OUT94	O3		<b>LTCA2 Output 94</b>
9	P5.15	I/O0	A1+/ PU	<b>Port 5 General Purpose I/O Line 15</b>
	RXDB1	I		<b>E-Ray Channel B Receive Data Input 1 <sup>1)</sup></b>
	TCLK0	O1		<b>MLI0 Transmitter Clock Output</b>
	Reserved	O2		-
	OUT95	O3		<b>LTCA2 Output 95</b>
<b>Port 6</b>				
156	P6.0	I/O0	A1/ F/ PU	<b>Port 6 General Purpose I/O Line 0</b>
	IN14	I		<b>LTCA2 Input 14</b>
	FCLN0	O1		<b>MSC0 Clock Output Negative</b>
	OUT80	O2		<b>GPTA0 Output 80</b>
	OUT4	O3		<b>LTCA2 Output 4</b>
157	P6.1	I/O0	A1/ F/ PU	<b>Port 6 General Purpose I/O Line 1</b>
	IN15	I		<b>LTCA2 Input 15</b>
	FCLP0A	O1		<b>MSC0 Clock Output Positive A</b>
	OUT81	O2		<b>GPTA0 Output 81</b>
	OUT5	O3		<b>LTCA2 Output 5</b>
158	P6.2	I/O0	A1/ F/ PU	<b>Port 6 General Purpose I/O Line 2</b>
	IN24	I		<b>LTCA2 Input 24</b>
	SON0	O1		<b>MSC0 Serial Data Output Negative</b>
	OUT82	O2		<b>GPTA0 Output 82</b>
	OUT6	O3		<b>LTCA2 Output 6</b>

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
159	P6.3	I/O0	A1/ F/ PU	Port 6 General Purpose I/O Line 3
	IN25	I		LTCA2 Input 25
	SOP0A	O1		MSC0 Serial Data Output Positive A
	OUT83	O2		GPTA0 Output 83
	OUT7	O3		LTCA2 Output 7

**Analog Input Port**

67	AN0	I	D	ADC0 Analog Input Channel 0
66	AN1	I	D	ADC0 Analog Input Channel 1
65	AN2	I	D	ADC0 Analog Input Channel 2
64	AN3	I	D	ADC0 Analog Input Channel 3
63	AN4	I	D	ADC0 Analog Input Channel 4
62	AN5	I	D	ADC0 Analog Input Channel 5
61	AN6	I	D	ADC0 Analog Input Channel 6
36	AN7	I	D	ADC0 Analog Input Channel 7
60	AN8	I	D	ADC0 Analog Input Channel 8
59	AN9	I	D	ADC0 Analog Input Channel 9
58	AN10	I	D	ADC0 Analog Input Channel 10
57	AN11	I	D	ADC0 Analog Input Channel 11
56	AN12	I	D	ADC0 Analog Input Channel 12
55	AN13	I	D	ADC0 Analog Input Channel 13
50	AN14	I	D	ADC0 Analog Input Channel 14
49	AN15	I	D	ADC0 Analog Input Channel 15
48	AN16	I	D	ADC1 Analog Input Channel 16
47	AN17	I	D	ADC1 Analog Input Channel 17
46	AN18	I	D	ADC1 Analog Input Channel 18
45	AN19	I	D	ADC1 Analog Input Channel 19
44	AN20	I	D	ADC1 Analog Input Channel 20
43	AN21	I	D	ADC1 Analog Input Channel 21
42	AN22	I	D	ADC1 Analog Input Channel 22
41	AN23	I	D	ADC1 Analog Input Channel 23

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
40	AN24	I	D	ADC1 Analog Input Channel 24
39	AN25	I	D	ADC1 Analog Input Channel 25
38	AN26	I	D	ADC1 Analog Input Channel 26
37	AN27	I	D	ADC1 Analog Input Channel 27
35	AN28	I	D	ADC1 / FADC Analog Input Channel 28
34	AN29	I	D	ADC1 / FADC Analog Input Channel 29
33	AN30	I	D	ADC1 / FADC Analog Input Channel 30
32	AN31	I	D	ADC1 / FADC Analog Input Channel 31
31	AN32	I	D	FADC Analog Input P Channel 0
30	AN33	I	D	FADC Analog Input N Channel 0
29	AN34	I	D	FADC Analog Input P Channel 1
28	AN35	I	D	FADC Analog Input N Channel 1
54	V <sub>DDM</sub>	-	-	ADC Analog Part Power Supply (3.3V - 5V)
53	V <sub>S<sub>SSM</sub></sub>	-	-	ADC Analog Part Ground
52	V <sub>AREF0</sub>	-	-	ADC0 and ADC1 Reference Voltage
51	V <sub>AGND0</sub>	-	-	ADC Reference Ground
24	V <sub>DDMF</sub>	-	-	FADC Analog Part Power Supply (3.3V)
23	V <sub>DDAF</sub>	-	-	FADC Analog Part Logic Power Supply (1.3V)
25	V <sub>S<sub>SSMF</sub></sub>	-	-	FADC Analog Part Ground
	V <sub>S<sub>SSAF</sub></sub>	-	-	FADC Analog Part Ground
26	V <sub>FAREF</sub>	-	-	FADC Reference Voltage
27	V <sub>FAGND</sub>	-	-	FADC Reference Ground
10, 21 <sup>2)</sup> , 68, 84, 91, 99, 123, 153, 170 2)	V <sub>DD</sub>	-	-	Digital Core Power Supply (1.3V)

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
11, 20, 69, 83, 89, 100, 124, 139, 154, 171	$V_{DDP}$	-	-	<b>Port Power Supply (3.3V)</b>
12, 22, 70, 82, 85, 92, 101, 125, 140, 155, 172	$V_{SS}$	-	-	<b>Digital Ground</b>
105	$V_{DDOSC}$	-	-	<b>Main Oscillator and PLL Power Supply (1.3V)</b>
106	$V_{DDOSC3}$	-	-	<b>Main Oscillator Power Supply (3.3V)</b>
104	$V_{SSOSC}$	-	-	<b>Main Oscillator and PLL Ground</b>
141	$V_{DDFL3}$	-	-	<b>Power Supply for Flash (3.3V)</b>
102	XTAL1	I		<b>Main Oscillator Input</b>
103	XTAL2	O		<b>Main Oscillator Output</b>
111	TDI	I	A2/ PU	<b>JTAG Serial Data Input</b>
	BRKIN	I		<b>OCDS Break Input Line</b>
	BRKOUT	O		<b>OCDS Break Output Line</b>
112	TMS	I	A2/ PD	<b>JTAG State Machine Control Input</b>
	DAP1	I/O		<b>Device Access Port Line 1</b>

## Pinning TC1782 Pin Configuration

**Table 2 Pin Definitions and Functions (PG-LQFP-176-10 / PG-LQFP-176-20 Package) (cont'd)**

Pin	Symbol	Ctrl.	Type	Function
113	TDO	I/O	A2/ PU	<b>JTAG Serial Data Output</b>
	DAP2	I/O		<b>Device Access Port Line 2</b>
	BRKIN	I		<b>OCDS Break Input Line</b>
	BRKOUT	O		<b>OCDS Break Output Line</b>
114	TRST	I	I / PD	<b>JTAG Reset Input</b>
115	TCK	I	A1/ PD	<b>JTAG Clock Input</b>
	DAP0	I		<b>Device Access Port Line 0</b>
118	TESTMODE	I	I / PU	<b>Test Mode Select Input</b>
120	ESR1	I/O	A2/ PD	<b>External System Request Reset Input 1</b>
121	PORST	I	I / PD	<b>Power On Reset Input</b>
122	ESR0	I/O	A2	<b>External System Request Reset Input 0</b> Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset.

- 1) Only available for SAK-TC1782F-320F180HR, SAK-TC1782F-320F180HL, and SAK-TC1782F-320F160HR.
- 2) For the emulation device (ED), this pin is bonded to VDDSB (ED Stand By RAM supply). In the production device, this pin is bonded to a VDD pad.

**Legend for Table 2**

Column "Ctrl.":

 I = Input (for GPIO port lines with IOCR bit field selection  $PC_x = 0XXX_B$ )

O = Output

 O0 = Output with IOCR bit field selection  $PC_x = 1X00_B$ 

 O1 = Output with IOCR bit field selection  $PC_x = 1X01_B$  (ALT1)

 O2 = Output with IOCR bit field selection  $PC_x = 1X10_B$  (ALT2)

 O3 = Output with IOCR bit field selection  $PC_x = 1X11$  (ALT3)

Column "Type":

A1 = Pad class A1 (LVTTTL)

A1+ = Pad class A1+ (LVTTTL)

A2 = Pad class A2 (LVTTTL)

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**PinningTC1782 Pin Configuration**

F = Pad class F (LVDS/CMOS)

D = Pad class D (ADC)

I = Pad class I (LVTTTL)

PU = with pull-up device connected during reset ( $\overline{\text{PORST}} = 0$ )

PD = with pull-down device connected during reset ( $\overline{\text{PORST}} = 0$ )

TR = tri-state during reset ( $\overline{\text{PORST}} = 0$ )



## 4 Identification Registers

The Identification Registers uniquely identify the whole device.

**Table 3 SAK-TC1782F-320F180HR Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	8500 9310 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 4 SAK-TC1782F-320F180HL Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	0500 9310 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 5 SAK-TC1782N-320F180HR Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	8500 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 6 SAK-TC1782N-320F180HL Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	0500 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA

**Identification Registers**
**Table 6 SAK-TC1782N-320F180HL Identification Registers (cont'd)**

Short Name	Value	Address	Stepping
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 7 SAK-TC1782N-256F133HR Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	9400 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 8 SAK-TC1782N-256F133HL Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	1400 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 9 SAK-TC1782F-320F160HR Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	A500 9310 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Identification Registers**
**Table 10 SAK-TC1782F-320F160HL Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	2500 9310 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 11 SAK-TC1782N-320F160HR Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	A500 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

**Table 12 SAK-TC1782N-320F160HL Identification Registers**

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350 <sub>H</sub>	F000 0408 <sub>H</sub>	BA
CBS_JTAGID	1018 E083 <sub>H</sub>	F000 0464 <sub>H</sub>	BA
SCU_CHIPID	2500 9410 <sub>H</sub>	F000 0640 <sub>H</sub>	BA
SCU_MANID	0000 1820 <sub>H</sub>	F000 0644 <sub>H</sub>	BA
SCU_RTID	0000 0000 <sub>H</sub>	F000 0648 <sub>H</sub>	BA

## 5 Electrical Parameters

This specification provides all electrical parameters of the TC1782.

### 5.1 General Parameters

#### 5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1782 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column "Symbol":

- **CC**  
Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1782 and must be regarded for a system design.
- **SR**  
Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1782 designed in.

## Electrical Parameters General Parameters

## 5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the [Section 5.2.1](#).

Table 13 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade <sup>1)</sup>	Load <sup>1)</sup>	Leakage 150°C <sup>1)</sup>	Termination
A	3.3 V	LVTTTL I/O, LVTTTL outputs	A1 (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	1 μA	Series termination recommended
			A2 (e.g. serial I/Os)	40 MHz	50 pF	3 μA	Series termination recommended
F	3.3 V	LVDS	–	50 MHz	–	–	Parallel termination, 100 Ω ± 10% <sup>2)</sup>
		CMOS	–	6 MHz	50 pF	–	
D <sub>E</sub>	5 V	ADC	–	–	–	–	
I	3.3 V	LVTTTL (input only)	–	–	–	–	

1) These values show typical application configurations for the pad. Complete and detailed pad parameters are available in the individual pad parameter table on the following pages.

2) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

## Electrical Parameters General Parameters

**5.1.3 Absolute Maximum Ratings**

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 14 Absolute Maximum Rating Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	$T_{ST}$	SR	-65	–	150	°C	
Voltage at 1.3 V power supply pins with respect to $V_{SS}$	$V_{DD}$	SR	–	–	2.0	V	
Voltage at 3.3 V power supply pins with respect to $V_{SS}$	$V_{DDP}$ SR		–	–	4.33	V	
Voltage at 5 V power supply pins with respect to $V_{SS}$	$V_{DDM}$	SR	–	–	7.0	V	
Voltage on any Class A input pin and dedicated input pins with respect to $V_{SS}$	$V_{IN}$	SR	-0.6	–	$V_{DDP} + 0.7$ or max. 4.33	V	Whatever is lower
Voltage on any Class D analog input pin with respect to $V_{AGND0}$	$V_{AIN}$ $V_{AREF0}$	SR	-0.6	–	7.0	V	
Voltage on any shared Class D analog input pin with respect to $V_{SSAF}$ , if the FADC is switched through to the pin.	$V_{AINF}$	SR	-0.6	–	7.0	V	
Input current on any pin during overload condition	$I_{IN}$		-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$I_{IN}$		-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	$\Sigma I_{IN}$		–	–	200	mA	

1) The port groups are defined in [Table 19](#).

### 5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 15** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ( $V_{DDP}$  or  $V_{DDM}$ )
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

**Table 15** Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition except LVDS pins	$I_{IN}$	-5	–	+5	mA	
Input current on LVDS pins	$I_{INLVDS}$	-3	–	+3	mA	
Absolute sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$I_{ING}$	-20	–	+20	mA	
Input current on analog pins	$I_{INANA}$	-3	–	+3	mA	
Absolute sum of all analog input currents for analog inputs of a single ADC during overload condition	$I_{INSAS}$	-15	–	+15	mA	
Absolute sum of all input circuit currents during overload condition	$\Sigma I_{INS}$	-100	–	100	mA	

1) The port groups are defined in **Table 19**.

*Note: FADC input pins count as analog pin as they are overlaid with an ADC pins.*

**Table 16 PN-Junction Characteristics for positive Overload**

Pad Type	$I_{IN} = 3 \text{ mA}$	$I_{IN} = 5 \text{ mA}$
A1 / A1+ / F	$U_{IN} = V_{DDP} + 0.6 \text{ V}$	$U_{IN} = V_{DDP} + 0.7 \text{ V}$
A2	$U_{IN} = V_{DDP} + 0.5 \text{ V}$	$U_{IN} = V_{DDP} + 0.6 \text{ V}$
LVDS	$U_{IN} = V_{DDP} + 0.7 \text{ V}$	-
D	$U_{IN} = V_{DDM} + 0.6 \text{ V}$	-

**Table 17 PN-Junction Characteristics for negative Overload**

Pad Type	$I_{IN} = -3 \text{ mA}$	$I_{IN} = -5 \text{ mA}$
A1 / A1+ / F	$U_{IN} = V_{SS} - 0.6 \text{ V}$	$U_{IN} = V_{SS} - 0.7 \text{ V}$
A2	$U_{IN} = V_{SS} - 0.5 \text{ V}$	$U_{IN} = V_{SS} - 0.6 \text{ V}$
LVDS	$U_{IN} = V_{SS} - 0.7 \text{ V}$	-
D	$U_{IN} = V_{SSM} - 0.6 \text{ V}$	-

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery without having any negative reliability impact on the operational life-time.*



## Electrical Parameters General Parameters

## 5.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1782.

Digital supply voltages applied to the TC1782 must be static regulated voltages which allow a typical voltage swing of  $\pm 5\%$ .

All parameters specified in the following tables refer to these operating conditions (**Table 18**), unless otherwise noticed in the Note / Test Condition column.

The **Voltage Operating Timing Profiles** did not increase area of validity of the parameters defined in table 8 and later.

**Table 18 Operating Conditions Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, negative	$K_{OVAN}$ CC	–	–	0.000 1		$I_{OV} \leq 0$ mA; $I_{OV} \geq -2$ mA; analog pad= 5.0 V
Overload coupling factor for analog inputs, positive	$K_{OVAP}$ CC	–	–	0.000 01		$I_{OV} \leq 3$ mA; $I_{OV} \geq 0$ mA; analog pad= 5.0 V
CPU Frequency	$f_{CPU}$ SR	–	–	133	MHz	SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	180	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL
		–	–	160	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

## Electrical Parameters General Parameters

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FPI bus frequency	$f_{\text{FPI SR}}$	–	–	90	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782F-256F133HR / SAK-TC1782F-256F133HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	80	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

**Electrical Parameters General Parameters**
**Table 18 Operating Conditions Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
LMB frequency	$f_{LMB}$ CC	–	–	133	MHz	SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	180	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL
		–	–	160	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL

## Electrical Parameters General Parameters

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PCP Frequency	$f_{PCP}$ SR	–	–	133	MHz	SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL
		–	–	180	MHz	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL
		–	–	160	MHz	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL
Inactive device pin current	$I_{ID}$ SR	-1	–	1	mA	All power supply voltages $V_{DDx} = 0$
Short circuit current of digital outputs <sup>1)</sup>	$I_{SC}$ SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	$\Sigma I_{SC\_D}$ CC	–	–	100	mA	
Absolute sum of short circuit currents per pin group	$\Sigma I_{SC\_PG}$ CC	–	–	20	mA	
Ambient Temperature	$T_A$ SR	-40	–	125	°C	
Junction temperature	$T_J$ SR	-40	–	150	°C	

## Electrical Parameters General Parameters

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Core Supply Voltage	$V_{DD}$ SR	1.235	1.3	1.365 <sup>2)</sup>	V	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
		1.17	1.3	1.43 <sup>2)</sup>	V	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
Flash supply voltage 3.3V	$V_{DDFL3}$ SR	2.97	3.3	3.63 <sup>4)</sup>	V	for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
ADC analog supply voltage	$V_{DDM}$ SR	2.97	3.3	5.5 <sup>3)</sup>	V	

## Electrical Parameters General Parameters

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator core supply voltage	V <sub>DDOSC</sub> SR	1.235	1.3	1.365 <sup>2)</sup>	V	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
		1.17	1.3	1.43 <sup>2)</sup>	V	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
Oscillator 3.3V supply voltage	V <sub>DDOSC3</sub> SR	2.97	3.3	3.63 <sup>4)</sup>	V	for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
Digital supply voltage for IO pads	V <sub>DDP</sub> SR	2.97	3.3	3.63 <sup>4)</sup>	V	for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>

## Electrical Parameters General Parameters

Table 18 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VDDP voltage to ensure defined pad states <sup>5)</sup>	$V_{DDPPA}$ CC	0.65	–	–	V	
Digital ground voltage	$V_{SS}$ SR	0	–	–	V	
Analog ground voltage for $V_{DDM}$	$V_{SSM}$ SR	-0.1	0	0.1	V	
Analog core supply	$V_{DDAF}$ SR	1.235	1.3	1.365 <sup>2)</sup>	V	SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782N-320F180HR / SAK-TC1782N-320F180HL / SAK-TC1782N-256F133HR / SAK-TC1782N-256F133HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
		1.17	1.3	1.43 <sup>2)</sup>	V	SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782N-320F160HR / SAK-TC1782N-320F160HL; for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>

## Electrical Parameters General Parameters

**Table 18 Operating Conditions Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FADC / ADC analog supply voltage	$V_{DDMF}$ SR	2.97	3.3	3.63 <sup>4)</sup>	V	for duration limitation see <a href="#">Voltage Operating Timing Profiles</a>
Analog ground voltage for $V_{DDMF}$	$V_{SSAF}$ SR	-0.1	0	0.1	V	

- 1) Applicable for digital outputs.
- 2) Voltage overshoot to 1.7V is permissible at Power-Up and  $\overline{PORST}$  low, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h.
- 3) Voltage overshoot to 6.5V is permissible at Power-Up and  $\overline{PORST}$  low, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h.
- 4) Voltage overshoot to 4.0V is permissible at Power-Up and  $\overline{PORST}$  low, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h.
- 5) This parameter is valid under the assumption the  $\overline{PORST}$  signal is constantly at low level during the power-up/power-down of  $V_{DDP}$ .

**Voltage Operating Timing Profiles**

- $1.3V < V_{DD} / V_{DDOSC} / V_{DDAF} < 1.3V + 5\%$ :
  - limited to Operation Lifetime ( $t_{OP}$ ) (see [Table 46](#))
- $1.3V + 5\% < V_{DD} / V_{DDOSC} / V_{DDAF} < 1.3V + 7.5\%$  (overvoltage condition):
  - limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $1.3V + 7.5\% < V_{DD} / V_{DDOSC} / V_{DDAF} < 1.3V + 10\%$  (overvoltage condition):
  - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $3.3V < V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF} < 3.3V + 5\%$ :
  - limited to Operation Lifetime ( $t_{OP}$ ) (see [Table 46](#))
- $V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF} < 3.3V + 10\%$ 
  - $3.3V + 5\% < V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF} < 3.3V + 10\%$  (overvoltage condition):
    - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $5V < V_{DDM} < 5V + 10\%$ :
  - limited to Operation Lifetime ( $t_{OP}$ ) (see [Table 46](#))



**Table 19 Pin Groups for Overload / Short-Circuit Current Sum Parameter**

Group	Pins
1	P5.[7:2], P5.15
2	P5.[9:8]
3	P5.[11:10]
4	P5.[14:12]
5	P1.[14:12], P2.0
6	P2.[4:1]
7	P2.[7:5]
8	P4.[2:0]
9	P4.3
10	P1.2, P1.8
11	P1.[10:9]
12	P1.3, P1.11
13	P1.[7:4]
14	P1.[1:0], P1.15
15	P3.[8:5], P3.[3:2]
16	P3.[1:0], P3.4, P3.[10:9], P3.[15:14]
17	P0.[1:0], P3.[13:11]
18	P0.[3:2], P0.[9:8]
19	P0.[11:10]
20	P6.[3:0]
21	P2.[13:8]
22	P0.[5:4], P0.[13:12]
23	P0.[7:6], P0.[15:14], P5.[1:0]

## 5.2 DC Parameters

### 5.2.1 Input/Output Pins

**Table 20 Standard\_Pads Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	$C_{IO}$ CC	–	–	10	pF	$T_A = 25\text{ }^\circ\text{C}$ ; $f = 1\text{ MHz}$
Pull-down current	$ I_{PDL} $ CC	–	–	150	$\mu\text{A}$	$V_i \geq 0.6 \times V_{DDP}$ V
		10	–	–	$\mu\text{A}$	$V_i \geq 0.36 \times V_{DDP}$ V
Pull-Up current	$ I_{PUH} $ CC	10	–	–	$\mu\text{A}$	$V_i \leq 0.6 \times V_{DDP}$ V
		–	–	100	$\mu\text{A}$	$V_i \leq 0.36 \times V_{DDP}$ V
Spike filter always blocked pulse duration	$t_{SF1}$ CC	–	–	10	ns	only PORST pin
Spike filter pass-through pulse duration	$t_{SF2}$ CC	100	–	–	ns	only PORST pin

**Table 21 Standard\_Pads Class\_A1**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1 pads <sup>1)</sup>	$HYS_{AI}$ CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage Current Class A1	$I_{OZA1}$ CC	-500	–	500	nA	$V_i \geq 0\text{ V}$ ; $V_i \leq V_{DDP}$ V
Ratio $V_{ih}/V_{il}$ , A1 pads	$V_{ILA1} / V_{IHA1}$ CC	0.6	–	–		
On-Resistance of the class A1 pad, weak driver	$R_{DSONW}$ CC	–	450	600	Ohm	$I_{OH} < -0.5\text{ mA}$ ; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5\text{ mA}$ ; N_MOS

## Electrical Parameters DC Parameters

Table 21 Standard\_Pads Class\_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1 pad, medium driver	$R_{DSONM}$ CC	–	–	155	Ohm	$I_{OH} < -2$ mA; P_MOS
		–	–	110	Ohm	$I_{OL} < 2$ mA; N_MOS
Fall time, pad type A1	$t_{FA1}$ CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak

## Electrical Parameters DC Parameters

Table 21 Standard\_Pads Class\_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1	$t_{RA1}$ CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak
Input high voltage class A1 pads	$V_{IHA1}$ SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage class A1 pads	$V_{ILA1}$ SR	-0.3	–	$0.36 \times V_{DDP}$	V	

## Electrical Parameters DC Parameters

Table 21 Standard\_Pads Class\_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1 pads	$V_{\text{OHA1}}$ CC	$V_{\text{DDP}} - 0.4$	–	–	V	$I_{\text{OH}} \geq -1.4$ mA; pin out driver= medium
		2.4	–	–	V	$I_{\text{OH}} \geq -2$ mA; pin out driver= medium
		$V_{\text{DDP}} - 0.4$	–	–	V	$I_{\text{OH}} \geq -400$ $\mu$ A; pin out driver= weak
		2.4	–	–	V	$I_{\text{OH}} \geq -500$ $\mu$ A; pin out driver= weak
Output voltage low class A1 pads	$V_{\text{OLA1}}$ CC	–	–	0.4	V	$I_{\text{OL}} \leq 2$ mA; pin out driver= medium
		–	–	0.4	V	$I_{\text{OL}} \leq 500$ $\mu$ A; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 22 Standard\_Pads Class\_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1+ pads <sup>1)</sup>	$H_{\text{YSA1}}$ + CC	$0.1 \times V_{\text{DDP}}$	–	–	V	
Input Leakage Current Class A1+	$I_{\text{OZA1+}}$ CC	-1000	–	1000	nA	
On-Resistance of the class A1+ pad, weak driver	$R_{\text{DSONW}}$ CC	–	450	600	Ohm	$I_{\text{OH}} < -0.5$ mA; P_MOS
		–	210	340	Ohm	$I_{\text{OL}} < 0.5$ mA; N_MOS

## Electrical Parameters DC Parameters

Table 22 Standard\_Pads Class\_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, medium driver	$R_{DSONM}$ CC	–	–	155	Ohm	$I_{OH} < -2$ mA; P_MOS
		–	–	110	Ohm	$I_{OL} < 2$ mA; N_MOS
On-Resistance of the class A1+ pad, strong driver	$R_{DSON1+}$ CC	–	–	100	Ohm	$I_{OH} < -2$ mA; P_MOS
		–	–	80	Ohm	$I_{OL} < 2$ mA; N_MOS
Fall time, pad type A1+	$t_{FA1+}$ CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	28	ns	$C_L = 50$ pF; edge= slow ; pin out driver= strong
		–	–	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak
		–	–			

## Electrical Parameters DC Parameters

Table 22 Standard\_Pads Class\_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	$t_{RA1+}$ CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	28	ns	$C_L = 50$ pF; edge= slow ; pin out driver= strong
		–	–	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak
Input high voltage, Class A1+ pads	$V_{IHA1+}$ SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage Class A1+ pads	$V_{ILA1+}$ SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Ratio $V_{il}/V_{ih}$ , A1+ pads	$V_{ILA1+} / V_{IHA1+}$ CC	0.6	–	–		

## Electrical Parameters DC Parameters

Table 22 Standard\_Pads Class\_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1+ pads	$V_{\text{OHA1+CC}}$	$V_{\text{DDP}} - 0.4$	—	—	V	$I_{\text{OH}} \geq -1.4 \text{ mA}$ ; pin out driver= medium
		$V_{\text{DDP}} - 0.4$	—	—	V	$I_{\text{OH}} \geq -1.4 \text{ mA}$ ; pin out driver= strong
		2.4	—	—	V	$I_{\text{OH}} \geq -2 \text{ mA}$ ; pin out driver= medium
		2.4	—	—	V	$I_{\text{OH}} \geq -2 \text{ mA}$ ; pin out driver= strong
		$V_{\text{DDP}} - 0.4$	—	—	V	$I_{\text{OH}} \geq -400 \mu\text{A}$ ; pin out driver= weak
		2.4	—	—	V	$I_{\text{OH}} \geq -500 \mu\text{A}$ ; pin out driver= weak
Output voltage low class A1+ pads	$V_{\text{OLA1+CC}}$	—	—	0.4	V	$I_{\text{OL}} \leq 2 \text{ mA}$ ; pin out driver= medium
		—	—	0.4	V	$I_{\text{OL}} \leq 2 \text{ mA}$ ; pin out driver= strong
		—	—	0.4	V	$I_{\text{OL}} \leq 500 \mu\text{A}$ ; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.



## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads <sup>1)</sup>	$H Y S A 2$ CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage current Class A2	$I_{O Z A 2}$ CC	-6000	–	6000	nA	$V_i < V_{DDP} / 2 - 1 \text{ V}; V_i > V_{DDP} / 2 + 1 \text{ V}; V_i \geq 0 \text{ V}; V_i \leq V_{DDP} \text{ V}$
		-3000	–	3000	nA	$V_i > V_{DDP} / 2 - 1 \text{ V}; V_i < V_{DDP} / 2 + 1 \text{ V}$
Ratio $V_{il}/V_{ih}$ , A2 pads	$V_{I L A 2} / V_{I H A 2}$ CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	$R_{D S O N W}$ CC	–	450	600	Ohm	$I_{OH} < -0.5 \text{ mA}; P\_MOS$
		–	210	340	Ohm	$I_{OL} < 0.5 \text{ mA}; N\_MOS$
On-Resistance of the class A2 pad, medium driver	$R_{D S O N M}$ CC	–	–	155	Ohm	$I_{OH} < -2 \text{ mA}; P\_MOS$
		–	–	110	Ohm	$I_{OL} < 2 \text{ mA}; N\_MOS$
On-Resistance of the class A2 pad, strong driver	$R_{D S O N 2}$ CC	–	–	28	Ohm	$I_{OH} < -2 \text{ mA}; P\_MOS$
		–	–	22	Ohm	$I_{OL} < 2 \text{ mA}; N\_MOS$

## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, pad type A2	$t_{FA2}$ CC	–	–	150	ns	$C_L = 20$ pF; pin out driver= weak
		–	–	7	ns	$C_L = 50$ pF; edge= medium ; pin out driver= strong
		–	–	10	ns	$C_L = 50$ pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	$C_L = 50$ pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	$C_L = 50$ pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	$C_L = 50$ pF; edge= soft ; pin out driver= strong
		–	–	50	ns	$C_L = 50$ pF; pin out driver= medium
		–	–	7.5	ns	$C_L = 100$ pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	$C_L = 150$ pF; pin out driver= medium

## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	$C_L = 150 \text{ pF}$ ; pin out driver= weak
		–	–	18000	ns	$C_L = 20000 \text{ pF}$ ; pin out driver= medium
		–	–	65000	ns	$C_L = 20000 \text{ pF}$ ; pin out driver= weak

## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A2	$t_{RA2\ CC}$	–	–	150	ns	$C_L = 20\ \text{pF}$ ; pin out driver= weak
		–	–	7.0	ns	$C_L = 50\ \text{pF}$ ; edge= medium ; pin out driver= strong
		–	–	10	ns	$C_L = 50\ \text{pF}$ ; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	$C_L = 50\ \text{pF}$ ; edge= sharp ; pin out driver= strong
		–	–	5	ns	$C_L = 50\ \text{pF}$ ; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	$C_L = 50\ \text{pF}$ ; edge= soft ; pin out driver= strong
		–	–	50	ns	$C_L = 50\ \text{pF}$ ; pin out driver= medium
		–	–	7.5	ns	$C_L = 100\ \text{pF}$ ; edge= sharp ; pin out driver= strong
		–	–	140	ns	$C_L = 150\ \text{pF}$ ; pin out driver= medium

## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	$C_L = 150$ pF; pin out driver= weak
		–	–	18000	ns	$C_L = 20000$ pF; pin out driver= medium
		–	–	65000	ns	$C_L = 20000$ pF; pin out driver= weak
Input high voltage, class A2 pads	$V_{IHA2}$ SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage Class A2 pads	$V_{ILA2}$ SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Output voltage high class A2 pads	$V_{OHA2}$ CC	$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4$ mA; pin out driver= medium
		$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4$ mA; pin out driver= strong
		2.4	–	–	V	$I_{OH} \geq -2$ mA; pin out driver= medium
		2.4	–	–	V	$I_{OH} \geq -2$ mA; pin out driver= strong
		$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -400$ $\mu$ A; pin out driver= weak
		2.4	–	–	V	$I_{OH} \geq -500$ $\mu$ A; pin out driver= weak

## Electrical Parameters DC Parameters

Table 23 Standard\_Pads Class\_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage low class A2 pads	$V_{OLA2}$ CC	–	–	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= medium
		–	–	0.4	V	$I_{OL} \leq 2$ mA; pin out driver= strong
		–	–	0.4	V	$I_{OL} \leq 500$ $\mu$ A; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

Table 24 Standard\_Pads Class\_F

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis F <sup>1)</sup>	$HYSF$ CC	$0.05 \times V_{DDP}$	–	–	V	
Input Leakage Current Class F	$I_{OZF}$ CC	-6000	–	6000	nA	$V_i < V_{DDP} / 2 - 1$ V; $V_i > V_{DDP} / 2 + 1$ V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP} / 2 - 1$ V; $V_i < V_{DDP} / 2 + 1$ V
Ratio $V_{il}$ / $V_{ih}$ , F pads	$V_{ILF} / V_{IHF}$ CC	0.6	–	–		
On-Resistance of the class F pad, medium driver	$R_{DSONM}$ CC	–	–	170	Ohm	$I_{OH} < -2$ mA; P_MOS
		–	–	175	Ohm	$I_{OH} < -2$ mA; P_MOS; $V_{DDP} \geq \pm 5\% \cdot V_D$ DP
		–	–	145	Ohm	$I_{OL} < 2$ mA; N_MOS

## Electrical Parameters DC Parameters

**Table 24 Standard\_Pads Class\_F (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, pad type F, CMOS mode	$t_{FF}$ CC	–	–	60	ns	$C_L = 50$ pF
Rise time, pad type F, CMOS mode	$t_{RF}$ CC	–	–	60	ns	$C_L = 50$ pF
Input high voltage, pad class F, CMOS mode	$V_{IHF}$ SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage, Class F pads, CMOS mode	$V_{ILF}$ SR	-0.3	–	$0.36 \times V_{DDP}$	V	
Output high voltage, class F pads, CMOS mode	$V_{OHF}$ CC	$V_{DDP} - 0.4$	–	–	V	$I_{OH} \geq -1.4$ mA
		2.4	–	–	V	$I_{OH} \geq -2$ mA
Output low voltage, class F pads, CMOS mode	$V_{OLF}$ CC	–	–	0.4	V	$I_{OL} \leq 2$ mA

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

**Table 25 Standard\_Pads Class\_I**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis Class I <sup>1)</sup>	$HYSI$ CC	$0.1 \times V_{DDP}$	–	–	V	
Input Leakage Current	$I_{OZI}$ CC	-1000	–	1000	nA	
Ratio between low and high input threshold	$V_{ILI} / V_{IHI}$ CC	0.6	–	–		
Input high voltage, class I pins	$V_{IHI}$ SR	$0.6 \times V_{DDP}$	–	$\min(V_{DDP} + 0.3, 3.6)$	V	
Input low voltage, Class I pads	$V_{ILI}$ SR	-0.3	–	$0.36 \times V_{DDP}$	V	

**Electrical Parameters DC Parameters**

- 1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

**Table 26 LVDS\_Pads Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance, pad class F, LVDS mode	$R_O$ CC	40	–	140	Ohm	
Fall time, pad type LVDS	$t_{FL}$ CC	–	–	2	ns	termination 100 $\Omega$ $\pm$ 1 %
Rise time, pad type LVDS	$t_{RL}$ CC	–	–	2	ns	termination 100 $\Omega$ $\pm$ 1 %
Pad set-up time	$t_{SET\_LVD}$ $S$ CC	–	–	13	$\mu$ s	termination 100 $\Omega$ $\pm$ 1 %
Output Differential Voltage	$V_{OD}$ CC	150	–	400	mV	termination 100 $\Omega$ $\pm$ 1 %
Output voltage high, pad class F, LVDS mode	$V_{OH}$ CC	–	–	1525	mV	termination 100 $\Omega$ $\pm$ 1 %
Output voltage low, pad class F, LVDS mode	$V_{OL}$ CC	875	–	–	mV	termination 100 $\Omega$ $\pm$ 1 %
Output Offset Voltage	$V_{OS}$ CC	1075	–	1325	mV	termination 100 $\Omega$ $\pm$ 1 %



## Electrical Parameters DC Parameters

## 5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for  $V_{DD} / V_{DDAF} = 1.17 \text{ V to } 1.43 \text{ V}$ ;  $V_{DDM} = 4.5 \text{ V to } 5.5 \text{ V}$ .

Table 27 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs <sup>1)</sup>	$C_{AINSW}$ CC	–	9	20	pF	
Total capacitance of an analog input	$C_{AINTOT}$ CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input <sup>2)(3)</sup>	$C_{AREFSW}$ CC	–	15	30	pF	
Total capacitance of the voltage reference inputs <sup>2)</sup>	$C_{AREFTO}$ T CC	–	20	40	pF	
Differential Non-Linearity Error <sup>4)(5)(6)(7)</sup>	$EA_{DNL}$ CC	-3	–	3	LSB	ADC resolution= 12-bit <sup>8) 9)</sup>
Gain Error <sup>4)(6)(5)(7)</sup>	$EA_{GAIN}$ CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit <sup>8) 9)</sup>
Integral Non-Linearity <sup>4)(6)(5)(7)</sup>	$EA_{INL}$ CC	-3	–	3	LSB	ADC resolution= 12-bit <sup>8) 9)</sup>
Offset Error <sup>4)(6)(5)(7)</sup>	$EA_{OFF}$ CC	-4	–	4	LSB	ADC resolution= 12-bit <sup>8) 9)</sup>

**Electrical Parameters DC Parameters**
**Table 27 ADC Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Converter clock	$f_{\text{ADC SC}}$	4	–	90	MHz	$f_{\text{ADC}} = f_{\text{FPI}}$ ; SAK-TC1782F-320F180HR / S AK-TC1782F-320F180HL / S AK-TC1782N-320F180HR / S AK-TC1782N-320F180HL / S AK-TC1782N-256F133HR / S AK-TC1782N-256F133HL
		4	–	80	MHz	$f_{\text{ADC}} = f_{\text{FPI}}$ ; SAK-TC1782F-320F160HR / S AK-TC1782F-320F160HL / S AK-TC1782N-320F160HR / S AK-TC1782N-320F160HL
Internal ADC clock	$f_{\text{ADCI CC}}$	1	–	18	MHz	
Charge consumption per conversion	$Q_{\text{CONV CC}}$	70	85 <sup>(10)</sup>	100	pC	charge needs to be provided via $V_{\text{AREF0}}$

## Electrical Parameters DC Parameters

Table 27 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage at analog inputs <sup>11)</sup>	$I_{OZ1}$ CC	-100	–	500	nA	$V_i \leq V_{DDM} V$ ; $V_i \geq 0.97 \times V_{DDM} V$ ; overlaid= No
		-100	–	600	nA	$V_i \geq 0.97 \times V_{DDM} V$ ; $V_i \leq V_{DDM} V$ ; overlaid= Yes
		-500	–	100	nA	$V_i \leq 0.03 \times V_{DDM} V$ ; $V_i \geq 0 V$ ; overlaid= No
		-600	–	100	nA	$V_i \leq 0.03 \times V_{DDM} V$ ; $V_i \geq 0 V$ ; overlaid= Yes
		-100	–	200	nA	$V_i > 0.03 \times V_{DDM} V$ ; $V_i < 0.97 \times V_{DDM} V$ ; overlaid= No
		-100	–	300	nA	$V_i < 0.97 \times V_{DDM} V$ ; $V_i > 0.03 \times V_{DDM} V$ ; overlaid= Yes
Input leakage current at V <sub>aref0</sub>	$I_{OZ2}$ CC	-2	–	2	μA	$V_{AREF0} \leq V_{DDM} V$
Input leakage current at V <sub>agnd0</sub>	$I_{OZ3}$ CC	-2	–	2	μA	$V_{AGND0} \leq V_{DDM} V$
ON resistance of the transmission gates in the analog voltage path	$R_{AIN}$ CC	–	900	1500	Ohm	
ON resistance for the ADC test (pull down for AIN7)	$R_{AIN7T}$ CC	180	550	900	Ohm	

## Electrical Parameters DC Parameters

Table 27 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the reference voltage input path	$R_{AREF}$ CC	–	500	1000	Ohm	
Sample time	$t_S$ CC	2	–	257	$T_{ADCI}$	
Calibration time after bit ADC_GLOB_CFG.SUCAL is set	$t_{CAL}$ CC	–	–	4352	cycle s	
Total Unadjusted Error <sup>6)5)12)</sup>	$TUE$ CC	-4	–	4 <sup>13)</sup>	LSB	ADC resolution= 12-bit
Analog reference ground <sup>2)</sup>	$V_{AGND0}$ SR	$V_{SSM} - 0.05$	–	$V_{AREF0} - 1$	V	
Analog input voltage	$V_{AIN}$ SR	$V_{AGND0}$	–	$V_{AREF0}$	V	
Analog reference voltage <sup>2)</sup>	$V_{AREF0}$ SR	$V_{AGND0} + 1$	–	$V_{DDM} + 0.05$ <sup>14) 15)</sup>	V	
Analog reference voltage range <sup>6)5)2)</sup>	$V_{AREF0} - V_{AGND0}$ SR	$V_{DDM}/2$	–	$V_{DDM} + 0.05$	V	

- 1) The sampling capacity of the conversion C-network is pre-charged to  $V_{AREF0}/2$  before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from  $V_{AREF0}/2$ .
- 2) Applies to AINx, when used as auxiliary reference input.
- 3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.
- 4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
- 5) If a reduced analog reference voltage between 1V and  $V_{DDM}/2$  is used, then there are additional decrease in the ADC speed and accuracy.
- 6) If the analog reference voltage range is below  $V_{DDM}$  but still in the defined range of  $V_{DDM}/2$  and  $V_{DDM}$  is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k ( $k < 1$ ), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.
- 7) If the analog reference voltage is  $> V_{DDM}$ , then the ADC converter errors increase.
- 8) For 10-bit conversions the error value must be multiplied with a factor 0.25.
- 9) For 8-bit conversions the error value must be multiplied with a factor 0.0625.
- 10) For a conversion time of 1  $\mu$ s a rms value of 85 $\mu$ A result for  $I_{AREF0}$ .
- 11) The leakage current definition is a continuous function, as shown in figure ADCx Analogue Input Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

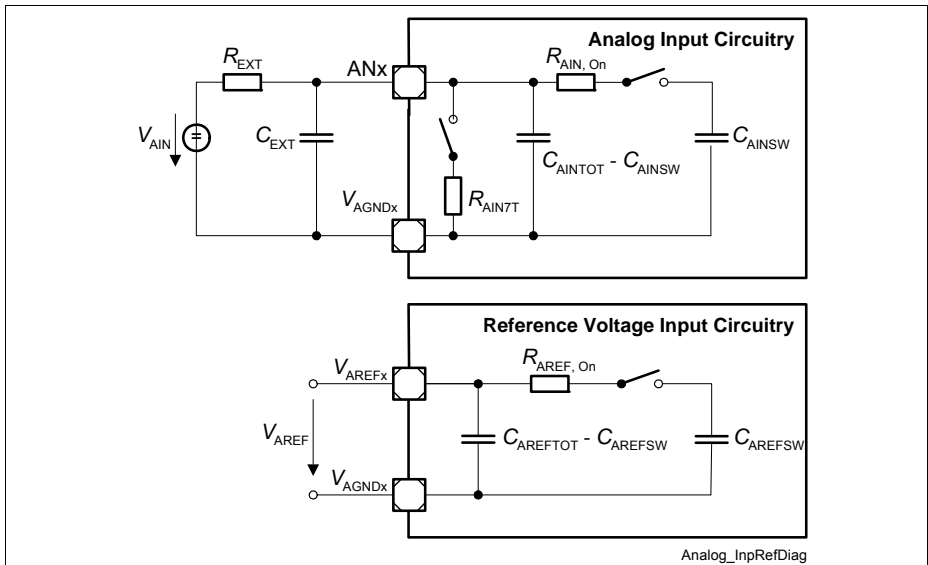
**Electrical Parameters DC Parameters**

- 12) Measured without noise.
- 13) For 10-bit conversion the TUE is  $\pm 2\text{LSB}$ ; for 8-bit conversion the TUE is  $\pm 1\text{LSB}$
- 14) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).
- 15) If the reference voltage  $V_{\text{AREF0}}$  increase or the  $V_{\text{DDM}}$  decrease, so that  $V_{\text{AREF}} = (V_{\text{DDM}} + 0.05\text{V to } V_{\text{DDM}} + 0.07\text{V})$ , then the accuracy of the ADC decrease by 4LSB12.

**Table 28 Conversion Time (Operating Conditions apply)**

Parameter	Symbol	Values	Unit	Note
Conversion time with post-calibration	$t_c$ CC	$2 \times T_{\text{ADC}} + (4 + \text{STC} + n) \times T_{\text{ADCI}}$	$\mu\text{s}$	$n = 8, 10, 12$ for $n$ -bit conversion $T_{\text{ADC}} = 1 / f_{\text{FPI}}$ $T_{\text{ADCI}} = 1 / f_{\text{ADCI}}$
Conversion time without post-calibration		$2 \times T_{\text{ADC}} + (2 + \text{STC} + n) \times T_{\text{ADCI}}$		

The power-up calibration of the ADC requires a maximum number of  $4352 \cdot f_{\text{ADCI}}$  cycles.



**Figure 7 ADCx Input Circuits**

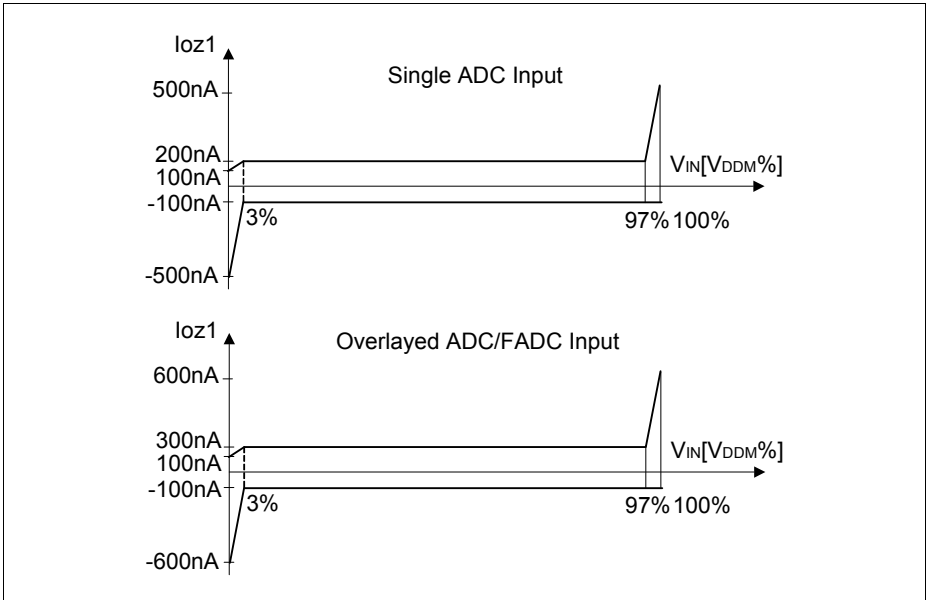


Figure 8 ADCx Analog Inputs Leakage

## 5.2.3 Fast Analog to Digital Converter (FADC)

Table 29 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at VFAREF	$I_{\text{FAREF CC}}$	–	–	120	$\mu\text{A}$	
Input leakage current at VFAREF <sup>1)</sup>	$I_{\text{FOZ2 CC}}$	-500	–	500	nA	$V_{\text{FAREF}} \leq V_{\text{DDMF}}$ $V; V_{\text{FAREF}} \geq 0 \text{ V}$
Input leakage current at VFAGND	$I_{\text{FOZ3 CC}}$	-500	–	500	nA	

## Electrical Parameters DC Parameters

Table 29 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DNL error	$EF_{DNL}$ CC	-1	–	1	LSB	$V_{IN}$ mode= differential; Gain = 1 or 2; Gain = 4 or 8 and $V_{DDAF} / V_{DDMF} \leq \pm 5\% * V_{DDAF} / V_{DDMF}$ [Typ]
		-1	–	1	LSB	$V_{IN}$ mode= single ended; Gain = 1 or 2; Gain = 4 or 8 and $V_{DDAF} / V_{DDMF} \leq \pm 5\% * V_{DDAF} / V_{DDMF}$ [Typ]
		-2	–	2	LSB	$V_{IN}$ mode= differential; Gain = 4 or 8 and $V_{DDAF} / V_{DDMF} > \pm 5\% * V_{DDAF} / V_{DDMF}$ [Typ] <sup>2)</sup>
		-2	–	2	LSB	$V_{IN}$ mode= single ended; Gain = 4 or 8 and $V_{DDAF} / V_{DDMF} > \pm 5\% * V_{DDAF} / V_{DDMF}$ [Typ] <sup>2)</sup>



## Electrical Parameters DC Parameters

Table 29 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GRADient error	$EF_{\text{GRAD CC}}$	-5	–	5	%	$V_{\text{IN}}$ mode= differential ; Gain $\leq 4$
		-5	–	5	%	$V_{\text{IN}}$ mode= single ended ; Gain $\leq 4$
		-6	–	6	%	$V_{\text{IN}}$ mode= differential ; Gain = 8
		-6	–	6	%	$V_{\text{IN}}$ mode= single ended ; Gain = 8
INL error	$EF_{\text{INL CC}}$	-4	–	4	LSB	$V_{\text{IN}}$ mode= differential
		-4	–	4	LSB	$V_{\text{IN}}$ mode= single ended
Offset error	$EF_{\text{OFF CC}}$	-90	–	90	mV	$V_{\text{IN}}$ mode= differential ; Calibration= No
		-90	–	90	mV	$V_{\text{IN}}$ mode= single ended ; Calibration= No
		-20	–	20	mV	$V_{\text{IN}}$ mode= differential ; Calibration= $Y_{\text{eS}}^{3(4)}$
		-20	–	20	mV	$V_{\text{IN}}$ mode= single ended ; Calibration= $Y_{\text{eS}}^{3(4)}$
Error of common mode voltage $V_{\text{FAREF}}/2$	$EF_{\text{REF CC}}$	-60	–	60	mV	
Channel amplifier cutoff frequency	$f_{\text{COFF CC}}$	2	–	–	MHz	

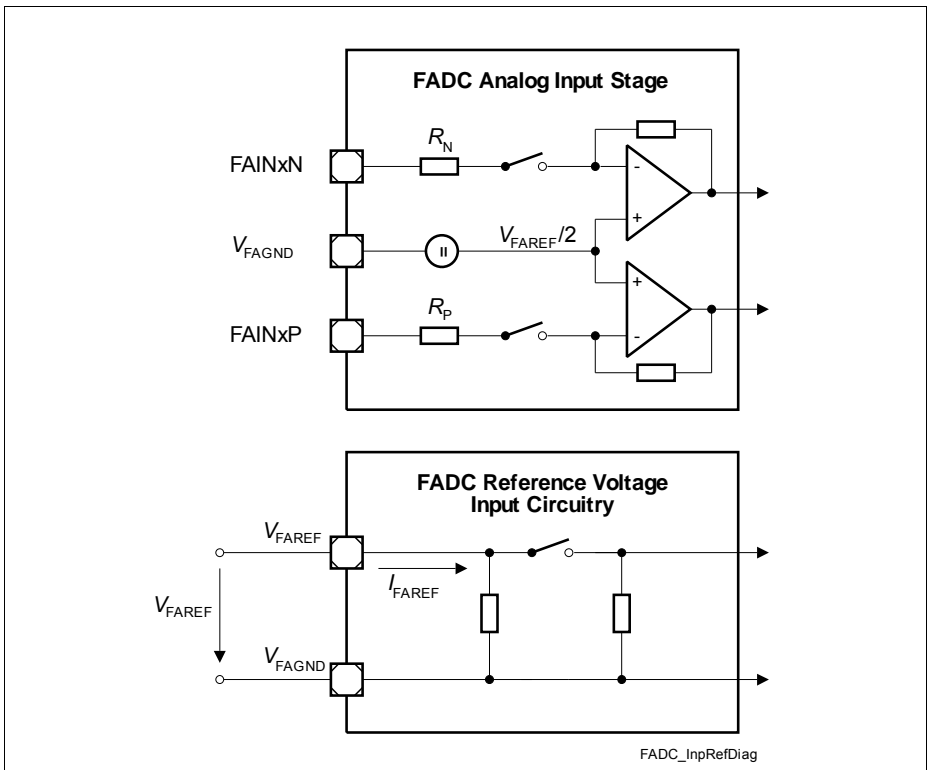
**Electrical Parameters DC Parameters**
**Table 29 FADC Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Converter clock	$f_{FADC}$ SC	1	–	90	MHz	$f_{FADC} = f_{FPI}$ ; SAK-TC1782F-320F180HR / S AK-TC1782F-320F180HL / S AK-TC1782N-320F180HR / S AK-TC1782N-320F180HL / S AK-TC1782N-256F133HR / S AK-TC1782N-256F133HL
		1	–	80	MHz	$f_{FADC} = f_{FPI}$ ; SAK-TC1782F-320F160HR / S AK-TC1782F-320F160HL / S AK-TC1782N-320F160HR / S AK-TC1782N-320F160HL
Conversion time	$t_C$ CC	–	–	21	1 / $f_{FADC}$	For 10-bit conversion
Input resistance of the analog voltage path (Rn, Rp)	$R_{FAIN}$ CC	100	–	200	kOh m	
Settling time of a channel amplifier after changing ENN or ENP	$t_{SET}$ CC	–	–	5	$\mu$ s	
Analog input voltage range	$V_{AINF}$ SR	$V_{FAGND}$	–	$V_{DDMF}$	V	
Analog reference ground	$V_{FAGND}$ SR	$V_{SSAF} - 0.05$	–	$V_{SSAF} + 0.05$	V	
Analog reference voltage	$V_{FAREF}$ SR	3.0	–	3.63 <sup>5)</sup> 6)	V	

**Electrical Parameters DC Parameters**

- 1) This value applies in power-down mode.
- 2) No missing codes.
- 3) Calibration should be preformed at each power-up. In case of a continuous operation, it should be performed minimum once per week.
- 4) The offset error voltage drifts over the whole temperature range maximum +3LSB.
- 5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h.
- 6) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.



**Figure 9 FADC Input Circuits**

## 5.2.4 Oscillator Pins

Table 30 OSC\_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	$I_{IX1}$ CC	-25	–	25	$\mu\text{A}$	$V_{IN} < V_{DDOSC3}$ ; $V_{IN} > 0$ V
Input frequency	$f_{OSC}$ SR	4	–	40	MHz	Direct Input Mode selected
		8	–	25	MHz	External Crystal Mode selected
Oscillator start-up time <sup>1)</sup>	$t_{OSCS}$ CC	–	–	10	ms	
Input high voltage at XTAL1 <sup>2)</sup>	$V_{IHx}$ SR	$0.7 \times V_{DDOS C3}$	–	$V_{DDOS C3} + 0.5$	V	
Input low voltage at XTAL1	$V_{ILx}$ SR	-0.5	–	$0.3 \times V_{DDOS C3}$	V	
Input Hysteresis for XTAL1 pad <sup>3)</sup>	$HYSAX$ CC	–	–	200	mV	

1)  $t_{OSCS}$  is defined from the moment when  $V_{DDOSC3} = 3.13\text{V}$  until the oscillations reach an amplitude at XTAL1 of  $0.3 \times V_{DDOSC3}$ . The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of  $0.4 \times V_{DDOSC3}$  is necessary.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

### 5.2.5 Temperature Sensor

**Table 31 DTS Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	$t_M$ CC	–	–	100	μs	
Temperature sensor range	$T_{SR}$ SR	-40	–	150	°C	
Sensor Accuracy (calibrated)	$T_{TSA}$ CC	-6	–	6	°C	
Start-up time after resets inactive	$t_{TSST}$ SR	–	–	20	μs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(1)

$$T_j = \frac{DTSSTAT_{RESULT} - 596}{2,03}$$

### 5.2.6 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following two tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

$V_{DD}=1.365\text{ V}$ ,  $V_{DDP}=3.47\text{ V}$ ,  $V_{DDM}=5.1\text{ V}$ ,  $f_{LMB}=180 / 160\text{ MHz} / 133\text{ MHz}$ ,  $T_J=150\text{ °C}$

The realistic power pattern defines the following conditions:

- $T_J=150\text{ °C}$
- $f_{LMB} = f_{PCP} = f_{CPU} = 180 / 160\text{ MHz} / 133\text{ MHz}$
- $f_{FPI} = 90\text{ MHz} / 80\text{ MHz} / 66.5\text{ MHz}$
- $V_{DD} = V_{DDOSC} = V_{DDAF} = 1.326\text{ V}$
- $V_{DDP} = V_{DDOSC3} = V_{DDFL3} = V_{DDMF} = 3.366\text{ V}$
- $V_{DDM} = 5.1\text{ V}$

The max power pattern defines the following conditions:

- $T_J=150\text{ °C}$
- $f_{LMB} = f_{PCP} = f_{CPU} = 180 / 160\text{ MHz} / 133\text{ MHz}$
- $f_{FPI} = 90\text{ MHz} / 80\text{ MHz} / 66.5\text{ MHz}$
- $V_{DD} = V_{DDOSC} = V_{DDAF} = 1.365\text{ V} / 1.43\text{ V} / 1.365\text{ V}$
- $V_{DDP} = V_{DDOSC3} = V_{DDFL3} = V_{DDMF} = 3.47\text{ V} / 3.63\text{ V} / 3.47\text{ V}$
- $V_{DDM} = 5.5\text{ V}$

**Electrical Parameters DC Parameters**
**Table 32 Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Core active mode supply current <sup>1)2)</sup>	$I_{DD\ CC}$	–	–	486 <sup>3)</sup>	mA	power pattern= max ; SAK-TC1782N-256F133HR SAK-TC1782N-256F133HL
		–	–	550 <sup>3)</sup>	mA	power pattern= max ; SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N-320F180HL
		–	–	550 <sup>3)</sup>	mA	power pattern= max ; SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL SAK-TC1782N-320F160HR SAK-TC1782N-320F160HL
		–	–	370 <sup>4)</sup>	mA	power pattern= realistic ; SAK-TC1782N-256F133HR SAK-TC1782N- 256F133HL; $V_{DD}=1.326\ V$
		–	–	398 <sup>4)</sup>	mA	power pattern= realistic ; SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N- 320F180HL; $V_{DD}=1.326\ V$
		–	–	386 <sup>4)</sup>	mA	power pattern= realistic ; SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL SAK-TC1782N-320F160HR SAK-TC1782N- 320F160HL; $V_{DD}=1.326\ V$
$I_{DD}$ current at PORST Low	$I_{DD\_PORS\ T\ CC}$	–	–	300	mA	
		–	–	291	mA	$V_{DD}=1.326\ V$
		–	–	314	mA	$V_{DD}=1.43\ V$
Analog core supply current	$I_{DDAF\ CC}$	–	–	23	mA	

## Electrical Parameters DC Parameters

Table 32 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator core supply current	$I_{DDOSC}$ CC	–	–	4	mA	
$I_{DDP}$ current at PORST Low	$I_{DDP\_PORST}$ CC	–	–	2.5	mA	
$I_{DDP}$ current no pad activity, LVDS off <sup>5)</sup>	$I_{DDP}$ CC	–	–	$I_{DDP\_PORST}^{+12}$	mA	including flash read current
		–	–	$I_{DDP\_PORST}^{+27}$	mA	including flash programming current <sup>6)</sup>
		–	–	$I_{DDP\_PORST}^{+20}^{7)}$	mA	including flash erase current <sup>6)</sup>
Flash memory current <sup>5)</sup>	$I_{DDFL3}$ CC	–	–	56	mA	flash read current
		–	–	21	mA	flash programming current <sup>6)</sup>
		–	–	56	mA	flash erase current <sup>6)</sup>
Oscillator power supply current, 3.3V	$I_{DDOSC3}$ CC	–	–	15	mA	
FADC analog supply current, 3.3V	$I_{DDMF}$ CC	–	–	15	mA	
Current Consumption of LVDS Pad Pairs	$I_{LVDS}$ CC	–	–	12	mA	for all LVDS pads in total
ADC 5V power supply current	$I_{DDM}$ CC	–	–	2	mA	



**Electrical Parameters DC Parameters**
**Table 32 Power Supply Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum power dissipation	PD CC	–	–	1143	mW	power pattern= max ; SAK-TC1782N-256F133HR SAK-TC1782N-256F133HL
		–	–	1231	mW	power pattern= max ; SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N-320F180HL
		–	–	1231	mW	power pattern= max ; SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL SAK-TC1782N-320F160HR SAK-TC1782N-320F160HL
		–	–	957	mW	power pattern= realistic ; SAK-TC1782N-256F133HR SAK-TC1782N-256F133HL; $V_{DD}=1.326\text{ V}$
		–	–	994	mW	power pattern= realistic ; SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N-320F180HL; $V_{DD}=1.326\text{ V}$
		–	–	979	mW	power pattern= realistic ; SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL SAK-TC1782N-320F160HR SAK-TC1782N-320F160HL; $V_{DD}=1.326\text{ V}$

- 1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
- 2) This current includes the E-Ray module power consumption, including the PCP operation component.
- 3) The  $I_{DD}$  decreases typically by 68mA if the  $f_{CPU}$  decreases by 50MHz, at constant  $T_J$
- 4) The  $I_{DD}$  decreases typically by 30mA if the  $f_{CPU}$  decreases by 50MHz, at constant  $T_J$
- 5) For operations including the D-Flash the required currents are always lower than the currents for non D-Flash operation.
- 6) Relevant for the power supply dimensioning, not for thermal considerations.

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**Electrical Parameters DC Parameters**

- 7) In case of erase of Program Flash PF, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.

**5.2.6.1 Calculating the 1.3 V Current Consumption**

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature  $T_J$  and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(2)

$$I_0 = 2,20897 \left[ \frac{\text{mA}}{\text{C}} \right] \times e^{0,02696 \times T_J[\text{C}]}$$

(3)

$$I_0 = 10,68 \left[ \frac{\text{mA}}{\text{C}} \right] \times e^{0,02203 \times T_J[\text{C}]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for  $V_{DD} = 1.326 \text{ V}$ .

For the dynamic current consumption using the application pattern and  $f_{LMB} = 2 * f_{FPI}$  the function 4 applies:

(4)

$$I_{Dym} = 0,6 \left[ \frac{\text{mA}}{\text{MHz}} \right] \times f_{CPU}[\text{MHz}]$$

and this finally results in

(5)

$$I_{DD} = I_0 + I_{DYM}$$

### 5.3 AC Parameters

All AC parameters are defined with maximum driver strength unless otherwise noted.

#### 5.3.1 Testing Waveforms

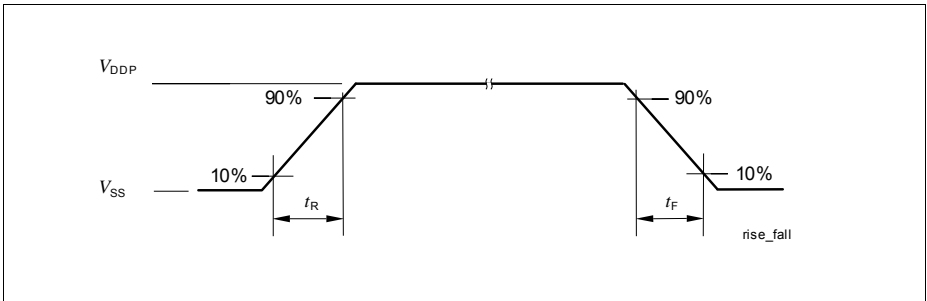


Figure 10 Rise/Fall Time Parameters

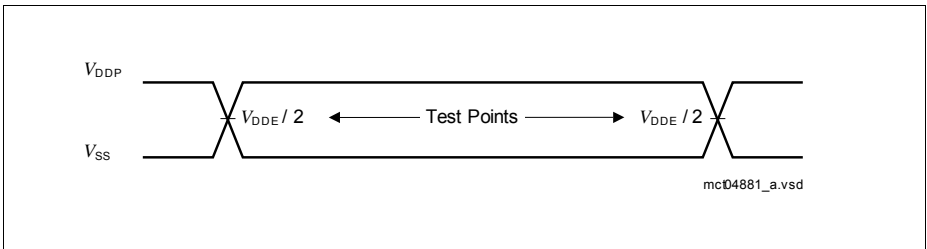


Figure 11 Testing Waveform, Output Delay

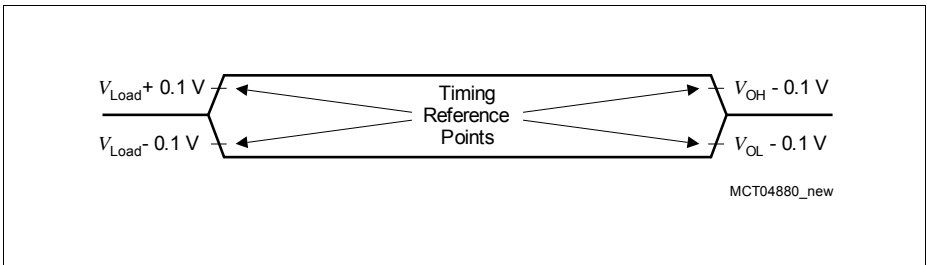
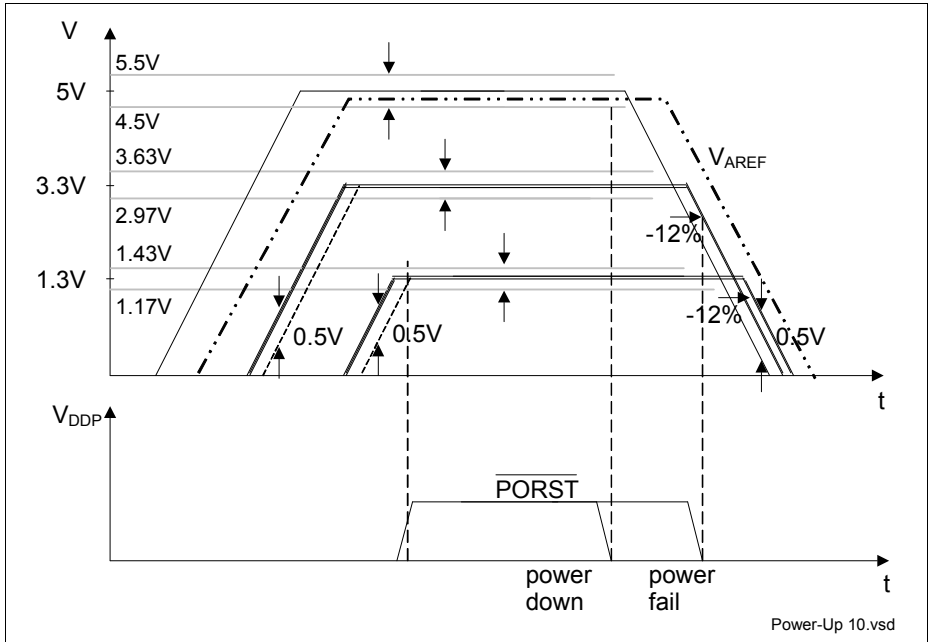
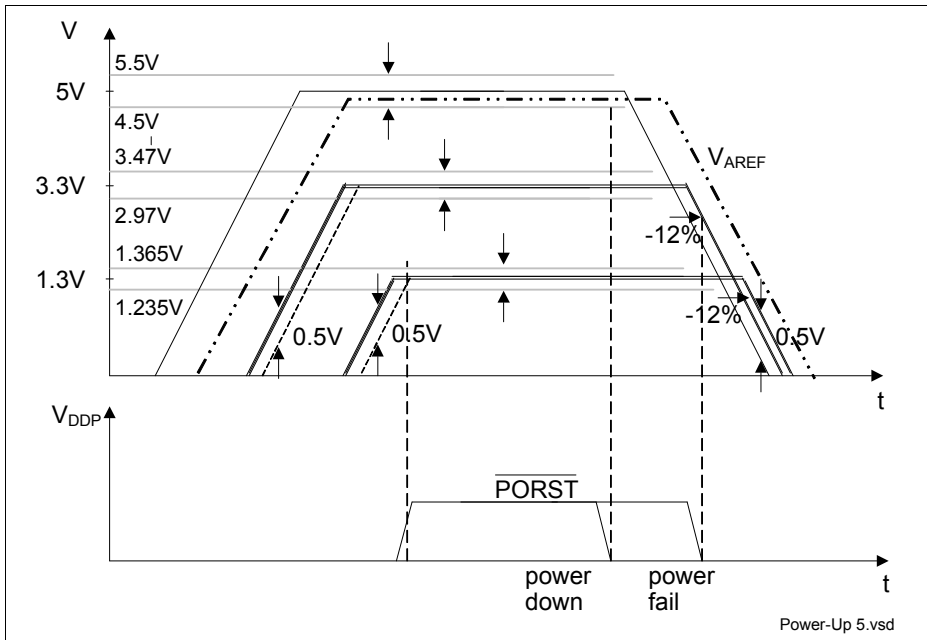


Figure 12 Testing Waveform, Output High Impedance

### 5.3.2 Power Sequencing



**Figure 13** 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence for 10% Operating Range



**Figure 14 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence for 5% Operating Range**

The following list of rules applies to the power-up/down sequence:

- All ground pins  $V_{SS}$  must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk, each power supply must be higher than any lower\_power\_supply - 0.5 V, or:  
 $V_{DD5} > V_{DD3.3} - 0.5 \text{ V}$ ;  $V_{DD5} > V_{DD1.3} - 0.5 \text{ V}$ ;  $V_{DD3.3} > V_{DD1.3} - 0.5 \text{ V}$ , see [Figure 14](#).
  - The latch-up risk is minimized if the I/O currents are limited to:
    - 20 mA for one pin group
    - AND 100 mA for the completed device I/Os
    - AND additionally before power-up / after power-down:
      - 1 mA for one pin in inactive mode (0 V on all power supplies)
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names (for example  $V_{DDP}$ ,  $V_{DDFL3}$  ...), that are internally connected via diodes, must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all  $V_{DDP}$ ), are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

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**Electrical Parameters AC Parameters**

1. The  $\overline{\text{PORST}}$  signal may be deactivated after all  $V_{\text{DD5}}$ ,  $V_{\text{DD3.3}}$ ,  $V_{\text{DD1.3}}$ , and  $V_{\text{AREF}}$  power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
2. At normal power down the  $\overline{\text{PORST}}$  signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
3. At power fail the  $\overline{\text{PORST}}$  signal must be activated at latest when any 3.3 V or 1.3 V power supply voltage falls 12% below the nominal level. If, under these conditions, the  $\overline{\text{PORST}}$  is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the  $\overline{\text{PORST}}$  signal should be activated as close as possible to the normal operating voltage range.
4. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
5. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
6. Additionally, regarding the ADC reference voltage  $V_{\text{AREF}}$ :
  - $V_{\text{AREF}}$  must power-up at the same time or later then  $V_{\text{DDM}}$ , and
  - $V_{\text{AREF}}$  must power-down either earlier or at latest to satisfy the condition  $V_{\text{AREF}} < V_{\text{DDM}} + 0.5 \text{ V}$ . This is required in order to prevent discharge of  $V_{\text{AREF}}$  filter capacitance through the ESD diodes through the  $V_{\text{DDM}}$  power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

## 5.3.3 Power, Pad and Reset Timing

Table 33 Reset Timings Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time <sup>1)2)</sup>	$t_B$ CC	150	–	810	$\mu\text{s}$	SAK-TC1782N-256F133HR SAK-TC1782N-256F133HL
		150	–	665	$\mu\text{s}$	SAK-TC1782F320F180HR SAK-TC1782F320F180HL SAK-TC1782N-320F180HR SAK-TC1782N-320F180HL
		150	–	740	$\mu\text{s}$	SAK-TC1782F-320F160HR SAK-TC1782F-320F160HL / S SAK-TC1782N-320F160HR SAK-TC1782N-320F160HL
Power on Reset Boot Time <sup>3)4)</sup>	$t_{BP}$ CC	–	–	2.5	ms	
HWCFG pins hold time from ESR0 rising edge	$t_{HDH}$ SR	16 / $f_{FPI}$	–	–	ns	
HWCFG pins setup time to ESR0 rising edge	$t_{HDS}$ CC	0	–	–	ns	
Ports inactive after ESR0 reset active	$t_{PI}$ CC	–	–	8 / $f_{FPI}$	ns	
Ports inactive after PORST reset active <sup>5)</sup>	$t_{PIP}$ CC	–	–	150	ns	

## Electrical Parameters AC Parameters

**Table 33** Reset Timings Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Minimum PORST active time after power supplies are stable at operating levels	$t_{POA}$ CC	10	–	–	ms	
$\overline{TESTMODE}$ / $\overline{TRST}$ hold time from PORST rising edge	$t_{POH}$ SR	100	–	–	ns	
PORST rise time	$t_{POR}$ SR	–	–	50	ms	
$\overline{TESTMODE}$ / $\overline{TRST}$ setup time to PORST rising edge	$t_{POS}$ SR	0	–	–	ns	

- 1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.
- 2) The given time includes the time of the internal reset extension for a configured value of SCU\_RSTCNTCON.RELSA = 0x05BE.
- 3) The duration of the boot time is defined between the rising edge of the  $\overline{PORST}$  and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.
- 4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.
- 5) This parameter includes the delay of the analog spike filter in the  $\overline{PORST}$  pad.



Electrical Parameters AC Parameters

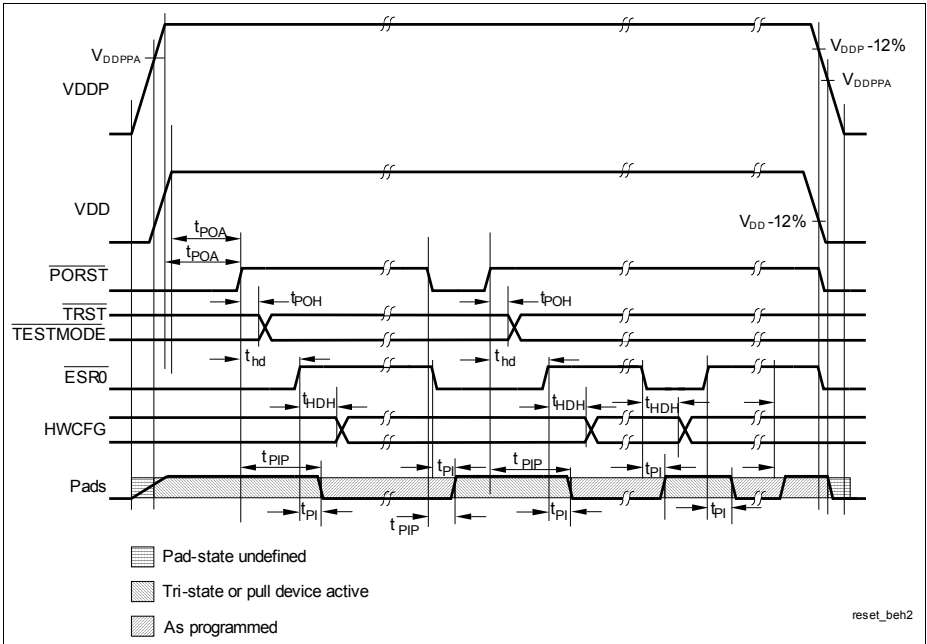


Figure 15 Power, Pad and Reset Timing

### 5.3.4 Phase Locked Loop (PLL)

**Table 34 PLL\_SysClk Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	$D_p$ CC	-7	–	7	ns	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	$f_{REF}$ CC	8	–	16	MHz	
VCO frequency range	$f_{VCO}$ CC	400	–	720	MHz	
PLL lock-in time	$t_L$ CC	14	–	200	$\mu$ s	$N > 32$
		14	–	400	$\mu$ s	$N \leq 32$

#### Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock  $f_{VCO}$  (and with it the LMB-Bus clock  $f_{LMB}$ ) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter  $D_m$  in [ns] dependent on the  $K2$ -factor, the LMB clock frequency  $f_{LMB}$  in [MHz], and the number  $m$  of consecutive  $f_{LMB}$  clock periods.

$$\text{for } (K2 \leq 100) \quad \text{and} \quad (m \leq (f_{LMB}[\text{MHz}]) / 2)$$

$$|D_m[\text{ns}]| = \left( \frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \right) \times \left( \frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[\text{MHz}] - 1} + 0,01 \times K2 \right) \quad (6)$$

$$\text{else} \quad |D_m[\text{ns}]| = \frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \quad (7)$$

With rising number  $m$  of clock cycles the maximum jitter increases linearly up to a value of  $m$  that is defined by the  $K2$ -factor of the PLL. Beyond this value of  $m$  the maximum

## Electrical Parameters AC Parameters

accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency  $f_{LMB}$  results in a higher absolute maximum jitter value.

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed  $C_L = 20$  pF with the maximum driver and sharp edge.*

*Note: The maximum peak-to-peak noise on the pad supply voltage, measured between  $V_{DDOSC3}$  and  $V_{SSOSC}$ , is limited to a peak-to-peak voltage of  $V_{PP} = 100$  mV for noise frequencies below 300 KHz and  $V_{PP} = 40$  mV for noise frequencies above 300 KHz.*

*The maximum peak-to-peak noise on the pad supply voltage, measured between  $V_{DDOSC}$  and  $V_{SSOSC}$ , is limited to a peak-to-peak voltage of  $V_{PP} = 100$  mV for noise frequencies below 300 KHz and  $V_{PP} = 40$  mV for noise frequencies above 300 KHz.*

*These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

### Oscillator Watchdog (OSC\_WDT)

The expected input frequency is selected via the bit field SCU\_OSCCON.OSCVAL. The OSC\_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is  $f_{OSCREF}$  which is derived for  $f_{OSC}$ .

(8)

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1}$$

The divider value SCU\_OSCCON.OSCVAL has to be selected in a way that  $f_{OSCREF}$  is 2.5 MHz.

*Note:  $f_{OSCREF}$  has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.*

The monitored frequency is too low if it is below 1.25 MHz and too high if it is above 7.5 MHz. This leads to the following two conditions:

- Too low:  $f_{OSC} < 1.25 \text{ MHz} \times (\text{SCU\_OSCCON.OSCVAL} + 1)$
- Too high:  $f_{OSC} > 7.5 \text{ MHz} \times (\text{SCU\_OSCCON.OSCVAL} + 1)$

*Note: The accuracy is 30% for these boundaries.*

### 5.3.5 ERAY Phase Locked Loop (ERAY\_PLL)

**Table 35 PLL\_ERAY Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at SYSCLK pin	$D_{PP}$ CC	-0.8	–	0.8	ns	
Accumulated_Jitter	$D_p$ CC	-0.5	–	0.5	ns	
PLL Base Frequency of the ERAY PLL	$f_{PLLBASE\_ERAY}$ CC	50	250	360	MHz	
VCO input frequency of the ERAY PLL	$f_{REF}$ CC	20	–	40	MHz	
VCO frequency range of the ERAY PLL	$f_{VCO\_ERA}$ CC	450	–	500	MHz	
PLL lock-in time	$t_L$ CC	5.6	–	200	μs	

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed  $C_L = 20$  pF with the maximum driver and sharp edge.*

*Note: The maximum peak-to-peak noise on the pad supply voltage, measured between  $V_{DDOSC3}$  and  $V_{SSOSC}$ , is limited to a peak-to-peak voltage of  $V_{PP} = 100$  mV for noise frequencies below 300 KHz and  $V_{PP} = 40$  mV for noise frequencies above 300 KHz.*

*These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.*

### 5.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 36 JTAG Interface Timing Parameters  
(Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	$t_1$ SR	25	–	–	ns	–
TCK high time	$t_2$ SR	10	–	–	ns	–
TCK low time	$t_3$ SR	10	–	–	ns	–
TCK clock rise time	$t_4$ SR	–	–	4	ns	–
TCK clock fall time	$t_5$ SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	$t_6$ SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	$t_7$ SR	6	–	–	ns	–
TDO valid after TCK falling edge <sup>1)</sup> (propagation delay)	$t_8$ CC	–	–	13	ns	$C_L = 50$ pF
	$t_8$ CC	3	–	–	ns	$C_L = 20$ pF
TDO hold after TCK falling edge <sup>1)</sup>	$t_{18}$ CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge <sup>1)2)</sup>	$t_9$ CC	–	–	14	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge <sup>1)</sup>	$t_{10}$ CC	–	–	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

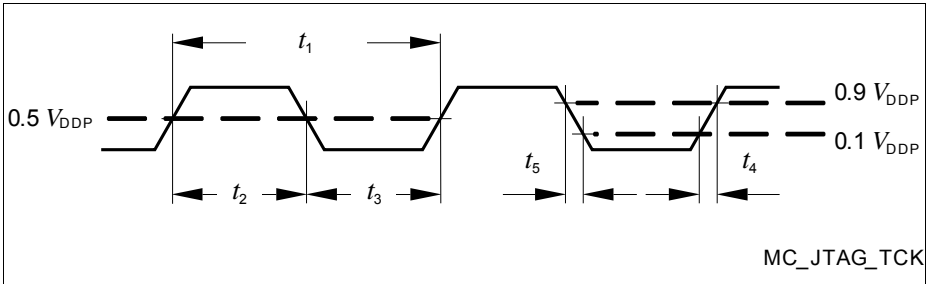


Figure 16 Test Clock Timing (TCK)

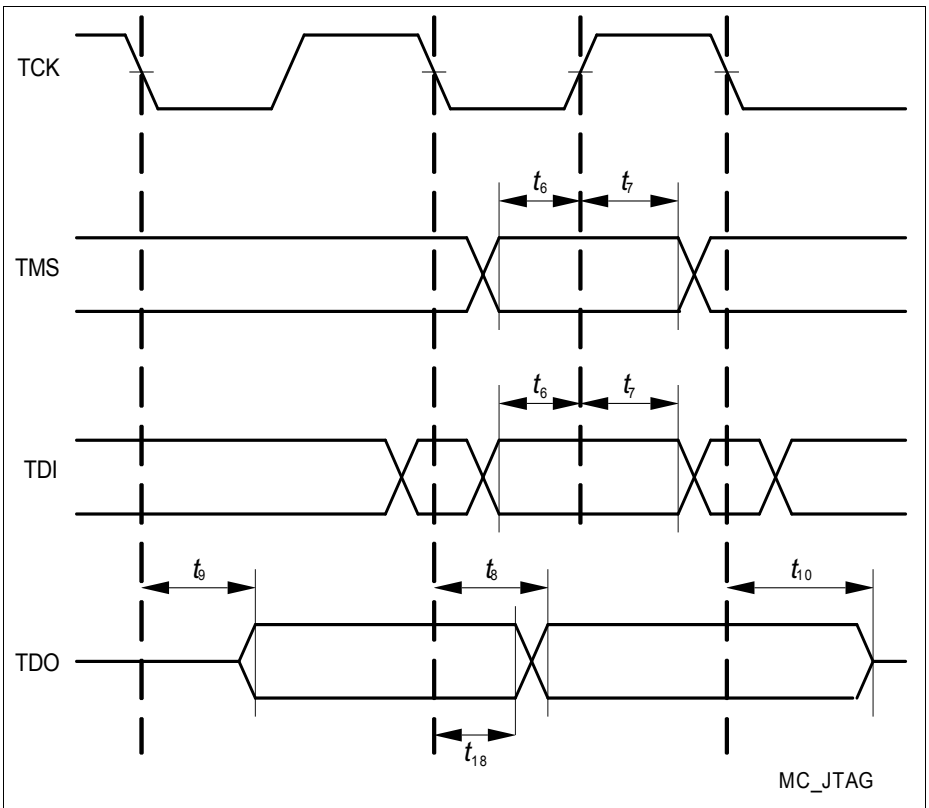


Figure 17 JTAG Timing

### 5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

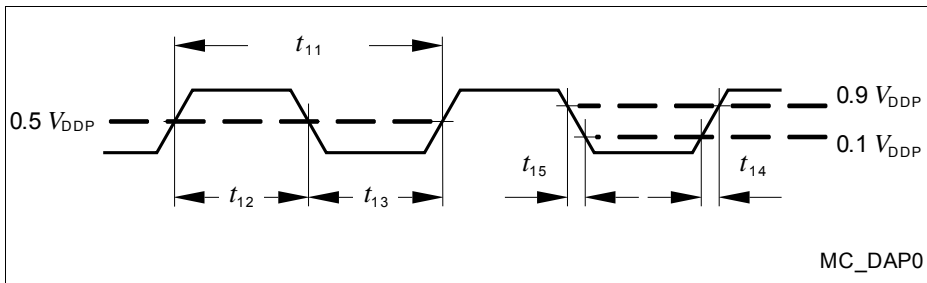
*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 37 DAP Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period <sup>1)</sup>	$t_{TCK}$ SR	12.5	–	–	ns	
DAP0 high time	$t_{12}$ SR	4	–	–	ns	
DAP0 low time <sup>1)</sup>	$t_{13}$ SR	4	–	–	ns	
DAP0 clock rise time	$t_{14}$ SR	–	–	2	ns	
DAP0 clock fall time	$t_{15}$ SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	$t_{16}$ SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	$t_{17}$ SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period <sup>2)</sup>	$t_{19}$ CC	8	–	–	ns	$C_L = 20$ pF; $f = 80$ MHz
		10	–	–	ns	$C_L = 50$ pF; $f = 40$ MHz

1) See the DAP chapter for clock rate restrictions in the Active:IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.



**Figure 18 Test Clock Timing (DAP0)**

Electrical Parameters AC Parameters

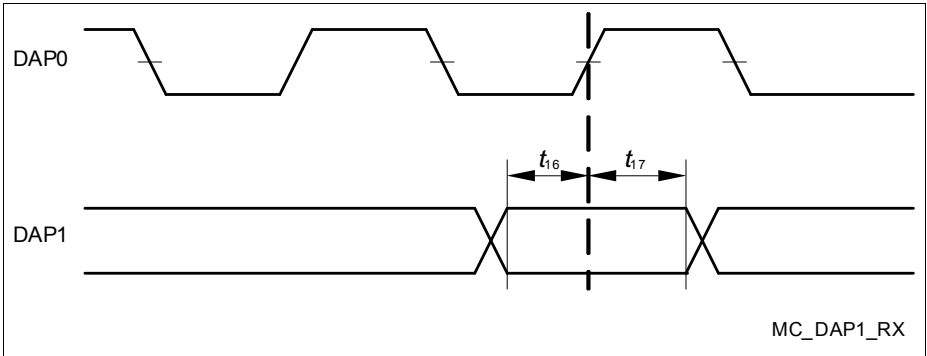


Figure 19 DAP Timing Host to Device

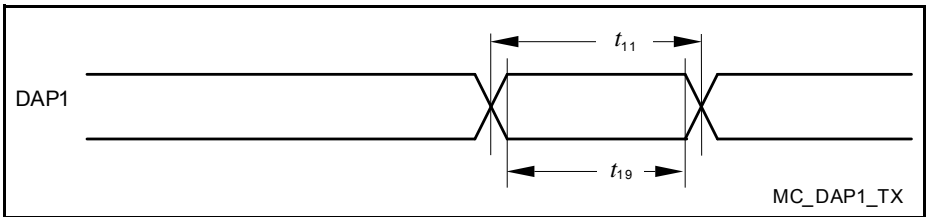


Figure 20 DAP Timing Device to Host



### 5.3.8 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

#### 5.3.8.1 Micro Link Interface (MLI) Timing

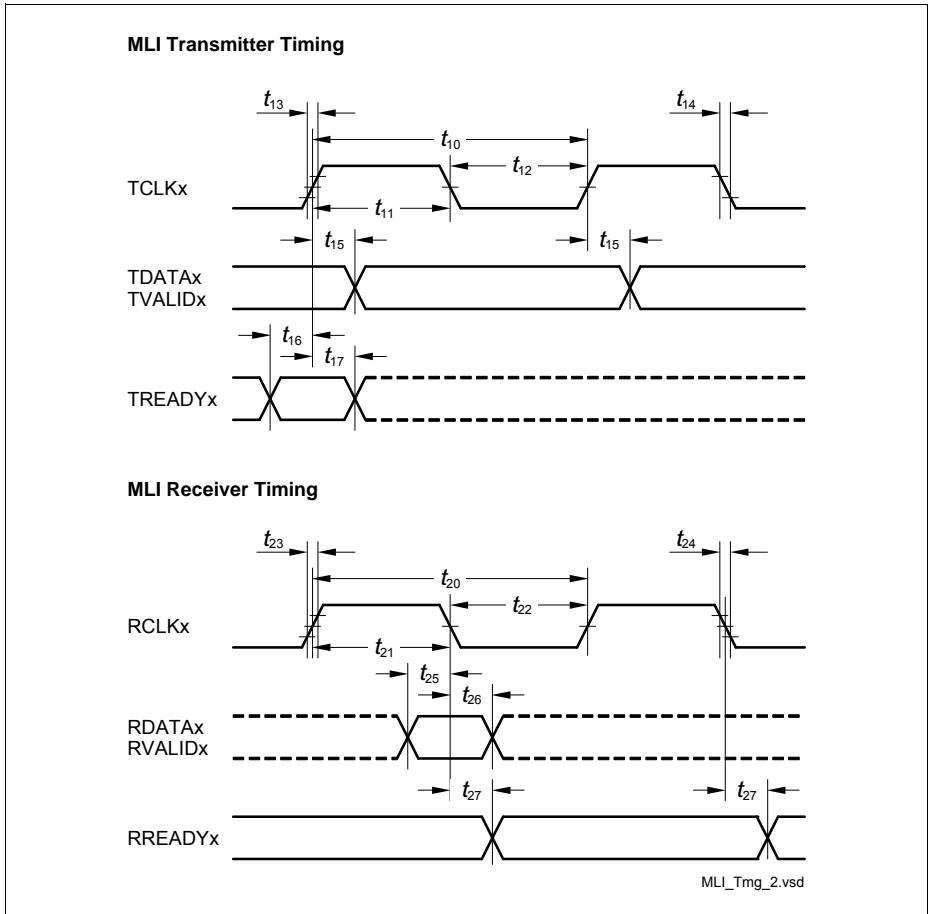


Figure 21 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

**Electrical Parameters AC Parameters**

The MLI parameters are valid for  $C_L = 50$  pF and for strong driver medium edge.

**Table 38 MLI Receiver**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	$t_{20}$ SR	$1 / f_{FPI}$	–	–	ns	
RCLK high time <sup>1)2)</sup>	$t_{21}$ SR	–	0.5 x $t_{20}$	–	ns	
RCLK low time <sup>1)2)</sup>	$t_{22}$ SR	–	0.5 x $t_{20}$	–	ns	
RCLK rise time <sup>3)</sup>	$t_{23}$ SR	–	–	4	ns	
RCLK fall time <sup>3)</sup>	$t_{24}$ SR	–	–	4	ns	
RDATA/RVALID setup time before RCLK falling edge	$t_{25}$ SR	4.2	–	–	ns	
RDATA/RVALID hold time after RCLK falling edge	$t_{26}$ CC	2.2	–	–	ns	
RREADY output delay time	$t_{27}$ CC	0	–	16	ns	

1) The following formula is valid:  $t_{21} + t_{22} = t_{20}$ .

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for  $f_{SYS} = 90$  MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

**Table 39 MLI Transmitter**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	$t_{10}$ CC	$2 \times 1 / f_{FPI}$	–	–	ns	
TCLK high time <sup>1)2)</sup>	$t_{11}$ CC	0.45 x $t_{10}$	0.5 x $t_{10}$	0.55 x $t_{10}$	ns	
TCLK low time <sup>1)2)</sup>	$t_{12}$ CC	0.45 x $t_{10}$	0.5 x $t_{10}$	0.55 x $t_{10}$	ns	
TCLK rise time	$t_{13}$ CC	–	–	0.3 x $t_{10}$ <sup>3)</sup>	ns	

## Electrical Parameters AC Parameters

**Table 39 MLI Transmitter (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK fall time	$t_{14}$ CC	–	–	$0.3 \times t_{10}^{3)}$	ns	
TDATA/TVALID output delay time	$t_{15}$ CC	-3	–	4.4	ns	
TREADY setup time before TCLK rising edge	$t_{16}$ SR	18	–	–	ns	
TREADY hold time after TCLK rising edge	$t_{17}$ SR	-2	–	–	ns	

1) The following formula is valid:  $t_{11} + t_{12} = t_{10}$ .

2) The min./max. TCLK low/high times  $t_{11}/t_{12}$  include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to  $t_{11} / t_{12}$ .

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

### 5.3.8.2 Micro Second Channel (MSC) Interface Timing

The MSC parameters are valid for  $C_L = 50$  pF.

**Table 40 MSC Parameters**

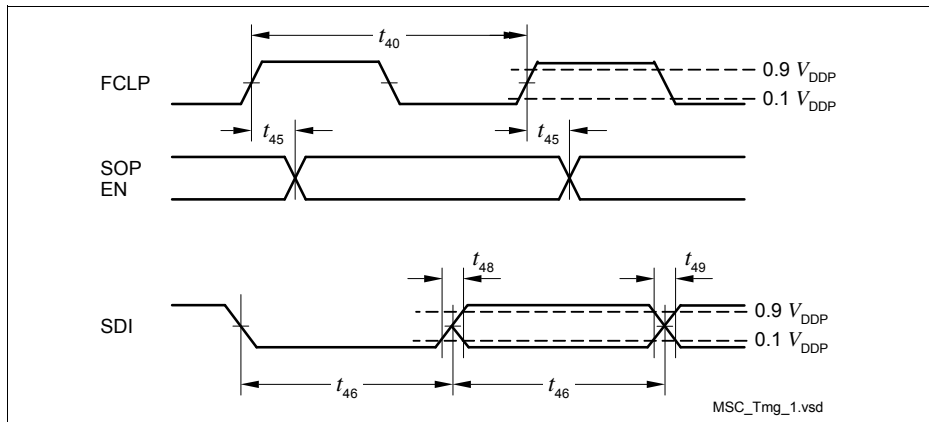
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period <sup>1)2)</sup>	$t_{40}$ CC	$2 \times T_{MSC}^{3)}$	–	–	ns	
SOP <sup>4)</sup> /ENx outputs delay from FCLP <sup>4)</sup> rising edge	$t_{45}$ CC	-2	–	5	ns	ENx with strong driver and sharp (minus) edge
		-2	–	10	ns	ENx with strong driver and medium (minus) edge
		0	–	21	ns	ENx with strong driver and soft edge

## Electrical Parameters AC Parameters

**Table 40 MSC Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	$t_{46}$ CC	$8 \times T_{MSC}$	—	—	ns	
SDI rise time <sup>5)</sup>	$t_{48}$ SR	—	—	200	ns	
SDI fall time <sup>5)</sup>	$t_{49}$ SR	—	—	200	ns	

- 1) FCLP signal rise/fall times are only defined by the pad rise/fall times.
- 2) FCLP signal high and low can be minimum  $1 \times T_{MSC}$
- 3)  $T_{MSC} = T_{SYS} = 1 / f_{SYS}$ .
- 4) SOP / FCLP either propagated by LVDS or by CMOS strong driver and non soft edge.
- 5) When using slow and asymmetrical edges, like in case of open drain upstream connection, the application must take care that the bit is long enough (the baud rate is low enough) so that under worst case conditions the three sampling points in the middle of the bit are not violated.


**Figure 22 MSC Interface Timing**

*Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.*

### 5.3.8.3 SSC Master/Slave Mode Timing

The SSC parameters are valid for  $C_L = 50$  pF and for strong driver medium edge.

**Table 41 SSC Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period <sup>1)2)3)</sup>	$t_{50}$ CC	$2 \times 1 / f_{FPI}$	–	–	ns	
MTRSR/SLSOx delay from SCLK rising edge	$t_{51}$ CC	0	–	8	ns	
MRST setup to SCLK falling edge <sup>3)</sup>	$t_{52}$ SR	16.5	–	–	ns	
MRST hold from SCLK falling edge <sup>3)</sup>	$t_{53}$ SR	0	–	–	ns	
SCLK input clock period <sup>1)3)</sup>	$t_{54}$ SR	$4 \times 1 / f_{FPI}$	–	–	ns	
SCLK input clock duty cycle	$t_{55}$ - $t_{54}$ SR	45	–	55	%	
MTRSR setup to SCLK latching edge <sup>3)4)</sup>	$t_{56}$ CC	$1 / f_{FPI}$	–	–	ns	
MTRSR hold from SCLK latching edge	$t_{57}$ CC	$1 / f_{FPI} + 5$	–	–	ns	
SLSI setup to first SCLK latching edge	$t_{58}$ CC	$1 / f_{FPI} + 5$	–	–	ns	
SLSI hold from last SCLK latching edge <sup>5)</sup>	$t_{59}$ CC	7	–	–	ns	
MRST delay from SCLK shift edge	$t_{60}$ CC	0	–	16.5	ns	
SLSI to valid data on MRST	$t_{61}$ CC	–	–	16.5	ns	

1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum  $1 \times TSSC$ .

3)  $TSSC_{min} = T_{SYS} = 1/f_{SYS}$ .

4) Fractional divider switched off, SSC internal baud rate generation used.

5) For CON.PH=1 slave select must not be removed before the following shifting edge. This means, that whatever is configured (shifting / latching first), SLSI must not be de-activated before the last trailing edge from the pair of shifting / latching edges.

Electrical Parameters AC Parameters

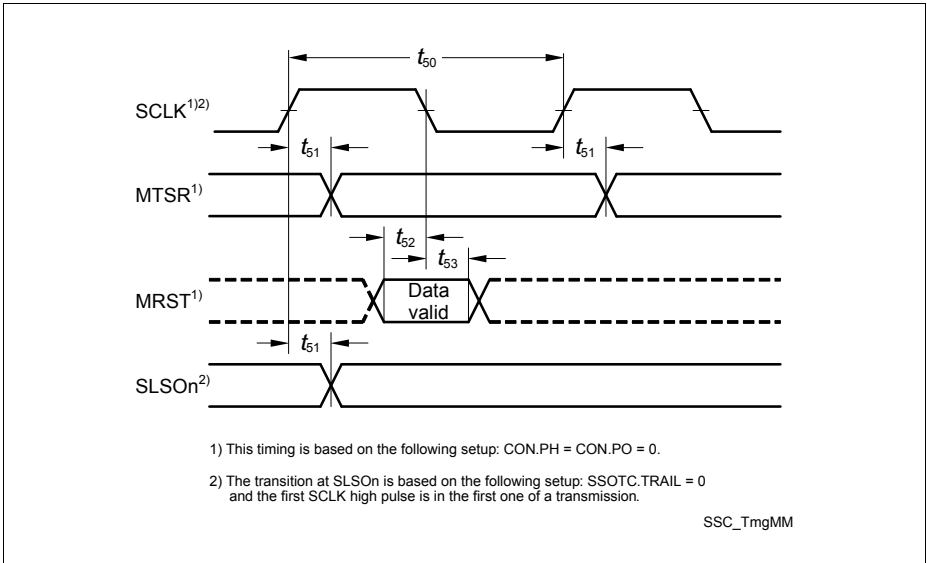


Figure 23 SSC Master Mode Timing

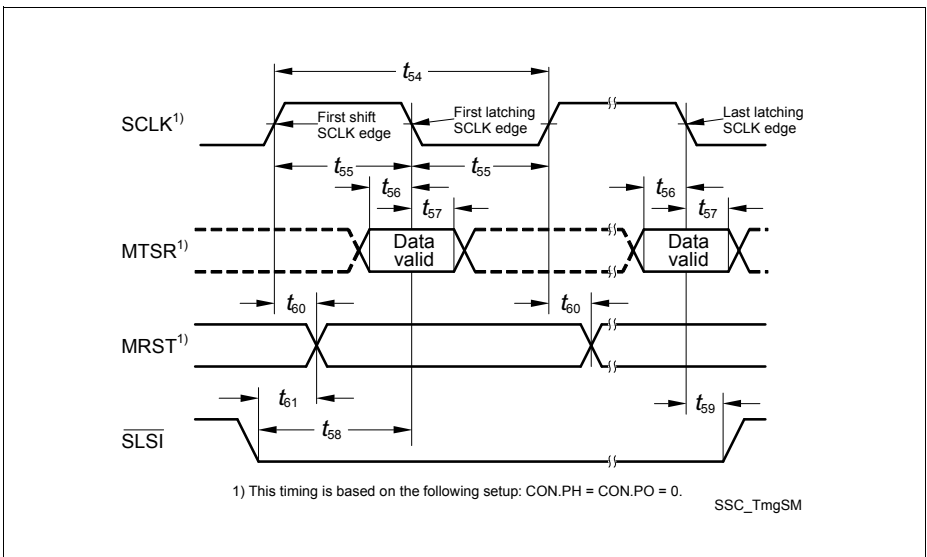


Figure 24 SSC Slave Mode Timing

**5.3.8.4 ERAY Interface Timing**

The timings of this section are valid for the strong driver and either sharp edge or medium edge settings of the output drivers with  $C_L = 25$  pF.

The ERAY interface is only available for the SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL / SAK-TC1782F-320F160HR / SAK-TC1782F-320F160HL / SAK-TC1782F-320F133HR / SAK-TC1782F-320F133HL.

**Table 42 ERAY Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Time span from last BSS to FES without the influence of quartz tolerancies (d10Bit_TX) <sup>1)</sup>	$t_{60}$ CC	997.75	–	1002.25	ns	
TxD data valid from fsample flip flop txd_reg TxDA, TxDB (dTxAsym) <sup>2)3)</sup>	$t_{61}$ - $t_{62}$ CC	–	–	1.5	ns	Asymmetrical delay of rising and falling edge (TxDA, TxDB)
Time span between last BSS and FES without influence of quartz tolerancies (d10Bit_RX) <sup>1)4)5)</sup>	$t_{63}$ SR	966	–	1046.1	ns	
RxD capture by fsample (RxDA/RxDB sampling flip-flop) (dRxAsym) <sup>5)</sup>	$t_{64}$ - $t_{65}$ CC	–	–	3.0	ns	Asymmetrical delay of rising and falling edge (RxDA, RxDB)
TxD data delay from sampling flip-flop	$dTxdly$ CC	–	–	10.0	ns	Px_PDR.PDy = 000 <sub>B</sub>
		–	–	15.0	ns	Px_PDR.PDy = 001 <sub>B</sub>
RxD capture delay by sampling flip-flop	$dRxdly$ CC	–	–	10.0	ns	

1) This includes the PLL\_ERAY accumulated jitter.

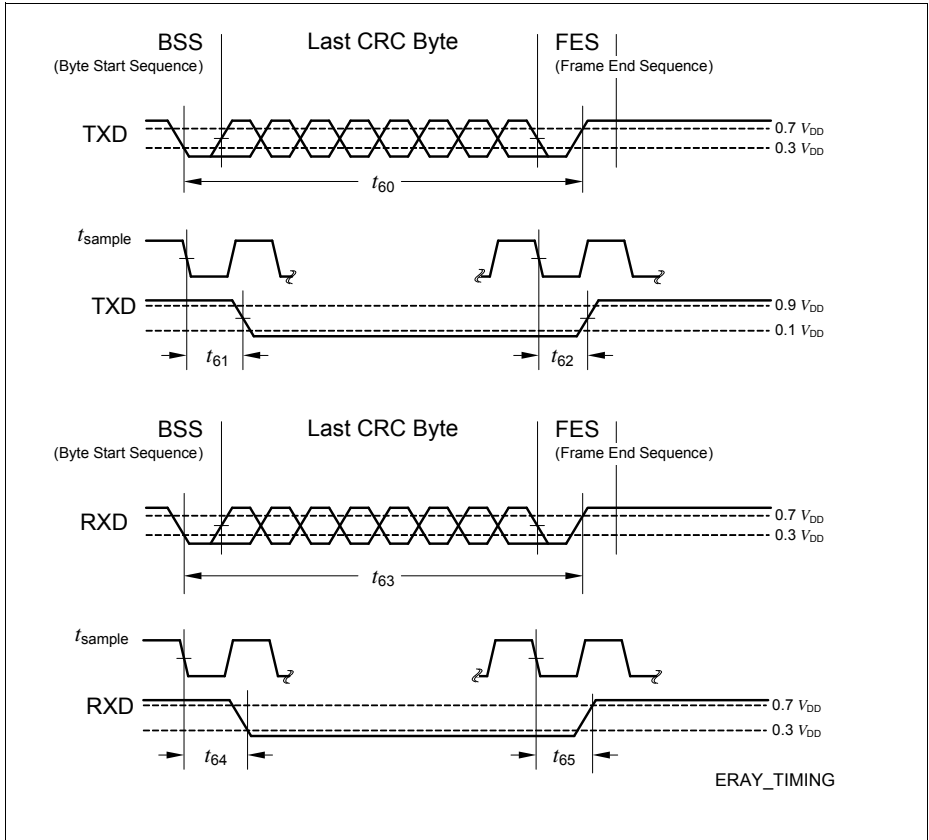
2) Refers to delays caused by the asymmetries of the output drivers of the digital logic and the GPIO pad drivers. Quartz tolerance and PLL\_ERAY accumulated jitter are not included.

3) E-Ray TxD output drivers have an asymmetry of rising and falling edges of  $|t_{FA2} - t_{RA2}| \leq 1$  ns.

4) Limits of 966ns and 1046.1ns correspond to (30%, 70%) \*  $V_{DDP}$  FlexRay standard input thresholds. For input thresholds of this product, a correction of - 0.5 ns and +0.1 ns has to be applied.

**Electrical Parameters AC Parameters**

- 5) Valid for output slopes of the bus driver of  $dRxSlope \leq 5ns$ ,  $20\% * V_{DDP}$  to  $80\% * V_{DDP}$ , according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality:  $-1.6ns \leq t_{FA2} - t_{RA2} \leq 1.3ns$ .



**Figure 25 ERAY Timing**



## 5.4 Package and Reliability

### 5.4.1 Package Parameters

**Table 43 Thermal Characteristics of the Package**

Device	Package	$R_{\Theta JCT}$ <sup>1)</sup>	$R_{\Theta JCB}$ <sup>1)</sup>	$R_{\Theta JLead}$	Unit	Note
TC1782	PG-LQFP-176-10 / PG-LQFP-176-20	8,1	0,3	30,9	K/W	with soldered exposed pad <sup>2)</sup>
TC1782	PG-LQFP-176-10 / PG-LQFP-176-20	8,1	12,6	30,9	K/W	with not soldered exposed pad

1) The top and bottom thermal resistances between the case and the ambient ( $R_{TCAT}$ ,  $R_{TCAB}$ ) are to be combined with the thermal resistances between the junction and the case given above ( $R_{TJCT}$ ,  $R_{TJCB}$ ), in order to calculate the total thermal resistance between the junction and the ambient ( $R_{TJA}$ ). The thermal resistances between the case and the ambient ( $R_{TCAT}$ ,  $R_{TCAB}$ ) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation:  $T_J = T_A + R_{TJA} \times P_D$ , where the  $R_{TJA}$  is the total thermal resistance between the junction and the ambient. This total junction ambient resistance  $R_{TJA}$  can be obtained from the upper four partial thermal resistances.

Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

2) It is recommended by Infineon Technologies AG to connect the exposed pad.

### 5.4.2 Package Outline

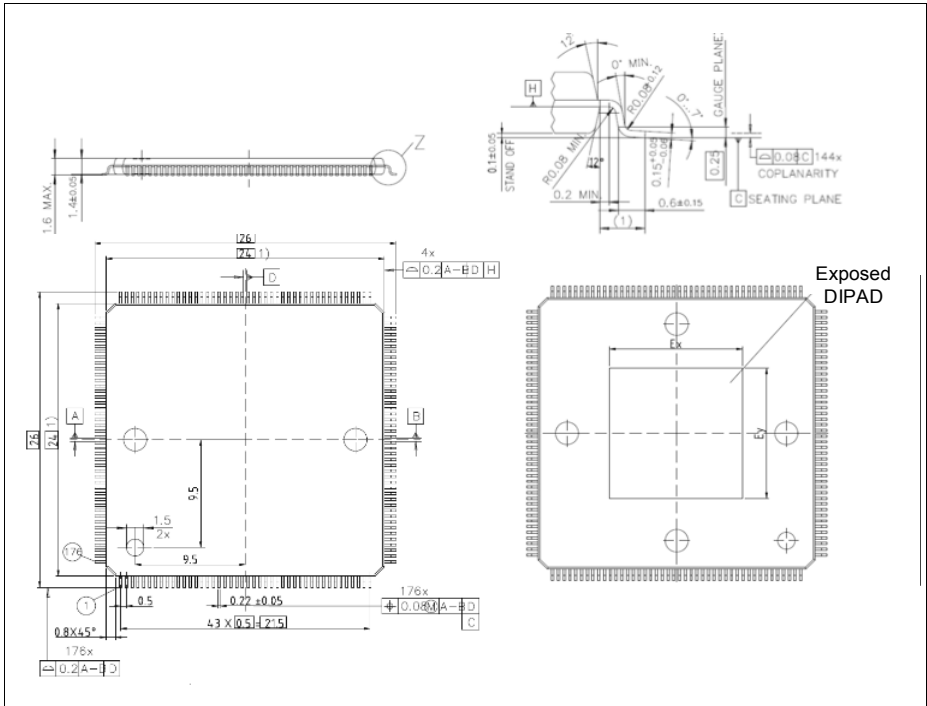


Figure 26 Package Outlines PG-LQFP-176-10 / PG-LQFP-176-20

Table 44 Exposed pad Dimensions

Ex	7.8 mm
Ey	7.8 mm

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

### 5.4.3 Flash Memory Parameters

The data retention time of the TC1782's Flash memory depends on the number of times the Flash memory has been erased and programmed.

## Electrical Parameters Package and Reliability

Table 45 FLASH32 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Sector	$t_{ERD}$ CC	–	–	3 <sup>1)</sup>	s	
Program Flash Erase Time per 256 KByte Sector	$t_{ERP}$ CC	–	–	5	s	
Program time data flash per page <sup>2)</sup>	$t_{PRD}$ CC	–	–	5.3	ms	without reprogramming
		–	–	15.9	ms	with two reprogramming cycles
Program time program flash per page <sup>3)</sup>	$t_{PRP}$ CC	–	–	5.3	ms	without reprogramming
		–	–	10.6	ms	with one reprogramming cycle
Data Flash Endurance	$N_E$ CC	60000 <sup>4)</sup>	–	–	cycle s	Min. data retention time 5 years
Erase suspend delay	$t_{FL\_ErSusp}$ CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	μs	
Program Flash Retention Time, Physical Sector <sup>5)6)</sup>	$t_{RET}$ CC	20	–	–	year s	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector <sup>5)6)</sup>	$t_{RETL}$ CC	20	–	–	year s	Max. 100 erase/program cycles
UCB Retention Time <sup>5)6)</sup>	$t_{RTU}$ CC	20	–	–	year s	Max. 4 erase/program cycles per UCB
Wake-Up time	$t_{WU}$ CC	–	–	270	μs	

**Electrical Parameters Package and Reliability**
**Table 45 FLASH32 Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DFlash wait state configuration	$WS_{DF}$ CC	$50\text{ ns} \times f_{FSI}$	–	–		
PFlash wait state configuration	$WS_{PF}$ CC	$26\text{ ns} \times f_{FSI}$	–	–		

- 1) In case of wordline oriented defects (see robust EEPROM emulation in the User's Manual) this erase time can increase by up to 100%.
- 2) In case the Program Verify feature detects weak bits, these bits will be programmed up to twice more. Each reprogramming takes additional 5 ms.
- 3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.
- 4) Only valid when a robust EEPROM emulation algorithm is used. For more details see the User's Manual.
- 5) Storage and inactive time included.
- 6) At average weighted junction temperature  $T_j = 100^\circ\text{C}$ , or the retention time at average weighted temperature of  $T_j = 110^\circ\text{C}$  is minimum 10 years, or the retention time at average weighted temperature of  $T_j = 150^\circ\text{C}$  is minimum 0.7 years.

#### 5.4.4 Quality Declarations

**Table 46 Quality Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime <sup>1)</sup>	$t_{OP}$	–	–	24000	hours	– <sup>2)</sup>
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM}$	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	$V_{HBM1}$	–	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM}$	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

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**Electrical Parameters Package and Reliability**

- 1) This lifetime refers only to the time when the device is powered on.
- 2) For worst-case temperature profile equivalent to:
  - 1200 hours at  $T_j = 125...150^{\circ}\text{C}$
  - 3600 hours at  $T_j = 110...125^{\circ}\text{C}$
  - 7200 hours at  $T_j = 100...110^{\circ}\text{C}$
  - 11000 hours at  $T_j = 25...100^{\circ}\text{C}$
  - 1000 hours at  $T_j = -40...25^{\circ}\text{C}$

## 6 History

The following changes were done between Version 0.7 and 0.8 of this document:

- Change product name from SAK-TC1782-320F180HL to SAK-TC1782-320F180HR
- Change product name from SAK-TC1782-256F133HL to SAK-TC1782-256F133HR
- Change DFLASH size from 64Kbyte to 128Kbyte in chapter 1
- Add ADC module abbreviation to table 1 Analog Input Port Function description
- Change SCU\_RTID and SCU\_CHIPID values to match the step
- Extend  $V_{DDOSC3}$  to -7.5 %
- Add parameter  $HYSAI+$
- Add parameter  $HYSAI2$
- Add parameter  $V_{ILF} / V_{IHF}$
- Add parameter  $R_{DSONF}$
- Changed typical value of  $C_{AINSW}$  from 7 to 9 pF
- Changed typical value of  $C_{AINTOT}$  from 25 to 20 pF
- Remove 3.3 V values from ADC section
- Add parameter  $f_{ADC}$
- Changed max. value of  $f_{ADCI}$  from 20 to 18 MHz
- Remove parameter  $I_{AIN7T}$  (covered by  $R_{AIN7T}$ )
- Replace parameter  $I_{AREF}$  by  $Q_{CONV}$
- Changed typical value of  $R_{AIN}$  from 700 to 900 Ohm
- Add parameter  $t_S$
- Add footnote to max value of  $TUE$
- Add parameter  $f_{FADC}$
- Add parameter  $t_C$
- Add formula for DTS temperature calculation
- Adapt current values to reduced limits of BA step
- Add clarification to parameter  $I_{LVDS}$
- Remove parameter  $R_{THJA}$  (not required)
- Add clarification to parameter  $t_{POH}$  description
- Add clarification to parameter  $t_{POS}$  description
- Add min. value to parameters  $t_L$
- Changed typical value of  $f_{PLLBASE\_ERAY}$  from 200 to 250 MHz
- Add MSC  $t_{45}$  behavior for CMOS / LVDS usage
- Add  $R_{THS}$  for non soldered exposed pad
- Add table 33
- Change DTS accuracy to 6°C of the complete temperature range
- Remove limitations of the DFLASH and PFLASH operating in extended Range operating conditions
- Change package version von PG-LQFP-176-6 to PG-LQFP-176-12

The following changes were done between Version 0.8 and 1.0 of this document:

- Change package version von PG-LQFP-176-12 to PG-LQFP-176-10

- improve description in table 2 for analog channels
- add class A1+ to type list of table 2
- add clarification that table 7 defines the conditions for all other parameters
- add note the spike filter is only available for the PORST pin
- add  $V_{il}$  to  $V_{ih}$  ratio for A1+ pad
- remove irritating Note / Test Conditions
- adapt maximum power dissipation values
- add conditions for MLI, MSC, SSC, parameters
- changed definition for t13 and t14 of the MLI timing
- changed definition for t45 of the MSC timing
- add parameters dTx<sub>dly</sub> and dRx<sub>dly</sub> to ERAY parameters
- correct ERAY parameters t60 and t63 values
- correct footnotes for ERAY parameters
- split flash parameters tPRD and tPRP in two conditions
- add conditions to LVDS pad parameters
- Changed VAREF<sub>x</sub> to VAREF0 and VAGND<sub>x</sub> to VAGND0
- remove Pin Reliability in Overload section
- add parameters IIN and Sum IIN to absolute ratings
- adjust thresholds in figure 28 (ERAY)
- add parameter HYSX to PSC\_XTAL
- added RDSON values for all driver settings (weak, medium, and strong)
- removed footnote 2 of table 6
- change conditions for RDSON weak parameters
- change load for timing of SSC, MSC, and MLI from  $C_L = 25$  pF to  $C_L = 50$  pF (typical)
- add type I to legend of table 2
- add SAK-TC1782-320F180HL and SAK-TC1782-256F133HL
- changed timing checkpoints in figure 23
- add section 5.2.6.1
- add to parameters  $t_{RF}$  and  $t_{FF}$  condition  $C_L = 50$  pF
- add new footnote 7) to ADC parameter table
- add min and max value for  $Q_{CONV}$  and adapt typ value
- add load conditions for  $t_{FF1}$  and  $t_{RF1}$
- add conditions to PLL parameter  $t_L$
- change DAP parameter  $t_{i9}$  from SR to CC classification
- remove footnote 2 for the FADC
- increase current for  $I_{DDP\_POR}$  from 2 to 2.5mA
- add footnote 3 to table 9
- change **SAK-TC1782-320F180HR / SAK-TC1782-320F180HL** to **SAK-TC1782F-320F180HR / SAK-TC1782F-320F180HL**
- change **SAK-TC1782-256F133HR / SAK-TC1782-256F133HL** to **SAK-TC1782F-256F133HR / SAK-TC1782F-256F133HL**
- add information for the following products:
  - **SAK-TC1782N-320F180HR**

- **SAK-TC1782N-320F180HL**
- **SAK-TC1182N-320F180HR**
- **SAK-TC1182N-320F180HL**
- **SAK-TC1782N-256F133HR**
- **SAK-TC1782N-256F133HL**
- **SAK-TC1182N-256F133HR**
- **SAK-TC1182N-156F133HL**

The following changes were done between Version 1.0 and 1.1 of this document:

- add section Pin Reliability in Overload
- remove sentence 'Exposure to conditions within the maximum ratings will not affect device reliability. To replace this sentence section Pin Reliability in Overload was added.
- increase values for absolute maximum parameters  $I_{IN}$  and  $\text{Sum}I_{IN}$
- remove capacitance conditions for LVDS pad parameters as loads are defined by interface (MSC) timings
- remove term typical from load of Peripheral Timings
- add definition of driver strength settings for ERAY Interface Timing
- change footnote 4 wording for ERAY timing back to TC1797 wording
- increase flash parameters  $t_{PRD}$  and  $t_{PRP}$  values
- rework the 3.3 V current part of the Power Supply Parameters for better description and usage
  - Parameters  $I_{DDP\_FP}$ ,  $I_{DDFL3E}$  and  $I_{DDFL3R}$  are removed and replaced in the following way
    - $I_{DDP\_FP}$  is replaced by  $I_{DDP}$  with the condition including flash programming current
    - $I_{DDFL3E}$  is replaced by  $I_{DDP}$  with the condition including flash erase verify current
    - $I_{DDFL3R}$  is replaced by  $I_{DDP}$  with the condition including flash read current
    - parameter  $I_{DDFL3R}$  was renamed to  $I_{DDFL3}$

The rework of the 3.3 V current part of the Power Supply Parameters was done for simplification and clarification. Former given values could still be used if liked, the new definition results in the same resulting values or slightly better values. The flash module is supplied via  $I_{DDFL3}$  and  $I_{DDP}$ . For the different flash operating modes in worst case different allocations for the two domains resulting.

The application typical case 'flash read' has max  $I_{DDP}$  of 12 mA and max  $I_{DDFL3}$  of 56 mA resulting is a sum of 68 mA.

The case 'flash programming' has max  $I_{DDP}$  of 27 mA and max  $I_{DDFL3}$  of 21 mA resulting is a sum of 48 mA.

The case 'flash erase verify' has max  $I_{DDP}$  of 20 mA and max  $I_{DDFL3}$  of 56 mA resulting is a sum of 76 mA.

So for the old parameter  $I_{DDP}$  with 15 mA, the new version reads as  $I_{DDP} = 12 + I_{DDP\_PORST} = 14.5$  mA for the same application relevant case.

The following changes were done between Version 1.1 and 1.2 of this document:



**History**

- removed products SAK-TC1182N-320F180HR, SAK-TC1182N-320F180HL, SAK-TC1182N-256F133HR, and SAK-TC1182N-256F133HL
- improve parameters  $I_{DDFL3}$
- change for parameter  $N_E$  note from Max. data retention to Min.
- removed the term (typical)
- change description of parameter  $t_{CAL}$  for the ADC
- correct typo for class D pads in tables 14 and 15
- adapt Absolute Maximum Rating
- add footnote to Flash parameter  $t_{ERD}$
- add note at the end of Pin Reliability in Overload section
- clarify pad supply levels in Pin Reliability in Overload section
- add footnote for D-Flash currents in power section

The following changes were done between Version 1.2 and 1.3 of this document:

- add product option SAK-TC1782F-320F160HL, SAK-TC1782F-320F160HR, SAK-TC1782N-320F160HL and SAK-TC1782N-320F160HR
- update block diagrams to cover new option
- add identification registers for new product option
- rework first sentence for chapter 5.3
- reduce min value for  $t_L$  for both PLLs
- add for MLI and SSC parameter: valid strong driver medium edge only
- add footnote 5) for SSC parameters
- update FADC parameter  $EF_{DNL}$
- change MLI parameter  $t_{17}$  min value
- rename section Extended Range Operating Conditions to Voltage Operating timing Profiles and remove limitations on GPIOs
- split  $R_{DSONM}$  for class F pads into two conditions

The following changes were done between Version 1.3 and 1.3.1 of this document:

- correct typos in table 1
  - SAK-TC1782N-320N160HR -> SAK-TC1782F-320F160HR
  - SAK-TC1782N-320N160HL -> SAK-TC1782F-320F160HL
- reduce current for  $I_{LVDS}$  from 24mA to 12mA (only 2 pairs are available)

The following changes were done between Version 1.3.1 and 1.4 of this document:

- remove the following product options:
  - SAK-TC1782F-256F133HR
  - SAK-TC1782F-256F133HL
- change  $t_{48}$  from 100ns to 200ns in table 42
- change  $t_{49}$  from 100ns to 200ns in table 42
- extend  $K_{OVAN}$  condition from  $I_{OV} \leq 0$  mA;  $I_{OV} \geq -1$  mA to  $I_{OV} \leq 0$  mA;  $I_{OV} \geq -2$  mA
- change parameter  $EF_{OFF}$  from +90mV to +120 for condition Calibration = No

The following changes were done between Version 1.4 and 1.4.1 of this document:

- change parameter  $EF_{OFF}$  from +120mV to +90 for condition Calibration = No

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.