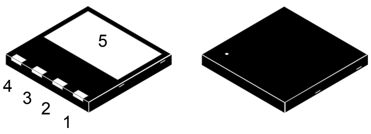
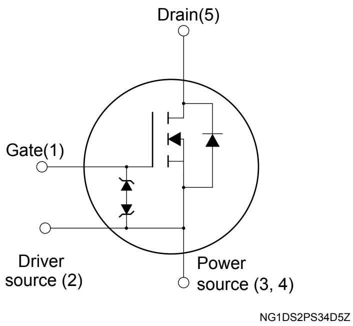
STL19N60DM2

Datasheet

N-channel 600 V, 0.280 Ω typ., 11 A, MDmesh DM2 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT™ 8x8 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL19N60DM2	600 V	0.320 Ω	11 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link
STL19N60DM2

Product summary	
Order code	STL19N60DM2
Marking	19N60DM2
Package	PowerFLAT™ 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	11	A
	Drain current (continuous) at T_{case} = 100 °C	6.8	
I_{DM} (1)	Drain current (pulsed)	44	A
P_{TOT}	Total power dissipation at T_{case} = 25 °C	90	W
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. $I_{SD} \leq 11$ *A, di/dt=400 A/μs,* $V_{DD} = 400$ *V,* $V_{DS(peak)} < V_{(BR)DSS}$
3. $V_{DS} \leq 480$ *V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.39	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb	45	

1. *When mounted on an 1-inch² FR-4, 2oz Cu board*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	2.5	A
E_{AS}(2)	Single pulse avalanche energy	380	mJ

1. *Pulse width is limited by* $T_{j\ max}$.
2. *Starting* T_j = 25 °C, $I_D = I_{AR}$, $V_{DD} = 50$ *V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A		0.280	0.320	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	800	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	1.33	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, f = 1 MHz, V_{GS} = 0 V	-	80	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	20	-	nC
Q_{gs}	Gate-source charge		-	5.2	-	nC
Q_{gd}	Gate-drain charge		-	8.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6 A R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	13.5	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	9.5	-	ns
t_f	Fall time		-	32.5	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 11 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	125		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	0.675		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	190		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	1.225		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	13		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

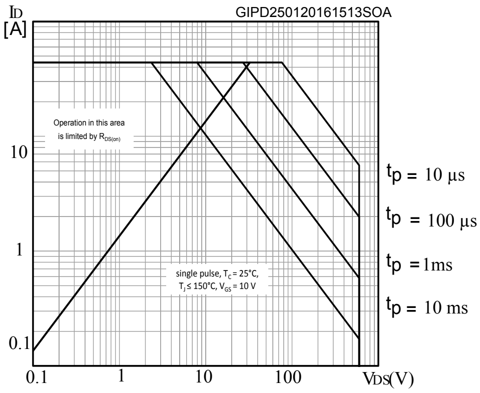


Figure 2. Thermal impedance

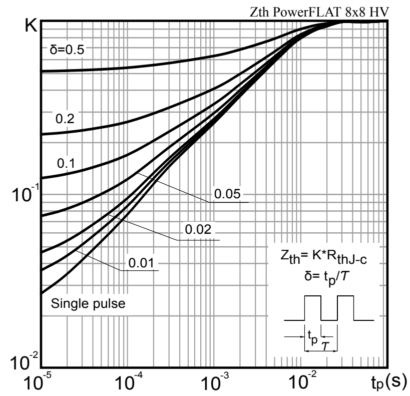


Figure 3. Output characteristics

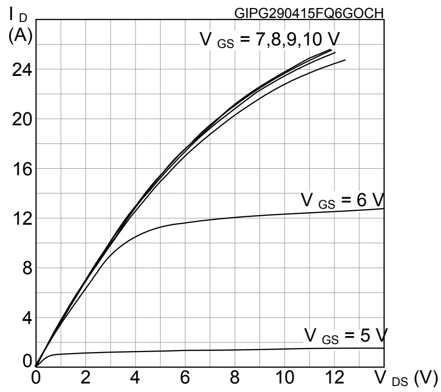


Figure 4. Transfer characteristics

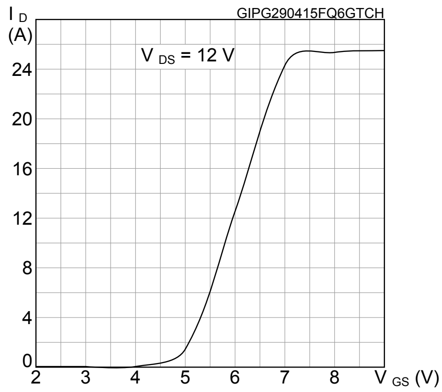


Figure 5. Gate charge vs gate-source voltage

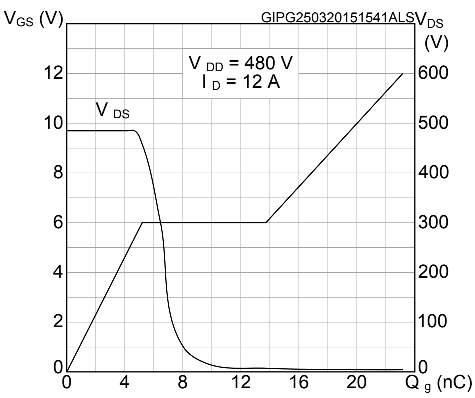


Figure 6. Static drain-source on-resistance

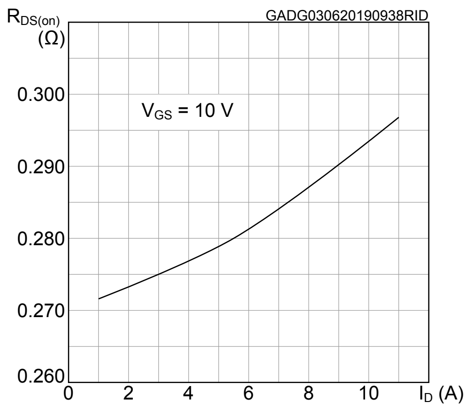


Figure 7. Capacitance variations

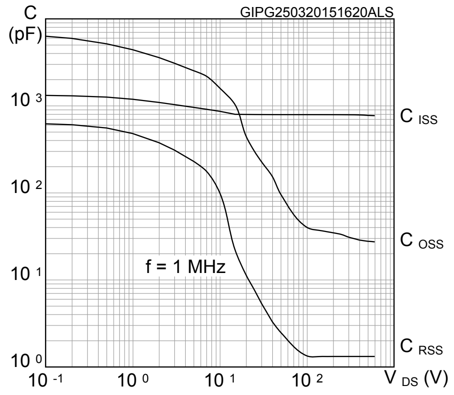


Figure 8. Normalized gate threshold voltage vs temperature

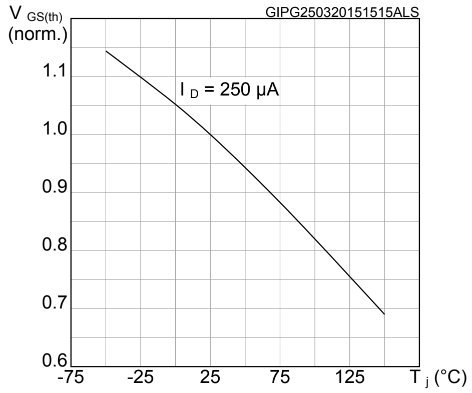


Figure 9. Normalized on-resistance vs temperature

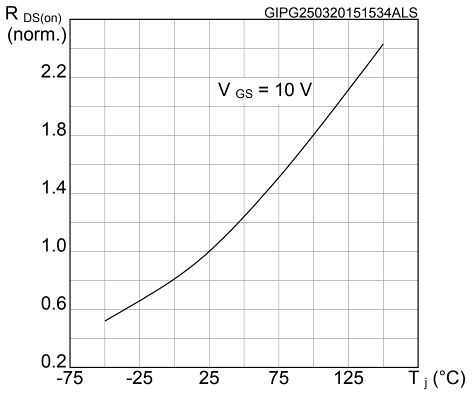


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

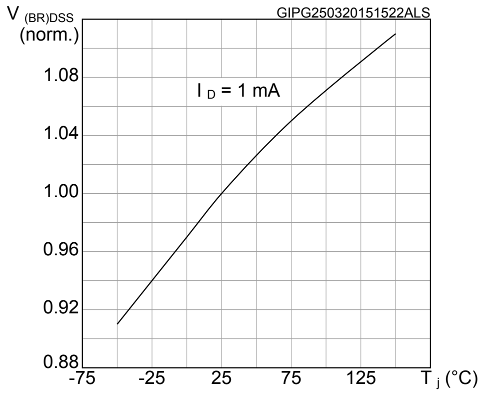


Figure 11. Source-drain diode forward characteristics

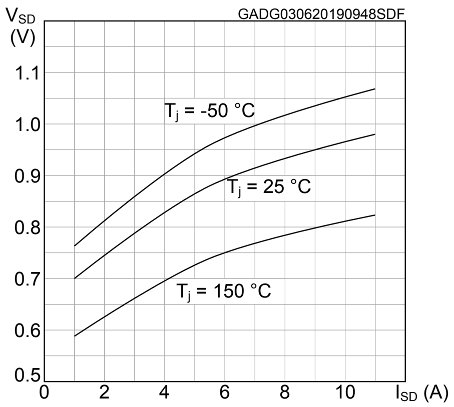
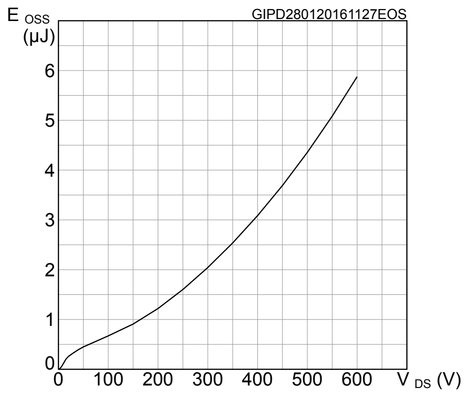


Figure 12. Output capacitance stored energy



3 Test circuits

Figure 13. Switching times test circuit for resistive load

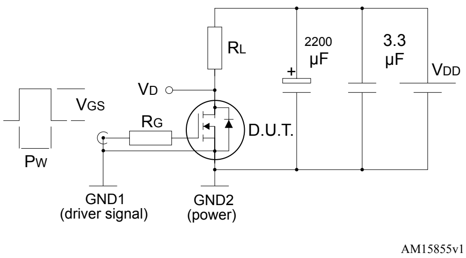


Figure 14. Test circuit for gate charge behavior

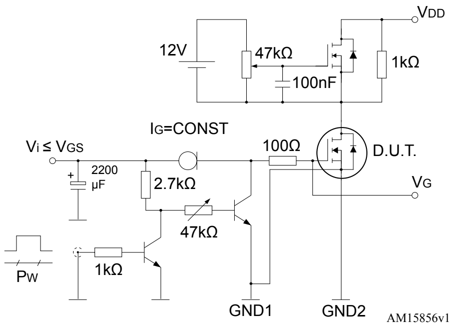


Figure 15. Test circuit for inductive load switching and diode recovery times

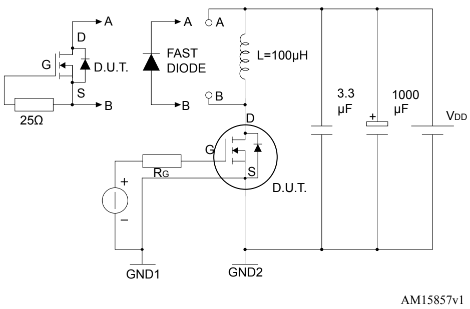


Figure 16. Unclamped inductive load test circuit

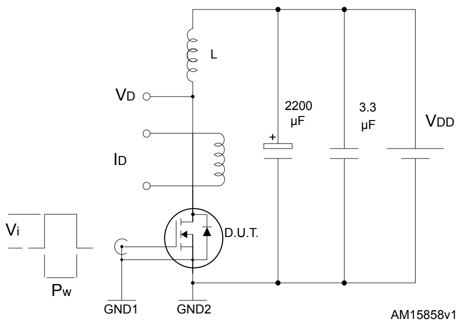


Figure 17. Unclamped inductive waveform

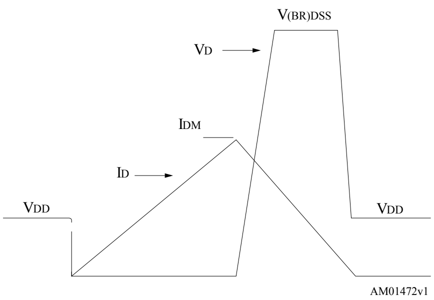
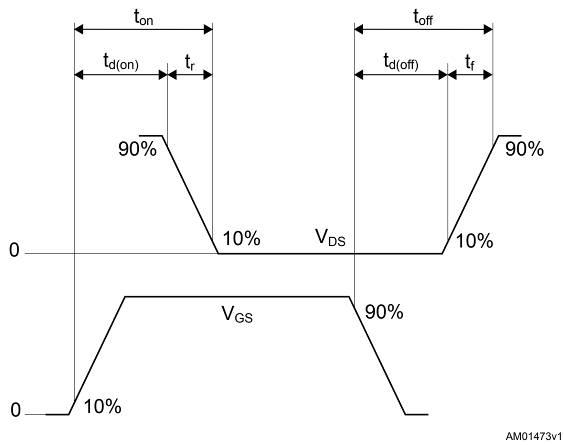


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 19. **PowerFLAT 8x8 HV package outline**

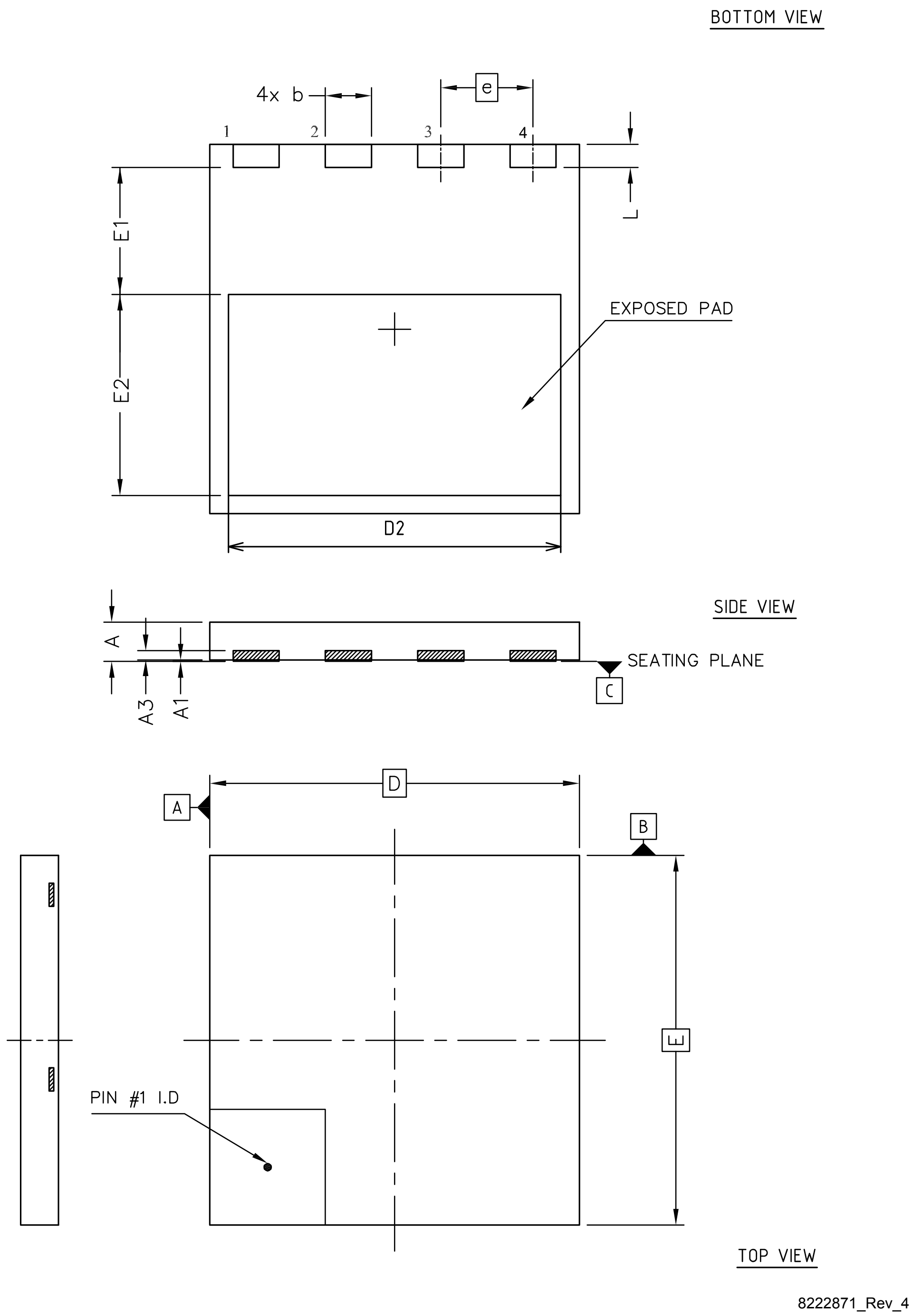
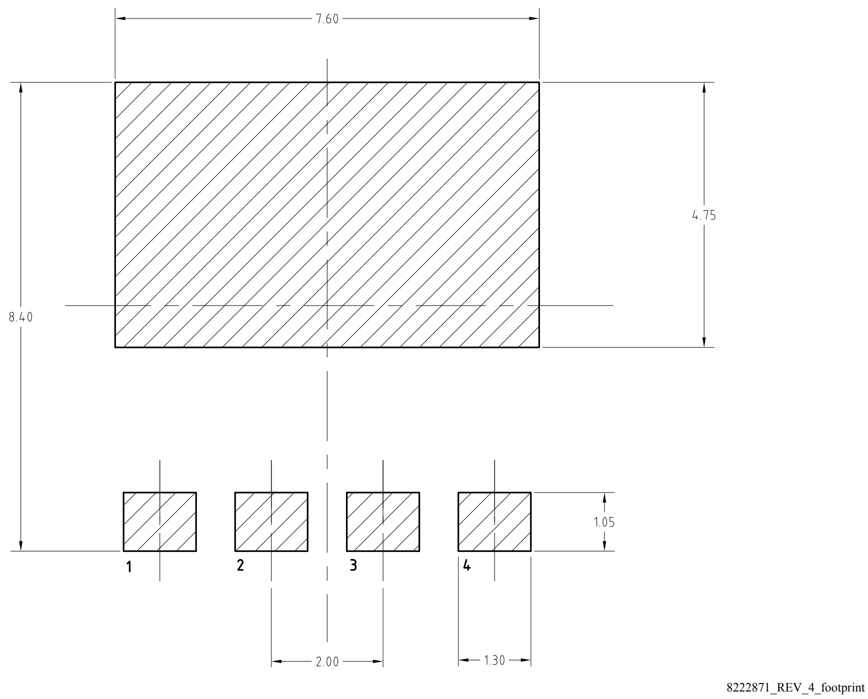


Table 8. PowerFLAT 8x8 HV mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

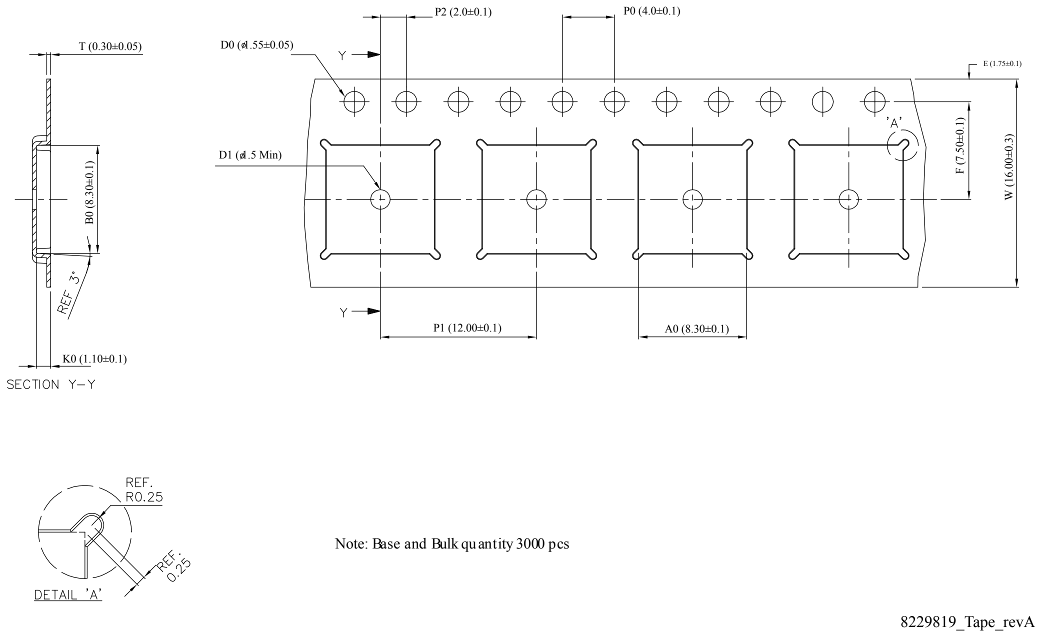
Figure 20. PowerFLAT 8x8 HV footprint



Note: All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 21. PowerFLAT 8x8 HV tape



Note: All dimensions are in millimeters.

Figure 22. PowerFLAT 8x8 HV package orientation in carrier tape

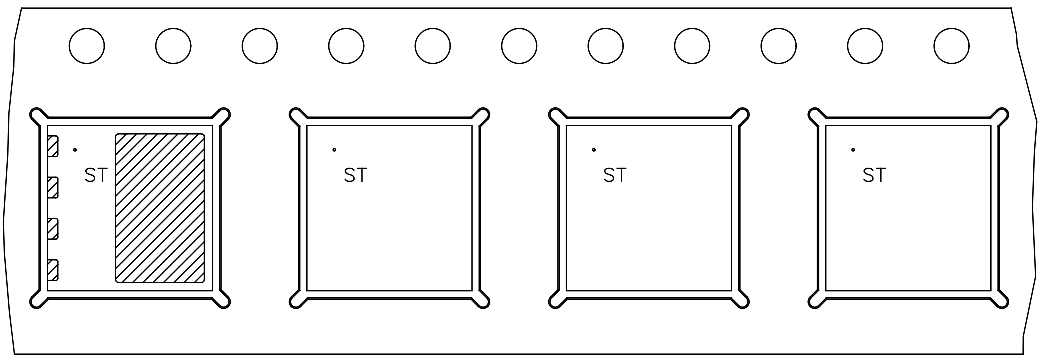
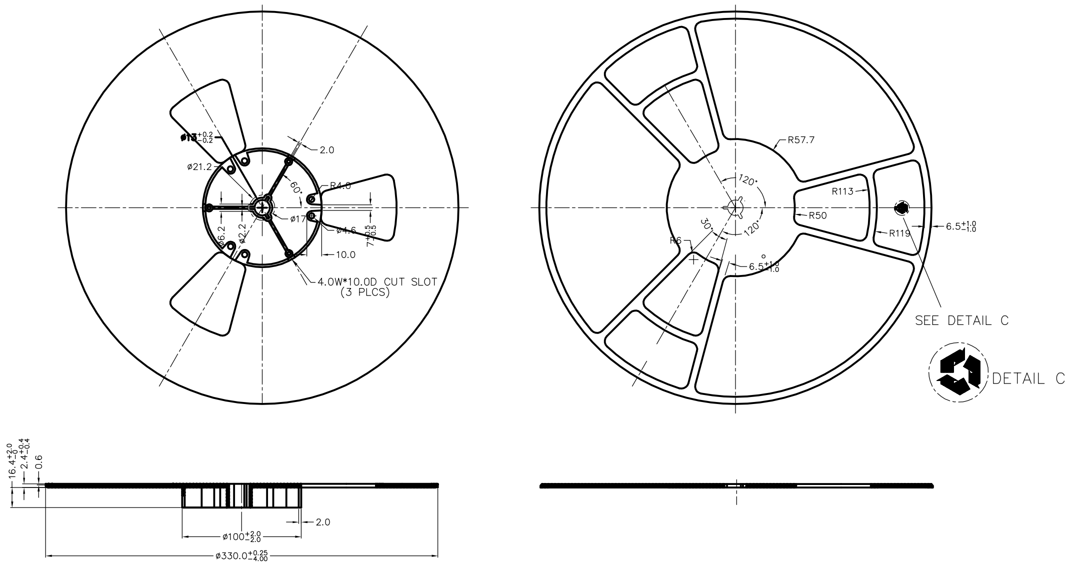


Figure 23. PowerFLAT 8x8 HV reel



8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 9. Document revision history

Date	Version	Changes
08-Aug-2014	1	Initial release.
05-Jun-2019	2	Modified Table 4. Static, Table 5. Dynamic, Table 6. Switching times and Table 7. Source-drain diode. Added Section 2.1 Electrical characteristics (curves). Modified Section 4.1 PowerFLAT 8x8 HV package information. Minor text changes.

Contents

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