APD-192G064-1

Vishay Dale

Plasma Panel Display Modules

192 x 64 Graphics Display with Drive Electronics
TTL Level Data Interface and Integrated DC Converter



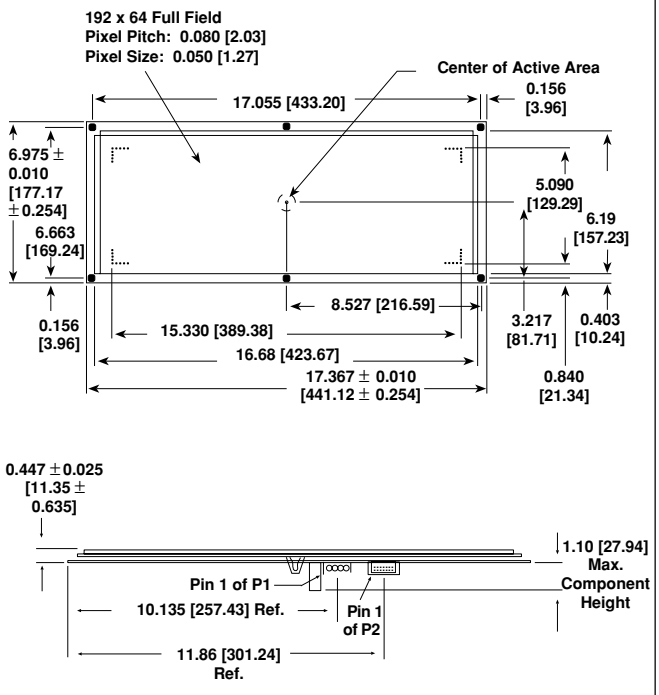
The APD-192G064-1 has been designed to offer high brightness and superior viewing aesthetics in a package that is very affordable. This display is ideal for low to medium level information content messages and would be ideal for applications such as arcade games, process control, POS terminals, medical equipment, message centers and ATM machines.

STANDARD ELECTRICAL SPECIFICATIONS*

DESCRIPTION	SYMBOL	MIN.	TYP.	MAX.	UNITS
DC converter input	VDC	+ 10.0	+ 24.0	+ 28.0	VDC
DC converter power @ + 12 V	Amps	Screen Clear 0.100	50% Lit 1.7	100% Lit 3.5	—
Logic 1 Input	V_{ih}	2.0	—	—	VDC
Logic 0 Input	V_{il}	—	—	0.8	VDC

*Recommended operating voltages. All maximums are absolute maximum.

DIMENSIONS in inches [millimeters]



FEATURES

- TTL level video interface.
- On board DC converter.
- Slim profile.
- Large, bright characters and graphics.
- Highly visible for long distance viewing.

ELECTRICAL SPECIFICATIONS

Voltages Required: VDC: + 12 to + 24 VDC.

Power Required: Typical = 12 watts.
Maximum = 55 watts.

OPTICAL SPECIFICATIONS

Viewing Area: 15.33" [389.38] W x 5.09" [129.29] H.

Pixel Pitch: 0.080" [2.032].

Pixel Size: 0.050" [1.27].

Color: Neon orange.

Character Array: 8 x 8: 24 x 16. 6 x 8: 32 x 16.

Character Size: 0.48" [12.19] W x 0.64" [16.26] H .

Luminance: 50 foot lamberts minimum.

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0°C to + 70°C.

Storage Temperature: - 40°C to + 85°C.

Relative Operating Humidity: To 95% non-condensing.

Mechanical Shock: 30 G.

Vibration: 3 G.

Operating Altitude: 10,000 feet.

GENERAL DESCRIPTION

The APD-192G064-1 DC Plasma display offers viewing qualities designers seek such as high contrast, viewing angle of 150° minimum, and long distance readability. It is bright (50 foot lamberts minimum) with characters and graphics figures presented in a pleasing neon orange color against a black background. Plasma is much more readable and eye-pleasing than liquid crystal or vacuum fluorescent displays and is filterable to red, amber, or neutral density. These plasma display panels are driven in a standard row - column refresh method much like a CRT display. The designer need only supply TTL level signals for SERIAL DATA, DOT CLOCK, COLUMN LATCH, ROW DATA, ROW CLOCK and DISPLAY ENABLE. The SERIAL DATA is entered with the DOT CLOCK up to frequencies as high as 8mHz. After a row of 192 pixels is clocked in, the COLUMN LATCH signal is toggled and the data is latched. At the time the data is latched, the display is briefly disabled using the DISPLAY ENABLE signal, then the row pointer is advanced with the ROW CLOCK signal. Once each frame the ROW DATA must be asserted to synchronize the column serial data with the beginning row. The recommended scanning frequency is approximately 70 Hz but may be as high as 200 Hz. The high clock rate on the data clock allows for rapid refresh and maximum access time to the refresh ram.

PIN DESCRIPTION

P3, POWER CONNECTOR

AMP #641737-1 or equivalent.
(Mates with AMP 1-480424-0 or equivalent.)

PIN	SIGNAL	DESCRIPTION
4	N/C	Reserved
3	GND	Ground
2	GND	Ground
1	VDC	DC Converter Supply

P2, DATA CONNECTOR

AMP #103309-2 or equivalent.
(Mates with AMP 746195-2, MOLEX 39-27-1146 or equivalent.)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	DISPLAY ENABLE	2	GROUND
3	ROW DATA	4	GROUND
5	ROW CLOCK	6	GROUND
7	COLUMN LATCH	8	GROUND
9	DOT CLOCK	10	GROUND
11	SERIAL DATA	12	GROUND
13	No connect	14	GROUND

DESCRIPTION OF INPUT SIGNALS

DOT CLOCK - This signal enters the SERIAL DATA on each low to high transition. A total of 192 DOT CLOCK transitions must be present for each line of column/anode data.

SERIAL DATA - This signal presents the pixel data in positive logic format. A logic one represents a lit pixel and a logic zero represents an extinguished pixel. Data is entered from right to left. The first pixel data entered will represent the leftmost pixel in the row.

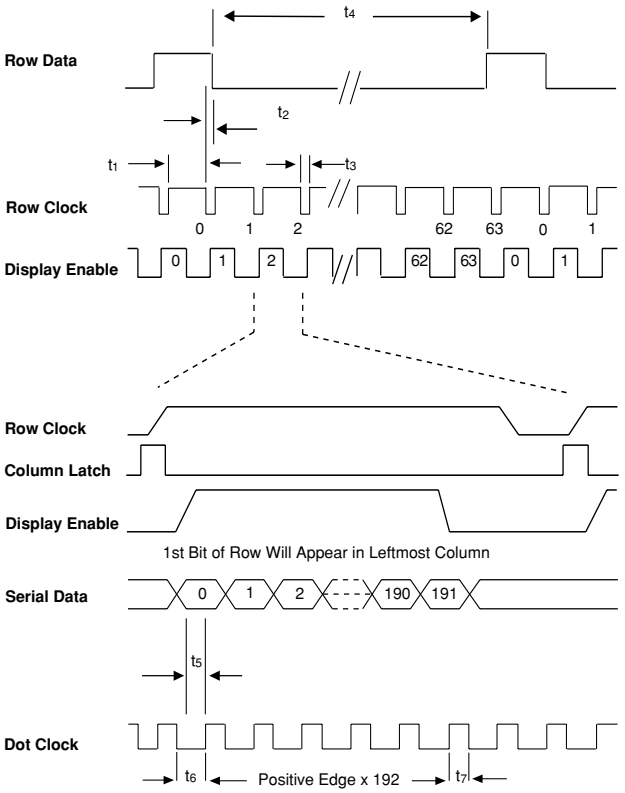
COLUMN LATCH - This signal latches the pixel data into the driver outputs. When the COLUMN LATCH signal goes to logic one the data entered previously will fall through to the driver outputs. When the signal returns to a logic zero, the data is latched and the shift register is now ready to accept the next row of data. Must be held low while entering new SERIAL DATA.

DISPLAY ENABLE - This signal enables the output drivers. Using a duty cycle control, this signal may also be used for intensity control. The DISPLAY ENABLE must be at logic zero before the COLUMN LATCH signal transitions. To avoid display blurring, the ROW CLOCK signal should also transition while DISPLAY ENABLE is a logic zero. It is recommended that this signal remain low for 10µS min.

ROW DATA - This signal is the first line marker for the scan. This input should be held high to correspond to the first row of pixel data.

ROW CLOCK - This signal clocks ROW DATA on the falling edge. The ROW CLOCK signal is repetitive and must be present for proper scanning of the display module.
The APD-192G064-1 has a unique input protection circuit that assures the column drivers stay blanked on power up. The protection circuit unblanks the column drivers when the ROW CLOCK signal begins (i.e. the display begins scanning).

LOGIC AND DATA TIMING



PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS
t_1	100	—	—	nS
t_2	5	—	—	uS
t_3	1	—	—	uS
t_4	—	70	200	Hz
t_5	25	—	—	nS
t_6	75	—	—	nS
t_7	75	—	—	nS

ORDERING INFORMATION

Display Module with Drivers, TTL Interface and On Board DC Converter APD-192G064-1
Data Connector Kit 280105-05
Power Connector Kit 280108-13
Video Controller (+5V) PDS-500
Video Contoller (+ 12V) PDS-500-1

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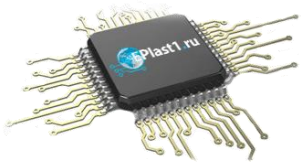
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- Техническая поддержка проекта;
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Как с нами связаться

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