

Panasonic

MOS FET

MTM131270BBF

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Silicon P-channel MOS FET

For switching

■ Features

- Low Drain-source On-state Resistance : $R_{DS(on)}$ typ = $92\text{ m}\Omega$ ($V_{GS} = -4.0\text{ V}$)
- Low drive voltage: 1.8 V drive
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : EU

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

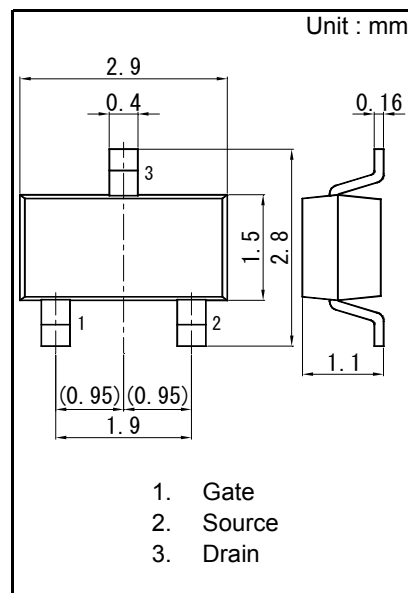
■ Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

項目	記号	定格	単位
Drain-source Voltage	VDS	-20	V
Gate-source Voltage	VGS	± 10	
Drain current	ID	-2	A
Peak drain current ^{*1}	IDp	-8	A
Power dissipation ^{*2}	PD	700	mW
Channel temperature	Tch	150	$^\circ\text{C}$
Operating ambient temperature	Topr	-40 to +85	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$

Note *1 Pulse width $\leq 10\text{ }\mu\text{s}$, Duty cycle $\leq 1\%$

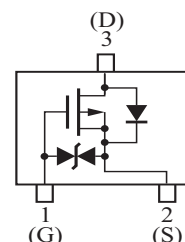
*2 Measuring on ceramic board at $40 \times 38 \times 0.1\text{ mm}$.

Absolute maximum rating PD without heat sink shall be made 200 mW.



Panasonic	Mini3-G3-B
JEITA	SC-59A
Code	TO-236AA/SOT-23

Internal Connection



Pin Name

1. Gate
2. Source
3. Drain

■ Electrical Characteristics Ta = 25 °C ± 3 °C

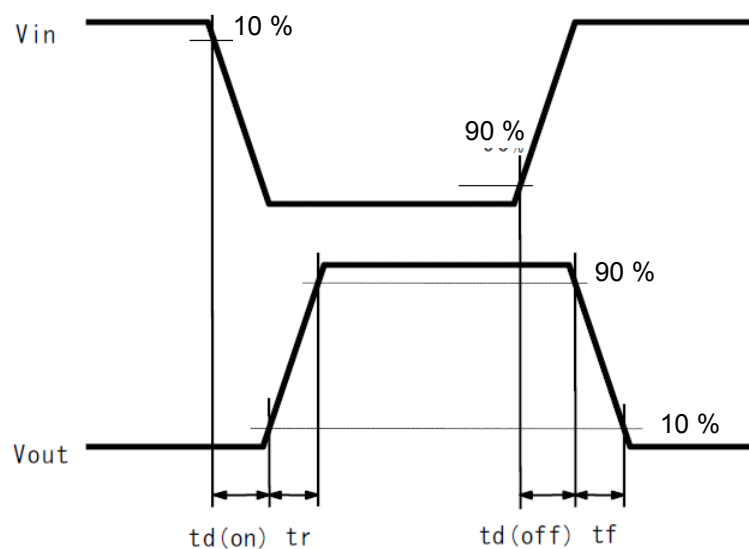
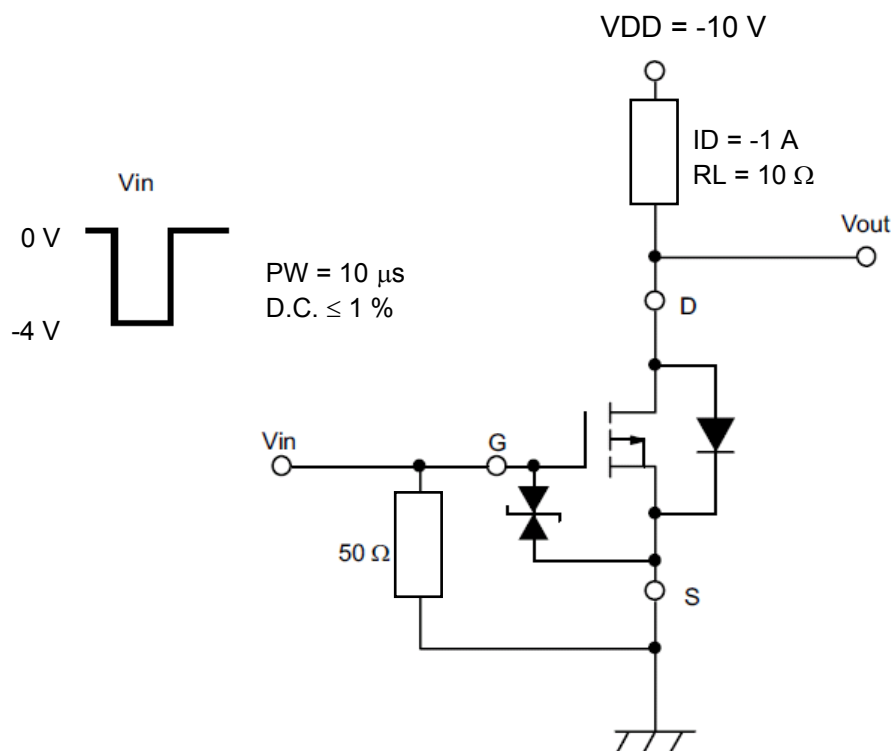
項目	記号	条件	最小	標準	最大	単位
Drain-source surrender voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V
Drain-source cutoff current	IDSS	VDS = -20 V, VGS = 0 V			-1	μA
Gate-source cutoff current	IGSS	VGS = ±8 V, VDS = 0 V			±10	
Gate threshold voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.75	-1.1	V
Drain-source ON resistance *1	RDS(on)1	ID = -1 A, VGS = -4 V		92	130	mΩ
	RDS(on)2	ID = -1 A, VGS = -2.5 V		115	210	
	RDS(on)3	ID = -0.5 A, VGS = -1.8 V		161	280	
Forward transfer admittance *1	Yfs	ID = -1 A, VDS = -10 V, f = 1 kHz	3			S
Short-circuit input capacitance (Common source)	Ciss	VDS = -10 V, VGS = 0 V f = 1 MHz		300		pF
Short-circuit output capacitance (Common source)	Coss			30		
Reverse transfer capacitance (Common source)	Crss			35		
Turn-on Delay Time *2	td(on)	VDD = -10 V, VGS = 0 to -4 V		6		ns
Rise Time *2	tr	ID = -1 A		8		
Turn-off Delay Time *2	td(off)	VDD = -10 V, VGS = -4 to 0 V		57		
Fall Time *2	tf	ID = -1 A		55		

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. *1 Pulse test

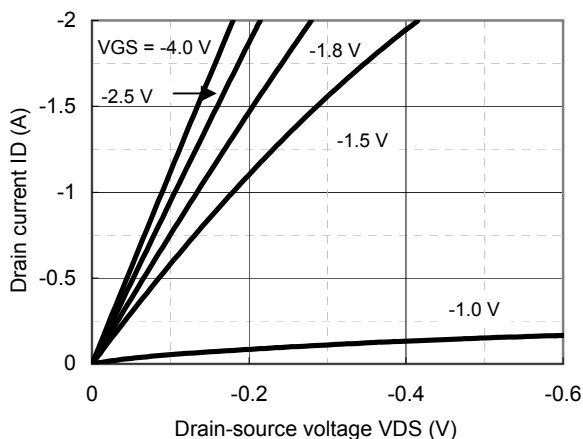
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

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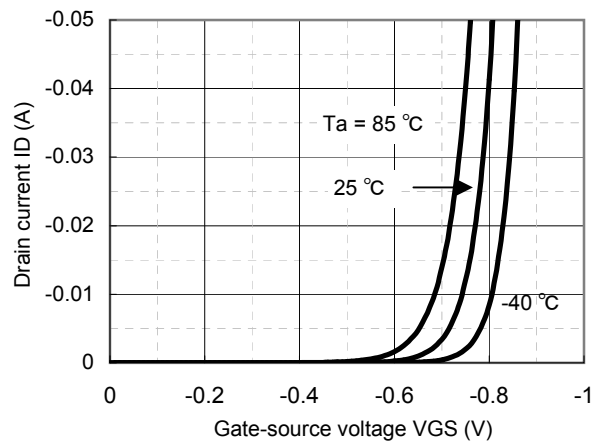


Technical Data (reference)

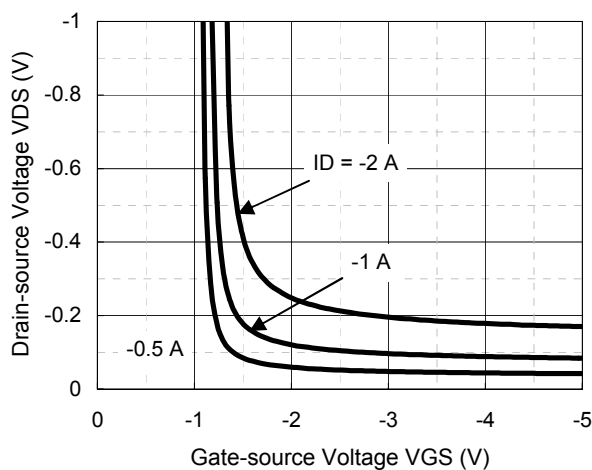
ID - VDS



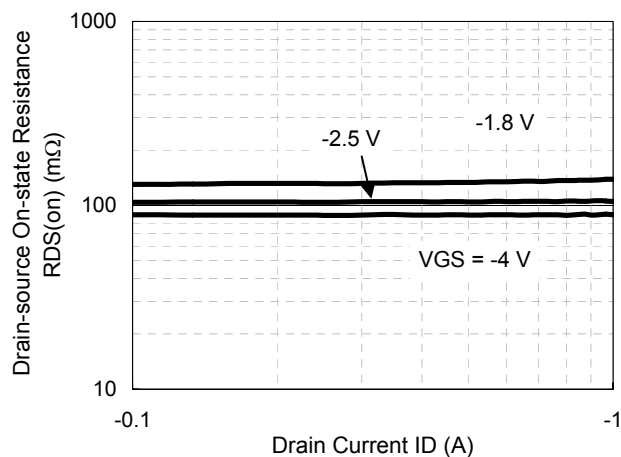
ID - VGS



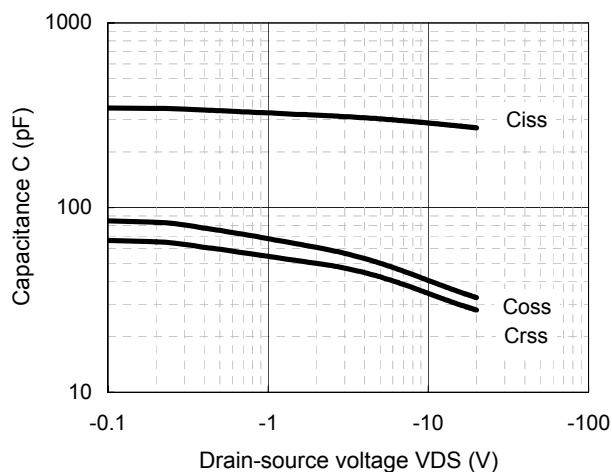
VDS - VGS



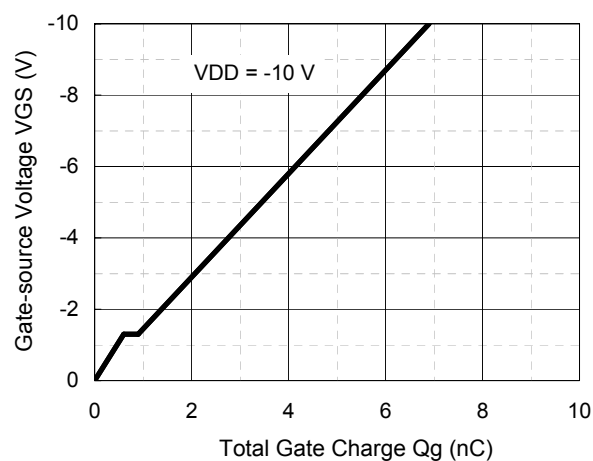
RDS(on) - ID



Capacitance - VDS

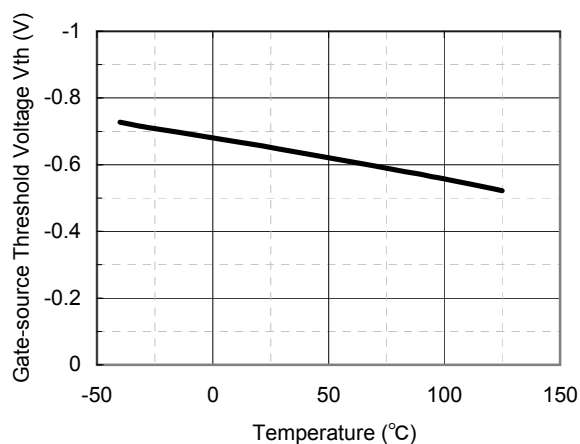


Dynamic Input/Output Characteristics

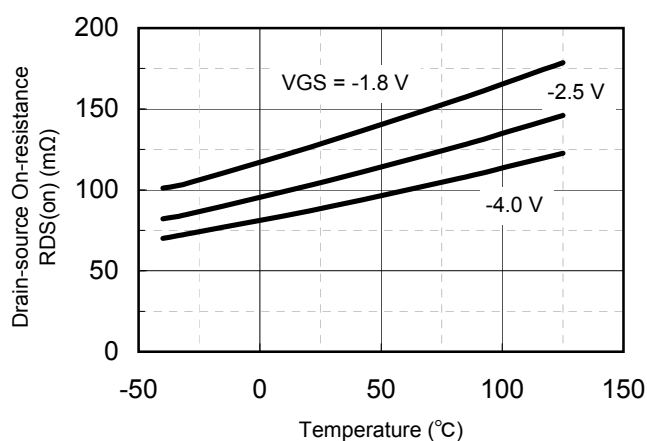


Technical Data (reference)

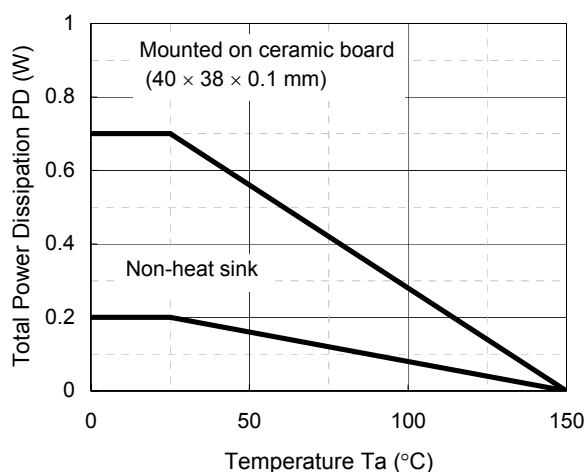
V_{th} - T_a



R_{DS(on)} - T_a

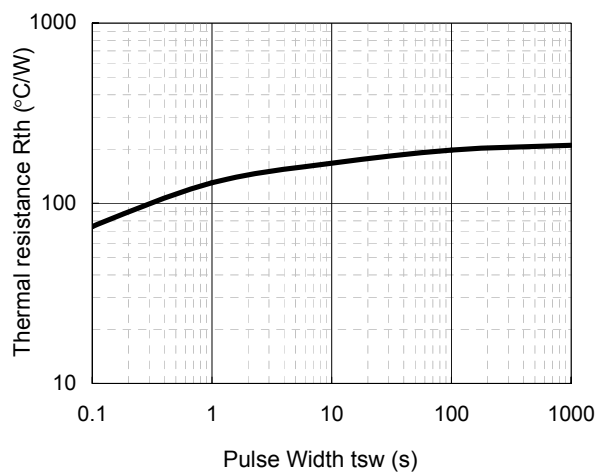


PD - T_a

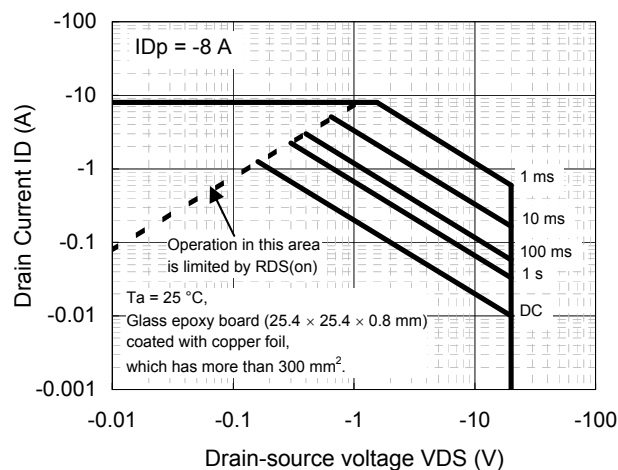


PD - T_c

R_{th} - t_{sw}



Safe Operating Area

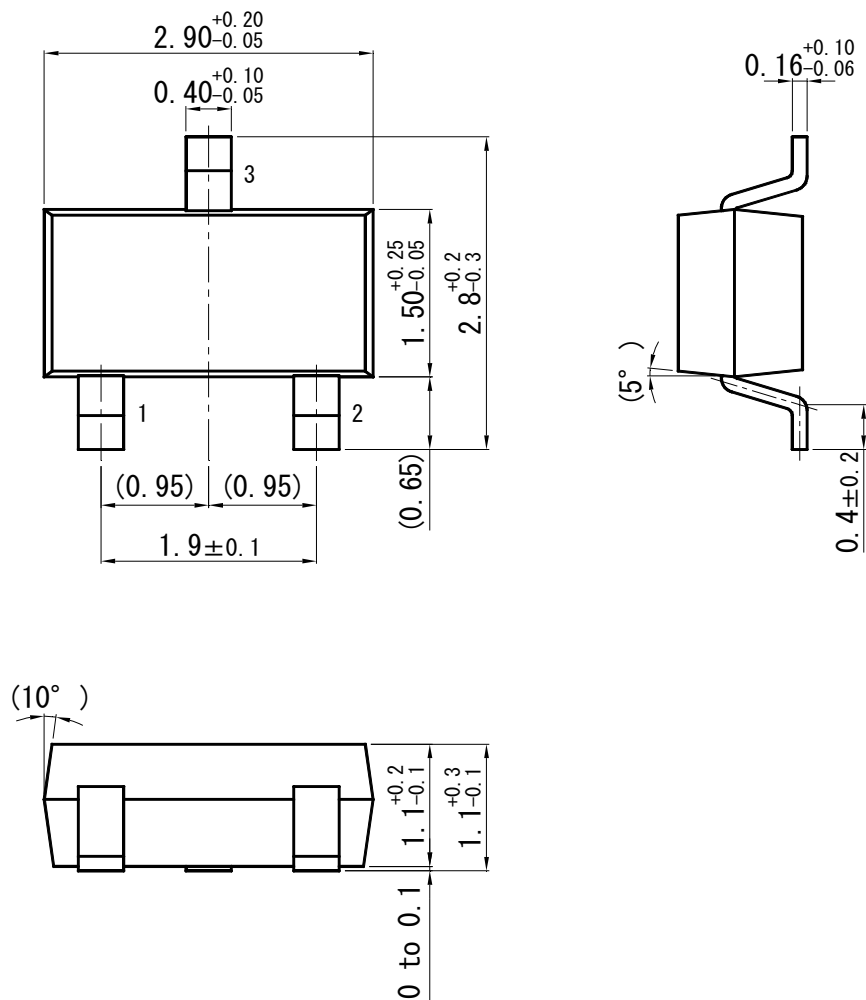


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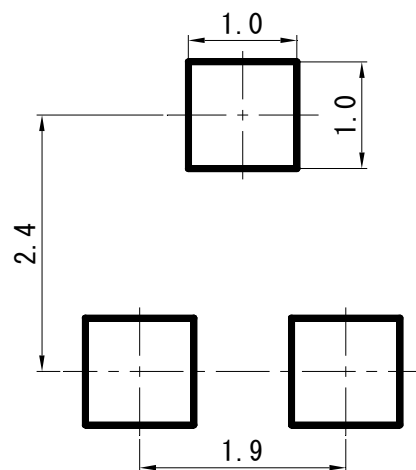
MOS FET
MTM131270BBF

Mini3-G3-B

Unit: mm



■ Land Pattern (Reference) (Unit : mm)



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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.