



Integrated Device Technology, Inc.

CMOS StaticRAM 16K (4K x 4-BIT) CACHE-TAG RAM

IDT6178S

FEATURES:

- High-speed Address to MATCH Valid time
 - Military: 12/15/20/25ns
 - Commercial: 10/12/15/20/25ns (max.)
- High-speed Address Access time
 - Military: 12/15/20/25ns
 - Commercial: 10/12/15/20/25ns (max.)
- Low-power consumption
 - IDT6178S
 Active: 300mW (typ.)
- Produced with advanced CMOS high-performance technology
- Input and output TTL-compatible
- Standard 22-pin Plastic or Ceramic DIP, 24-pin SOJ
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

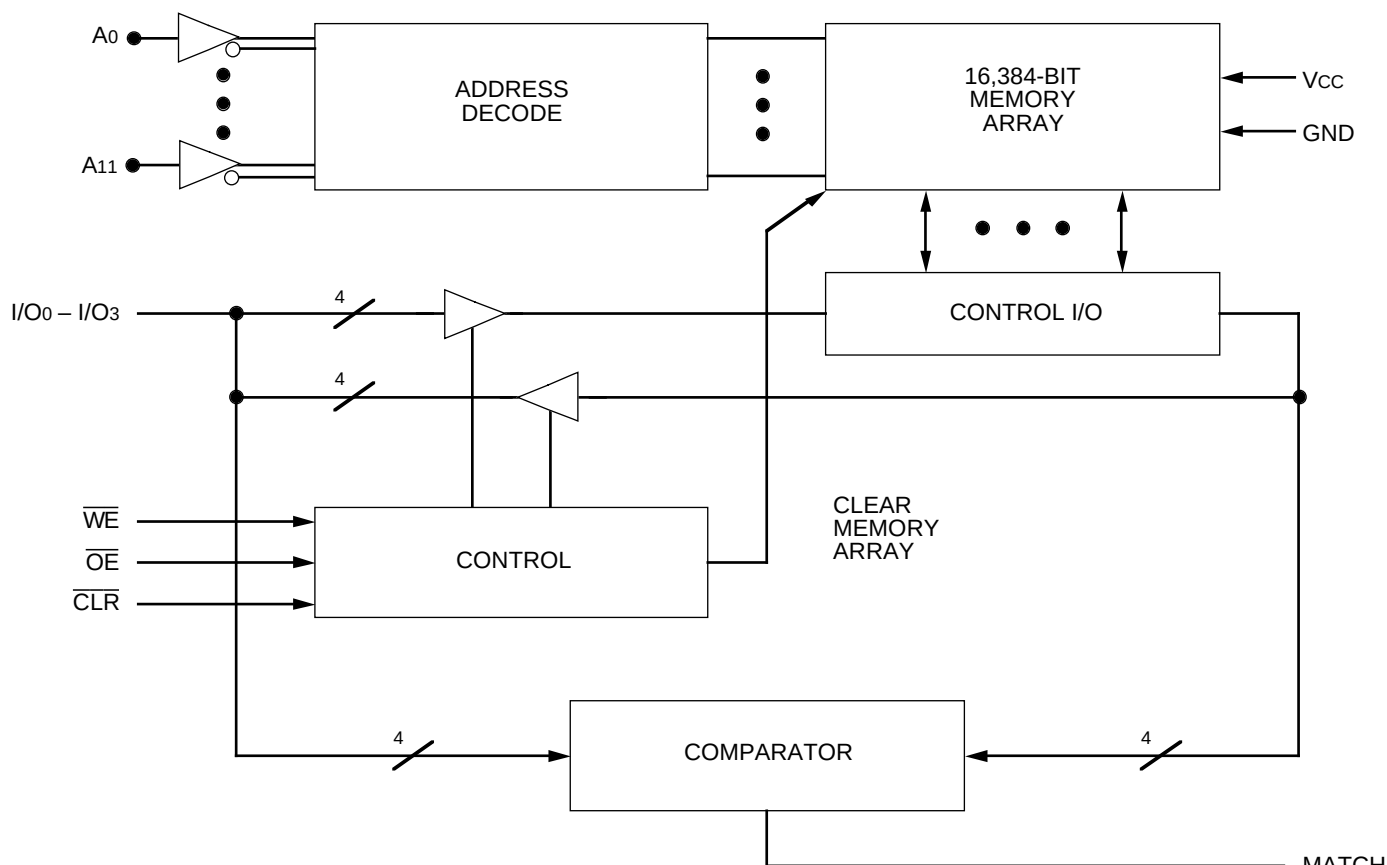
The IDT6178 is a high-speed cache address comparator sub-system consisting of a 16,384-bit StaticRAM organized as 4K x 4. Cycle Time and Address to MATCH Valid are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active HIGH on the MATCH pin. The MATCH pins of several IDT6178s can be handed together to provide enabling or acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability CMOS technology. Address to MATCH and Data to MATCH times are as fast as 10ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply.

The IDT6178 is packaged in either a 22-pin, 300-mil Plastic or Ceramic DIP package or 24-pin SOJ. Military grade product is manufactured in compliance with latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



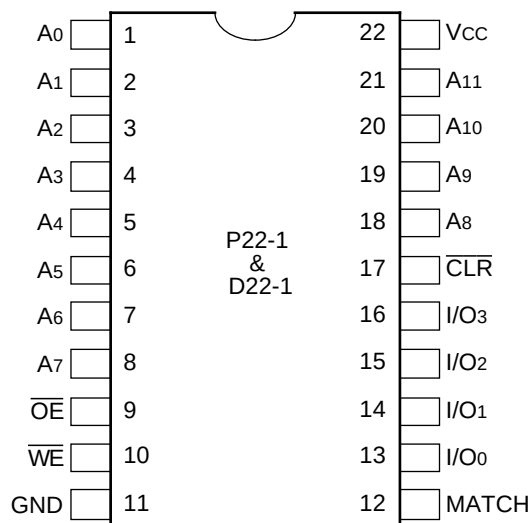
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2953 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1994

PIN CONFIGURATIONS

DIP
TOP VIEW

2953 drw 02

PIN DESCRIPTIONS

A0–A11	Address Inputs
I/O0–I/O3	Data Input/Output
MATCH	Match
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
VCC	Power
GND	Ground

2953 tbl 01

RECOMMENDED OPERATING
TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	–55°C to +125°C	0V	5.0V ± 10%

2953 tbl 02

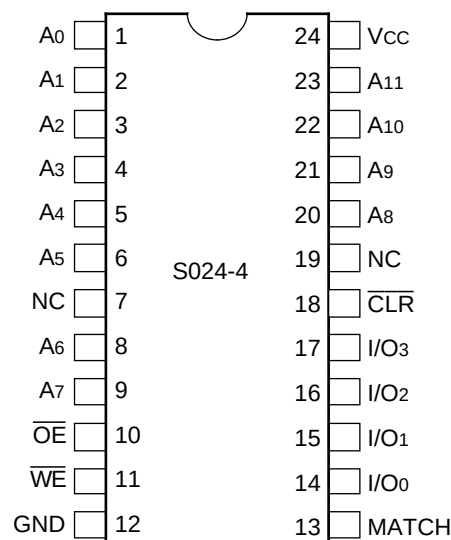
TRUTH TABLES⁽¹⁾

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	Mode
H	H	H	Valid ⁽²⁾	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

NOTE:

- H = V_{IH}, L = V_{IL}, X = Don't care.
- Valid Match = V_{OH}, Valid Non-Match = V_{OL}.

2953 tbl 03

SOJ
TOP VIEW

2953 drw 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
V _{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T _A	Operating Temperature	–55 to +125	°C
T _{BIAS}	Temperature Under Bias	–65 to +135	°C
T _{STG}	Storage Temperature	–65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

NOTE:

2953 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC
OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2 ⁽²⁾	–	6.0	V
V _{IL}	Input Low Voltage	–0.5 ⁽¹⁾	–	0.8	V

NOTES:

2953 tbl 05

- V_{IL} = –3.0V for pulse width less than 20ns, once per cycle.
- V_{IH} = 2.5V for clear pin.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Symbol	Parameter	Condition	Max	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	pF

NOTE:

2953 tbl 06

- This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

Symbol	Parameter	Test Condition	6178S		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current	$V_{CC} = 5.5V, V_{IN} = 0V \text{ to } V_{CC}$	—	10	μA
$ I_{LO} $	Output Leakage Current	$\overline{OE} = V_{IH}, V_{OUT} = 0V \text{ to } V_{CC}$	—	10	μA
V_{OL}	Output Low Voltage	$I_{OL} = 8mA (I/O_0 - I/O_3)$	—	0.4	V
		$I_{OL} = 10mA (I/O_0 - I/O_3)$	—	0.5	V
		$I_{OL} = 16mA \text{ (Match)}$	—	0.4	V
		$I_{OL} = 20mA \text{ (Match)}$	—	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA (I/O_0 - I/O_3)$	2.4	—	V
		$I_{OH} = -8mA \text{ (Match)}$	2.4	—	V

2953 tbl 07

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

Symbol	Parameter		6178S10 Max.	6178S12 ⁽¹⁾ Max.	6178S15 ⁽¹⁾ Max.	6178S20/25 Max.	Unit
ICC1	Operating Power Supply Current Outputs Open, $V_{CC} = \text{Max.}$, $f = 0^{(2)}$	COM'L.	90	90	90	90	mA
		MIL.	—	110	110	110	mA
ICC2	Dynamic Operating Current Outputs Open, $V_{CC} = \text{Max.}$, $f = f_{MAX}^{(2)}$	COM'L.	180	160	140	140	mA
		MIL.	—	180	160	160	mA

NOTES:

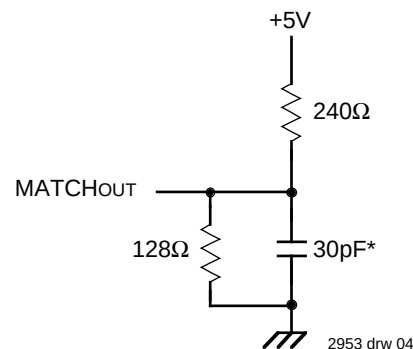
- Military values are preliminary only.
- $f_{MAX} = 1/t_{RC}$, only address inputs are cycling at f_{MAX} . $f = 0$ means no address inputs change.

2953 tbl 08

AC TEST CONDITIONS

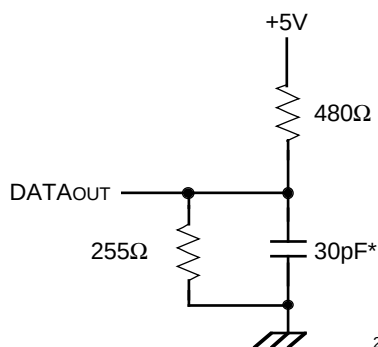
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 2 and 3
AC Test Load for Match Cycle	See Figure 1

2953 tbl 09



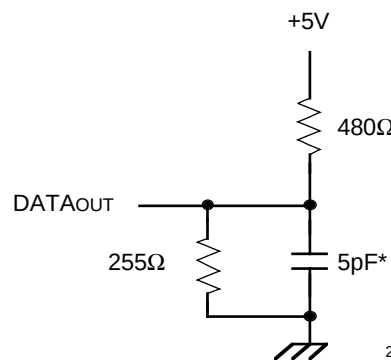
2953 drw 04

Figure 1. AC Test Load for MATCH



2953 drw 05

Figure 2. AC Test Load



2953 drw 06

Figure 3. AC Test Load
(for t_{OLZ} , t_{OHZ} , t_{WHZ} , t_{OW})

* Including scope and jig.

CYCLE DESCRIPTION

Match Cycle: A match cycle occurs when all control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CLR}$) are HIGH. At that time, data supplied to the RAM on the I/O pins is compared with the data stored at the specified address. The totem-pole match output is HIGH when there is a match at all data bits, and drives LOW if there is not a match.

Write Cycle: The write cycle is conventional, occurring when $\overline{WE}$ is LOW and $\overline{CLR}$ is HIGH. $\overline{OE}$ may be either HIGH or LOW, since it is overridden by $\overline{WE}$. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during write cycles since the data at the specified address is the same as the data (being written) at the I/Os of the RAM.

Read Cycle: When $\overline{WE}$ and $\overline{CLR}$ are HIGH and $\overline{OE}$ is LOW, the RAM is in a read cycle. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during read cycles since the data at the specified address is the same as the data (being read) at the I/Os of the RAM.

Clear Cycle: When $\overline{CLR}$ is asserted, every bit in the RAM is cleared to zero. If $\overline{OE}$ is LOW during a clear cycle, the RAM I/Os will be driven. However, this data is not necessarily zeros, even after a considerable time. The Match pin is enabled, but its state is not predicable.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

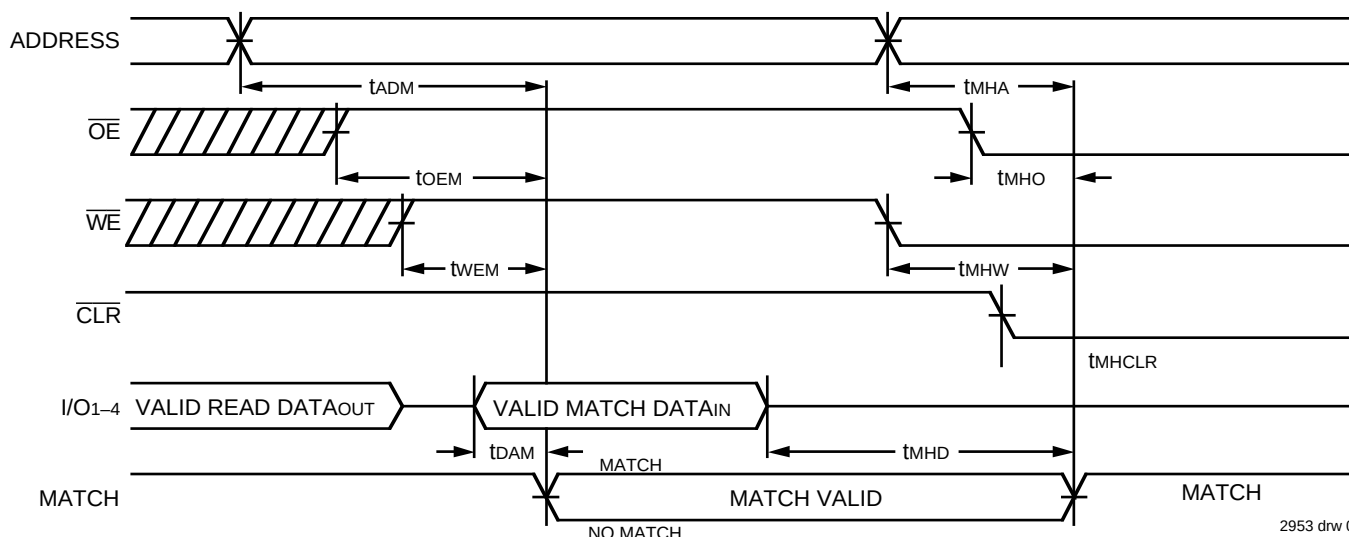
Symbol	Parameter	6178S10 ⁽¹⁾		6178S12		6178S15		6178S20		6178S25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle												
tADM	Address to Match Valid	—	10	—	12	—	15	—	20	—	25	ns
tDAM	Data Input to Match Valid	—	8	—	11	—	13	—	15	—	15	ns
tMHO	Match Valid Hold from $\overline{OE}$	0	—	0	—	0	—	0	—	0	—	ns
tOEM	$\overline{OE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
tMHW	Match Valid Hold from $\overline{WE}$	0	—	0	—	0	—	0	—	0	—	ns
tWEM	$\overline{WE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
tMHCLR	Match Valid Hold from $\overline{CLR}$	0	—	0	—	0	—	0	—	0	—	ns
tMHA	Match Valid Hold from Address	3	—	3	—	3	—	3	—	3	—	ns
tMHD	Match Valid Hold from Data	3	—	3	—	3	—	3	—	3	—	ns

NOTE:

1. 0°C to +70°C temperature range only.

2953 tbl 10

TIMING WAVEFORM OF MATCH CYCLE⁽¹⁾



2953 drw 07

NOTE:

1. It is not recommended to let address and data input pins float while MATCH pin is active.

Symbol	Parameter	6178S10 ⁽¹⁾		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20/25	ns
tOE	Output Enable Access Time	—	7	—	8	—	10	—	15	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tOLZ ⁽²⁾	Output Enable to Output in Low-Z Time	2	—	2	—	2	—	2	—	ns
tOHZ ⁽²⁾	Output Disable to Output in High-Z Time	—	6	—	7	—	9	—	12	ns

2953 tbl 11

1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

The timing diagram illustrates the relationship between the ADDRESS, OE (Output Enable), and DATAOUT signals. The ADDRESS signal is shown as a bus with a period labeled t_{RC} . The OE signal is an active-low pulse, with its pulse width labeled t_{AA} . The DATAOUT signal is shown as a bus that becomes valid when OE is asserted. The time from the falling edge of OE to the start of DATAOUT validity is labeled $t_{OLZ}^{(3)}$. The time from the start of DATAOUT validity to the rising edge of OE is labeled t_{OE} . The time from the rising edge of OE to the end of DATAOUT validity is labeled $t_{OH}^{(3)}$. The time from the falling edge of OE to the end of DATAOUT validity is labeled t_{OH} . The DATAOUT signal is labeled "DATAOUT VALID" during its active period. The diagram is identified by the number 2953 drw 08.

Timing diagram for a 16-bit parallel data bus. The diagram shows the ADDRESS and DATAout signals over time. The ADDRESS signal is valid for a duration t_{AA} . The DATAout signal is valid for a duration t_{RC} . The time interval t_{OH} is the time from the address becoming invalid to the data becoming invalid. The data bus is shown in two states: "PREVIOUS DATAout VALID" and "DATAout VALID".

2953 drw 09

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Output enable is continuously active, $\overline{OE}$ is LOW.
3. Transition is measured $\pm 200V$ from steady state.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

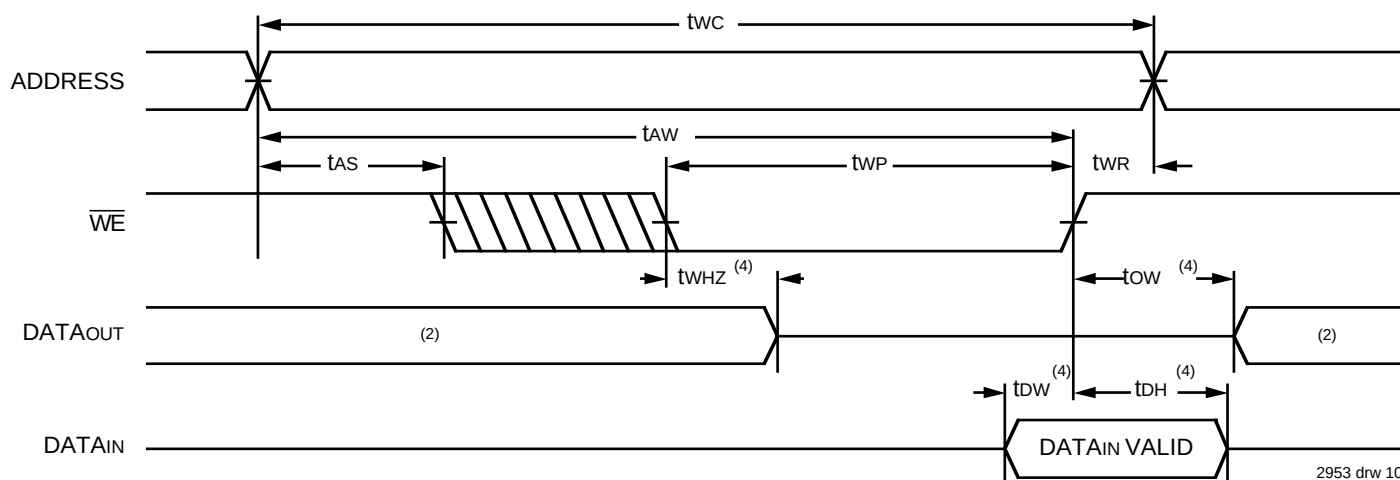
Symbol	Parameter	6178S10 ⁽¹⁾		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	8	—	10	—	12	—	14	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	10	—	12	—	14	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tdW	Data Valid to End-of-Write	6	—	8	—	10	—	12	—	ns
tdH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tWHZ ⁽²⁾	Write Enable to Output in High-Z	—	5	—	6	—	7	—	9	ns
tOW ⁽²⁾	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

NOTES:

2953 tbl 12

1. 0°C to +70°C temperature range only.

2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE^(1,3)

2953 drw 10

NOTES:1. $\overline{WE}$ must be HIGH during all address transitions.

2. During this period, I/O pins are in the output state and the input signals must not be applied.

3. $\overline{OE}$ is HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}.4. Transition is measured $\pm 200mV$ from steady state.**AC ELECTRICAL CHARACTERISTICS** ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

Symbol	Parameter	6178S10 ⁽¹⁾		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clear Cycle										
tCLPW ⁽²⁾	$\overline{\text{CLR}}$ Pulse Width	12	—	15	—	20	—	25	—	ns
tCLRC	$\overline{\text{CLR}}$ HIGH to $\overline{\text{WE}}$ LOW	5	—	5	—	5	—	5	—	ns
tPOCL ⁽³⁾	Power on Reset	50	—	60	—	80	—	100	—	ns
tWECL	$\overline{\text{WE}}$ HIGH to Clear HIGH	5	—	5	—	5	—	5	—	ns

NOTES:

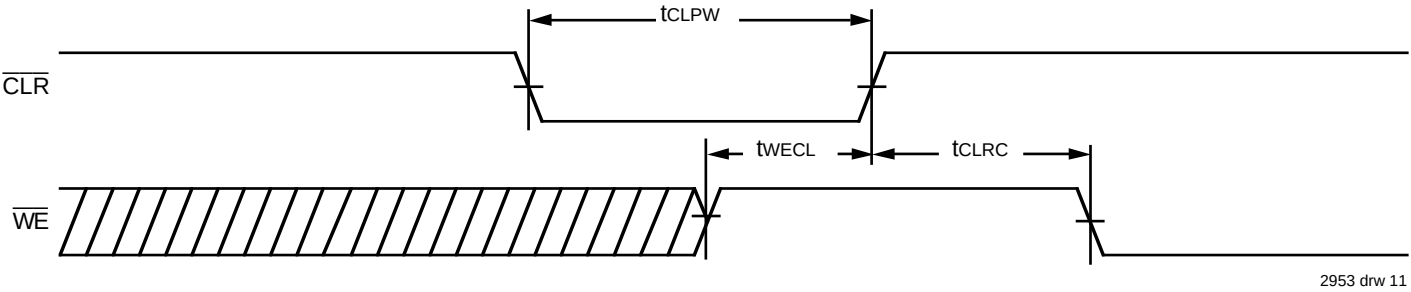
2953 tbl 13

1. 0°C to +70°C temperature range only.

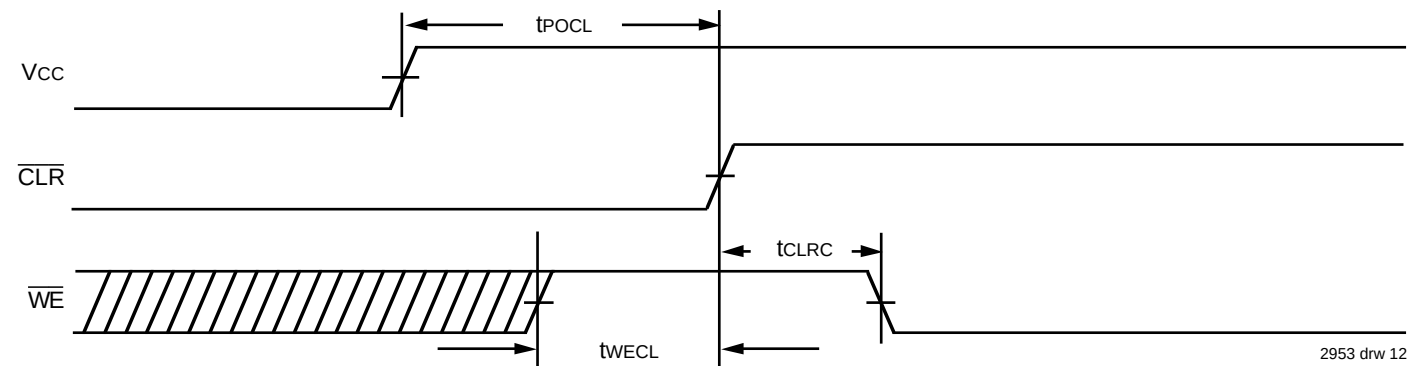
2. Recommended duty cycle of 10% maximum.

3. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF CLEAR CYCLE



POWER ON RESET TIMING



ORDERING INFORMATION

IDT	6178	S	XX	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature	
					Blank B	Commercial (0°C to +70°C) Military (–55°C to +125°C, Compliant to MIL-STD-883, Class B)
					P Y D	300 mil Plastic DIP (P22-1) 300 mil Small Outline, J bend (SO24-4) 300 mil Ceramic DIP (D22-1)
					10 12 15 20 25	Commercial only
						Speed in nanoseconds

2953 drw 13



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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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