BUJ303AD

NPN power transistor

23 July 2018

Product data sheet

1. General description

High voltage, high speed planar passivated NPN power switching transistor in a SOT428 (DPAK) surface mountable plastic package.

2. Features and benefits

- Fast switching
- Low thermal resistance
- Surface mountable package
- Very high voltage capability
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- High frequency electronic lighting ballasts
- Inverters
- Motor control systems

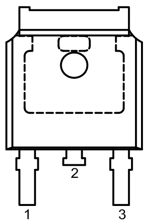
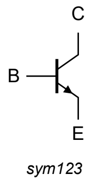
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CM}	peak collector current	Fig. 1; Fig. 2; Fig. 3		-	-	10	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; Fig. 4		-	-	80	W
V_{CESM}	collector-emitter peak voltage	$V_{BE} = 0$ V		-	-	1000	V
Static characteristics							
h_{FE}	DC current gain	$I_C = 5$ mA; $V_{CE} = 5$ V; $T_{mb} = 25$ °C; Fig. 11		10	22	30	
		$I_C = 500$ mA; $V_{CE} = 5$ V; $T_{mb} = 25$ °C; Fig. 11		14	25	35	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 DPAK (SOT428)	
2	C	collector[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package.

6. Ordering information

Table 3. Ordering information

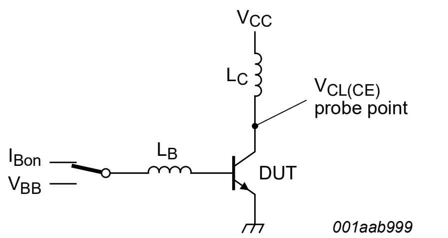
Type number	Package		
	Name	Description	Version
BUJ303AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

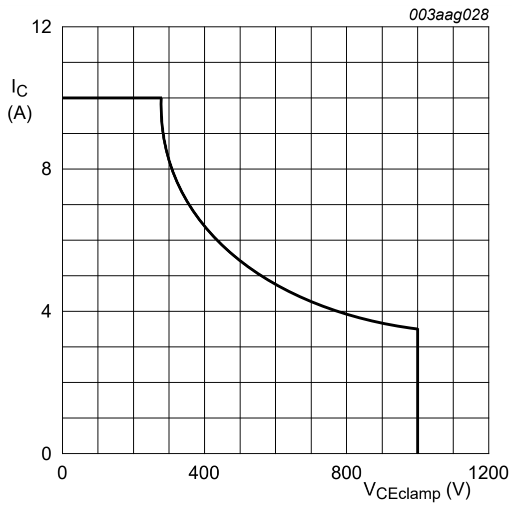
Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	1000	V
V_{CEO}	collector-emitter voltage	I_B = 0 A		-	500	V
I_C	collector current	Fig. 1; Fig. 2; Fig. 3		-	5	A
I_{CM}	peak collector current			-	10	A
I_B	base current			-	2	A
I_{BM}	peak base current			-	4	A
P_{tot}	total power dissipation	$T_{mb} \leq$ 25 °C; Fig. 4		-	80	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C



$V_{CL(CE)} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V;

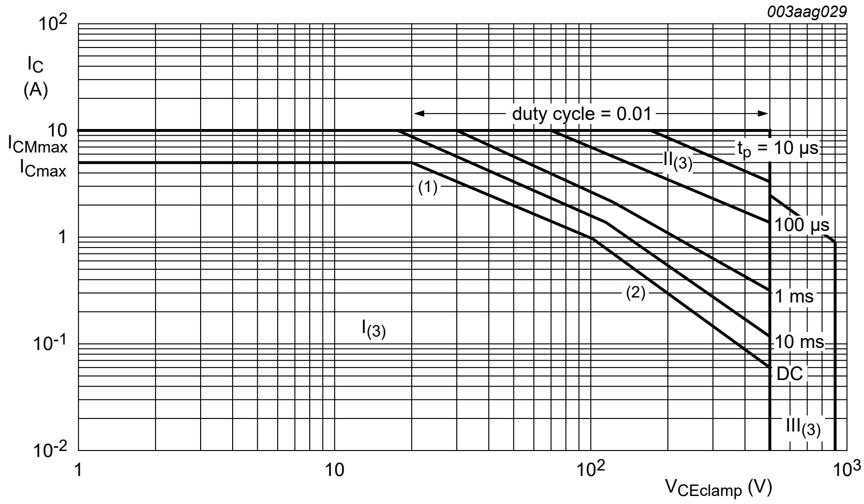
$L_B = 1$ µH; $L_C = 200$ µH

Fig. 1. Test circuit for reverse bias safe operating area



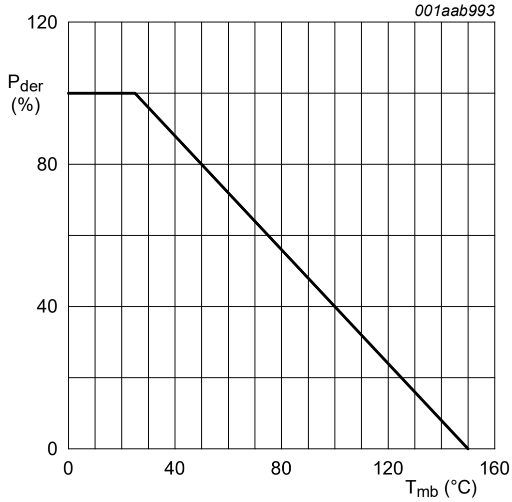
$T_j \leq T_{j(max)}$

Fig. 2. Reverse bias safe operating area



(1) P_{tot} maximum and P_{tot} peak maximum lines.
(2) Second breakdown limits.
(3) I = Region of permissible DC operation.
II = Extension for repetitive pulse operation.
III = Extension during turn-on in single transistor converters provided that $R_{BE} \leq 100\ \Omega$ and $t_p \leq 0.6$ µs.

Fig. 3. Forward bias safe operating area for Tmb ≤ 25 °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 4. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint		-	75	-	K/W

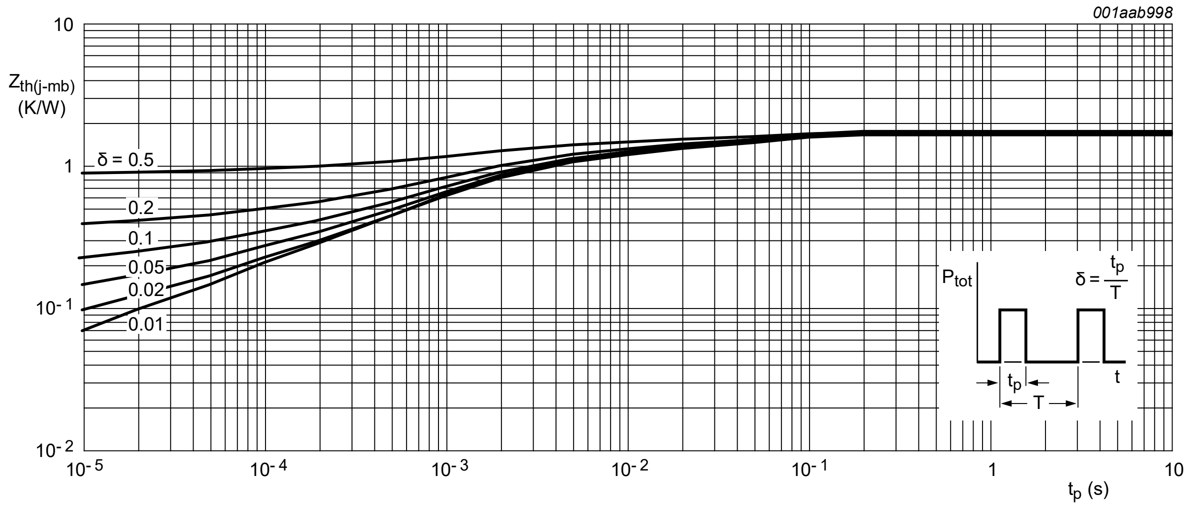


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	V_{BE} = 0 V; V_{CE} = 1000 V	[1]	-	-	1	mA
		V_{BE} = 0 V; V_{CE} = 1000 V; T_j = 125 °C	[1]	-	-	2	mA
I_{CBO}	collector-base cut-off current (emitter open)	V_{CB} = 1000 V; I_E = 0 A; T_{mb} = 25 °C	[1]	-	-	1	mA
I_{CEO}	collector-emitter cut-off current (base open)	V_{CE} = 500 V; I_B = 0 A; T_{mb} = 25 °C	[1]	-	-	0.1	mA
I_{EBO}	emitter-base cut-off current (collector open)	V_{EB} = 9 V; I_C = 0 A; T_{mb} = 25 °C		-	-	0.1	mA
V_{CEOsus}	collector-emitter sustaining voltage (base open)	I_B = 0 A; I_C = 100 mA; L_C = 25 mH; T_{mb} = 25 °C; Fig. 6; Fig. 7		500	-	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; T_{mb} = 25 °C; Fig. 8; Fig. 9		-	0.25	1.5	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3 A; I_B = 0.6 A; T_{mb} = 25 °C; Fig. 10		-	0.97	1.3	V
h_{FE}	DC current gain	I_C = 5 mA; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		10	22	30	
		I_C = 500 mA; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		14	25	35	
h_{FEsat}	DC saturation current gain	I_C = 2.5 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		10	13.5	17	
		I_C = 3 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11		-	12	-	
Dynamic characteristics (switching times - resistive load)							
t_s	storage time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 75 Ω; T_{mb} = 25 °C; Fig. 12; Fig. 13		-	3.4	4	µs
t_f	fall time			-	0.33	0.45	µs
Dynamic characteristics (switching times - inductive load)							
t_s	storage time	I_C = 2.5 A; I_{Bon} = 0.5 A; V_{BB} = -5 V; L_B = 1 µH; T_{mb} = 25 °C; Fig. 14; Fig. 15		-	1.4	1.6	µs
				-	1.7	1.9	µs
t_f	fall time	I_C = 2.5 A; I_{Bon} = 0.5 A; V_{BB} = -5 V; L_B = 1 µH; T_j = 100 °C; Fig. 14; Fig. 15		-	145	160	ns
				-	160	200	ns

[1] Measured with half-sine wave voltage (curve tracer).

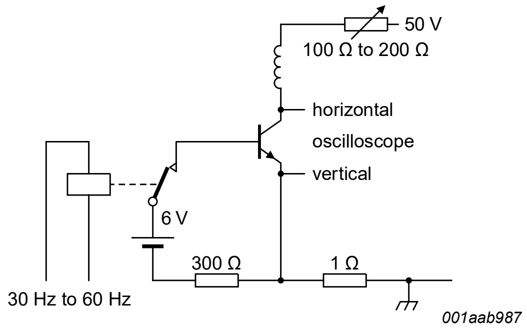


Fig. 6. Test circuit for collector-emitter sustaining voltage

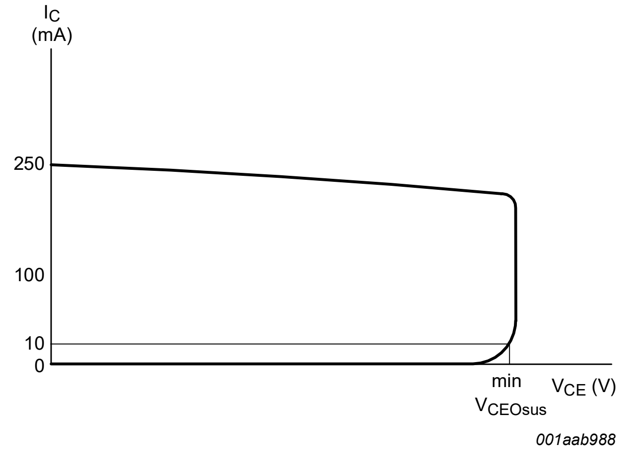


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

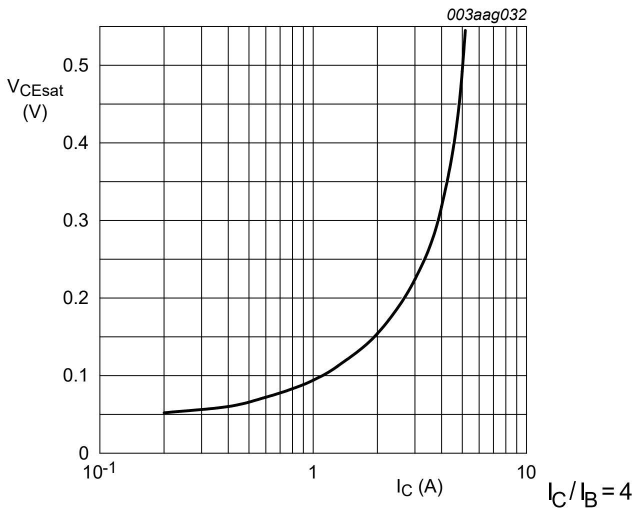


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

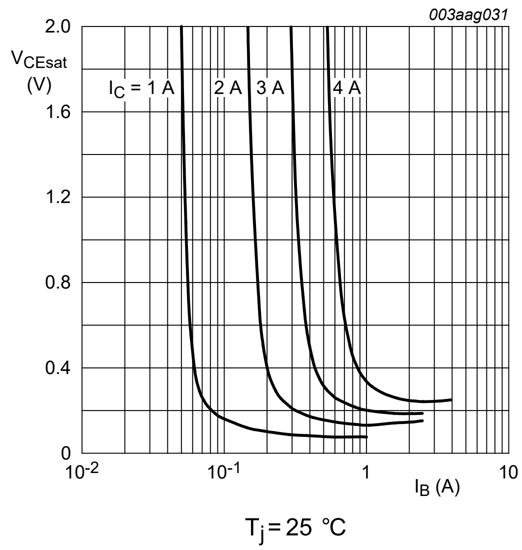
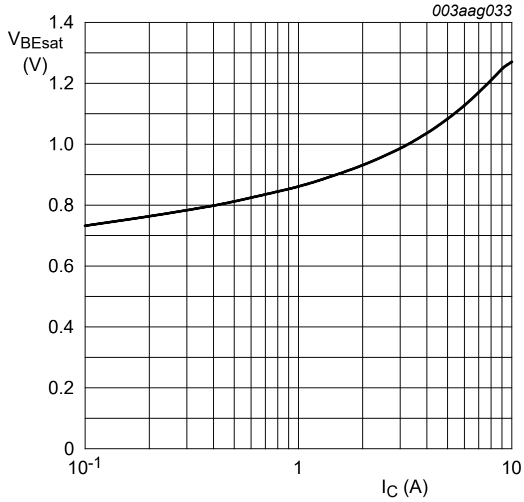
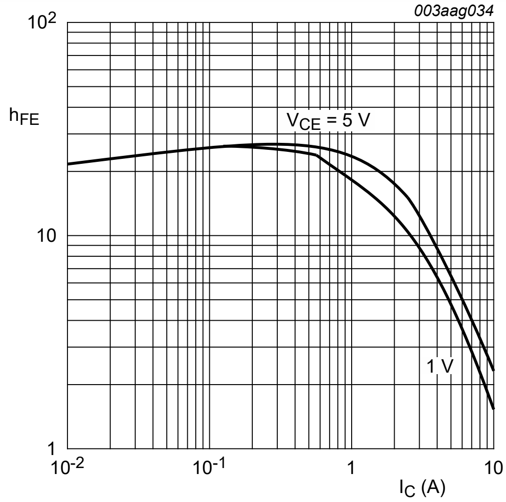


Fig. 9. Collector-emitter saturation voltage as a function of base current; typical values



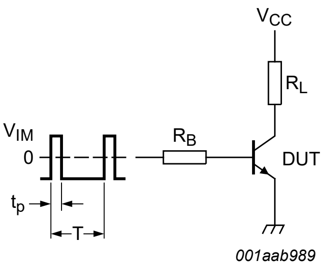
$I_C / I_B = 4$

Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values



$T_j = 25$ °C

Fig. 11. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20$ μs; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 12. Test circuit for resistive load switching

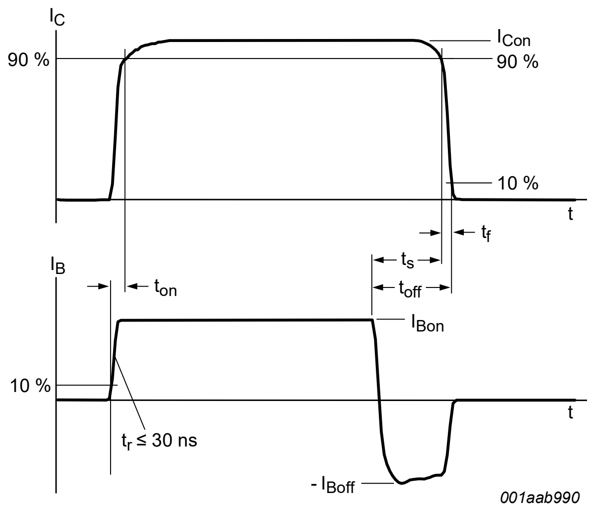
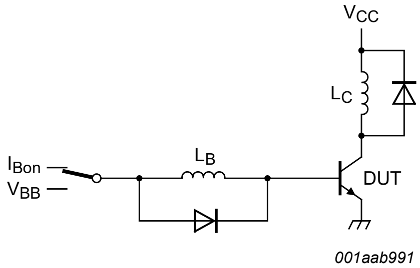


Fig. 13. Switching times waveforms for resistive load



$V_{BB} = -5$ V; $L_C = 200$ μH; $L_B = 1$ μH

Fig. 14. Test circuit for inductive load switching

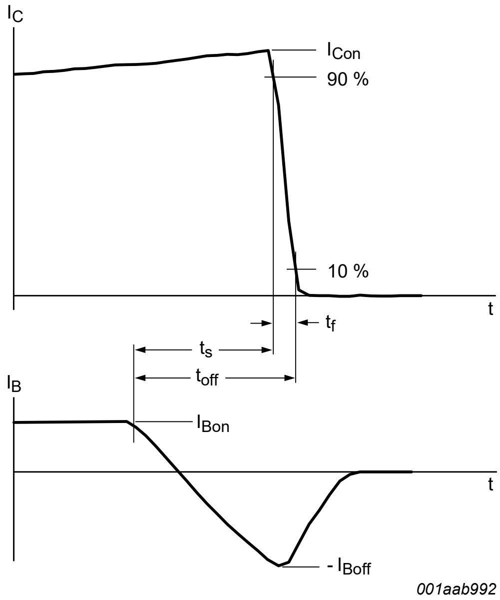
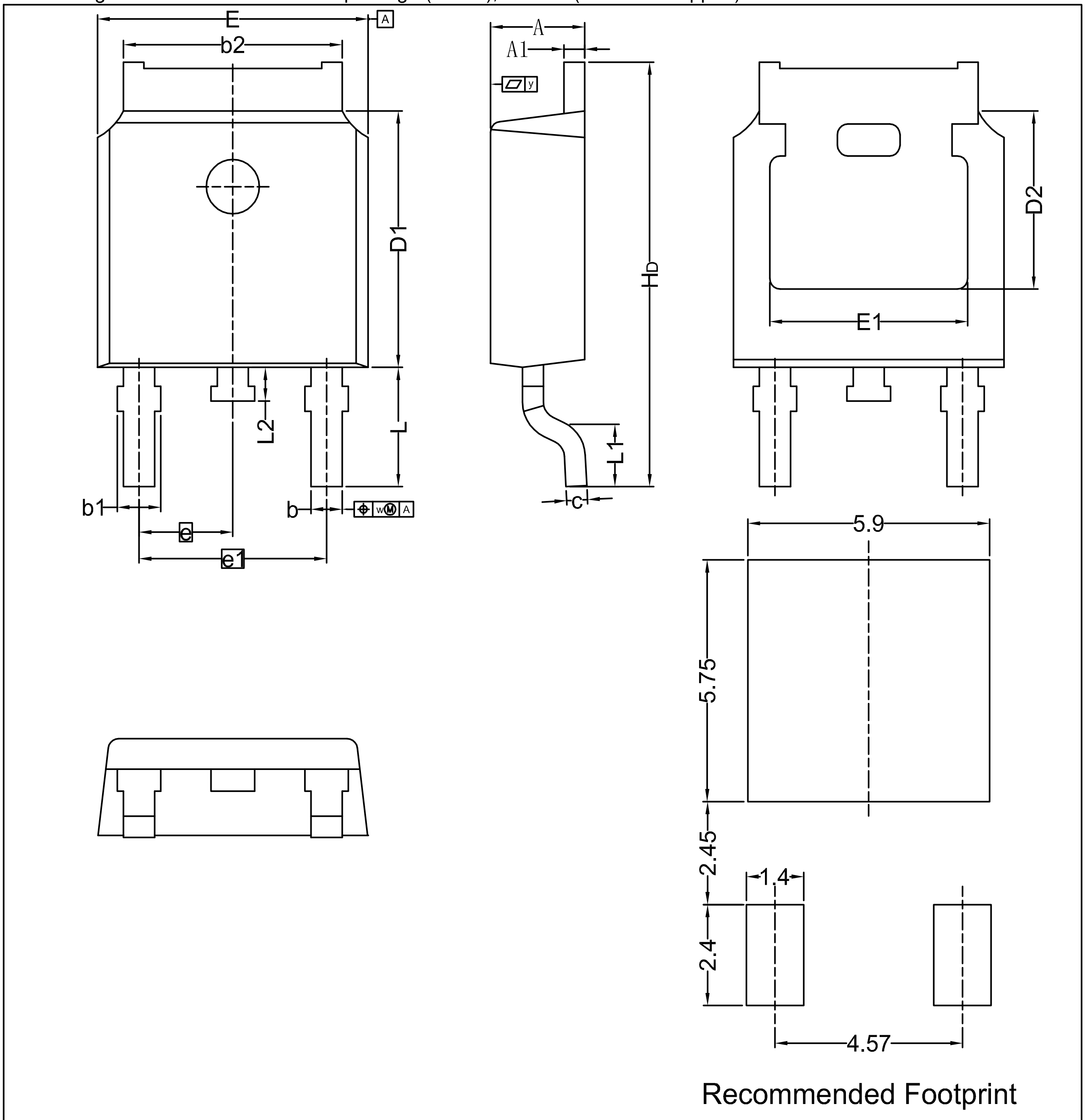


Fig. 15. Switching times waveforms for inductive load

10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) TO252



Unit		A	A1	b	b1	b2	c	D1	D2	E	E1	e	e1	H_D	L	L1	L2	w	y
mm	min	2.22	0.46	0.71	0.72	5.00	0.20	5.98	4.00	6.47	4.45			9.60		0.50	0.50		
	nom											2.285	4.57		2.90 (Ref.)			0.20	
	max	2.38	0.93	0.89	1.10	5.46	0.56	6.22	---	6.73	---			10.40		---	0.90		0.20

Fig. 16. Package outline DPAK (SOT428)

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Document status [1][2]	Product status [3]	Definition
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Date of release: 23 July 2018

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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.