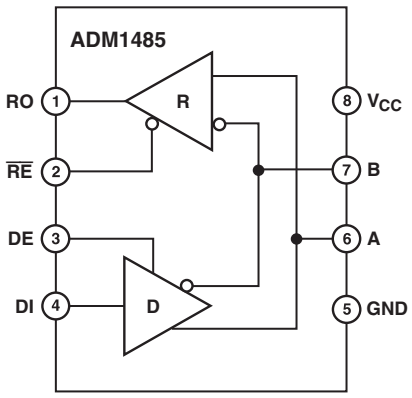
5 V Low Power EIA RS-485 Transceiver

ADM1485

FEATURES
Meets EIA RS-485 Standard
30 Mbps Data Rate
Single 5 V Supply
–7 V to +12 V Bus Common-Mode Range
High Speed, Low Power BiCMOS
Thermal Shutdown Protection
Short-Circuit Protection
Driver Propagation Delay: 10 ns
Receiver Propagation Delay: 15 ns
High-Z Outputs with Power Off
Superior Upgrade for LTC1485

APPLICATIONS
Low Power RS-485 Systems
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM
8-Lead



GENERAL DESCRIPTION

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both RS-485 and RS-422 EIA Standards. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are three-stated.

The ADM1485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down. This minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the entire common-mode voltage range from –7 V to +12 V.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at typical data rates of 30 Mbps while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in PDIP, SOIC, and small MSOP packages.

REV. F

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ADM1485–SPECIFICATIONS (V_{CC} = 5 V ± 5%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	R = ∞, Test Circuit 1
	2.0		5.0	V	V_{CC} = 5 V, R = 50 Ω (RS-422), Test Circuit 1
	1.5		5.0	V	R = 27 Ω (RS-485), Test Circuit 1
V_{OD3}	1.5		5.0	V	V_{TST} = –7 V to +12 V, Test Circuit 2
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Test Circuit 1
Common-Mode Output Voltage V_{OC}			3	V	R = 27 Ω or 50 Ω, Test Circuit 1
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short-Circuit Current (V_{OUT} = High)	35		250	mA	–7 V ≤ V_O ≤ +12 V
Output Short-Circuit Current (V_{OUT} = Low)	35		250	mA	–7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			±1.0	µA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	–0.2		+0.2	V	–7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	–7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			1	mA	V_{IN} = +12 V
			–0.8	mA	V_{IN} = –7 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Enable Input Current ($\overline{RE}$)			±1	µA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = –4.0 mA
Short-Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±1.0	µA	0.4 V ≤ V_{OUT} ≤ 2.4 V
POWER SUPPLY CURRENT					
I_{CC} (Outputs Enabled)		1.0	2.2	mA	Digital Inputs = GND or V_{CC}
I_{CC} (Outputs Disabled)		0.6	1	mA	Digital Inputs = GND or V_{CC}

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = 5 V ± 5%. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output t_{PLH}, t_{PHL}	2	10	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, Test Circuit 3
Driver O/P to $\overline{O/P}$ t_{SKEW}		1	5	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, Test Circuit 3
Driver Rise/Fall Time t_R, t_F		8	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, Test Circuit 3
Driver Enable to Output Valid		10	25	ns	R_L = 110 Ω, C_L = 50 pF, Test Circuit 4
Driver Disable Timing		10	25	ns	R_L = 110 Ω, C_L = 50 pF, Test Circuit 4
Matched Enable Switching $\|t_{AZH}-t_{BZL}\|$, $\|t_{BZH}-t_{AZL}\|$		0	2	ns	R_L = 110 Ω, C_L = 50 pF, Test Circuit 4*
Matched Disable Switching $\|t_{AHZ}-t_{BLZ}\|$, $\|t_{BHZ}-t_{ALZ}\|$		0	2	ns	R_L = 110 Ω, C_L = 50 pF, Test Circuit 4*
RECEIVER					
Propagation Delay Input to Output t_{PLH}, t_{PHL}	8	15	30	ns	C_L = 15 pF, Test Circuit 5
Skew $\|t_{PLH}-t_{PHL}\|$			5	ns	C_L = 15 pF, Test Circuit 5
Receiver Enable t_{EN1}		5	20	ns	C_L = 15 pF, R_L = 1 kΩ, Test Circuit 6
Receiver Disable t_{EN2}		5	20	ns	C_L = 15 pF, R_L = 1 kΩ, Test Circuit 6
Tx Pulse Width Distortion		1		ns	
Rx Pulse Width Distortion		1		ns	

*Guaranteed by characterization.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{CC} . . . . . –0.3 V to +7 V
Inputs
Driver Input (DI) . . . . . –0.3 V to V_{CC} + 0.3 V
Control Inputs (DE, $\overline{RE}$) . . . . . –0.3 V to V_{CC} + 0.3 V
Receiver Inputs (A, B) . . . . . –9 V to +14 V
Outputs
Driver Outputs (A, B) . . . . . –9 V to +14 V
Receiver Output . . . . . –0.5 V to V_{CC} + 0.5 V
Power Dissipation 8-Lead MSOP . . . . . 900 mW
θ_{JA}, Thermal Impedance . . . . . 206°C/W
Power Dissipation 8-Lead PDIP . . . . . 500 mW
θ_{JA}, Thermal Impedance . . . . . 130°C/W
Power Dissipation 8-Lead SOIC . . . . . 450 mW
θ_{JA}, Thermal Impedance . . . . . 170°C/W
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to 70°C
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

Inputs		Outputs	
DE	**DI**	**B**	**A**
1	1	0	1
1	0	1	0
0	X	Z	Z

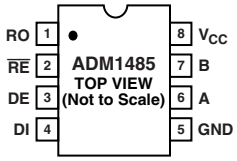
Table II. Receiving

$\overline{RE}$	Inputs A-B	Outputs RO
0	≥ +0.2 V	1
0	≤ –0.2 V	0
0	Inputs Open	1
1	X	Z

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	RO	Receiver Output. When enabled if A > B by 200 mV, then RO = High. If A < B by 200 mV, then RO = Low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.
5	GND	Ground Connection, 0 V.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B
8	V_{CC}	Power Supply, 5 V ± 5%.

PIN CONFIGURATION

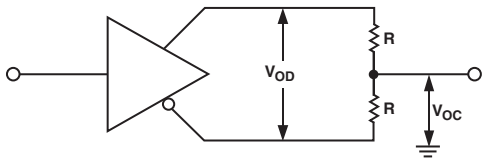


CAUTION

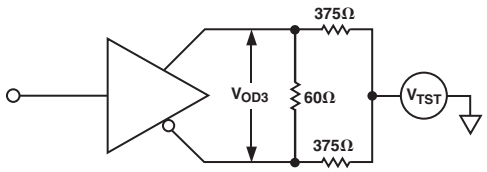
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



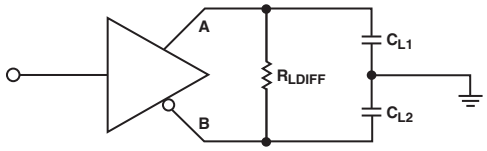
Test Circuits



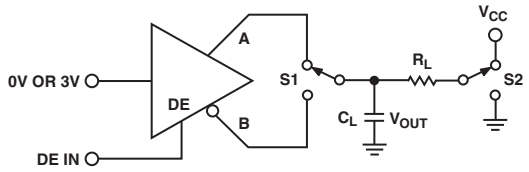
Test Circuit 1. Driver Voltage Measurement



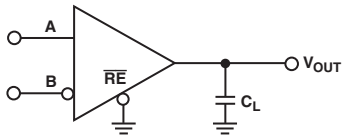
Test Circuit 2. Driver Voltage Measurement



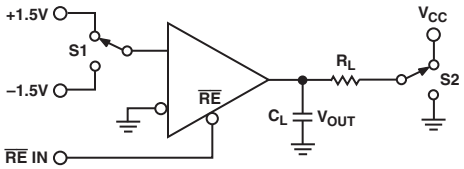
Test Circuit 3. Driver Propagation Delay



Test Circuit 4. Driver Enable/Disable



Test Circuit 5. Receiver Propagation Delay



Test Circuit 6. Receiver Enable/Disable

Switching Characteristics

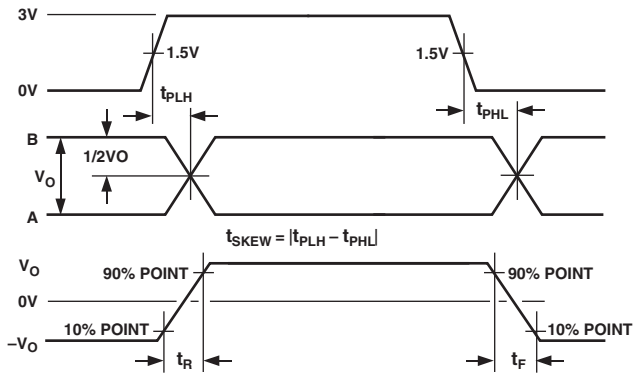


Figure 1. Driver Propagation Delay, Rise/Fall Timing

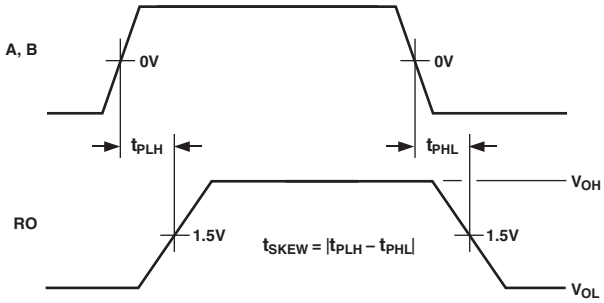


Figure 3. Receiver Propagation Delay

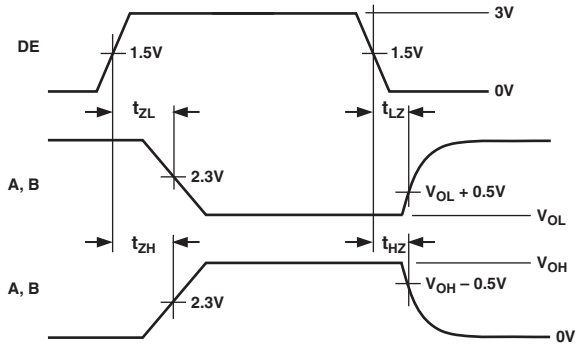


Figure 2. Driver Enable/Disable Timing

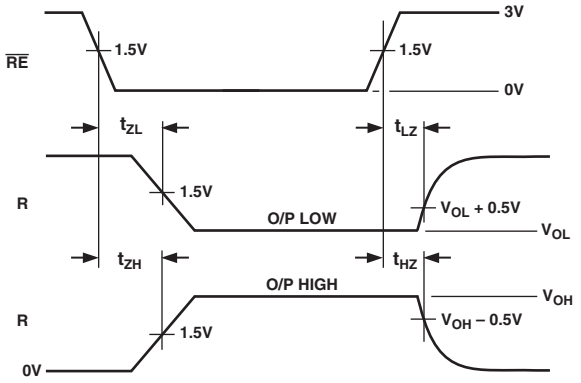
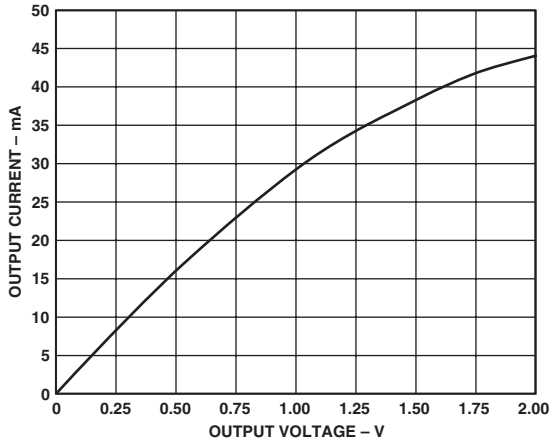
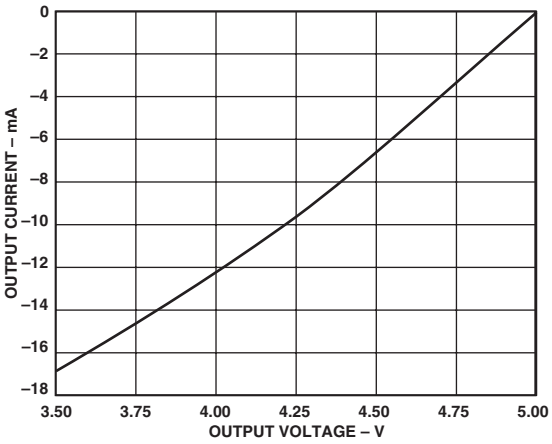


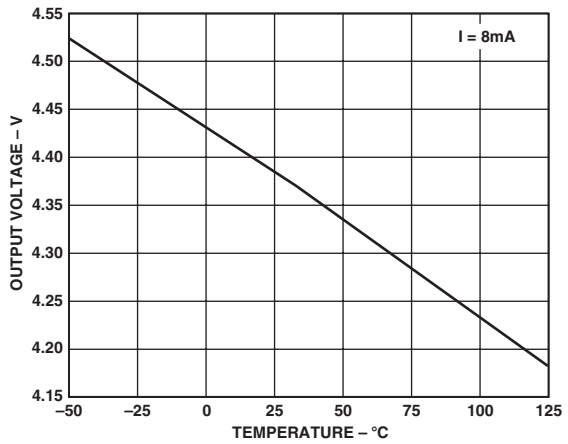
Figure 4. Receiver Enable/Disable Timing



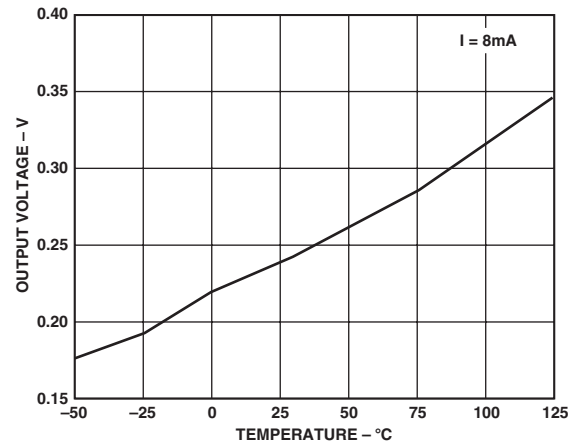
TPC 1. Output Current vs. Receiver Output Low Voltage



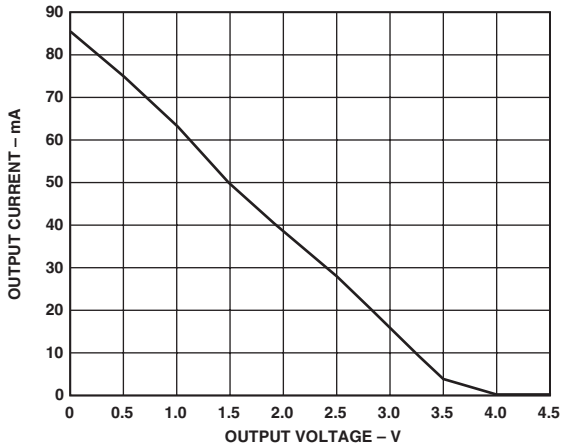
TPC 2. Output Current vs. Receiver Output High Voltage



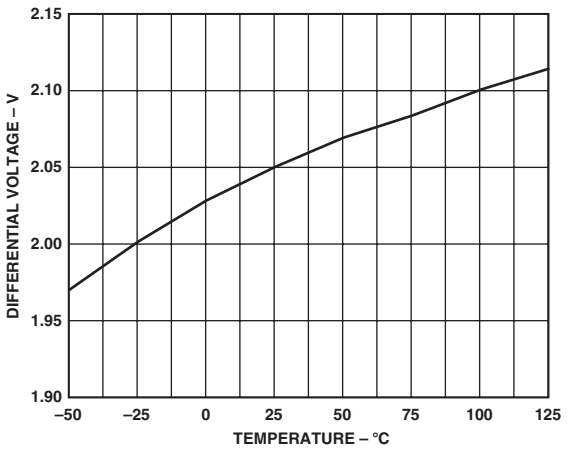
TPC 3. Receiver Output High Voltage vs. Temperature



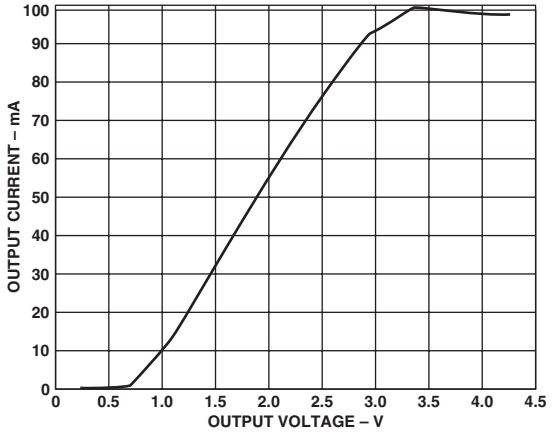
TPC 4. Receiver Output Low Voltage vs. Temperature



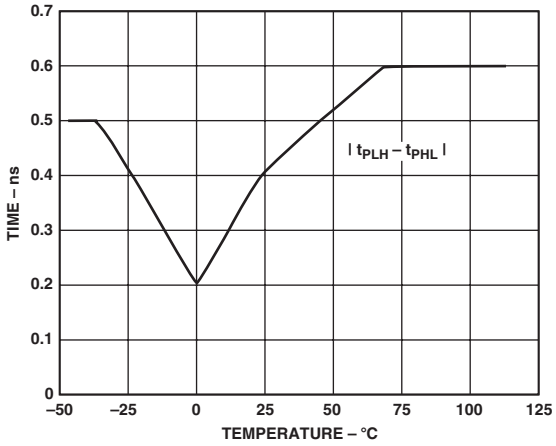
TPC 5. Output Current vs. Driver Differential Output Voltage



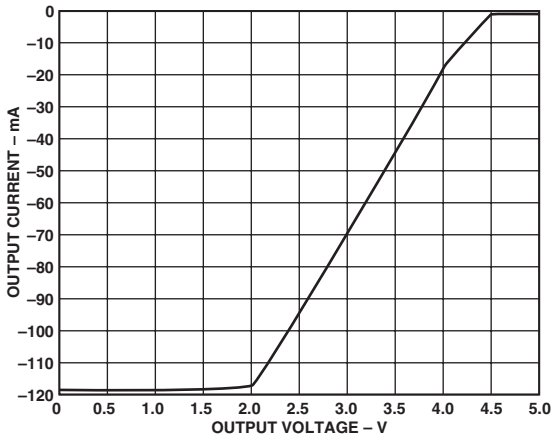
TPC 6. Driver Differential Output Voltage vs. Temperature, R_L = 26.8 Ω



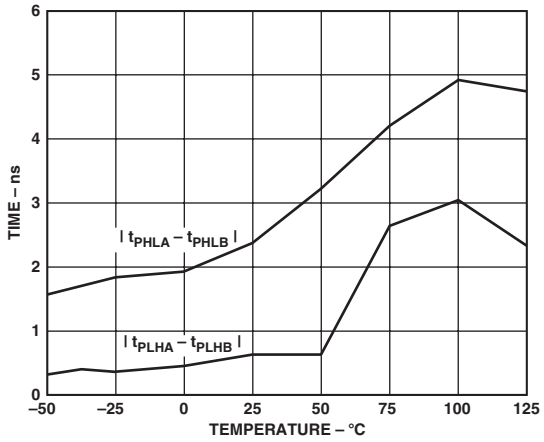
TPC 7. Output Current vs. Driver Output Low Voltage



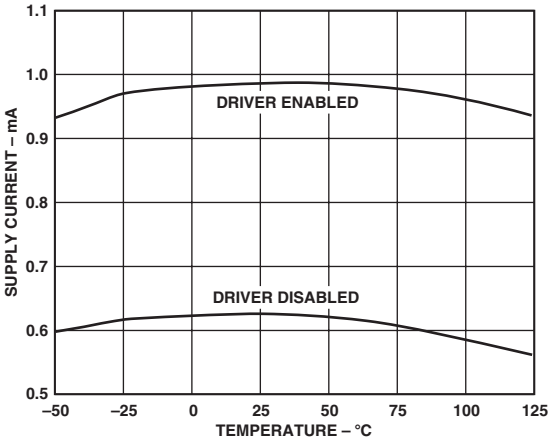
TPC 10. Rx Skew vs. Temperature



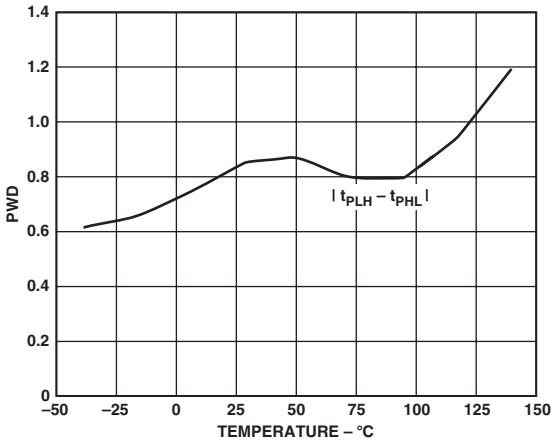
TPC 8. Output Current vs. Driver Output High Voltage



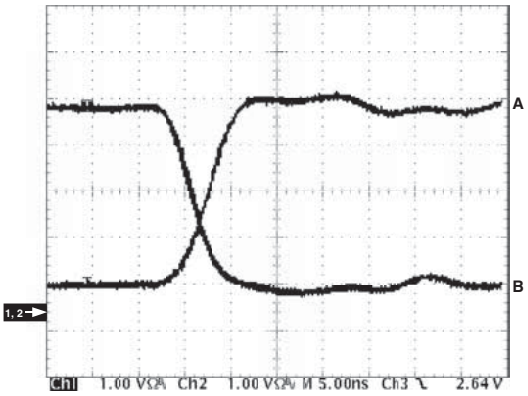
TPC 11. Tx Skew vs. Temperature



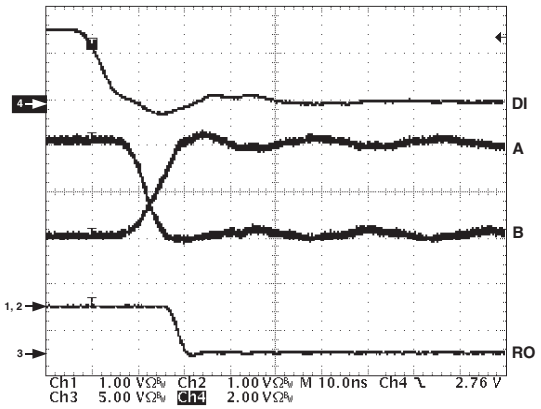
TPC 9. Supply Current vs. Temperature



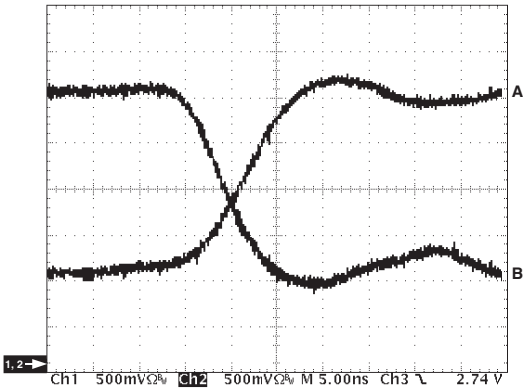
TPC 12. Tx Pulse Width Distortion



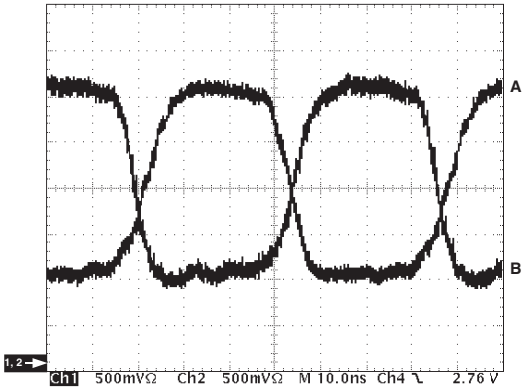
TPC 13. Unloaded Driver Differential Outputs



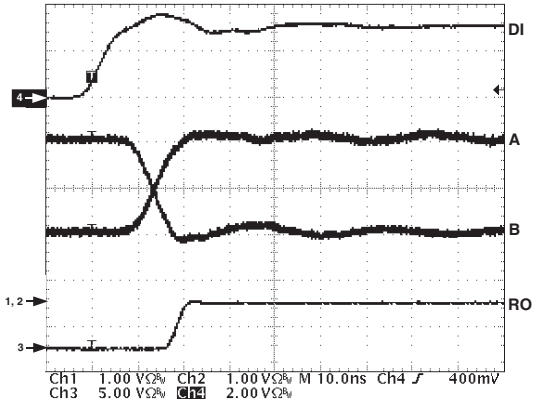
TPC 16. Driver/Receiver Propagation Delays High to Low



TPC 14. Loaded Driver Differential Outputs



TPC 17. Driver Output at 30 Mbps



TPC 15. Driver/Receiver Propagation Delays Low to High

APPLICATION INFORMATION

Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) that specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

In order to cater to true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of the RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of –7 V to +12 V is defined. The most significant difference between the RS-422 and the RS-485 is the fact that the drivers may be disabled, thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Table III. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	–7 V to +7 V	–7 V to +12 V
No. of Drivers/Receivers per Line	1/10	32/32

Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM1485 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 5. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

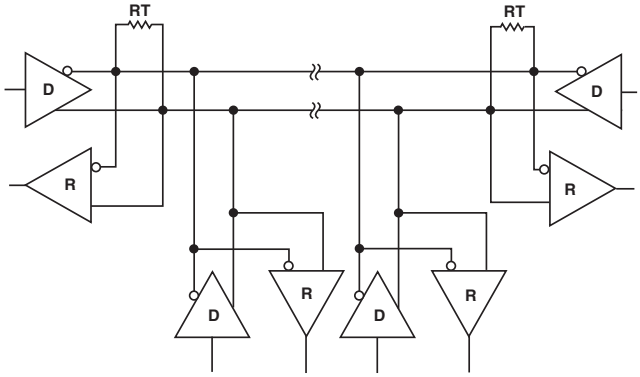


Figure 5. Typical RS-485 Network

Thermal Shutdown

The ADM1485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C.

Propagation Delay

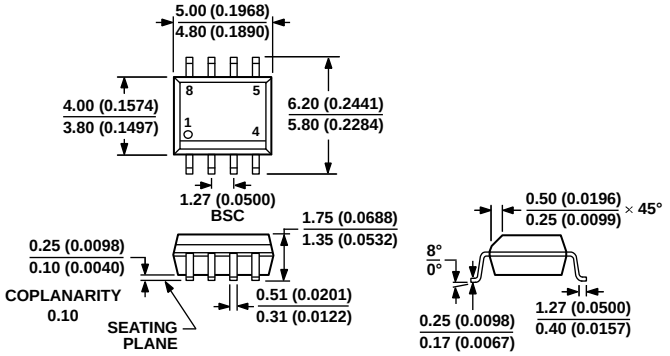
The ADM1485 features very low propagation delay, ensuring maximum baud rate operation. The driver is well balanced, ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

Receiver Open-Circuit Fail-Safe

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

OUTLINE DIMENSIONS

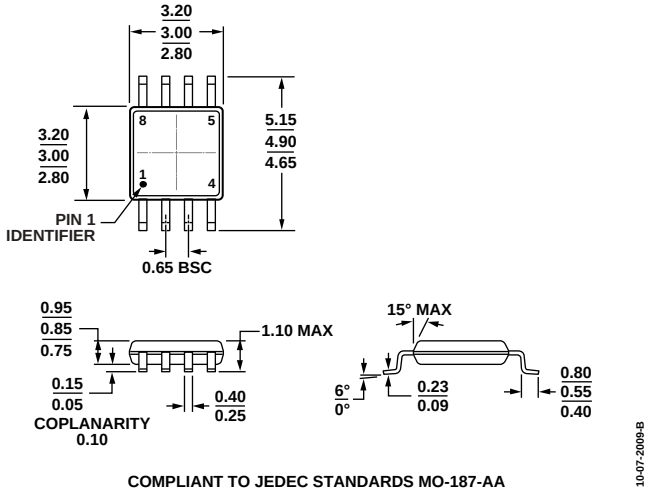


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CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 6. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 7. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

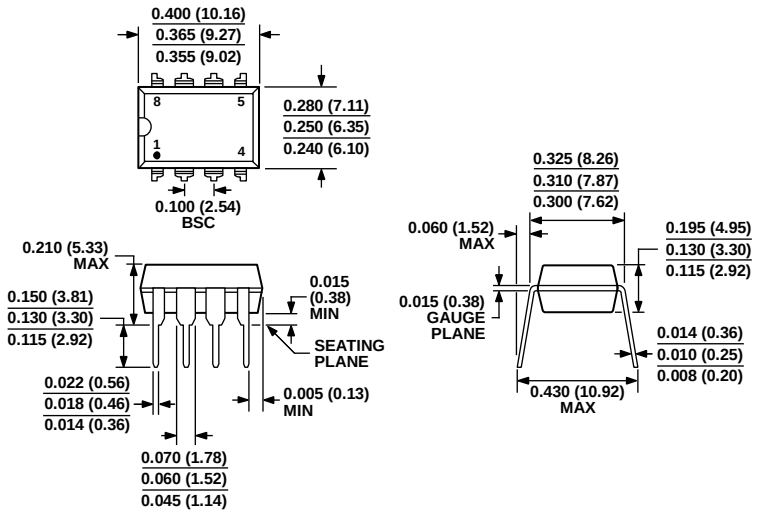


Figure 8. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Brand
ADM1485JNZ	0°C to 70°C	8-Lead PDIP	N-8	
ADM1485JRZ	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM1485JR-REEL	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM1485JRZ-REEL	0°C to 70°C	8-Lead SOIC_N	R-8	
ADM1485ANZ	−40°C to +85°C	8-Lead PDIP	N-8	
ADM1485ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	M42
ADM1485ARMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	M42
ADM1485ARMZ-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	M42
ADM1485ARZ		8-Lead SOIC_N	R-8	
ADM1485ARZ-REEL		8-Lead SOIC_N	R-8	
ADM1485ARZ-REEL7		8-Lead SOIC_N	R-8	
ADM1485JCHIPS			Die	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

8/12—Rev. E to Rev. F

Changed Data Rates of Up to 5 Mbps to Typical Data Rates of 30 Mbps....1
Updated Outline Dimensions....9
Changes to Ordering Guide....10

9/03—Data Sheet changed from REV. D to REV. E.

Change to SPECIFICATIONS....2
Changes to ORDERING GUIDE....3
Updated OUTLINE DIMENSIONS....9

7/03—Data Sheet changed from REV. C to REV. D.

Changes to SPECIFICATIONS....2
Changes to ABSOLUTE MAXIMUM RATINGS....3
Updated ORDERING GUIDE....3

1/03—Data Sheet changed from REV. B to REV. C.

Change to SPECIFICATIONS....2
Change to ORDERING GUIDE....3

12/02—Data Sheet changed from REV. A to REV. B.

Deleted Q-8 Package....Universal
Edits to FEATURES....1
Edits to GENERAL DESCRIPTION....1
Edits, additions to SPECIFICATIONS....2
Edits, additions to ABSOLUTE MAXIMUM RATINGS....3
Additions to ORDERING GUIDE....3
TPCs updated and reformatted....5
Addition of 8-Lead MSOP Package....9
Update to OUTLINE DIMENSIONS....9

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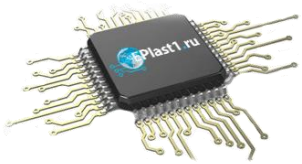
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