

# PBSS4021SP

# 20 V, 6.3 A PNP/PNP low V<sub>CEsat</sub> (BISS) transistor Rev. 2 — 11 October 2010 Pro

Product data sheet

#### 1. **Product profile**

### 1.1 General description

PNP/PNP low V<sub>CEsat</sub> Breakthrough In Small Signal (BISS) transistor in a SOT96-1 (SO8) medium power Surface-Mounted Device (SMD) plastic package.

Table 1. **Product overview** 

Type number	Package		NPN/NPN	NPN/PNP
	Nexperia	Name	complement	complement
PBSS4021SP	SOT96-1	SO8	PBSS4021SN	PBSS4021SPN

### 1.2 Features and benefits

- Low collector-emitter saturation voltage V<sub>CEsat</sub>
- High collector current capability I<sub>C</sub> and I<sub>CM</sub>
- High collector current gain (h<sub>FF</sub>) at high I<sub>C</sub>
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

### 1.3 Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

#### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{\text{CEO}}$	collector-emitter voltage	open base	-	-	-20	V
I <sub>C</sub>	collector current		-	-	-6.3	Α
I <sub>CM</sub>	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-	-15	Α
R <sub>CEsat</sub>	collector-emitter saturation resistance	$I_C = -5 \text{ A}; I_B = -0.5 \text{ A}$	-	36	54	mΩ

<sup>[1]</sup> Pulse test:  $t_p \le 300 \ \mu s; \ \delta \le 0.02.$ 



# 2. Pinning information

Table 3. Pinning

	3		
Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		
2	base TR1	8	8 7 6 5
3	emitter TR2		TR1 L TR2 L
4	base TR2		
5	collector TR2	1 H H H 4	1 2 3 4
6	collector TR2		006aaa976
7	collector TR1		
8	collector TR1		

# 3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4021SP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

# 4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4021SP	4021SP

# 5. Limiting values

Table 6. Limiting values

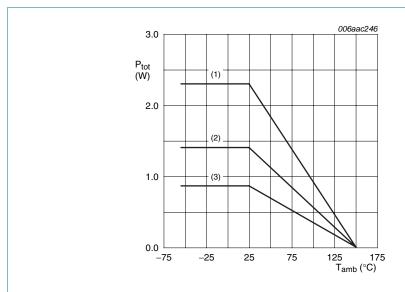
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transis	stor				
$V_{CBO}$	collector-base voltage	open emitter	-	-20	V
$V_{CEO}$	collector-emitter voltage	open base	-	-20	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	<b>-5</b>	V
I <sub>C</sub>	collector current		-	-6.3	Α
I <sub>CM</sub>	peak collector current	single pulse; $t_p \le 1$ ms	-	-15	Α
I <sub>B</sub>	base current		-	-1	Α
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$	[1] -	0.73	W
			[2] -	1	W
			[3]	1.7	W

**Table 6.** Limiting values ...continued
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
P <sub>tot</sub>	total power dissipation	$T_{amb} \le 25  ^{\circ}C$	[1] _	0.86	W
			[2] -	1.4	W
			[3] _	2.3	W
Tj	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-55	+150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.



- (1) Ceramic PCB,  $Al_2O_3$ , standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>
- (3) FR4 PCB, standard footprint

Fig 1. Per device: Power derating curves

### 6. Thermal characteristics

Table 7. Thermal characteristics

Table 1.	Thermal Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Per trans	istor					
R <sub>th(j-a)</sub>	-(11()-a)	in free air	<u>[1]</u> _	-	170	K/W
	[2] _	-	125	K/W		
			[3]	-	75	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W
Per devic	e					
R <sub>th(j-a)</sub>	thermal resistance from	in free air	<u>[1]</u> -	-	145	K/W
	junction to ambient		[2] _	-	90	K/W
			[3] _	-	55	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

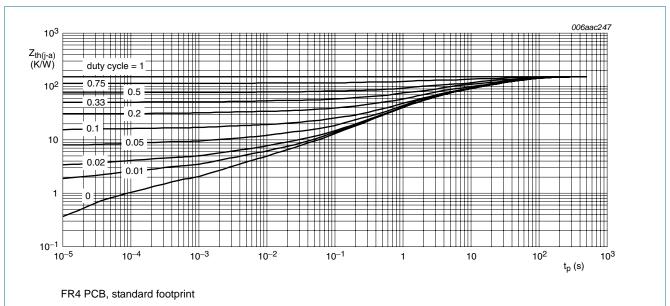
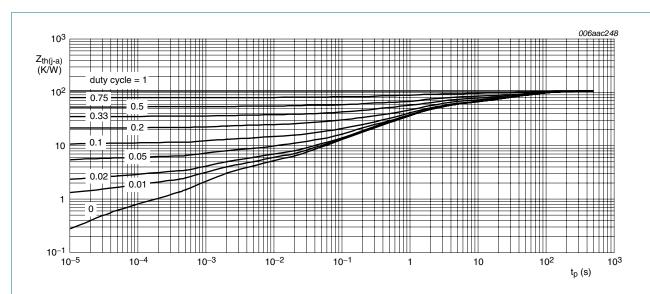
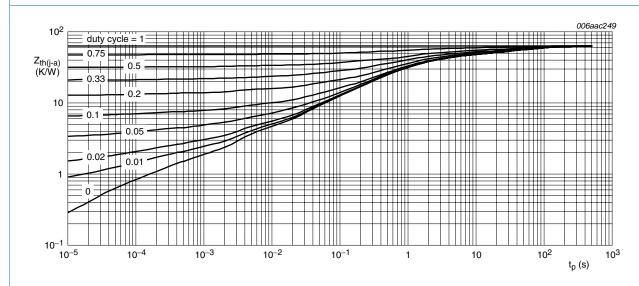


Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

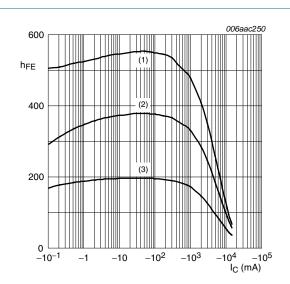
### 7. Characteristics

Table 8. Characteristics

 $T_{amb} = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per tran	sistor						
I <sub>CBO</sub>	collector-base	$V_{CB} = -20 \text{ V}; I_E = 0 \text{ A}$		-	-	-100	nΑ
	cut-off current	$V_{CB} = -20 \text{ V}; I_E = 0 \text{ A};$ $T_j = 150 \text{ °C}$		-	-	-50	μА
I <sub>CES</sub>	collector-emitter cut-off current	$V_{CE} = -16 \text{ V}; V_{BE} = 0 \text{ V}$		-	-	-100	nA
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = -5 \text{ V}; I_C = 0 \text{ A}$		-	-	-100	nA
h <sub>FE</sub>	DC current gain	$V_{CE} = -2 \text{ V}$	[1]				
		$I_C = -500 \text{ mA}$		250	400	-	
		I <sub>C</sub> = -1 A		250	400	-	
		I <sub>C</sub> = −2 A		200	350	-	
	I <sub>C</sub> = -4 A		150	300	-		
		$I_C = -7 \text{ A}$		80	200	-	
$V_{CEsat}$	collector-emitter		[1]				
	saturation voltage	$I_C = -1 \text{ A}; I_B = -50 \text{ mA}$		-	-45	-68	mV
	$I_C = -1 \text{ A}; I_B = -10 \text{ mA}$		-	-70	-115	mV	
	$I_C = -2 \text{ A}; I_B = -40 \text{ mA}$		-	-100	-150	mV	
		$I_C = -4 \text{ A}; I_B = -200 \text{ mA}$		-	-150	-225	mV
		$I_C = -4 \text{ A}; I_B = -40 \text{ mA}$		-	-250	-375	mV
		$I_C = -6.5 \text{ A}; I_B = -325 \text{ mA}$		-	-235	-350	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	$I_C = -5 \text{ A}; I_B = -500 \text{ mA}$	[1]	-	36	54	mΩ
$V_{BEsat}$	base-emitter		[1]				
	saturation voltage	$I_C = -1 \text{ A}; I_B = -100 \text{ mA}$		-	-0.85	-1	V
		$I_C = -4 \text{ A}; I_B = -400 \text{ mA}$		-	-1	-1.2	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2 \text{ V}; I_{C} = -2 \text{ A}$	<u>[1]</u>	-	-0.76	-0.85	V
t <sub>d</sub>	delay time	$V_{CC} = -12.5 \text{ V}; I_C = -1 \text{ A};$		-	40	-	ns
t <sub>r</sub>	rise time	$I_{Bon} = -0.05 \text{ A}; I_{Boff} = 0.05 \text{ A}$		-	55	-	ns
t <sub>on</sub>	turn-on time			-	95	-	ns
ts	storage time			-	340	-	ns
t <sub>f</sub>	fall time			-	85	-	ns
t <sub>off</sub>	turn-off time			-	425	-	ns
f <sub>T</sub>	transition frequency	$V_{CE} = -10 \text{ V}; I_{C} = -100 \text{ mA};$ f = 100 MHz		-	105	-	MHz
C <sub>c</sub>	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz		-	95	-	pF

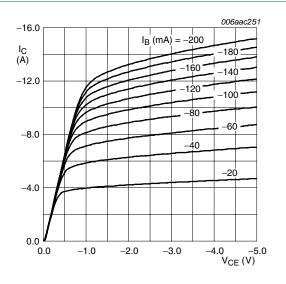
<sup>[1]</sup> Pulse test:  $t_p \le 300 \ \mu s; \ \delta \le 0.02.$ 



 $V_{CE} = -2 V$ 

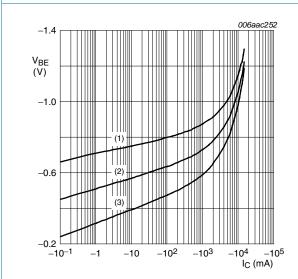
- (1)  $T_{amb} = 100 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = -55 \, ^{\circ}C$

Fig 5. DC current gain as a function of collector current; typical values



T<sub>amb</sub> = 25 °C

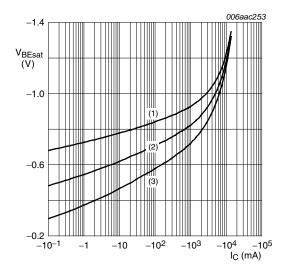
Fig 6. Collector current as a function of collector-emitter voltage; typical values



 $V_{CE} = -2 \text{ V}$ 

- (1)  $T_{amb} = -55 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

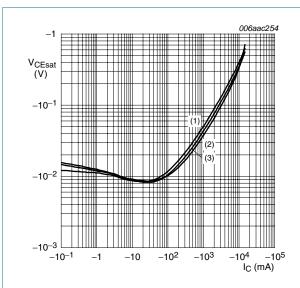
Fig 7. Base-emitter voltage as a function of collector current; typical values



 $I_C/I_B = 20$ 

- (1)  $T_{amb} = -55 \, ^{\circ}C$
- (2)  $T_{amb} = 25 \, ^{\circ}C$
- (3)  $T_{amb} = 100 \, ^{\circ}C$

Fig 8. Base-emitter saturation voltage as a function of collector current; typical values



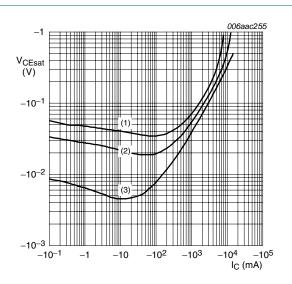
$$I_{\rm C}/I_{\rm B} = 20$$

(1) 
$$T_{amb} = 100 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3) 
$$T_{amb} = -55 \, ^{\circ}C$$

Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values

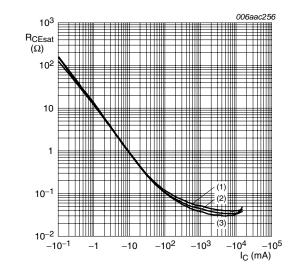


(1) 
$$I_C/I_B = 100$$

(2) 
$$I_C/I_B = 50$$

(3) 
$$I_C/I_B = 10$$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



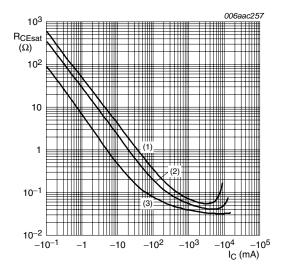
$$I_{\rm C}/I_{\rm B} = 20$$

(1) 
$$T_{amb} = 100 \, ^{\circ}C$$

(2) 
$$T_{amb} = 25 \, ^{\circ}C$$

(3)  $T_{amb} = -55 \, ^{\circ}C$ 

Fig 11. Collector-emitter saturation resistance as a function of collector current; typical values



$$T_{amb} = 25 \, ^{\circ}C$$

(1) 
$$I_C/I_B = 100$$

(2) 
$$I_C/I_B = 50$$

(3) 
$$I_C/I_B = 10$$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values

### 8. Test information

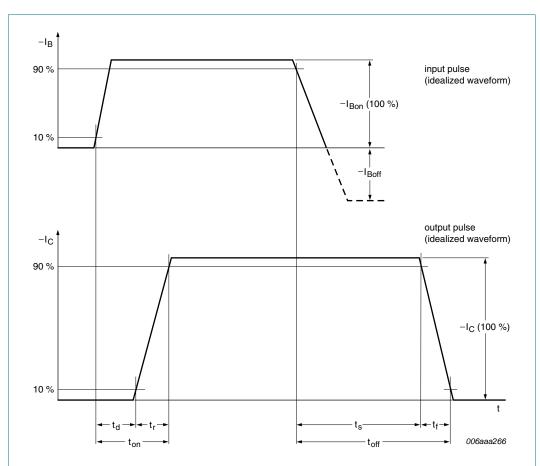


Fig 13. BISS transistor switching time definition

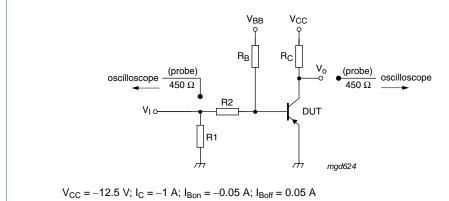
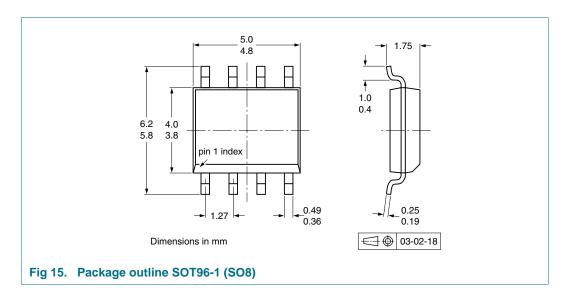


Fig 14. Test circuit for switching times

# 9. Package outline



# 10. Packing information

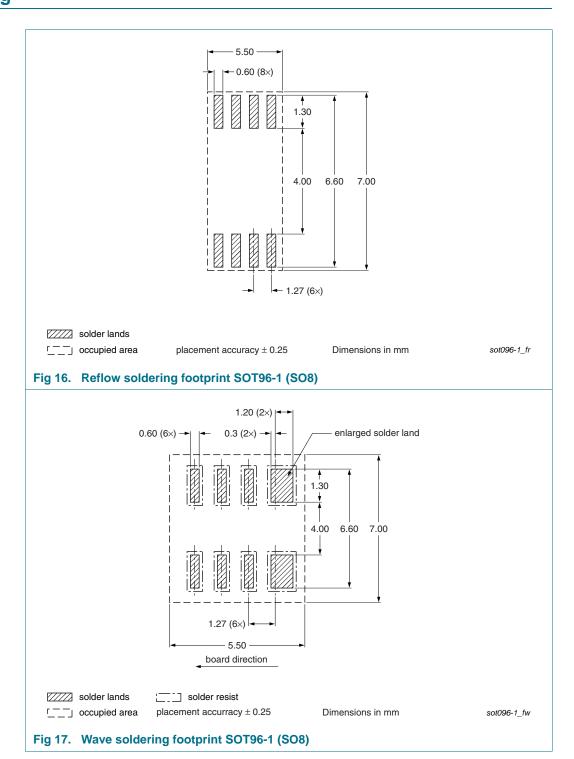
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing	quantity
			1000	2500
PBSS4021SP	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

<sup>[1]</sup> For further information and the availability of packing methods, see Section 14.

# 11. Soldering



PBSS4021SP

20 V, 6.3 A PNP/PNP low V<sub>CEsat</sub> (BISS) transistor

# 12. Revision history

### Table 10. Revision history

**Nexperia** 

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4021SP v.2	20101011	Product data sheet	-	PBSS4021SP v.1
Modifications:	• Figure 1 "Pe	er device: Power derating o	urves": updated.	
PBSS4021SP v.1	20100714	Product data sheet	-	-

### 13. Legal information

#### 13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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Nexperia PBSS4021SP

20 V, 6.3 A PNP/PNP low V<sub>CEsat</sub> (BISS) transistor

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

### 13.4 Trademarks

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**PBSS4021SP** 

### **Nexperia**

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### 15. Contents

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