Micron Parallel NOR Flash Embedded Memory (P30-65nm)

JS28F256P30B/TFx, RC28F256P30B/TFx, PC28F256P30B/TFx, RD48F4400P0VBQEx, RC48F4400P0VB0Ex, PC48F4400P0VB0Ex, PF48F4000P0ZB/TQEx

Features

- High performance
  - 100ns initial access for Easy BGA
  - 110ns initial access for TSOP
  - 25ns 16-word asychronous page read mode
  - 52 MHz (Easy BGA) with zero WAIT states and 17ns clock-to-data output synchronous burst read mode
  - 4-, 8-, 16-, and continuous word options for burst mode
  - Buffered enhanced factory programming (BEFP) at 2MB/s (TYP) using a 512 word buffer
  - 1.8V buffered programming at 1.14MB/s (TYP) using a 512 word buffer
- Architecture
  - MLC: highest density at lowest cost
  - Asymmetrically blocked architecture
  - Four 32-KB parameter blocks: top or bottom configuration
  - 128KB main blocks
  - Blank check to verify an erased block
- Voltage and power
  - V_{CC} (core) voltage: 1.7V to 2.0V
  - V_{CCQ} (I/O) voltage: 1.7V to 3.6V
  - Standy current: 65µA (TYP) for 256Mb
  - 52 MHz continuous synchronous read current: 21mA (TYP), 24mA (MAX)

- Security
  - One-Time Programmable Register: 64 OTP bits, programmed with unique information from Micron; 2112 OTP bits available for customer programming
  - Absolute write protection: VPP = VSS
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
  - Password access
- Software
  - 25µs (TYP) program suspend
  - 25µs (TYP) erase suspend
  - Flash Data Integrator optimized
  - Basic command set and extended function Interface (EFI) command set compatible
  - Common flash interface
- Density and Packaging
  - 56-lead TSOP package (256Mb only)
  - 64-ball Easy BGA package (256Mb, 512Mb)
  - QUAD+ and SCSP packages (256Mb, 512Mb)
  - 16-bit wide data bus
- Quality and Reliabilty
  - JESD47E compliant
  - Operating temperature: –40 °C to +85 °C
  - Minimum 100,000 erase cycles per block
  - 65nm process technology

Discrete and MCP Part Numbering Information

Devices are shipped from the factory with memory content bits erased to 1. For available options, such as packages or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Table 1: Discrete Part Number Information

Part Number Category	Category Details
Package	JS = 56-lead TSOP, lead free
	PC = 64-ball Easy BGA, lead-free
	RC = 64-ball Easy BGA, leaded
Product Line	28F = Micron Flash memory
Density	256 = 256Mb
Product Family	P30 (VCC = 1.7 to 2.0V; VCCQ = 1.7 to 3.6V)
Parameter Location	B/T = Bottom/Top parameter
Lithography	F = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: JS28F256P30BF*

Table 2: MCP Part Number Information

Part Number Category	Category Details
Package	RD = Micron MCP, leaded
	PF = Micron MCP, lead-free
	RC = 64-ball Easy BGA, leaded
	PC = 64-ball Easy BGA, lead-free
Product Line	48F = Micron Flash memory only
Density	0 = No die
	4 = 256Mb
Product Family	P = Micron Flash memory (P30)
	0 = No die
IO Voltage and Chip Configuration	Z = Individual Chip Enables
	V = Virtual Chip Enables
	VCC = 1.7 to 2.0V; VCCQ = 1.7 to 3.6V
Parameter Location	B/T = Bottom/Top parameter
Ballout	Q = QUAD+
	0 = Discrete
Lithography	E = 65nm
Features	*

Note: 1. The last digit is assigned randomly to cover packaging media, features, or other specific configuration information. Sample part number: RD48F4400P0VB0E*

Table 3: Discrete and MCP Part Combinations

Package	Density	Packing Media	Boot Configuration [1]	Part Number
JS	256Mb	Tray	B	JS28F256P30BFE
		Tape and Reel		JS28F256P30BFF
		Tray	T	JS28F256P30TFE
PC	256Mb	Tray	B	PC28F256P30BFE
		Tape and Reel		PC28F256P30BFF
		Tray	T	PC28F256P30TFE
	512Mb (256Mb/256Mb)	Tray	B/T	PC48F4400P0VB0EE
		Tape and Reel		PC48F4400P0VB0EF
PF	256Mb	Tray	B	PF48F4000P0ZBQEF
		Tray	T	PF48F4000P0ZTQEJ
	512Mb (256Mb/256Mb)	Tray	B/T	PF48F4400P0VBQEF
		Tape and Reel		PF48F4400P0VBQEK

Table 3: Discrete and MCP Part Combinations (Continued)

Package	Density	Packing Media	Boot Configuration [1]	Part Number
RC	256Mb	Tray	B	RC28F256P30BFE
		Tray	T	RC28F256P30TFE
		Tape and Reel		RC28F256P30TFF
	512Mb (256Mb/256Mb)	Tray	B/T	RC48F4400P0VB0EJ
RD	512Mb (256Mb/256Mb)	Tray	B/T	RD48F4400P0VBQEJ

Note: 1. Bottom Boot/Top Boot = B/T

Table 4: OTP Feature Part Combinations

Package	Density	Packing Media	Boot Configuration [1]	Part Number
JS	–	–	–	–
PC	256Mb	Tape and Reel	B	PC28F256P30BFR
PF	–	–	–	–
RC	–	–	–	–
RD	–	–	–	–

Notes: 1. This data sheet covers only standard parts. For OTP parts, contact your local Micron representative.
2. Bottom Boot/Top Boot = B/T

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Introduction

This document provides information about the Micron Flash memory (P30-65nm) product and describes its features, operations, and specifications.

The Micron Flash memory (P30-65nm) is the latest generation of flash memory devices. P30-65nm device will be offered in 64Mb up through 2Gb densities. This document covers specifically 256Mb and 512Mb (256Mb/256Mb) product information. Benefits include more density in less space, high-speed interface device, and support for code and data storage. Features include high-performance synchronous-burst read mode, fast asynchronous access times, low power, flexible security options, and three industry-standard package choices. The P30-65nm product family is manufactured using Micron 65nm process technology.

Overview

This section provides an overview of the features and capabilities of the P30-65nm.

The P30-65nm family devices provides high performance at low voltage on a 16-bit data bus. Individually erasable memory blocks are sized for optimum code and data storage.

Upon initial power up or return from reset, the device defaults to asynchronous page-mode read. Configuring the Read Configuration Register enables synchronous burst-mode reads. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

In addition to the enhanced architecture and interface, the device incorporates technology that enables fast factory program and erase operations. Designed for low-voltage systems, the P30-65nm supports read operations with V_{CC} at 1.8 V, and erase and program operations with V_{PP} at 1.8 V or 9.0 V. Buffered Enhanced Factory Programming (BEFP) provides the fastest flash array programming performance with V_{PP} at 9.0 V, which increases factory throughput. With V_{PP} at 1.8 V, VCC and VPP can be tied together for a simple, ultra low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when $V_{PP} \leq V_{PPLK}$.

A Command User Interface (CUI) is the interface between the system processor and all internal operations of the device. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and program. A Status Register indicates erase or program completion and any errors that may have occurred.

An industry-standard command sequence invokes program and erase automation. Each erase operation erases one block. The Erase Suspend feature allows system software to pause an erase cycle to read or program data in another block. Program Suspend allows system software to pause programming to read other locations. Data is programmed in word increments (16 bits).

The P30-65nm protection register allows unique flash device identification that can be used to increase system security. The individual Block Lock feature provides zero-latency block locking and unlocking. The P30-65nm device includes enhanced protection via Password Access; this new feature allows write and/or read access protection of user-defined blocks. In addition, the P30-65nm device also provides the full-device One-Time Programmable (OTP) security feature.

Virtual Chip Enable Description

The P30-65nm 512Mb devices employ a virtual chip enable feature, which combines two 256Mb die with a common chip enable, F1-CE# for QUAD+ packages, or CE# for Easy BGA Packages. The maximum address bit is then used to select between the die pair with F1-CE#/CE# asserted depending upon the package option used. When chip enable is asserted and the maximum address bit is LOW (V_{IL}), the lower parameter die is selected; when chip enable is asserted and the maximum address bit is HIGH (V_{IH}), the upper parameter die is selected (see the tables below).

Table 5: Virtual Chip Enable Truth Table for 512Mb (QUAD+ Package)

Die Selected	F1-CE#	A24
Lower Param Die	L	L
Upper Param Die	L	H

Table 6: Virtual Chip Enable Truth Table for 512Mb (Easy BGA Packages)

Die Selected	CE#	A25
Lower Param Die	L	L
Upper Param Die	L	H

Figure 1: 512Mb Easy BGA Block Diagram
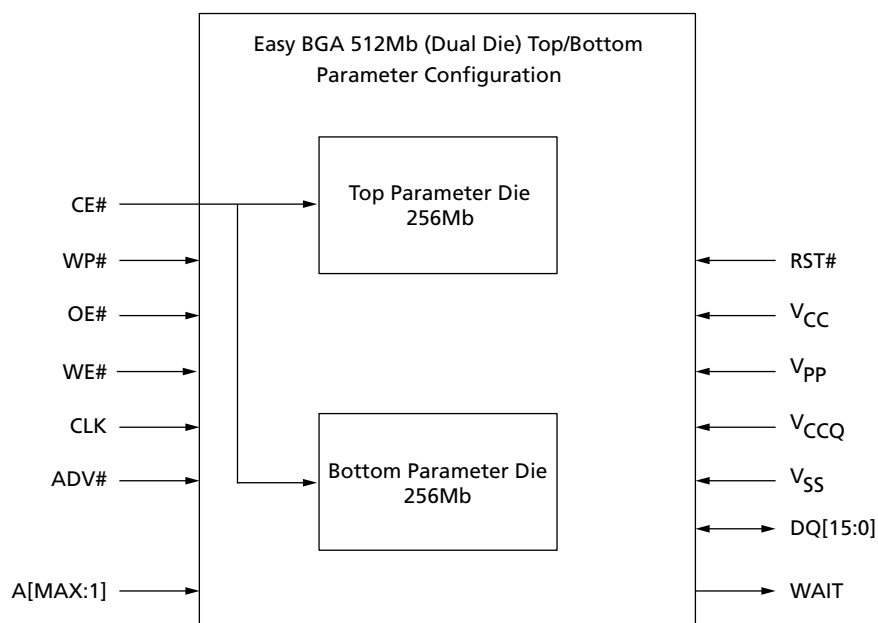
Figure 2: 512Mb QUAD+ Block Diagram
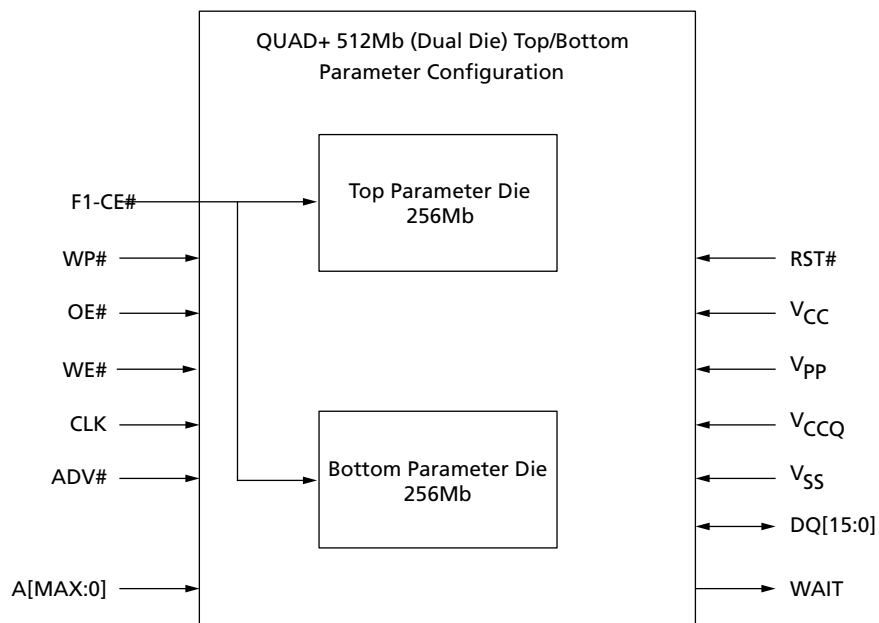
Memory Map

Figure 3: P30-65nm, 256Mb and 512Mb Memory Map

A[24:1] 256Mb, Easy BGA, TSOP
A[23:0] 256Mb, Quad+

FF0000 - FFFFFF	64 KWord Block 258
...	
7F0000 - 7FFFFF	64 KWord Block 130
...	
3F0000 - 3FFFFF	64 KWord Block 66
...	
020000 - 02FFFF	64 KWord Block 5
010000 - 01FFFF	64 KWord Block 4
00C000 - 00FFFF	16 KWord Block 3
008000 - 00BFFF	16 KWord Block 2
004000 - 007FFF	16 KWord Block 1
000000 - 003FFF	16 KWord Block 0

256Mb

Bottom Boot 256Mb, World-Wide x16 Mode

A[24:1] 256Mb, Easy BGA, TSOP
A[23:0] 256Mb, Quad+

FFC000 - FFFFFF	16 KWord Block 258
FF8000 - FFBFFF	16 KWord Block 257
FF4000 - FF7FFF	16 KWord Block 256
FF0000 - FF3FFF	16 KWord Block 255
FE0000 - FEFFFF	64 KWord Block 254
...	
010000 - 01FFFF	64 KWord Block 1
000000 - 00FFFF	64 KWord Block 0

256Mb

Top Boot 256Mb, World-Wide x16 Mode

A[25:1] 512Mb (256Mb/256Mb), Easy BGA, TSOP
A[24:0] 512Mb (256Mb/256Mb), Quad+

1FFC000 - 1FFFFFF	16 KWord Block 517
1FF8000 - 1FFBFFF	16 KWord Block 516
1FF4000 - 1FF7FFF	16 KWord Block 515
1FF0000 - 1FF3FFF	16 KWord Block 514
1FE0000 - 1FEFFFF	64 KWord Block 513
1FD0000 - 1FDFFFF	64 KWord Block 512
...	
020000 - 02FFFF	64 KWord Block 5
010000 - 01FFFF	64 KWord Block 4
00C000 - 00FFFF	16 KWord Block 3
008000 - 00BFFF	16 KWord Block 2
004000 - 007FFF	16 KWord Block 1
000000 - 003FFF	16 KWord Block 0

512Mb (256Mb/256Mb)

512Mb (256Mb/256Mb), World Wide x16 Mode

Package Dimensions

Figure 4: 56-Pin TSOP – 14mm x 20mm
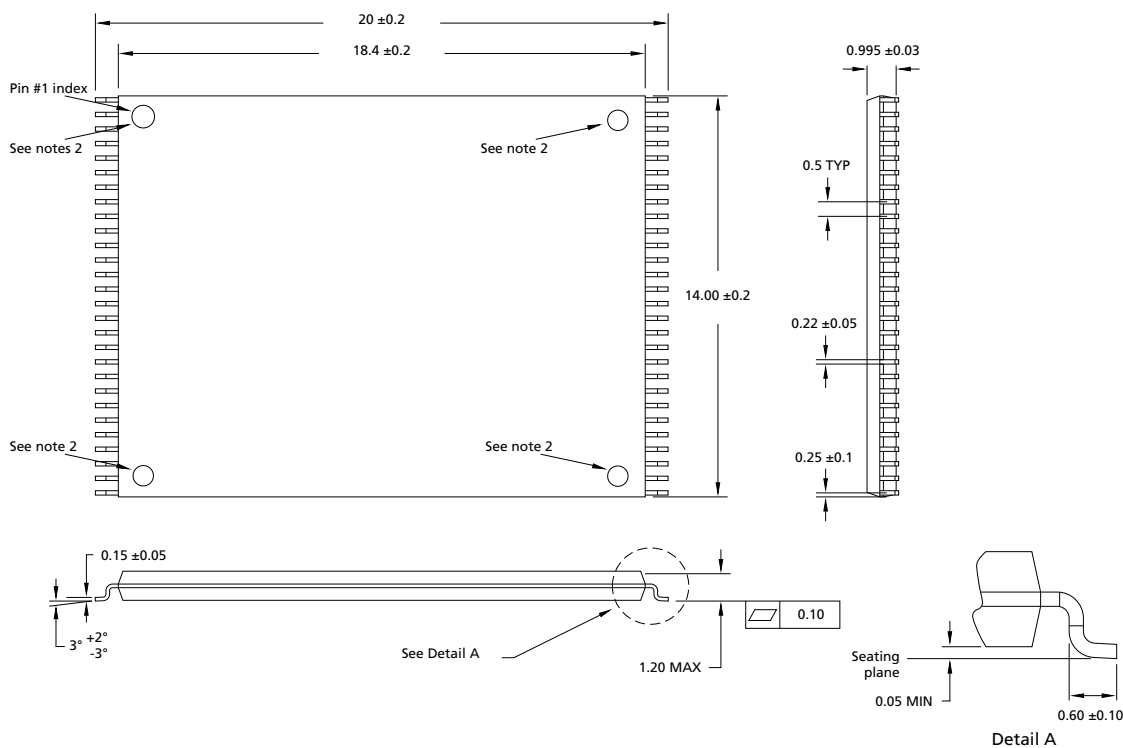
Notes:
1. All dimensions are in millimeters. Drawing not to scale.
2. One dimple on package denotes pin 1; if two dimples, then the larger dimple denotes pin 1. Pin 1 will always be in the upper left corner of the package, in reference to the product mark.
3. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

Figure 5: 64-Ball Easy BGA – 10mm x 13mm x 1.2mm
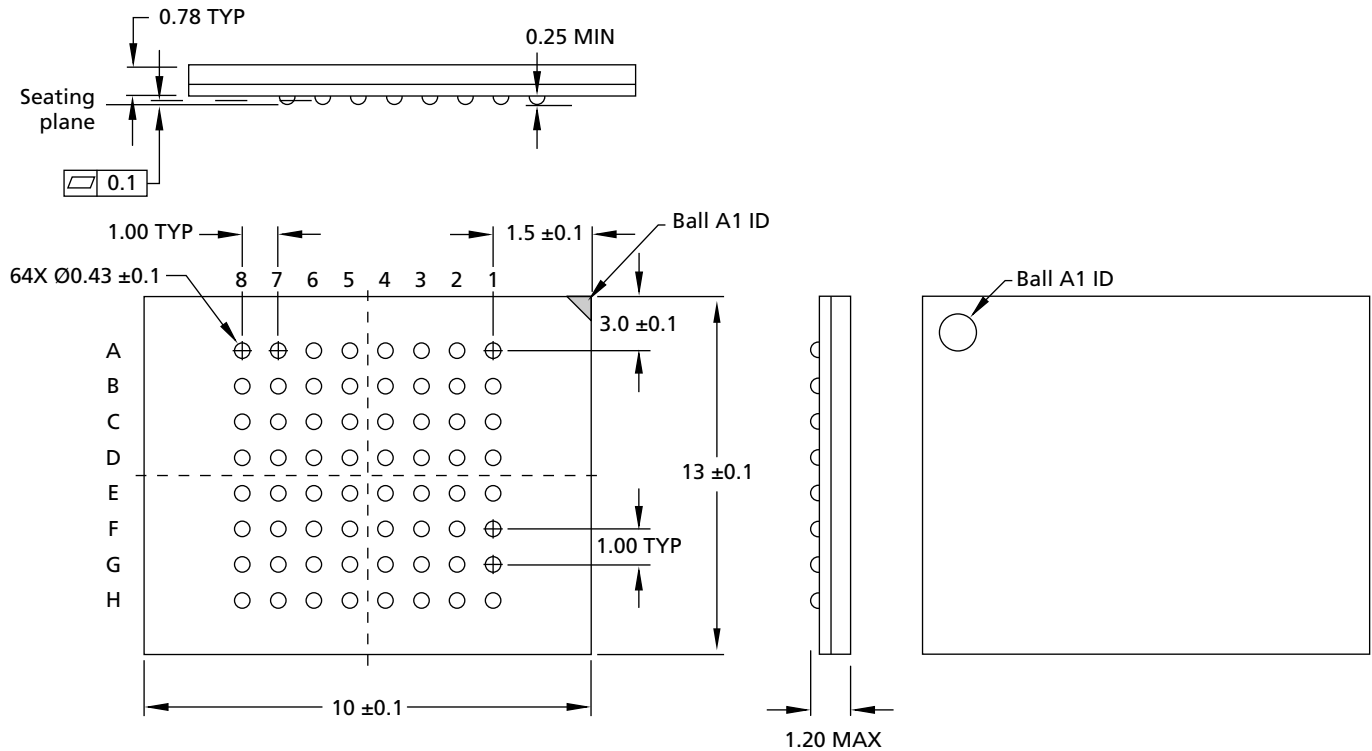
Note: 1. All dimensions are in millimeters. Drawing not to scale.

Figure 6: 88-Ball QUAD+ – 8mm x 11mm x 1.0mm
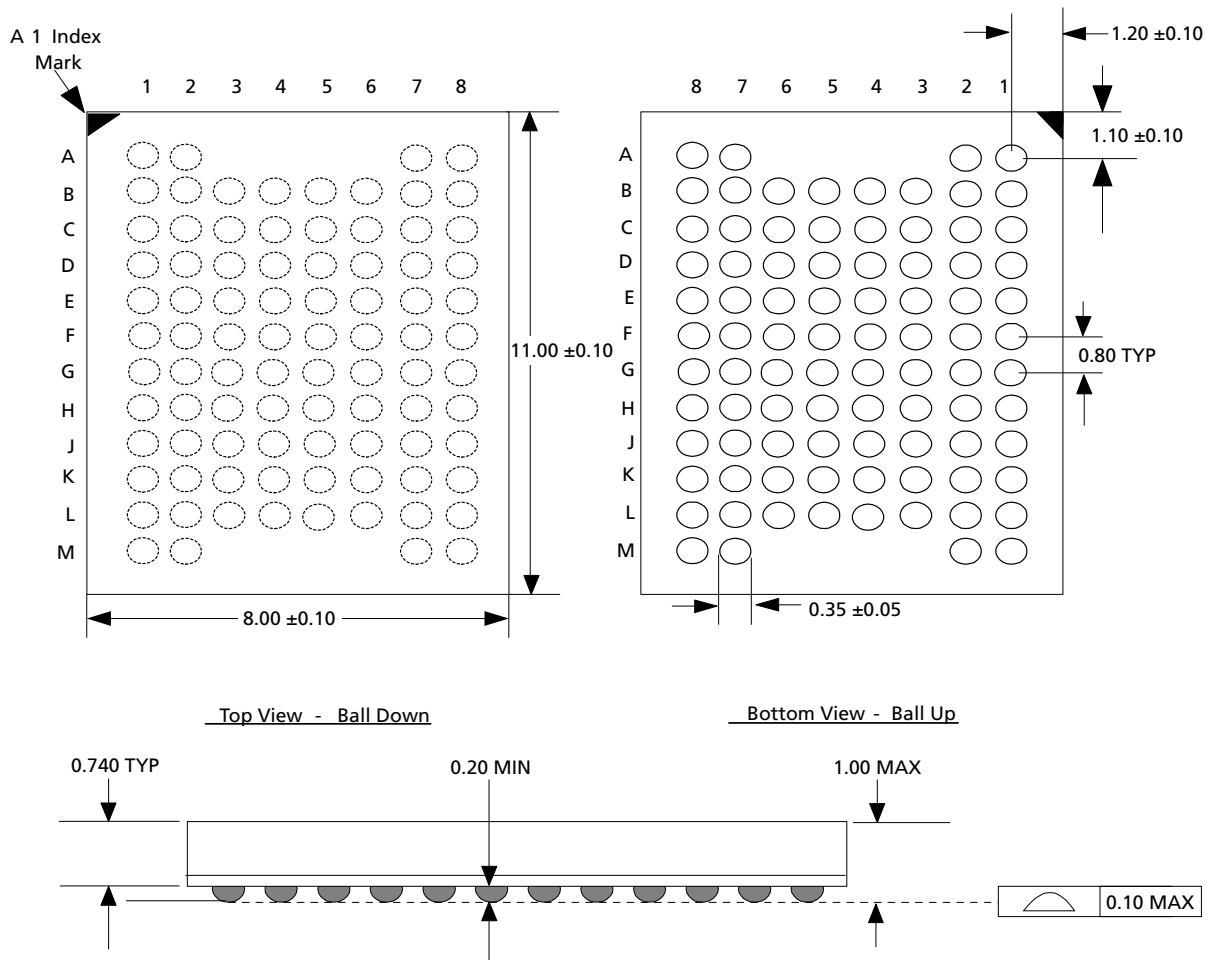
Note: 1. All dimensions are in millimeters. Drawing not to scale.

Figure 7: 88-Ball QUAD+ – 8mm x 11mm x 1.2mm
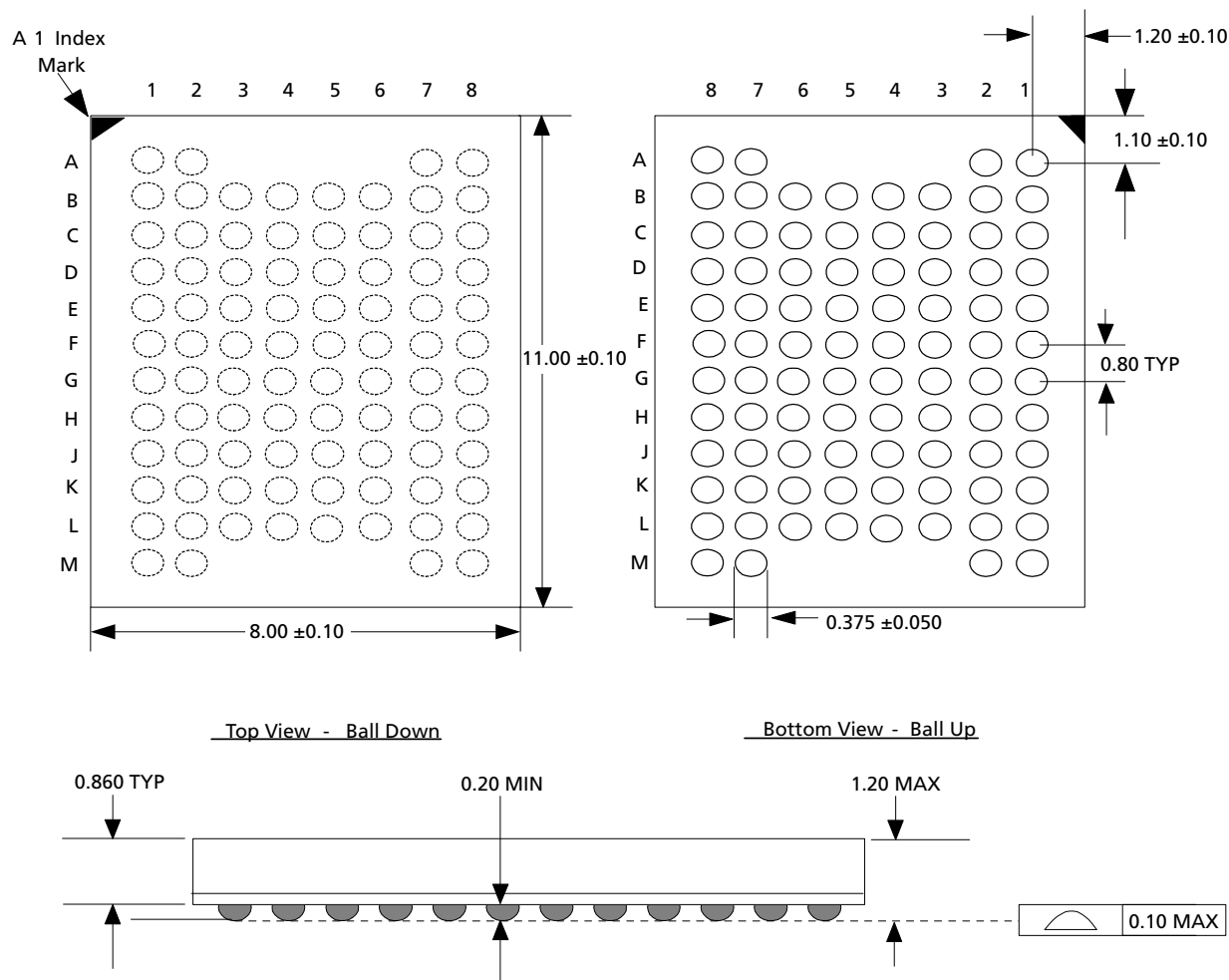
Note: 1. All dimensions are in millimeters. Drawing not to scale.

Pinouts and Ballouts

Figure 8: 56-Lead TSOP Pinout (256Mb)

Left	Pin		Pin	Right
A 16	1		56	WAIT
A 15	2		55	A 17
A 14	3		54	DQ 15
A 13	4		53	DQ 7
A 12	5		52	DQ 14
A 11	6		51	DQ 6
A 10	7		50	DQ 13
A 9	8		49	DQ 5
A 23	9		48	DQ 12
A 22	10		47	DQ 4
A 21	11		46	ADV #
VSS	12	56-Lead TSOP Pinout	45	CLK
RFU	13	14mm x 20mm	44	RST #
WE #	14	Top View	43	VPP
WP #	15		42	DQ 11
A 20	16		41	DQ 3
A 19	17		40	DQ 10
A 18	18		39	DQ 2
A 8	19		38	VCCQ
A 7	20		37	DQ 9
A 6	21		36	DQ 1
A 5	22		35	DQ 8
A 4	23		34	DQ 0
A 3	24		33	VCC
A 2	25		32	OE #
A 24	26		31	VSS
RFU	27		30	CE #
VSS	28		29	A 1
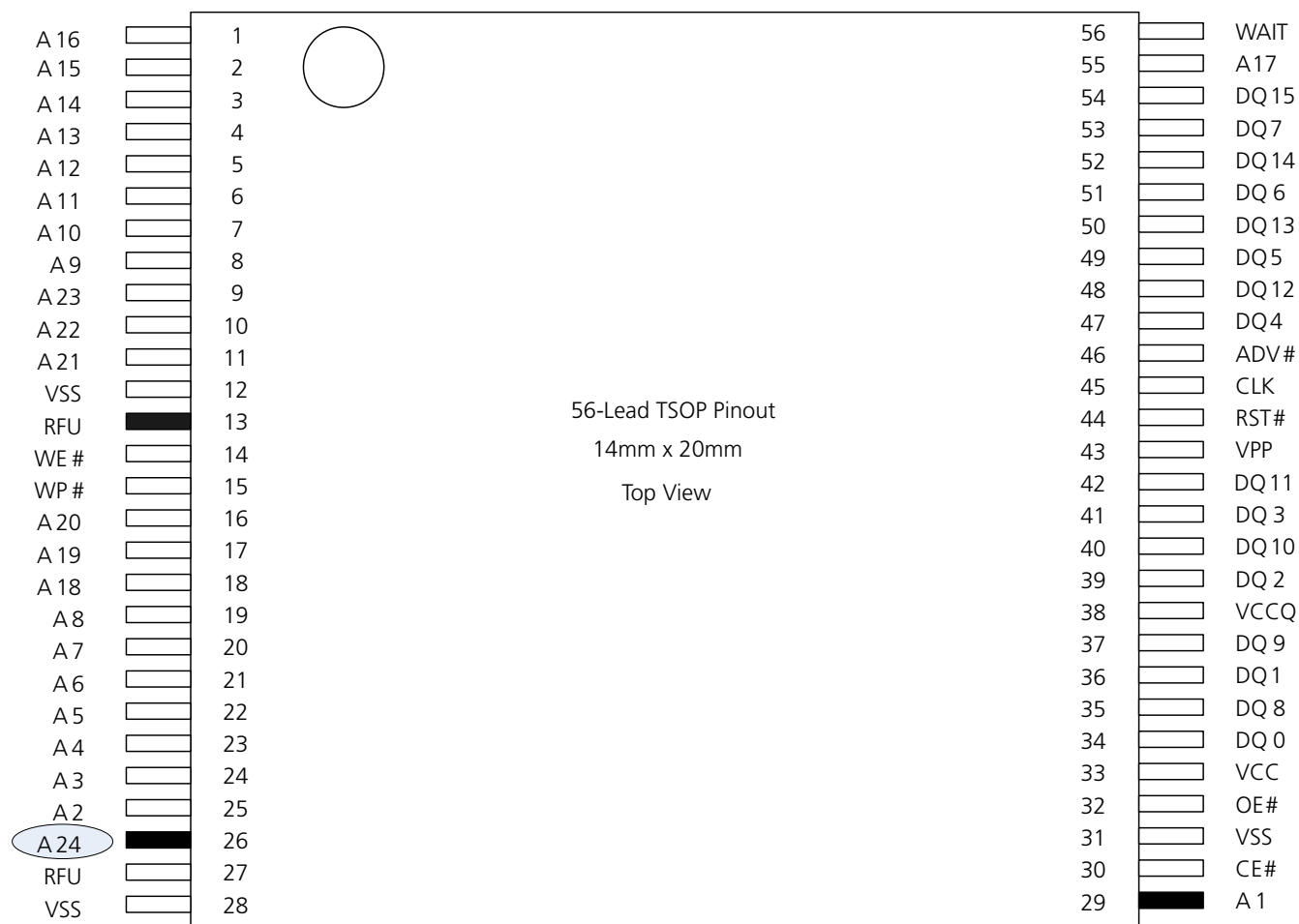
Notes: 1. A1 is the least significant address bit.
2. A24 is valid for 256Mb densities; otherwise, it is a no connect (NC).
3. No Internal Connection on Pin 13; it may be driven or floated. For legacy designs, it is VCC pin and can be tied to Vcc.
4. One dimple on package denotes Pin 1 which will always be in the upper left corner of the package, in reference to the product mark.

Figure 9: 64-Ball Easy BGA Ballout (256Mb, 512Mb)
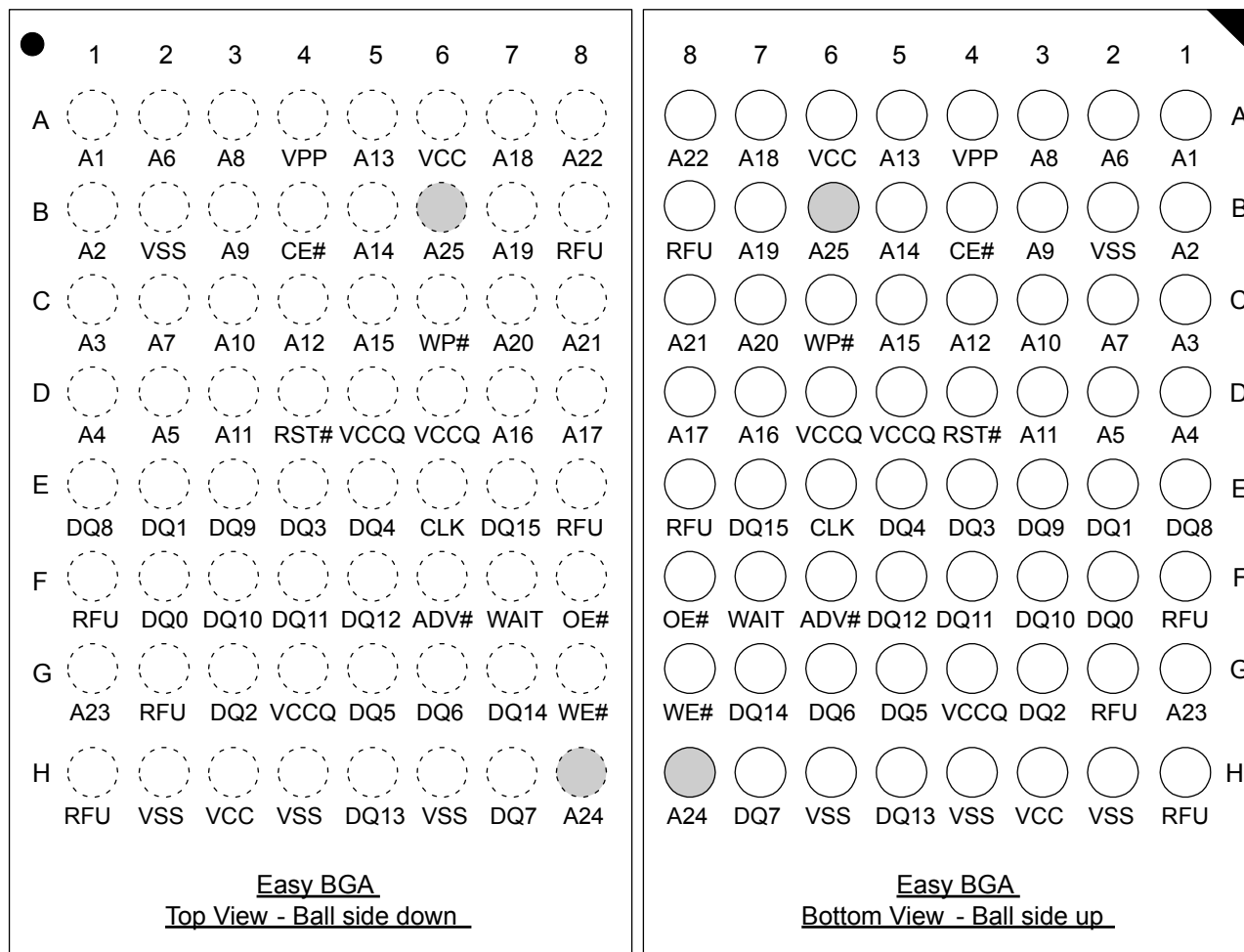
Easy BGA
Top View - Ball side down

Easy BGA
Bottom View - Ball side up

Notes:
1. A1 is the least significant address bit.
2. A24 is valid for 256Mb densities and above; otherwise, it is a no connect (NC).
3. A25 is valid for 512-Mbit densities; otherwise, it is a no connect.
4. One dimple on package denotes A1 Pin which will always be in the upper left corner of the package, in reference to the product mark.

Figure 10: QUAD+ MCP Ballout

Pin 1

	1	2	3	4	5	6	7	8	
A	DU	DU	Depop	Depop	Depop	Depop	DU	DU	A
B	A4	A18	A19	VSS	VCC	VCC	A21	A11	B
C	A5	RFU	A23	VSS	RFU	CLK	A22	A12	C
D	A3	A17	A24	VPP	RFU	RFU	A9	A13	D
E	A2	A7	RFU	WP#	ADV#	A20	A10	A15	E
F	A1	A6	RFU	RST#	WE#	A8	A14	A16	F
G	A0	DQ8	DQ2	DQ10	DQ5	DQ13	WAIT	F2-CE#	G
H	RFU	DQ0	DQ1	DQ3	DQ12	DQ14	DQ7	F2-OE#	H
J	RFU	OE#	DQ9	DQ11	DQ4	DQ6	DQ15	VCCQ	J
K	F1-CE#	RFU	RFU	RFU	RFU	VCC	VCCQ	RFU	K
L	VSS	VSS	VCCQ	VCC	VSS	VSS	VSS	VSS	L
M	DU	DU	Depop	Depop	Depop	Depop	DU	DU	M
	1	2	3	4	5	6	7	8	

Top View - Ball Side Down

Legends :		De-Populated Ball		Control Signals
		De-Populated Ball		Address
		Reserved for Future Use		Data
		Do Not Use		Power/Ground

Notes:
1. A23 is valid for 256Mb densities and above; otherwise, it is a no connect.
2. A24 is valid for 512Mb densities and above; otherwise, it is a no connect.
3. F2-CE# and F2-OE# are no connect for all densities.
4. A0 is LSB for Address.

Signals

Table 7: TSOP and Easy BGA Signal Descriptions

Symbol	Type	Name and Function
A[MAX:1]	Input	**Address inputs:** Device address inputs. 256Mb: A[24:1]; 512Mb: A[25:1]. **Note:** The virtual selection of the 256Mb top parameter die in the dual-die 51Mb configuration is accomplished by setting A25 HIGH (V_{IH}). **Note:** The active address pins unused in design should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during write cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
CE#	Input	**Chip enable:** Active LOW input. CE# LOW selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated flash die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z state. **Note:** Chip enable must be driven HIGH when device is not in use.
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READs, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:** Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the device's output data buffers during read cycles. OE# HIGH places the data outputs and WAIT in High-Z.
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read Configuration Register bit 10 (RCR.10, WT) determines its polarity when asserted. This signal's active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, this signal indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, this signal is de-asserted.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the Unlock command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.

Table 7: TSOP and Easy BGA Signal Descriptions (Continued)

Symbol	Type	Name and Function
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system flash modification. V_{PP} may be 0V during READ operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \leq V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output-driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a Do Not Use (DNU) signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Table 8: QUAD+ SCSP Signal Descriptions

Symbol	Type	Name and Function
A[MAX:0]	Input	**Address inputs:** Device address inputs. 256Mb: A[23:0]; 512Mb: A[24:0]. **Note:** The virtual selection of the 256Mb top parameter die in the dual-die 512Mb configuration is accomplished by setting A24 HIGH (V_{IH}). **Note:** The address pins unused in design should not be left floating; tie them to V_{CCQ} or V_{SS} according to specific design requirements.
DQ[15:0]	Input/Output	**Data input/output:** Inputs data and commands during write cycles; outputs data during memory, status register, protection register, and read configuration register reads. Data balls float when the CE# or OE# are de-asserted. Data is internally latched during writes.
ADV#	Input	**Address valid:** Active LOW input. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. In asynchronous mode, the address is latched when ADV# goes HIGH or continuously flows through if ADV# is held LOW. **Note:** Designs not using ADV# must tie it to V_{SS} to allow addresses to flow through.
F1-CE#	Input	**Flash chip enable:** Active LOW input. CE# LOW selects the associated flash memory die. When asserted, flash internal control logic, input buffers, decoders, and sense amplifiers are active. When de-asserted, the associated flash die is deselected, power is reduced to standby levels, data and wait outputs are placed in High-Z state. **Note:** Chip enable must be driven HIGH when device is not in use.

Table 8: QUAD+ SCSP Signal Descriptions (Continued)

Symbol	Type	Name and Function
CLK	Input	**Clock:** Synchronizes the device with the system bus frequency in synchronous-read mode. During synchronous READ operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# LOW, whichever occurs first. **Note:** Designs not using CLK for synchronous read mode must tie it to V_{CCQ} or V_{SS}.
F1-OE#	Input	**Output enable:** Active LOW input. OE# LOW enables the device's output data buffers during read cycles. OE# HIGH places the data outputs and wait in High-Z.
RST#	Input	**Reset:** Active LOW input. RST# resets internal automation and inhibits WRITE operations. This provides data protection during power transitions. RST# HIGH enables normal operation. Exit from reset places the device in asynchronous read array mode.
WAIT	Output	**Wait:** Indicates data valid in synchronous array or non-array burst reads. Read configuration register bit 10 (RCR.10, WT) determines its polarity when asserted. The active output is V_{OL} or V_{OH} when CE# and OE# are V_{IL}. WAIT is High-Z if CE# or OE# is V_{IH}. • In synchronous array or non-array read modes, WAIT indicates invalid data when asserted and valid data when de-asserted. • In asynchronous page mode, and all write modes, WAIT is de-asserted.
WE#	Input	**Write enable:** Active LOW input. WE# controls writes to the device. Address and data are latched on the rising edge of WE# or CE#, whichever occurs first.
WP#	Input	**Write protect:** Active LOW input. WP# LOW enables the lock-down mechanism. Blocks in lock-down cannot be unlocked with the UNLOCK command. WP# HIGH overrides the lock-down function enabling blocks to be erased or programmed using software commands. **Note:** Designs not using WP# for protection could tie it to V_{CCQ} or V_{SS} without additional capacitor.
V_{PP}	Power/Input	**Erase and program power:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{PPL}$ for in-system PROGRAM and ERASE operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as $V_{PPL,min}$. V_{PP} must remain above $V_{PPL,min}$ to perform in-system flash modification. V_{PP} may be 0V during READ operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. V_{PP} can be connected to 9V for a cumulative total not to exceed 80 hours. Extended use of this pin at 9V may reduce block cycling capability.
V_{CC}	Power	**Device core power supply:** Core (logic) source voltage. Writes to the flash array are inhibited when $V_{CC} \leq V_{LKO}$. Operations at invalid V_{CC} voltages should not be attempted.
V_{CCQ}	Power	**Output power supply:** Output driver source voltage.
V_{SS}	Power	**Ground:** Connect to system ground. Do not float any V_{SS} connection.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. These should be treated in the same way as a Do Not Use (DNU) signal.
DU	—	**Do not use:** Do not connect to any other signal, or power supply; must be left floating.
NC	—	**No connect:** No internal connection; can be driven or floated.

Bus Operations

CE# low and RST# high enable device read operations. The device internally decodes upper address inputs to determine the accessed block. ADV# low opens the internal address latches. OE# low activates the outputs and gates selected data onto the I/O bus.

In asynchronous mode, the address is latched when ADV# goes high or continuously flows through if ADV# is held low. In synchronous mode, the address is latched by the first of either the rising ADV# edge or the next valid CLK edge with ADV# low (WE# and RST# must be V_{IH}; CE# must be V_{IL}).

Bus cycles to/from the P30-65nm device conform to standard microprocessor bus operations. The Bus Operations table shows the bus operations and the logic levels that must be applied to the device control signal inputs.

Table 9: Bus Operations

Bus Operation		RST#	CLK	ADV#	CE#	OE#	WE#	WAIT	DQ[15:0]	Notes
Read	Asynchronous	V_{IH}	X	L	L	L	H	Deasserted	Output	1
	Synchronous	V_{IH}	Running	L	L	L	H	Driven	Output	
Write		V_{IH}	X	L	L	H	L	High-Z	Input	1, 2
Output Disable		V_{IH}	X	X	L	H	H	High-Z	High-Z	1
Standby		V_{IH}	X	X	H	X	X	High-Z	High-Z	1
Reset		V_{IL}	X	X	X	X	X	High-Z	High-Z	1, 3

Notes:
1. X = Don't Care (H or L).
2. Refer to the Command Bus Cycles table for valid DQ[15:0] during a write operation.
3. RST# must be at V_{SS} ± 0.2 V to meet the maximum specified power-down current.

Reads

To perform a read operation, RST# and WE# must be deasserted while CE# and OE# are asserted. CE# is the device-select control. When asserted, it enables the flash memory device. OE# is the data-output control. When asserted, the addressed flash memory data is driven onto the I/O bus.

Writes

To perform a write operation, both CE# and WE# are asserted while RST# and OE# are deasserted. During a write operation, address and data are latched on the rising edge of WE# or CE#, whichever occurs first. The Command Bus Cycles table shows the bus cycle sequence for each of the supported device commands, while the Command Codes and Definitions table describes each command.

Note: Write operations with invalid V_{CC} and/or V_{PP} voltages can produce spurious results and should not be attempted.

Output Disable

When OE# is deasserted, device outputs DQ[15:0] are disabled and placed in a high-impedance (High-Z) state, WAIT is also placed in High-Z.

Standby

When CE# is deasserted the device is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, independent of the level placed on OE#. Standby current, I_{CCS}, is the average current measured over any 5 ms time interval, 5µs after CE# is deasserted. During standby, average current is measured over the same time interval 5µs after CE# is deasserted.

When the device is deselected (while CE# is deasserted) during a program or erase operation, it continues to consume active power until the program or erase operation is completed.

Reset

As with any automated device, it is important to assert RST# when the system is reset. When the system comes out of reset, the system processor attempts to read from the flash memory if it is the system boot device. If a CPU reset occurs with no flash memory reset, improper CPU initialization may occur because the flash memory may be providing status information rather than array data. Flash memory devices from Micron allow proper CPU initialization following a system reset through the use of the RST# input. RST# should be controlled by the same low-true reset signal that resets the system CPU.

After initial power-up or reset, the device defaults to asynchronous Read Array mode, and the Status Register is set to 0x80. Asserting RST# de-energizes all internal circuits, and places the output drivers in High-Z. When RST# is asserted, the device shuts down the operation in progress, a process which takes a minimum amount of time to complete. When RST# has been deasserted, the device is reset to asynchronous Read Array state.

When device returns from a reset (RST# deasserted), a minimum wait is required before the initial read access outputs valid data. Also, a minimum delay is required after a reset before a write cycle can be initiated. After this wake-up interval passes, normal operation is restored.

Note: If RST# is asserted during a program or erase operation, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, because the data may have been only partially written or erased.

Device Command Codes

The system CPU provides control of all in-system READ, WRITE, and ERASE operations of the device via the system bus. The device manages all block-erase and word-program algorithms.

Device commands are written to the command user interface (CUI) to control all flash memory device operations. The CUI does not occupy an addressable memory location; it is the mechanism through which the Flash device is controlled.

Note: For 512Mb (256Mb/256Mb) device, all the setup commands should be re-issued to the device when a different die is selected.

Table 10: Command Codes and Definitions

Mode	Code	Device Mode	Description
Read	0xFF	Read Array	Places the device in Read Array mode. Array data is output on DQ[15:0].
	0x70	Read Status Register	Places the device in Read Status Register mode. The device enters this mode after a program or erase command is issued. Status Register data is output on DQ[7:0].
	0x90	Read Device ID or Read Configuration Register (RCR)	Places device in Read Device Identifier mode. Subsequent reads output manufacturer/device codes, Configuration Register data, Block Lock status, or Protection Register data on DQ[15:0].
	0x98	Read CFI	Places the device in Read CFI mode. Subsequent reads output Common Flash Interface information on DQ[7:0].
	0x50	Clear Status Register	The device sets Status Register error bits. The Clear Status Register command is used to clear the SR error bits.
Write	0x40	Word Program Setup	First cycle of a 2-cycle programming command; prepares the CUI for a write operation. On the next write cycle, the address and data are latched and the device executes the programming algorithm at the addressed location. During program operations, the device responds only to Read Status Register and Program Suspend commands. CE# or OE# must be toggled to update the Status Register in asynchronous read. CE# or ADV# must be toggled to update the Status Register Data for synchronous Non-array reads. The Read Array command must be issued to read array data after programming has finished.
	0xE8	Buffered Program	This command loads a variable number of words up to the buffer size of 512 words onto the program buffer.
	0xD0	Buffered Program Confirm	The confirm command is issued after the data streaming for writing into the buffer is completed. The device then performs the Buffered Program algorithm, writing the data from the buffer to the Flash memory array.
	0x80	BEFP Setup	First cycle of a 2-cycle command; initiates Buffered Enhanced Factory Program mode (BEFP). The CUI then waits for the BEFP Confirm command, 0xD0, that initiates the BEFP algorithm. All other commands are ignored when BEFP mode begins.
	0xD0	BEFP Confirm	If the previous command was BEFP Setup (0x80), the CUI latches the address and data, and prepares the device for BEFP mode.

Table 10: Command Codes and Definitions (Continued)

Mode	Code	Device Mode	Description
Erase	0x20	Block Erase Setup	First cycle of a 2-cycle command; prepares the CUI for a block-erase operation. The device performs the erase algorithm on the block addressed by the Erase Confirm command. If the next command *is not* the Erase Confirm (0xD0) command, the CUI sets Status Register bits SR.4 and SR.5, and places the device in read status register mode.
	0xD0	Block Erase Confirm	If the first command was Block Erase Setup (0x20), the CUI latches the address and data, and the device erases the addressed block. During block-erase operations, the device responds only to Read Status Register and Erase Suspend commands. CE# or OE# must be toggled to update the Status Register in asynchronous read. CE# or ADV# must be toggled to update the Status Register Data for synchronous Non-array reads.
Suspend	0xB0	Program or Erase Suspend	This command issued to any device address initiates a suspend of the currently-executing program or block erase operation. The Status Register indicates successful suspend operation by setting either SR.2 (program suspended) or SR.6 (erase suspended), along with SR.7 (ready). The Write State Machine remains in the suspend mode regardless of control signal states (except for RST# asserted).
	0xD0	Suspend Resume	This command issued to any device address resumes the suspended program or block-erase operation.
Block Locking/ Unlocking	0x60	Block lock Setup	First cycle of a 2-cycle command; prepares the CUI for block lock configuration changes. If the next command is not Block Lock (0x01), Block Unlock (0xD0), or Block Lock-Down (0x2F), the CUI sets Status Register bits SR.5 and SR.4, indicating a command sequence error.
	0x01	Block lock	If the previous command was Block Lock Setup (0x60), the addressed block is locked.
	0xD0	Block Unlock	If the previous command was Block Lock Setup (0x60), the addressed block is unlocked. If the addressed block is in a lock-down state, the operation has no effect.
	0x2F	Block Lock-Down	If the previous command was Block Lock Setup (0x60), the addressed block is locked down.

Table 10: Command Codes and Definitions (Continued)

Mode	Code	Device Mode	Description
Protection	0x60	Block lock Setup	First cycle of a 2-cycle command; prepares the CUI for block lock configuration changes. If the next command is not Block Lock (0x01), Block Unlock (0xD0), or Block Lock-Down (0x2F), the CUI sets Status Register bits SR.5 and SR.4, indicating a command sequence error.
	0x01	Block lock	If the previous command was Block Lock Setup (0x60), the addressed block is locked.
	0xD0	Block Unlock	If the previous command was Block Lock Setup (0x60), the addressed block is unlocked. If the addressed block is in a lock-down state, the operation has no effect.
	0x2F	Block Lock-Down	If the previous command was Block Lock Setup (0x60), the addressed block is locked down.
	0xC0	OTP Register or Lock Register program setup	First cycle of a 2-cycle command; prepares the device for a OTP register or Lock Register program operation. The second cycle latches the register address and data, and starts the programming algorithm to program data the the OTP array.
Configuration	0x60	Read Configuration Register Setup	First cycle of a 2-cycle command; prepares the CUI for device read configuration. If the Set Read Configuration Register command (0x03) is not the next command, the CUI sets Status Register bits SR.4 and SR.5, indicating a command sequence error.
	0x03	Read Configuration Register	If the previous command was Read Configuration Register Setup (0x60), the CUI latches the address and writes A[16:1] to the Read Configuration Register for Easy BGA and TSOP, A[15:0] for QUAD+. Following a Configure Read Configuration Register command, subsequent read operations access array data.
Blank Check	0xBC	Block Blank Check	First cycle of a 2-cycle command; initiates the Blank Check operation on a main block.
	0xD0	Block Blank Check Confirm	Second cycle of blank check command sequence; it latches the block address and executes blank check on the main array block.
EFI	0xEB	Extended Function Interface command	First cycle of a multiple-cycle command; initiate operation using extended function interface. The second cycle is a Sub-Op-Code, the data written on third cycle is one less than the word count; the allowable value on this cycle are 0–511. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved.

Device Command Bus Cycles

Device operations are initiated by writing specific device commands to the command user interface (CUI). Several commands are used to modify array data including Word Program and Block Erase commands. Writing either command to the CUI initiates a sequence of internally timed functions that culminate in the completion of the requested task. However, the operation can be aborted by either asserting RST# or by issuing an appropriate suspend command.

Table 11: Command Bus Cycles

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Op	Addr[1]	Data[2]	Op	Addr[1]	Data[2]
Read	Read Array	1	Write	DnA	0xFF	–	–	–
	Read Device Identifier	≥2	Write	DnA	0x90	Read	DBA + IA	ID
	Read CFI	≥2	Write	DnA	0x98	Read	DBA + CFI-A	CFI-D
	Read Status Register	2	Write	DnA	0x70	Read	DnA	SRD
	Clear Status Register	1	Write	DnA	0x50	–	–	–
Program	Word Program	2	Write	WA	0x40	Write	WA	WD
	Buffered Program[3]	>2	Write	WA	0xE8	Write	WA	N - 1
	Buffered Enhanced Factory Program (BEFP)[4]	>2	Write	WA	0x80	Write	WA	0xD0
Erase	Block Erase	2	Write	BA	0x20	Write	BA	0xD0
Suspend	Program/Erase Suspend	1	Write	DnA	0xB0	–	–	–
	Program/Erase Resume	1	Write	DnA	0xD0	–	–	–
Block Locking/ Unlocking	Block Lock	2	Write	BA	0x60	Write	BA	0x01
	Block Unlock	2	Write	BA	0x60	Write	BA	0xD0
	Block Lock-down	2	Write	BA	0x60	Write	BA	0x2F
Protection	Block Lock	2	Write	BA	0x60	Write	BA	0x01
	Block Unlock	2	Write	BA	0x60	Write	BA	0xD0
	Block Lock-down	2	Write	BA	0x60	Write	BA	0x2F
	Program OTP register	2	Write	PRA	0xC0	Write	OTP-RA	OTP-D
	Program Lock Register	2	Write	LRA	0xC0	Write	LRA	LRD
Configuration	Configure Read Configuration Register	2	Write	RCD	0x60	Write	RCD	0x03
Blank Check	Block Blank Check	2	Write	BA	0xBC	Write	BA	D0
EFI	Extended Function Interface command [5]	>2	Write	WA	0xEB	Write	WA	Sub-Op code

Notes: 1. First command cycle address should be the same as the operation's target address. DBA = Device base address (needed for dual die 512Mb device); DnA = Address within the device; IA = Identification code address offset; CFI-A = Read CFI address offset; WA = Word address of memory location to be written; BA = Address within the block; OTP-RA = Protection register address; LRA = Lock register address; RCD = Read configuration register data on A[16:1] for Easy BGA and TSOP, A[15:0] for QUAD+ package.

2. ID = Identifier data; CFI-D = CFI data on DQ[15:0]; SRD = Status register data; WD = Word data; N = Word count of data to be loaded into the write buffer; OTP-D = Protection register data; LRD = Lock register data.

3. The second cycle of the BUFFERED PROGRAM command is the word count of the data to be loaded into the write buffer. This is followed by up to 512 words of data. Then the CONFIRM command (0xD0) is issued, triggering the array programming operation.

4. The CONFIRM command (0xD0) is followed by the buffer data.

5. The second cycle is a Sub-Op-Code, the data written on third cycle is N-1; 1≤ N ≤ 512. The subsequent cycles load data words into the program buffer at a specified address until word count is achieved, after the data words are loaded, the final cycle is the confirm cycle 0xD0).

Read Operation

The device supports two read modes: asynchronous page mode and synchronous burst mode. Asynchronous page mode is the default read mode after device power-up or a reset. The Read Configuration Register must be configured to enable synchronous burst reads of the flash memory array.

The device can be in any of four read states: Read Array, Read Identifier, Read Status or Read CFI. Upon power-up, or after a reset, the device defaults to Read Array. To change the read state, the appropriate read command must be written to the device.

Asynchronous Page-Mode Read

Following a device power-up or reset, asynchronous page mode is the default read mode and the device is set to Read Array. However, to perform array reads after any other device operation (e.g. write operation), the Read Array command must be issued in order to read from the flash memory array.

Asynchronous page-mode reads can only be performed when Read Configuration Register bit RCR.15 is set.

To perform an asynchronous page-mode read, an address is driven onto the Address bus, and CE# and ADV# are asserted. WE# and RST# must already have been deasserted. WAIT is deasserted during asynchronous page mode. ADV# can be driven high to latch the address, or it must be held low throughout the read cycle. CLK is not used for asynchronous page-mode reads, and is ignored. If only asynchronous reads are to be performed, CLK should be tied to a valid V_{IH} or V_{SS} level, WAIT signal can be floated and ADV# must be tied to ground. Array data is driven onto DQ[15:0] after an initial access time t_{AVQV} delay.

In asynchronous page mode, sixteen data words are "sensed" simultaneously from the flash memory array and loaded into an internal page buffer. The buffer word corresponding to the initial address on the Address bus is driven onto DQ[15:0] after the initial access delay. The lowest four address bits determine which word of the 16-word page is output from the data buffer at any given time.

Note: Asynchronous page read mode is only supported in main array.

Synchronous Burst-Mode Read

Read Configuration register bits RCR[15:0] must be set before synchronous burst operation can be performed. Synchronous burst mode can be performed for both array and non-array reads such as Read ID, Read Status or Read Query.

To perform a synchronous burst-read, an initial address is driven onto the Address bus, and CE# and ADV# are asserted. WE# and RST# must already have been deasserted. ADV# is asserted, and then deasserted to latch the address. Alternately, ADV# can remain asserted throughout the burst access, in which case the address is latched on the next valid CLK edge while ADV# is asserted.

During synchronous array and non-array read modes, the first word is output from the data buffer on the next valid CLK edge after the initial access latency delay. Subsequent data is output on valid CLK edges following a minimum delay. However, for a synchronous non-array read, the same word of data will be output on successive clock edges until the burst length requirements are satisfied. Refer to the timing diagrams for more detailed information.

Read Device Identifier

The Read Device Identifier command instructs the device to output manufacturer code, device identifier code, block-lock status, protection register data, or configuration register data.

Table 12: Device Identifier Information

Item	Address	Data
Manufacturer code	0x00	0x89h
Device ID code	0x01	ID (see the Device ID Codes table)
Block lock configuration:	Block base address + 0x02	Lock bit:
• Block is unlocked		$DQ_0 = 0b0$
• Block is locked		$DQ_0 = 0b1$
• Block is not locked down		$DQ_1 = 0b0$
• Block is locked down		$DQ_1 = 0b1$
Read configuration register	0x05	RCR contents
General purpose register	Device base address + 0x07	General purpose register data
Lock register 0	0x80	PR-LK0 data
64-bit factory-programmed OTP register	0x81–0x84	Factory OTP register data
64-bit user-programmable OTP register	0x85–0x88	User OTP register data
Lock register 1	0x89	PR-LK1 OTP register lock data
128-bit user-programmable protection registers	0x8A–0x109	OTP register data

Table 13: Device ID codes

		Device Identifier Codes	
ID Code Type	Device Density	–T (Top Parameter)	–B (Bottom Parameter)
Device Code	256Mb	8919	891C

Note: 1. The 512Mb devices do not have a unique device ID associated with them. Each die within the stack can be identified by either of the 256Mb Device ID codes depending on its parameter option.

Read CFI

The Read CFI command instructs the device to output Common Flash Interface (CFI) data when read. See READ CFI Structure Output for details on issuing the Read CFI command. The CFI Database: Addresses and Sections table shows CFI information and address offsets within the CFI database.

Program Operation

The device supports three programming methods: Word Programming (40h or 10h), Buffered Programming (E8h, D0h), and Buffered Enhanced Factory Programming (80h, D0h). See Device Command Codes for details on the various programming commands issued to the device. The following sections describe device programming in detail.

Successful programming requires the addressed block to be unlocked. If the block is locked down, WP# must be de-asserted and the block must be unlocked before attempting to program the block. Attempting to program a locked block causes a program error (SR.4 and SR.1 set) and termination of the operation. See Security Modes for details on locking and unlocking blocks.

Word Programming

Word programming operations are initiated by writing the Word Program Setup command to the device (see the Command Codes and Definitions table). This is followed by a second write to the device with the address and data to be programmed. The device outputs status register data when read (see the Word Program Flowchart). V_{PP} must be above V_{PPLK}, and within the specified V_{PPL} min/max values.

During programming, the write state machine (WSM) executes a sequence of internally-timed events that program the desired data bits at the addressed location, and verifies that the bits are sufficiently programmed. Programming the flash memory array changes 1s to 0s. Memory array bits that are 0s can be changed to 1s only by erasing the block (see Erase Operations).

The Status Register can be examined for programming progress and errors by reading at any address. The device remains in the read status register state until another command is written to the device.

Status Register bit SR.7 indicates the programming status while the sequence executes. Commands that can be issued to the device during programming are Program Suspend, Read Status Register, Read Device Identifier, Read CFI, and Read Array (this returns unknown data).

When programming has finished, status register bit SR.4 (when set) indicates a programming failure. If SR.3 is set, the WSM could not perform the word programming operation because V_{PP} was outside of its acceptable limits. If SR.1 is set, the word programming operation attempted to program a locked block, causing the operation to abort.

Before issuing a new command, the status register contents should be examined and then cleared using the Clear Status Register command. Any valid command can follow, when word programming has completed.

Buffered Programming

The device features a 512-word buffer to enable optimum programming performance. For Buffered Programming, data is first written to an on-chip write buffer. Then the buffer data is programmed into the flash memory array in buffer-size increments. This can improve system programming performance significantly over non-buffered programming.

When the Buffered Programming Setup command is issued, Status Register information is updated and reflects the availability of the buffer. SR.7 indicates buffer availability: if set, the buffer is available; if cleared, the buffer is not available.

Note: The device default state is to output SR data after the Buffer Programming Setup Command. CE# and OE# low drive device to update Status Register. It is not allowed to issue 70h to read SR data after E8h command otherwise 70h would be counted as Word Count.

On the next write, a word count is written to the device at the buffer address. This tells the device how many data words will be written to the buffer, up to the maximum size of the buffer.

On the next write, a device start address is given along with the first data to be written to the flash memory array. Subsequent writes provide additional device addresses and data. All data addresses must lie within the start address plus the word count. Optimum programming performance and lower power usage are obtained by aligning the starting address at the beginning of a 512-word boundary (A[9:1] = 0x00 for Easy BGA and TSOP, A[8:0] for QUAD+ package). The maximum buffer size would be 256-word if the misaligned address range is crossing a 512-word boundary during programming.

After the last data is written to the buffer, the Buffered Programming Confirm command must be issued to the original block address. The WSM begins to program buffer contents to the flash memory array. If a command other than the Buffered Programming Confirm command is written to the device, a command sequence error occurs and Status Register bits SR[7,5,4] are set. If an error occurs while writing to the array, the device stops programming, and Status Register bits SR[7,4] are set, indicating a programming failure.

When Buffered Programming has completed, additional buffer writes can be initiated by issuing another Buffered Programming Setup command and repeating the buffered program sequence. Buffered programming may be performed with $V_{PP} = V_{PPL}$ or V_{PPH} (see Operating Conditions for limitations when operating the device with $V_{PP} = V_{PPH}$).

If an attempt is made to program past an erase-block boundary using the Buffered Program command, the device aborts the operation. This generates a command sequence error, and Status Register bits SR[5,4] are set.

If Buffered programming is attempted while V_{PP} is at or below V_{PPLK}, Status Register bits SR[4,3] are set. If any errors are detected that have set Status Register bits, the Status Register should be cleared using the Clear Status Register command.

Buffered Enhanced Factory Programming

Buffered Enhanced Factory Programing (BEFP) speeds up multilevel cell (MLC) flash programming. The enhanced programming algorithm used in BEFP eliminates traditional programming elements that drive up overhead in device programmer systems.

BEFP consists of three phases: Setup, Program/Verify, and Exit (see the BEFP Flowchart). It uses a write buffer to spread MLC program performance across 512 data words. Verification occurs in the same phase as programming to accurately program the flash memory cell to the correct bit state.

A single two-cycle command sequence programs the entire block of data. This enhancement eliminates three write cycles per buffer: two commands and the word count for each set of 512 data words. Host programmer bus cycles fill the device write buffer

followed by a status check. SR.0 indicates when data from the buffer has been programmed into sequential flash memory array locations.

Following the buffer-to-flash array programming sequence, the write state machine (WSM) increments internal addressing to automatically select the next 512-word array boundary. This aspect of BEFP saves host programming equipment the address bus setup overhead.

With adequate continuity testing, programming equipment can rely on the WSM's internal verification to ensure that the device has programmed properly. This eliminates the external post-program verification and its associated overhead.

BEFP Requirements and Considerations

Table 14: BEFP Requirements

Parameter/Issue	Requirement	Notes
Case Temperature	T_C = 30°C ± 10 °C	
V_{CC}	Nominal V_{CC}	
V_{PP}	Driven to V_{PPH}	
Setup and Confirm	Target block must be unlocked before issuing the BEFP Setup and Confirm commands.	
Programming	The first-word address (WA0) of the block to be programmed must be held constant from the setup phase through all data streaming into the target block, until transition to the exit phase is desired.	
Buffer Alignment	WA0 must align with the start of an array buffer boundary.	1

Note: 1. Word buffer boundaries in the array are determined by A[9:1] for Easy BGA and TSOP; A[8:0] for QUAD+ package (0x000 through 0x1FF). The alignment start point is A[9:1] = 0x000 for Easy BGA and TSOP; A[8:0] = 0x000 for QUAD+ package.

Table 15: BEFP Considerations

Parameter/Issue	Requirement	Notes
Cycling	For optimum performance, cycling must be limited below 50 erase cycles per block.	1
Programming blocks	BEFP programs one block at a time; all buffer data must fall within a single block.	2
Suspend	BEFP cannot be suspended.	
Programming the flash memory array	Programming to the flash memory array can occur only when the buffer is full.	3

Notes: 1. Some degradation in performance may occur if this limit is exceeded, but the internal algorithm continues to work properly.
2. If the internal address counter increments beyond the block's maximum address, addressing wraps around to the beginning of the block.
3. If the number of words is less than 512, remaining locations must be filled with 0xFFFF.

BEFP Setup Phase

After receiving the BEFP Setup and Confirm command sequence, Status Register bit SR.7 (Ready) is cleared, indicating that the WSM is busy with BEFP algorithm startup. A delay before checking SR.7 is required to allow the WSM enough time to perform all of its setups and checks (Block-Lock status, V_{PP} level, etc.). If an error is detected, SR.4 is set

and BEFP operation terminates. If the block was found to be locked, SR.1 is also set. SR. 3 is set if the error occurred due to an incorrect V_{PP} level.

Note: Reading from the device after the BEFP Setup and Confirm command sequence outputs status register data. Do not issue the Read Status Register command; it will be interpreted as data to be loaded into the buffer.

BEFP Program/Verify Phase

After the BEFP Setup Phase has completed, the host programming system must check SR[7,0] to determine the availability of the write buffer for data streaming. SR.7 cleared indicates the device is busy and the BEFP program/verify phase is activated. SR.0 indicates the write buffer is available.

Two basic sequences repeat in this phase: loading of the write buffer, followed by buffer data programming to the array. For BEFP, the count value for buffer loading is always the maximum buffer size of 512 words. During the buffer-loading sequence, data is stored to sequential buffer locations starting at address 0x00. Programming of the buffer contents to the flash memory array starts as soon as the buffer is full. If the number of words is less than 512, the remaining buffer locations must be filled with 0xFFFF.

Note: The buffer must be completely filled for programming to occur. Supplying an address outside of the current block's range during a buffer-fill sequence causes the algorithm to exit immediately. Any data previously loaded into the buffer during the fill cycle is not programmed into the array.

The starting address for data entry must be buffer size aligned, if not the BEFP algorithm will be aborted and the program fails and (SR.4) flag will be set.

Data words from the write buffer are directed to sequential memory locations in the flash memory array; programming continues from where the previous buffer sequence ended. The host programming system must poll SR.0 to determine when the buffer program sequence completes. SR.0 cleared indicates that all buffer data has been transferred to the flash array; SR.0 set indicates that the buffer is not available yet for the next fill cycle. The host system may check full status for errors at any time, but it is only necessary on a block basis after BEFP exit. After the buffer fill cycle, no write cycles should be issued to the device until SR.0 = 0 and the device is ready for the next buffer fill.

Note: Any spurious writes are ignored after a buffer fill operation and when internal program is proceeding.

The host programming system continues the BEFP algorithm by providing the next group of data words to be written to the buffer. Alternatively, it can terminate this phase by changing the block address to one outside of the current block's range.

The Program/Verify phase concludes when the programmer writes to a different block address; data supplied must be 0xFFFF. Upon Program/Verify phase completion, the device enters the BEFP Exit phase.

BEFP Exit Phase

When SR.7 is set, the device has returned to normal operating conditions. A full status check should be performed at this time to ensure the entire block programmed successfully. When exiting the BEFP algorithm with a block address change, the read mode will not change. After BEFP exit, any valid command can be issued to the device.

Program Suspend

Issuing the Program Suspend command while programming suspends the programming operation. This allows data to be accessed from the device other than the one being programmed. The Program Suspend command can be issued to any device address. A program operation can be suspended to perform reads only. Additionally, a program operation that is running during an erase suspend can be suspended to perform a read operation.

When a programming operation is executing, issuing the Program Suspend command requests the WSM to suspend the programming algorithm at predetermined points. The device continues to output Status Register data after the Program Suspend command is issued. Programming is suspended when Status Register bits SR[7,2] are set.

To read data from the device, the Read Array command must be issued. Read Array, Read Status Register, Read Device Identifier, Read CFI, and Program Resume are valid commands during a program suspend.

During a program suspend, deasserting CE# places the device in standby, reducing active current. V_{PP} must remain at its programming level, and WP# must remain unchanged while in program suspend. If RST# is asserted, the device is reset.

Program Resume

The Resume command instructs the device to continue programming, and automatically clears Status Register bits SR[7,2]. This command can be written to any address. If error bits are set, the Status Register should be cleared before issuing the next instruction. RST# must remain deasserted.

Program Protection

When $V_{PP} = V_{IL}$, absolute hardware write protection is provided for all device blocks. If V_{PP} is at or below V_{PPLK}, programming operations halt and SR.3 is set indicating a V_{PP}-level error. Block lock registers are not affected by the voltage level on V_{PP}; they may still be programmed and read, even if V_{PP} is less than V_{PPLK}.

Figure 11: Example VPP Supply Connections
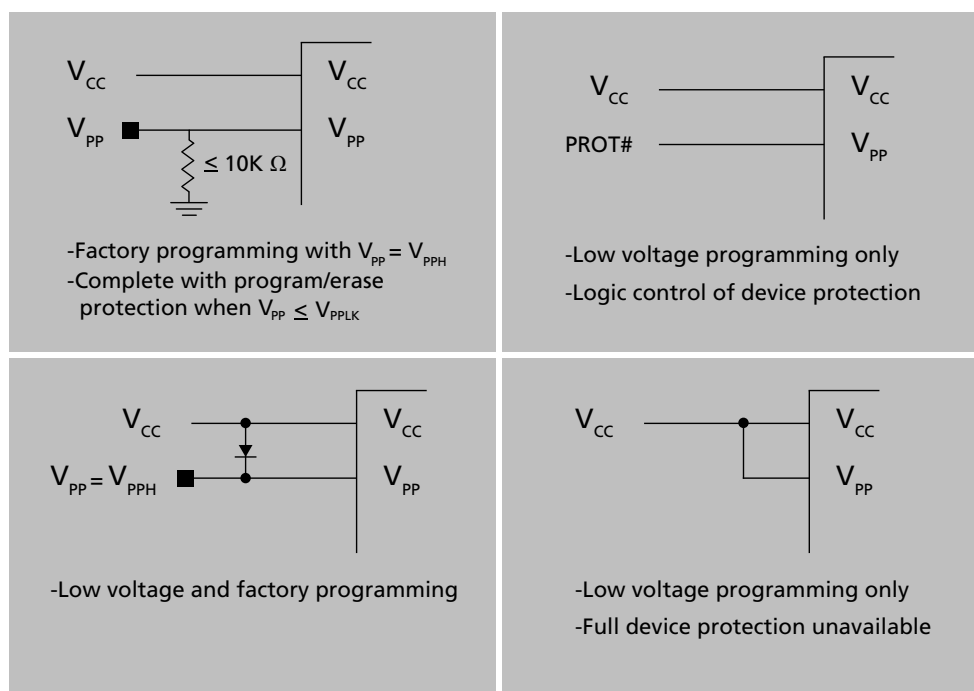
Erase Operations

Flash erasing is performed on a block basis. An entire block is erased each time an erase command sequence is issued, and only one block is erased at a time. When a block is erased, all bits within that block read as logical ones. The following sections describe block erase operations in detail.

Block Erase

Block erase operations are initiated by writing the Block Erase Setup command to the address of the block to be erased. Next, the Block Erase Confirm command is written to the address of the block to be erased. If the device is placed in standby (CE# deasserted) during an erase operation, the device completes the erase operation before entering standby. The V_{PP} value must be above V_{PPLK} and the block must be unlocked.

During a block erase, the Write State Machine (WSM) executes a sequence of internally-timed events that conditions, erases, and verifies all bits within the block. Erasing the flash memory array changes "zeros" to "ones". Memory block array that are ones can be changed to zeros only by programming the block.

The Status Register can be examined for block erase progress and errors by reading any address. The device remains in the Read Status Register state until another command is written. SR.0 indicates whether the addressed block is erasing. Status Register bit SR.7 is set upon erase completion.

Status Register bit SR.7 indicates block erase status while the sequence executes. When the erase operation has finished, Status Register bit SR.5 indicates an erase failure if set. SR.3 set would indicate that the WSM could not perform the erase operation because V_{PP} was outside of its acceptable limits. SR.1 set indicates that the erase operation attempted to erase a locked block, causing the operation to abort.

Before issuing a new command, the Status Register contents should be examined and then cleared using the Clear Status Register command. Any valid command can follow once the block erase operation has completed.

The Block Erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

Blank Check

The Blank Check operation determines whether a specified main block is blank; that is, completely erased. Without Blank Check, Block Erase would be the only other way to ensure a block is completely erased. Blank Check is especially useful in the case of erase operation interrupted by a power loss event.

Blank check can apply to only one block at a time, and no operations other than Status Register Reads are allowed during Blank Check (e.g. reading array data, program, erase etc). Suspend and resume operations are not supported during Blank Check, nor is Blank Check supported during any suspended operations.

Blank Check operations are initiated by writing the Blank Check Setup command to the block address. Next, the Check Confirm command is issued along with the same block address. When a successful command sequence is entered, the device automatically enters the Read Status State. The WSM then reads the entire specified block, and determines whether any bit in the block is programmed or over-erased.

The status register can be examined for Blank Check progress and errors by reading any address within the block being accessed. During a blank check operation, the Status Register indicates a busy status (SR.7 = 0). Upon completion, the Status Register indicates a ready status (SR.7 = 1). The Status Register should be checked for any errors, and then cleared. If the Blank Check operation fails, which means the block is not completely erased, the Status Register bit SR.5 will be set ("1"). CE# or OE# toggle (during polling) updates the Status Register.

After examining the Status Register, it should be cleared by the Clear Status Register command before issuing a new command. The device remains in Status Register Mode until another command is written to the device. Any command can follow once the Blank Check command is complete.

Erase Suspend

Issuing the Erase Suspend command while erasing suspends the block erase operation. This allows data to be accessed from memory locations other than the one being erased. The Erase Suspend command can be issued to any device address. A block erase operation can be suspended to perform a word or buffer program operation, or a read operation within any block except the block that is erase suspended.

When a block erase operation is executing, issuing the Erase Suspend command requests the WSM to suspend the erase algorithm at predetermined points. The device continues to output Status Register data after the Erase Suspend command is issued. Block erase is suspended when Status Register bits SR[7,6] are set.

To read data from the device (other than an erase-suspended block), the Read Array command must be issued. During Erase Suspend, a Program command can be issued to any block other than the erase-suspended block. Block erase cannot resume until program operations initiated during erase suspend complete. Read Array, Read Status Register, Read Device Identifier, Read CFI, and Erase Resume are valid commands during Erase Suspend. Additionally, Clear Status Register, Program, Program Suspend, Block Lock, Block Unlock, and Block Lock-Down are valid commands during Erase Suspend.

During an erase suspend, deasserting CE# places the device in standby, reducing active current. V_{PP} must remain at a valid level, and WP# must remain unchanged while in erase suspend. If RST# is asserted, the device is reset.

Erase Resume

The Erase Resume command instructs the device to continue erasing, and automatically clears status register bits SR[7,6]. This command can be written to any address. If status register error bits are set, the Status Register should be cleared before issuing the next instruction. RST# must remain deasserted.

Erase Protection

When $V_{PP} = V_{IL}$, absolute hardware erase protection is provided for all device blocks. If V_{PP} is at or below V_{PPLK}, erase operations halt and SR.3 is set indicating a V_{PP}-level error.

Security Modes

The device features security modes used to protect the information stored in the flash memory array. The following sections describe each security mode in detail.

Block Locking

Individual instant block locking is used to protect user code and/or data within the flash memory array. All blocks power-up in a locked state to protect array data from being altered during power transitions. Any block can be locked or unlocked with no latency. Locked blocks cannot be programmed or erased; they can only be read.

Software-controlled security is implemented using the Block Lock and Block Unlock commands. Hardware-controlled security can be implemented using the Block Lock-Down command along with asserting WP#. Also, V_{PP} data security can be used to inhibit program and erase operations.

Lock Block

To lock a block, issue the Block Lock Setup command, followed by the Block Lock command issued to the desired block's address. If the Set Read Configuration Register command is issued after the Block Lock Setup command, the device configures the RCR instead.

Block lock and unlock operations are not affected by the voltage level on V_{PP}. The block lock bits may be modified and/or read even if V_{PP} is at or below V_{PPLK}.

Unlock Block

The Block Unlock command is used to unlock blocks. Unlocked blocks can be read, programmed, and erased. Unlocked blocks return to a locked state when the device is reset or powered down. If a block is in a lock-down state, WP# must be deasserted before it can be unlocked.

Lock-Down Block

A locked or unlocked block can be locked-down by writing the Block Lock-Down command sequence. Blocks in a lock-down state cannot be programmed or erased; they can only be read. However, unlike locked blocks, their locked state cannot be changed by software commands alone. A locked-down block can only be unlocked by issuing the Block Unlock command with WP# deasserted. To return an unlocked block to locked-down state, a Block Lock-Down command must be issued prior to changing WP# to V_{IL}. Locked-down blocks revert to the locked state upon reset or power up the device.

Block Lock Status

The Read Device Identifier command is used to determine a block's lock status. Data bits DQ[1:0] display the addressed block's lock status; DQ0 is the addressed block's lock bit, while DQ1 is the addressed block's lock-down bit.

Figure 12: Block Locking State Diagram
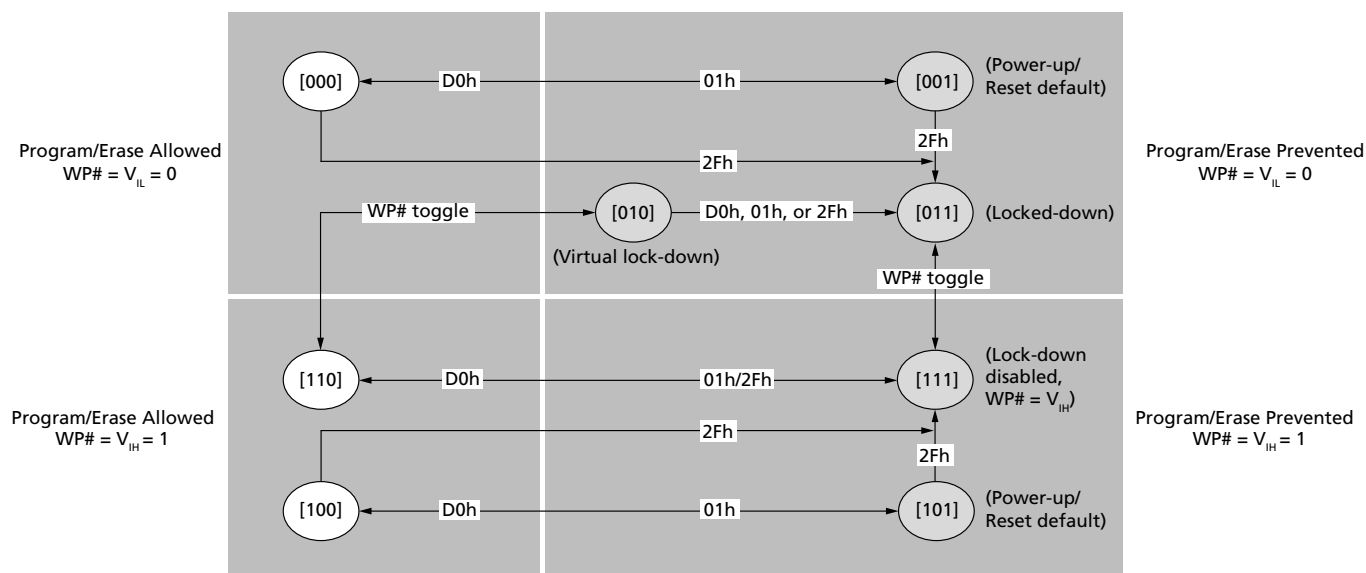
Note: 1. D0h = UNLOCK command; 01h = LOCK command; 60h (not shown) LOCK SETUP command; 2Fh = LOCK-DOWN command.

Block Locking During Suspend

Block lock and unlock changes can be performed during an erase suspend. To change block locking during an erase operation, first issue the Erase Suspend command. Monitor the Status Register until SR.7 and SR.6 are set, indicating the device is suspended and ready to accept another command.

Next, write the desired lock command sequence to a block, which changes the lock state of that block. After completing block lock or unlock operations, resume the erase operation using the Erase Resume command.

Note:

A Lock Block Setup command followed by any command other than Lock Block, Unlock Block, or Lock-Down Block produces a command sequence error and set Status Register bits SR.4 and SR.5. If a command sequence error occurs during an erase suspend, SR.4 and SR.5 remains set, even after the erase operation is resumed. Unless the Status Register is cleared using the Clear Status Register command before resuming the erase operation, possible erase errors may be masked by the command sequence error.

If a block is locked or locked-down during an erase suspend of the *same* block, the lock status bits change immediately. However, the erase operation completes when it is resumed. Block lock operations cannot occur during a program suspend.

Selectable One-Time Programmable Blocks

The OTP security feature on P30-65nm device is backward compatible to the P30-130nm device. Contact your local Micron representative for details about its implementation.

Password Access

The Password Access is a security enhancement offered on the P30-65nm device. This feature protects information stored in array blocks by preventing content alteration or reads until a valid 64-bit password is received. The Password Access may be combined with Non-Volatile Protection and/or Volatile Protection to create a multi-tiered solution.

Contact your Micron sales office for further details concerning Password Access.

Registers

When non-array reads are performed in asynchronous page mode only the first data is valid and all subsequent data are undefined. When a non-array read operation occurs as synchronous burst mode, the same word of data requested will be output on successive clock edges until the burst length requirements are satisfied.

Read Status Register

To read the Status Register, issue the Read Status Register command at any address. Status Register information is available to which the Read Status Register, Word Program, or Block Erase command was issued. Status Register data is automatically made available following a Word Program, Block Erase, or Block Lock command sequence. Reads from the device after any of these command sequences outputs the device's status until another valid command is written (e.g. Read Array command).

The Status Register is read using single asynchronous-mode or synchronous burst mode reads. Status Register data is output on DQ[7:0], while 0x00 is output on DQ[15:8]. In asynchronous mode the falling edge of OE#, or CE# (whichever occurs first) updates and latches the Status Register contents. However, reading the Status Register in synchronous burst mode, CE# or ADV# must be toggled to update status data.

The Device Write Status bit (SR.7) provides overall status of the device. Status register bits SR[6:1] present status and error information about the program, erase, suspend, V_{PP}, and block-locked operations.

Table 16: Status Register Description

Bit	Name		Description		
7	Device Ready Status (DWS)		0 = Device is busy; program or erase cycle in progress; SR.0 valid. 1 = Device is ready; SR[6:1] are valid.		
6	Erase Suspend Status (ESS)		0 = Erase suspend not in effect. 1 = Erase suspend in effect.		
5	Erase /Blank Check Status (ES)	Command Sequence Error	SR.5	SR.4	Description
4	Program Status (PS)		0 0 1 1	0 1 0 1	Program or Erase operation successful. Program error - operation aborted. Erase or Blank check error - operation aborted. Command sequence error - command aborted.
3	V_{PP} Status (VPPS)		0 = VPP within acceptable limits during program or erase operation. 1 = VPP ≤ VPPLK during program or erase operation.		
2	Program Suspend Status (PSS)		0 = Program suspend not in effect. 1 = Program suspend in effect.		
1	Block-Locked Status (BLS)		0 = Block not locked during program or erase. 1 = Block locked during program or erase; operation aborted.		
0	BEFP Status (BWS)		After Buffered Enhanced Factory Programming (BEFP) data is loaded into the buffer: 0 = BEFP complete. 1 = BEFP in-progress.		

Notes: 1. Default Value = 0x80

2. Always clear the Status Register prior to resuming erase operations. It avoids Status Register ambiguity when issuing commands during Erase Suspend. If a command sequence error occurs during an erase-suspend state, the Status Register contains the command sequence error status (SR[7,5,4] set). When the erase operation resumes and finishes, possible errors during the erase operation cannot be detected via the Status Register because it contains the previous error status.

3. A Clear SR command (50h) or Reset must be issued with 15µs delay after the Error bits (SR4 or SR5) is set during Program/Erase operations.

Clear Status Register

The Clear Status Register command clears the status register. It functions independent of V_{PP}. The Write State Machine (WSM) sets and clears SR[7,6,2], but it sets bits SR[5:3,1] without clearing them. The Status Register should be cleared before starting a command sequence to avoid any ambiguity. A device reset also clears the Status Register.

Read Configuration Register

The Read Configuration Register (RCR) is a 16-bit read/write register used to select bus-read mode (synchronous or asynchronous), and to configure device synchronous burst read characteristics. To modify RCR settings, use the Configure Read Configuration Register command. RCR contents can be examined using the Read Device Identifier command, and then reading from offset 0x05. On power-up or exit from reset, the RCR defaults to asynchronous mode. Details about each RCR bit follow the table.

Table 17: Read Configuration Register

Bit	Name	Description		
15	Read mode (RM)	0 = Synchronous burst-mode read 1 = Asynchronous page-mode read (default)		
14:11	Latency count (LC[3:0])	0000 = Code 0 (reserved) 0001 = Code 1 (reserved) 0010 = Code 2 0011 = Code 3 0100 = Code 4 0101 = Code 5	0110 = Code 6 0111 = Code 7 1000 = Code 8 1001 = Code 9 1010 = Code 10	1011 = Code11 1100 = Code 12 1101 = Code 13 1110 = Code 14 1111 = Code 15 (default)
10	WAIT polarity (WP)	0 = WAIT signal is active low (default) 1 = WAIT signal is active high		
9	Reserved (R)	Default 0, Non-changeable		
8	WAIT delay (WD)	0 = WAIT deasserted with valid data 1 = WAIT deasserted one data cycle before valid data (default)		
7	Burst sequence (BS)	Default 0, Non-changeable		
6	Clock edge (CE)	0 = Falling edge 1 = Rising edge (default)		
5:4	Reserved (R)	Default 0, Non-changeable		
3	Burst wrap (BW)	0 = Wrap; Burst accesses wrap within burst length set by BL[2:0] 1 = No Wrap; Burst accesses do not wrap within burst length (default)		
2:0	Burst length (BL[2:0])	001 = 4-word burst 010 = 8-word burst	011 = 16-word burst 111 = Continuous-word burst (default) (Other bit settings are reserved)	

Read Mode

The Read Mode (RM) bit selects synchronous burst-mode or asynchronous page-mode operation for the device. When the RM bit is set, asynchronous page mode is selected (default). When RM is cleared, synchronous burst mode is selected.

Latency Count

The Latency Count (LC) bits tell the device how many clock cycles must elapse from the rising edge of ADV# (or from the first valid clock edge after ADV# is asserted) until the first valid data word is to be driven onto DQ[15:0]. The input clock frequency is used to determine this value and the First Access Latency Count figure shows the data output latency for the different settings of LC. The minimum Latency Count for P30-65nm would be Code 4 based on the Max Clock frequency specification of 52 MHz, and there will be zero WAIT States when bursting within the word line. Refer to End of Word Line Considerations for more information on EOWL, and the Latency Count and Frequency Support table for latency code settings.

Figure 13: First Access Latency Count
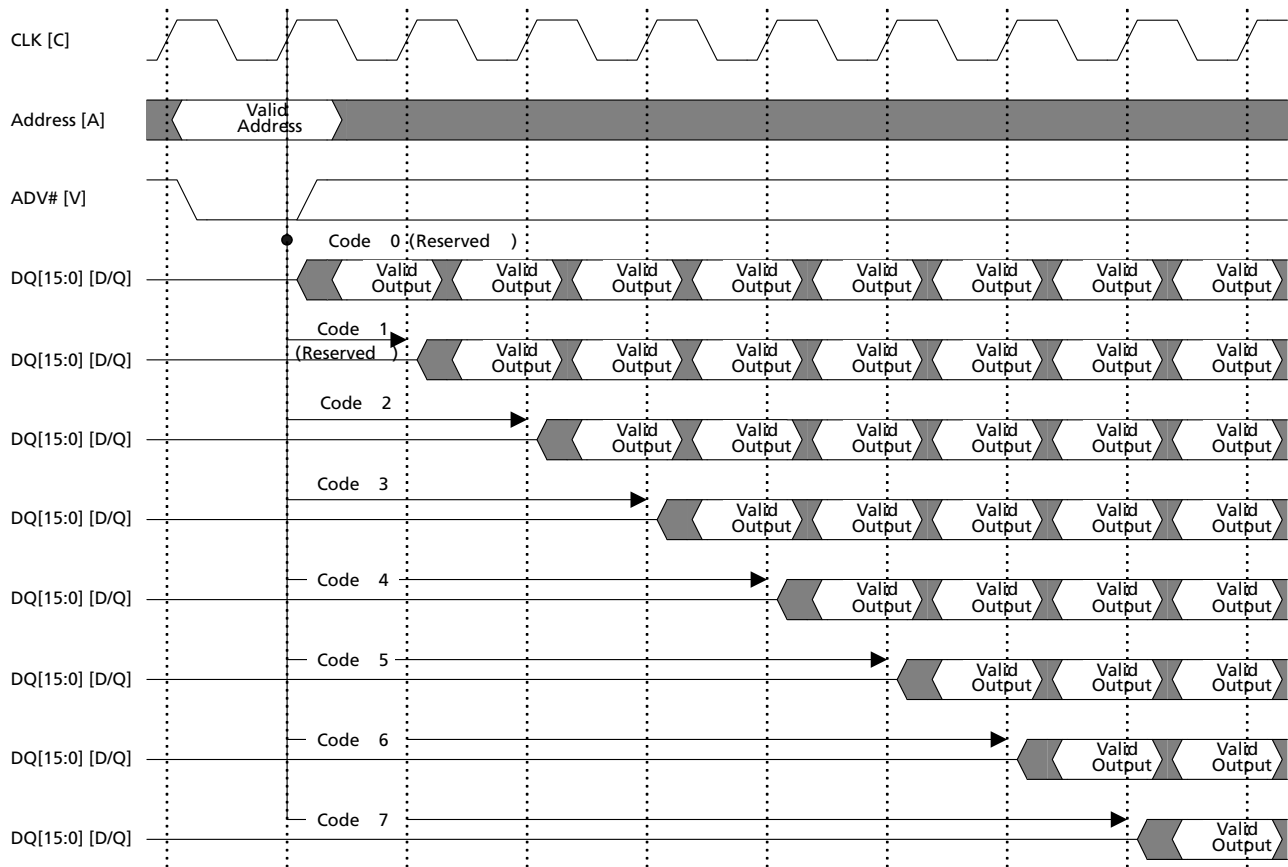
Table 18: Latency Count and Frequency Support

Latency Count Settings	Frequency Support (MHz)
5 (TSOP); 4 (Easy BGA)	≤ 40
5 (Easy BGA)	≤ 52

Figure 14: Example Latency Count Setting Using Code 3
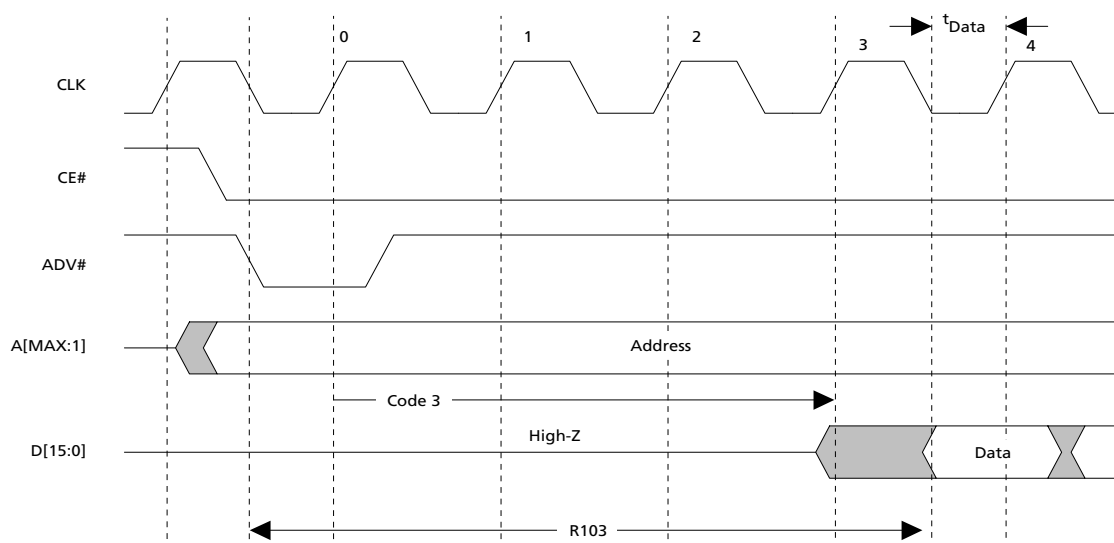
End of Word Line (EOWL) Considerations

End of Wordline (EOWL) WAIT states can result when the starting address of the burst operation is not aligned to a 16-word boundary; that is, A[3:0] of start address does not equal 0x0. The End of Wordline Timing Diagram illustrates the end of wordline WAIT state(s) that occur after the first 16-word boundary is reached. The number of data words and the number of WAIT states is summarized in the End of Wordline Data and WAIT State Comparison table for both P30-130nm and P30-65nm devices.

Figure 15: End of Wordline Timing Diagram
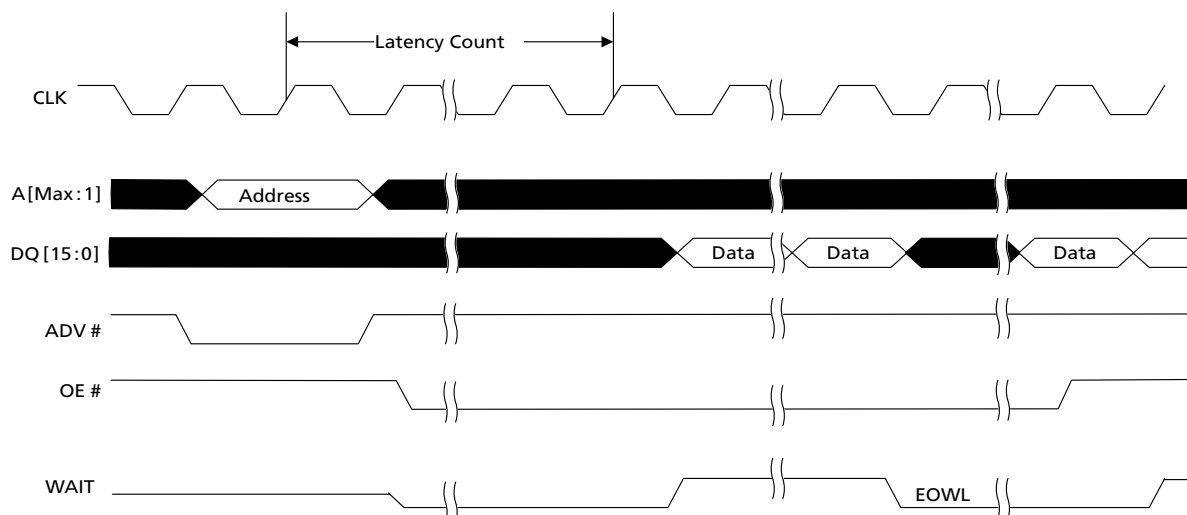
Table 19: End of Wordline Data and WAIT State Comparison

	P30-130nm		P30-65nm	
Latency Count	Data States	WAIT States	Data States	WAIT States
1	Not Supported	Not Supported	Not Supported	Not Supported
2	4	0 to 1	16	0 to 1
3	4	0 to 2	16	0 to 2
4	4	0 to 3	16	0 to 3
5	4	0 to 4	16	0 to 4
6	4	0 to 5	16	0 to 5
7	4	0 to 6	16	0 to 6
8	Not Supported	Not Supported	16	0 to 7
9			16	0 to 8
10			16	0 to 9
11			16	0 to 10
12			16	0 to 11
13			16	0 to 12
14			16	0 to 13
15			16	0 to 14

WAIT Signal Polarity and Functionality

The WAIT Polarity bit (WP), RCR.10 determines the asserted level (V_{OH} or V_{OL}) of WAIT. When WP is set, WAIT is asserted high (default). When WP is cleared, WAIT is asserted low. WAIT changes state on valid clock edges during active bus cycles (CE# asserted, OE# asserted, RST# deasserted).

The WAIT signal indicates data valid when the device is operating in synchronous mode (RCR.15 =0). The WAIT signal is only deasserted when data is valid on the bus. When the device is operating in synchronous non-array read mode, such as read status, read ID, or read CFI, the WAIT signal is also deasserted when data is valid on the bus. WAIT behavior during synchronous non-array reads at the end of word line works correctly only on the first data access. When the device is operating in asynchronous page mode, asynchronous single word read mode, and all write operations, WAIT is set to a deasserted state as determined by RCR.10.

Table 20: WAIT Functionality Table

Condition	WAIT	Notes
CE# = '1', OE# = 'X' or CE# = '0', OE# = '1'	High-Z	1, 2
CE# ='0', OE# = '0'	Active	1
Synchronous Array Reads	Active	1
Synchronous Non-Array Reads	Active	1
All Asynchronous Reads	Deasserted	1
All Writes	High-Z	1, 2

Notes: 1. Active means that WAIT is asserted until data becomes valid, then desserts.
2. When OE# = V_{IH} during writes, WAIT = High-Z.

WAIT Delay

The WAIT Delay (WD) bit controls the WAIT assertion-delay behavior during synchronous burst reads. WAIT can be asserted either during or one data cycle before valid data is output on DQ[15:0]. When WD is set, WAIT is deasserted one data cycle *before* valid data (default). When WD is cleared, WAIT is deasserted *during* valid data.

Burst Sequence

The Burst Sequence (BS) bit selects linear-burst sequence (default). Only linear-burst sequence is supported. The synchronous burst sequence for all burst lengths, as well as the effect of the Burst Wrap (BW) setting are shown here.

Table 21: Burst Sequence Word Ordering

Start Address (DEC)	Burst Wrap (RCR.3)	Burst Addressing Sequence (DEC)			
		4-Word Burst (BL[2:0] = 0b001)	8-Word Burst (BL[2:0] = 0b010)	16-Word Burst (BL[2:0] = 0b011)	Continuous Burst (BL[2:0] = 0b111)
0	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6-…
1	0	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5…15-0	1-2-3-4-5-6-7-…
2	0	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6…15-0-1	2-3-4-5-6-7-8-…
3	0	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7…15-0-1-2	3-4-5-6-7-8-9-…
4	0		4-5-6-7-0-1-2-3	4-5-6-7-8…15-0-1-2-3	4-5-6-7-8-9-10…
5	0		5-6-7-0-1-2-3-4	5-6-7-8-9…15-0-1-2-3-4	5-6-7-8-9-10-11…
6	0		6-7-0-1-2-3-4-5	6-7-8-9-10…15-0-1-2-3-4-5	6-7-8-9-10-11-12-…
7	0		7-0-1-2-3-4-5-6	7-8-9-10…15-0-1-2-3-4-5-6	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	0			14-15-0-1-2…12-13	14-15-16-17-18-19-20-…
15	0			15-0-1-2-3…13-14	15-16-17-18-19-20-21-…
⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6-…
1	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5…15-16	1-2-3-4-5-6-7-…
2	1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6…16-17	2-3-4-5-6-7-8-…
3	1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7…17-18	3-4-5-6-7-8-9-…
4	1		4-5-6-7-8-9-10-11	4-5-6-7-8…18-19	4-5-6-7-8-9-10…
5	1		5-6-7-8-9-10-11-12	5-6-7-8-9…19-20	5-6-7-8-9-10-11…
6	1		6-7-8-9-10-11-12-13	6-7-8-9-10…20-21	6-7-8-9-10-11-12-…
7	1		7-8-9-10-11-12-13-14	7-8-9-10-11…21-22	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	1			14-15-16-17-18…28-29	14-15-16-17-18-19-20-…
15	1			15-16-17-18-19…29-30	15-16-17-18-19-20-21-…

Clock Edge

The Clock Edge (CE) bit selects either a rising (default) or falling clock edge for CLK. This clock edge is used at the start of a burst cycle, to output synchronous data, and to assert/deassert WAIT.

Burst Wrap

The Burst Wrap (BW) bit determines whether 4-word, 8-word, or 16-word burst length accesses wrap within the selected word-length boundaries or cross word-length boundaries. When BW is set, burst wrapping does not occur (default). When BW is cleared, burst wrapping occurs.

When performing synchronous burst reads with BW set (no wrap), an output delay may occur when the burst sequence crosses its first device-row (16-word) boundary. If the burst sequence's start address is 4-word aligned, then no delay occurs. If the start address is at the end of a 4-word boundary, the worst case output delay is one clock cycle less than the first access Latency Count. This delay can take place only once, and doesn't occur if the burst sequence does not cross a device-row boundary. WAIT informs the system of this delay when it occurs.

Burst Length

The Burst Length bits (BL[2:0]) select the linear burst length for all synchronous burst reads of the flash memory array. The burst lengths are 4-word, 8-word, 16-word or continuous.

Continuous-burst accesses are linear only, and do not wrap within any word length boundaries. When a burst cycle begins, the device outputs synchronous burst data until it reaches the end of the "burstable" address space.

One-Time-Programmable (OTP) Registers

The device contains 17 one-time programmable (OTP) registers that can be used to implement system security measures and/or device identification. Each OTP register can be individually locked.

The first 128-bit OTP Register is comprised of two 64-bit (8-word) segments. The lower 64-bit segment is pre-programmed at the Micron factory with a unique 64-bit number. The upper 64-bit segment, as well as the other sixteen 128-bit OTP Registers, are blank. Users can program these registers as needed. Once programmed, users can then lock the OTP Register(s) to prevent additional bit programming (see the OTP Register Map figure).

The OTP Registers contain one-time programmable (OTP) bits; when programmed, PR bits cannot be erased. Each OTP Register can be accessed multiple times to program individual bits, as long as the register remains unlocked.

Each OTP Register has an associated Lock Register bit. When a Lock Register bit is programmed, the associated OTP Register can only be read; it can no longer be programmed. Additionally, because the Lock Register bits themselves are OTP, when programmed, Lock Register bits cannot be erased. Therefore, when a OTP Register is locked, it cannot be unlocked.

Figure 16: OTP Register Map
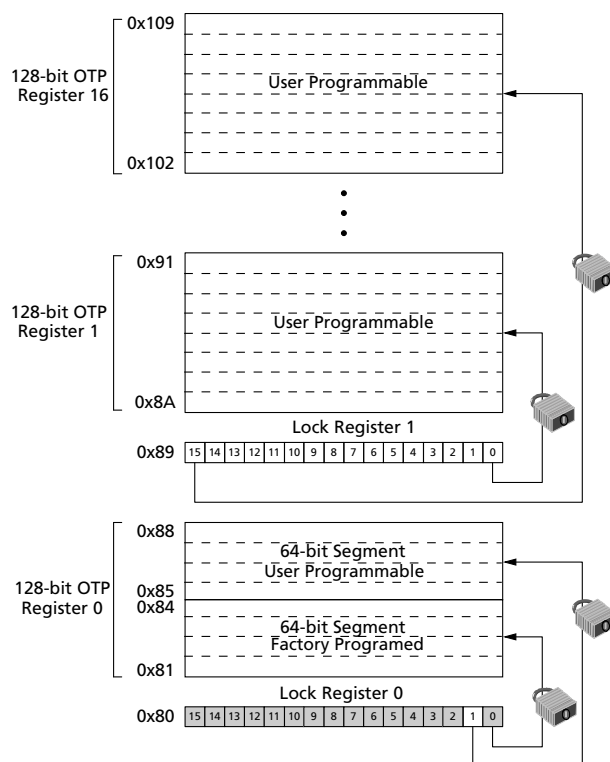
Reading the OTP Registers

The OTP Registers can be read from OTP-RA address. To read the OTP Register, first issue the Read Device Identifier command at OTP-RA address to place the device in the Read Device Identifier state. Next, perform a read operation using the address offset corresponding to the register to be read. The Device Identifier Information table shows the address offsets of the OTP Registers and Lock Registers. PR data is read 16 bits at a time.

Programming the OTP Registers

To program an OTP Register, first issue the Program OTP Register command at the parameter's base address plus the offset of the desired OTP Register location. Next, write the desired OTP Register data to the same OTP Register address.

The device programs the 64-bit and 128-bit user-programmable OTP Register data 16 bits at a time. Issuing the Program OTP Register command outside of the OTP Register's address space causes a program error (SR.4 set). Attempting to program a locked OTP Register causes a program error (SR.4 set) and a lock error (SR.1 set).
Note:

When programming the OTP bits in the OTP registers for a **Top Parameter Device**, the following upper address bits must also be driven properly: A[Max:17] driven high (V_{IH}) for TSOP and Easy BGA packages, and A[Max:16] driven high (V_{IH}) for QUAD+ SCSP.

Locking the OTP Registers

Each OTP Register can be locked by programming its respective lock bit in the Lock Register. To lock an OTP Register, program the corresponding bit in the Lock Register by issuing the Program Lock Register command, followed by the desired Lock Register data. The physical addresses of the Lock Registers are 0x80 for register 0 and 0x89 for register 1. These addresses are used when programming the lock registers.

Bit 0 of Lock Register 0 is already programmed during the manufacturing process, locking the lower half segment of the first 128-bit OTP Register. Bit 1 of Lock Register 0 can be programmed by user to the upper half segment of the first 128-bit OTP Register. When programming Bit 1 of Lock Register 0, all other bits need to be left as '1' such that the data programmed is 0xFFFD.

Lock Register 1 controls the locking of the upper sixteen 128-bit OTP Registers. Each bit of Lock Register 1 corresponds to a specific 128-bit OTP Register. Programming a bit in Lock Register 1 locks the corresponding 128-bit OTP Register; e.g., programming LR1.0 locks the corresponding OTP Register 1.

Note: After being locked, the OTP Registers cannot be unlocked.

Common Flash Interface

The Common Flash Interface (CFI) is part of an overall specification for multiple command-set and control-interface descriptions. System software can parse the CFI database structure to obtain information about the Flash device, such as block size, density, bus width, and electrical specifications. The system software determines which command set to use to properly perform a Flash WRITE command, a block ERASE or READ command, and to otherwise control the flash device. Information in the CFI database can be viewed by issuing the READ CFI command.

READ CFI Structure Output

The READ CFI command obtains CFI database structure information and always outputs it on the lower byte, DQ[7:0], for a word-wide (x16) Flash device. This CFI-compliant device always outputs 00h data on the upper byte (DQ[15:8]).

The numerical offset value is the address relative to the maximum bus width the Flash device supports. For this Flash device family, the starting address is a 10h, which is a word address for x16 devices. For example, at this starting address of 10h, a READ CFI command outputs an ASCII Q in the lower byte and 00h in the higher byte as shown here.

In all the CFI tables shown here, address and data are represented in hexadecimal notation. In addition, since the upper byte of word-wide devices is always 00h as shown in the example here, the leading 00 has been dropped and only the lower byte value is shown. Following is a table showing the CFI output for a x16 device, beginning at address 10h and a table showing an overview of the CFI database sections with their addresses.

Table 22: Example of CFI Output (x16 device) as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII Value (DQ[15:8])	ASCII Value (DQ[7:0])
Address	00010:	51	00	Q
	00011:	52	00	R
	00012:	59	00	Y
	00013:	P_ID_{LO}	00	Primary vendor ID
	00014:	P_ID_{HI}	00	
	00015:	P_{LO}	00	Primary vendor table address
	00016:	P_{HI}	00	
	00017:	A_ID_{LO}	00	Alternate vendor ID
	00018:	A_ID_{HI}	00	
	⋮	⋮	⋮	⋮

Table 23: CFI Database: Addresses and Sections

Address	Section Name	Description
00001:Fh	Reserved	Reserved for vendor-specific information
00010h	CFI ID string	Flash device command set ID (identification) and vendor data offset
0001Bh	System interface information	Flash device timing and voltage
00027h	Device geometry definition	Flash device layout
P	Primary Micron-specific extended query	Vendor-defined informaton specific to the primary vendor algorithm (offset 15 defines *P* which points to the primary Micron-specific extended query table.)

Table 24: CFI ID String

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
10h	3	Query unique ASCII string "QRY"	10:	- -51	Q
			11:	- -52	R
			12:	- -59	Y
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms.	13:	- -01	Primary vendor ID number
			14:	- -00	
15h	2	Extended query table primary algorithm address.	15:	- -0A	Primary vendor table address, primary algorithm
			16:	- -01	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists.	17:	- -00	Alternate vendor ID number
			18:	- -00	
19h	2	Secondary algorithm extended query table address. 0000h means none exists.	19:	- -00	Primary vendor table address, secondary algorithm
			1A:	- -00	

Note: 1. The CFI ID string provides verification that the device supports the CFI specification. It also indicates the specification version and supported vendor-specific command sets.

Table 25: System Interface Information

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
1Bh	1	V_{CC} logic supply minimum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 BCD volts	1Bh	- -17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 BCD volts	1Ch	- -20	2.0V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex volts	1Dh	- -85	8.5V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex volts	1Eh	- -95	9.5V
1Fh	1	"n" such that typical single word program timeout = 2^n μs.	1Fh	- -09	512μs
20h	1	"n" such that typical full buffer write timeout = 2^n μs.	20h	- -0A	1024μs
21h	1	"n" such that typical block erase timeout = 2^n ms.	21h	- -0A	1s
22h	1	"n" such that typical full chip erase timeout = 2^n ms.	22h	- -00	NA
23h	1	"n" such that maximum word program timeout = 2^n times typical.	23h	- -01	1024μs
24h	1	"n" such that maximum buffer write timeout = 2^n times typical.	24h	- -02	4096μs
25h	1	"n" such that maximum block erase timeout = 2^n times typical.	25h	- -02	4s
26h	1	"n" such that maximum chip erase timeout = 2^n times typical.	26h	- -00	NA

Table 26: Device Geometry

Hex Offset	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
27h	1	n such that device size in bytes = 2^n.	27:		1
28h	2	Flash device interface code assignment: n such that n + 1 specifies the bit field that represents the flash device width capabilities as described here: bit 0: x8 bit 1: x16 bit 2: x32 bit 3: x64 bits 4 - 7: – bits 8 - 15: –	28: 29:	- -01 - -00	x16
2Ah	2	n such that maximum number of bytes in write buffer = 2^n.	2Ah 2Bh	- -0A - -00	1024
2Ch	1	Number of erase block regions (x) within the device: 1) x = 0 means no erase blocking; the device erases in bulk. 2) x specifies the number of device regions with one or more contiguous, same-size erase blocks. 3) Symmetrically blocked partitions have one blocking region.	2Ch		See Note 1
2Dh	4	Erase block region 1 information: bits 0 - 15 = y, y + 1 = number of identical-size erase blocks. bits 16 - 31 = z, region erase block(s) size are z x 256 bytes.	2D: 2E: 2F: 30:		See Note 1
31h	4	Erase block region 2 information: bits 0 - 15 = y, y + 1 = number of identical-size erase blocks. bits 16 - 31 = z, region erase block(s) size are z x 256 bytes.	31: 32: 33: 34:		See Note 1
35h	4	Reserved for future erase block region information.	35: 36: 37: 38:		See Note 1

Note: 1. See Block Region Map Information table.

Table 27: Block Region Map Information

Address	256Mb		Address	256Mb	
	Bottom	Top		Bottom	Top
27:	--19	--19	30:	--00	--02
28:	--01	--01	31:	--FE	--03
29:	--00	--00	32:	--00	--00
2A:	--0A	--0A	33:	--00	--80
2B:	--00	--00	34:	--02	--00
2C:	--02	--02	35:	--00	--00
2D:	--03	--FE	36:	--00	--00

Table 27: Block Region Map Information (Continued)

| | 256Mb | | | 256Mb | |
Address	Bottom	Top	Address	Bottom	Top
2E:	--00	--00	37:	--00	--00
2F:	--80	--00	38:	--00	--00

Table 28: Primary Vendor-Specific Extended Query

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+0)h (P+1)h (P+2)h	3	Primary extended query table, unique ASCII string: PRI	10A:	- -50	P
			10B:	- -52	R
			10C:	- -49	I
(P+3)h	1	Major version number, ASCII	10D:	- -31	1
(P+4)h	1	Minor version number, ASCII	10E:	- -34	4
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support (1 = yes; 0 = no) Bits 11 - 29 are reserved; undefined bits are 0 If bit 31 = 1, then another 31-bit field of optional features follows at the end of the bit 30 field.	10F:	- -E6	–
			110:	- -01	–
			111:	- -00	–
			112:	See Note 1	–
		Bit 0: Chip erase supported.	bit 0 = 0		No
		Bit 1: Suspend erase supported.	bit 1 = 1		Yes
		Bit 2: Suspend program supported.	bit 2 = 1		Yes
		Bit 3: Legacy lock/unlock supported.	bit 3 = 0		No
		Bit 4: Queued erase supported.	bit 4 = 0		No
		Bit 5: Instant individual block locking supported.	bit 5 = 1		Yes
		Bit 6: OTP bits supported.	bit 6 = 1		Yes
		Bit 7: Page mode read supported.	bit 7 = 1		Yes
		Bit 8: Synchronous read supported.	bit 8 = 1		Yes
		Bit 9: Simultaneous operations supported.	bit 9 = 0		No
		Bit 10: Extended Flash array block supported	bit 10 = 0		No
		Bit 30: CFI links to follow:	bit 30 = 0		See Note 1
		Bit 31: Another optional features field to follow.	bit 31 = 0		
(P+9)h	1	Supported functions after SUSPEND: READ AR-RAY, STATUS, QUERY. Other supported options include: Bits 1 - 7: Reserved; undefined bits are 0.	113:	- -01	–
		Bit 0: Program supported after ERASE SUSPEND.	bit 0 = 1		Yes

Table 28: Primary Vendor-Specific Extended Query (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+A)h (P+B)h	2	Block Status Register mask: Bits 2 - 15 are reserved; undefined bits are 0.	114:	- -03	–
			115:	- -00	–
		Bit 0: Block lock-bit status register active.	bit 0 = 1		Yes
		Bit 1: Block lock-down bit status active.	bit 1 = 1		Yes
		Bit 4: EFA block lock-bit status register active.	bit 4 = 0		No
		Bit 5: EFA block lock-bit status active.	bit 5 = 0		No
(P+C)h	1	V_{CC} logic supply highest performance program/ erase voltage. bits 0 - 3 BCD 100 mV bits 4 - 7 hex value in volts	116:	- -18	1.8V
(P+D)h	1	V_{PP} optimum program/erase voltage. bits 0 - 3 BCD 100mV bits 4 - 7 hex value in volts	117:	- -90	9.0V

Note: 1. See Optional Features Fields table.

Table 29: Optional Features Field

Address	Discrete		512Mb			
	Bottom	Top	Bottom		Top	
	–	–	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
112:	--00	--00	40:	--00	--40	--00

Table 30: One Time Programmable (OTP) Space Information

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+E)h	1	Number of OTP block fields in JEDEC ID space. 00h indicates that 256 OTP fields are available.	118:	- -02	2

Table 30: One Time Programmable (OTP) Space Information (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+F)h (P+10)h (P+11)h (P+12)h	4	OTP Field 1: OTP Description: This field describes user-available OTP bytes. Some are preprogrammed with device-unique serial numbers. Others are user-programmable. Bits 0-15 point to the OTP Lock byte (the first byte). The following bytes are factory preprogrammed and user-programmable: Bits 0 - 7 = Lock/bytes JEDEC plane physical low address. Bits 8 - 15 = Lock/bytes JEDEC plane physical high address. Bits 16 - 23 = n where 2^n equals factory preprogrammed bytes. Bits 24 - 31 = n where 2^n equals user-programmable bytes.	119:	- -80	80h
			11A:	- -00	00h
			1B:	- -03	8 byte
			11C:	- -03	8 byte
(P+13)h (P+14)h (P+15)h (P+16)h	10	Protection field 2: protection description Bits 0 - 31 point to the protection register physical lock word address in the JEDEC plane. The bytes that follow are factory or user-programmable.	11D:	- -89	89h
			11E:	- -00	00h
			11F:	- -00	00h
			120:	- -00	00h
(P+17)h (P+18)h (P+19)h		Bits 32 - 39 = n where n equals factory programmed groups (low byte). Bits 40 - 47 = n where n equals factory programmed groups (high byte). Bits 48 - 55 = n where 2n equals factory programmed bytes/groups.	121:	- -00	0
			122:	- -00	0
			123:	- -00	0
(P+1A)h (P+1B)h (P+1C)h		Bits 56 - 63 = n where n equals user programmed groups (low byte). Bits 64 - 71 = n where n equals user programmed groups (high byte). Bits 72 - 79 = n where 2^n equals user programmable bytes/groups.	124:	- -10	16
			125:	- -00	0
			126:	- -04	16

Table 31: Burst Read Information

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+1D)h	1	Page Mode Read capability: Bits 7 - 0 = n where 2^n hex value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	127:	- -05	32 byte

Table 31: Burst Read Information (Continued)

Hex Offset P = 10Ah	Length	Description	Address	Hex Code	ASCII Value (DQ[7:0])
(P+1E)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	128:	- -04	4
(P+1F)h	1	Synchronous mode read capability configuration 1: Bits 3 - 7 = Reserved. Bits 0 - 2 = n where 2^{n+1} hex value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This fields's 3-bit value can be written directly to the Read Configuration Register bits 0 - 2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	129:	- -01	4
(P+20)h	1	Synchronous mode read capability configuration 2.	12A:	- -02	8
(P+21)h	1	Synchronous mode read capability configuration 3.	12B:	- -03	16
(P+22)	1	Synchronous mode read capability configuration 4.	12C:	- -07	Continued

Table 32: Partition and Block Erase Region Information

Hex Offset P = 10Ah		Description	Length	Address	
Bottom	Top	Optional Flash features and commands		Bottom	Top
(P+23)h	(P+23)h	Number of device hardware-partition regions within the device: x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions	1	12D:	12D:

Table 33: Partition Region 1 Information: Top and Bottom Offset/Address

Hex Offset P = 10Ah		Description Optional Flash features and commands	Length	Address	
Bottom	**Top**			**Bottom**	**Top**
(P+24)h (P+25)h	(P+24)h (P+25)h	Data size of this Partition Region information field (number of addressable locations, including this field.	2	12E: 12F:	12E: 12F:
(P+26)h (P+27)h	(P+26)h (P+27)h	Number of identical partitions within the partition region.	2	130: 131:	130: 131:
(P+28)h	(P+28)h	Number of program or erase operations allowed in a partition: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	132:	132:
(P+29)h	(P+29)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in program mode: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	133:	133:
(P+2A)h	(P+2A)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in erase mode: Bits 0 - 3 = Number of simultaneous program operations. Bits 4 - 7 = Number of simultaneous erase operations.	1	134:	134:
(P+2B)h	(P+2B)h	Types of erase block regions in this partition region: x=0: No erase blocking; the partition region erases in bulk. x = Number of erase block regions with contiguous, same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks) x (Type 1 block sizes) + (Type 2 blocks) x (Type 2 block sizes) +...+ (Type n blocks) x (Type n block sizes).	1	135:	135:

Table 34: Partition Region 1 Information

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+2C)h (P+2D)h (P+2E)h (P+2F)h	Partition region 1 erase block type 1 information: Bits 0-15 = y, y+1 = Number of identical-sized erase blocks in a partition. Bits 16-31 = z, where region erase block(s) size is z x 256 bytes.	4	136: 137: 138: 139:

Table 34: Partition Region 1 Information (Continued)

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+30)h (P+31)h	Partition 1 (erase block type 1): Minimum block erase cycles x 1000	2	13A: / 13B:
(P+32)h	Partition 1 (erase block type 1) bits per cell; internal ECC: Bits 0 - 3 = bits per cell in erase region Bit 4 = reserved for "internal ECC used" (1=yes, 0=no) Bit 5 - 7 = reserved for future use	1	13C:
(P+33)h	Partition 1 (erase block type 1) page mode and synchronous mode capabilities: Bits 0 = page-mode host reads permitted (1=yes, 0=no) Bit 1 = synchronous host reads permitted (1=yes, 0=no) Bit 2 = synchronous host writes permitted (1=yes, 0=no) Bit 3 - 7 = reserved for future use	1	13D:
(P+34)h (P+35)h (P+36)h (P+37)h (P+38)h (P+39)h	Partition 1 (erase block type 1) programming region information: Bits 0 - 7 = x, 2^x: programming region aligned size (bytes) Bit 8-14 = reserved for future use Bit 15 = legacy flash operation; ignore 0:7 Bit 16 - 23 = y: control mode valid size (bytes) Bit 24 - 31 = reserved for future use Bit 32 - 39 = z: control mode invalid size (bytes) Bit 40 - 46 = reserved for future use Bit 47 = legacy flash operation (ignore 23:16 and 39:32)	6	13E: / 13F: / 140: / 141: / 142: / 143:
(P+3A)h (P+3B)h (P+3C)h (P+3D)h	Partition 1 erase block type 2 information: Bits 0-15 = y, y+1 = Number of identical-size erase blocks in a partition. Bits 16 - 31 = z, where region erase block(s) size is z x 256 bytes. (bottom parameter device only)	4	144: / 145: / 146: / 147:
(P+3E)h (P+3F)h	Partition 1 (erase block type 2) Minimum block erase cycles x 1000	2	148: / 149:
(P+40)h	Partition 1 (erase block type 2) bits per cell, internal EDAC: Bits 0 - 3 = bits per cell in erase region Bit 4 = reserved for "internal ECC used" (1=yes, 0=no) Bits 5 - 7 = reserved for future use	1	14A:
(P+41)h	Partition 1 (erase block type 2) page mode and synchronous mode capabilities: Bit 0 = page-mode host reads permitted (1=yes, 0=no) Bit 1 = synchronous host reads permitted (1=yes, 0=no) Bit 2 = synchronous host writes permitted (1=yes, 0=no) Bits 3-7 = reserved for future use	1	14B:

Table 34: Partition Region 1 Information (Continued)

Hex Offset P = 10Ah Bottom/Top	Description Optional Flash features and commands	Length	Address Bottom/Top
(P+42)h	Partition 1 (erase block type 2) programming region information:	6	14C:
(P+43)h	Bits 0-7 = x, $2^n x$ = Programming region aligned size (bytes)		14D:
(P+44)h	Bits 8-14 = reserved for future use		14E:
(P+45)h	Bit 15 = legacy flash operation (ignore 0:7)		14F:
(P+46)h	Bits 16 - 23 = y = Control mode valid size in bytes Bits 24 - 31 = reserved		150:
(P+47)h	Bits 32 - 39 = z = Control mode invalid size in bytes		151:
	Bits 40 - 46 = reserved		
	Bit 47 = legacy flash operation (ignore 23:16 and 39:32)		

Table 35: Partition Region 1: Partition and Erase Block Map Information

Address	256Mb	
	Bottom	Top
12D:	- -01	- -01
12E:	- -24	- -24
12F:	- -00	- -00
130:	- -01	- -01
131:	- -00	- -00
132:	- -11	- -11
133:	- -00	- -00
134:	- -00	- -00
135:	- -02	- -02
136:	- -03	- -FE
137:	- -00	- -00
138:	- -80	- -00
139:	- -00	- -02
13A:	- -64	- -64
13B:	- -00	- -00
13C:	- -02	- -02
13D:	- -03	- -03
13E:	- -00	- -00
13F:	- -80	- -80
140:	- -00	- -00
141:	- -00	- -00
142:	- -00	- -00
143:	- -80	- -80
144:	- -FE	- -03
145:	- -00	- -00
146:	- -00	- -80
147:	- -02	- -00
148:	- -64	- -64
149:	- -00	- -00
14A:	- -02	- -02
14B:	- -03	- -03
14C:	- -00	- -00
14D:	- -80	- -80
14E:	- -00	- -00
14F:	- -00	- -00
150:	- -00	- -00
151:	- -80	- -80

Table 36: CFI Link Information

Offset P = 10Ah	Length	Description	Address	ASCII Value (DQ[7:0])
		CFI Link field bit definitions:		
(P+48)h	4	Bits 0 - 9 = Address offset (within 32Mbit segment of referenced CFI table)	152:	See Note 1
(P+49)h		Bits 10 - 27 = nth 32Mbit segment of referenced CFI table	153:	
(P+4A)h		Bits 28 - 30 = Memory Type	154:	
(P+4B)h		Bit 31 = Another CFI link field immediately follows	155:	
(P+4C)h	1	CFI Link field quantity subfield definitions: Bits 0 - 3 = Quantity field (n such that n+1 equals quantity) Bit 4 = Table and die relative location Bit 5 = Link field and table relative location Bits 6 - 7 = Reserved	156:	

Note: 1. See Additional CFI Link Field table.

Table 37: Additional CFI Link Field

Address	Discrete		512Mb			
	Bottom	Top	Bottom		Top	
	–	–	die 1 (B)	die 2 (T)	die 1 (T)	die 2 (B)
152:	--FF	--FF	--10	--FF	--10	--FF
153:	--FF	--FF	--20	--FF	--20	--FF
154:	--FF	--FF	--00	--FF	--00	--FF
155:	--FF	--FF	--00	--FF	--00	--FF
156:	--FF	--FF	--10	--FF	--10	--FF

Flowcharts

Figure 17: Word Program Procedure
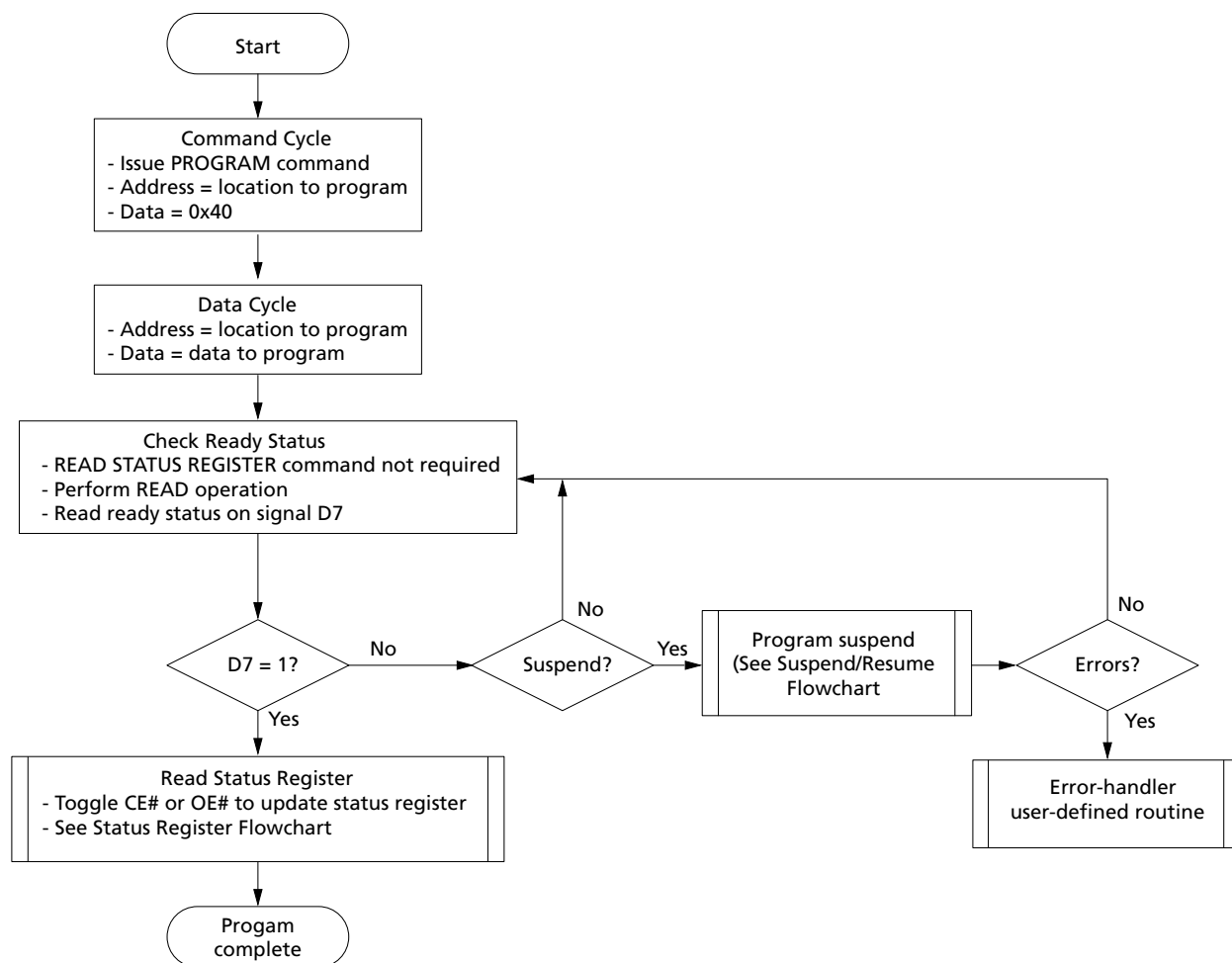
Figure 18: Buffer Program Procedure
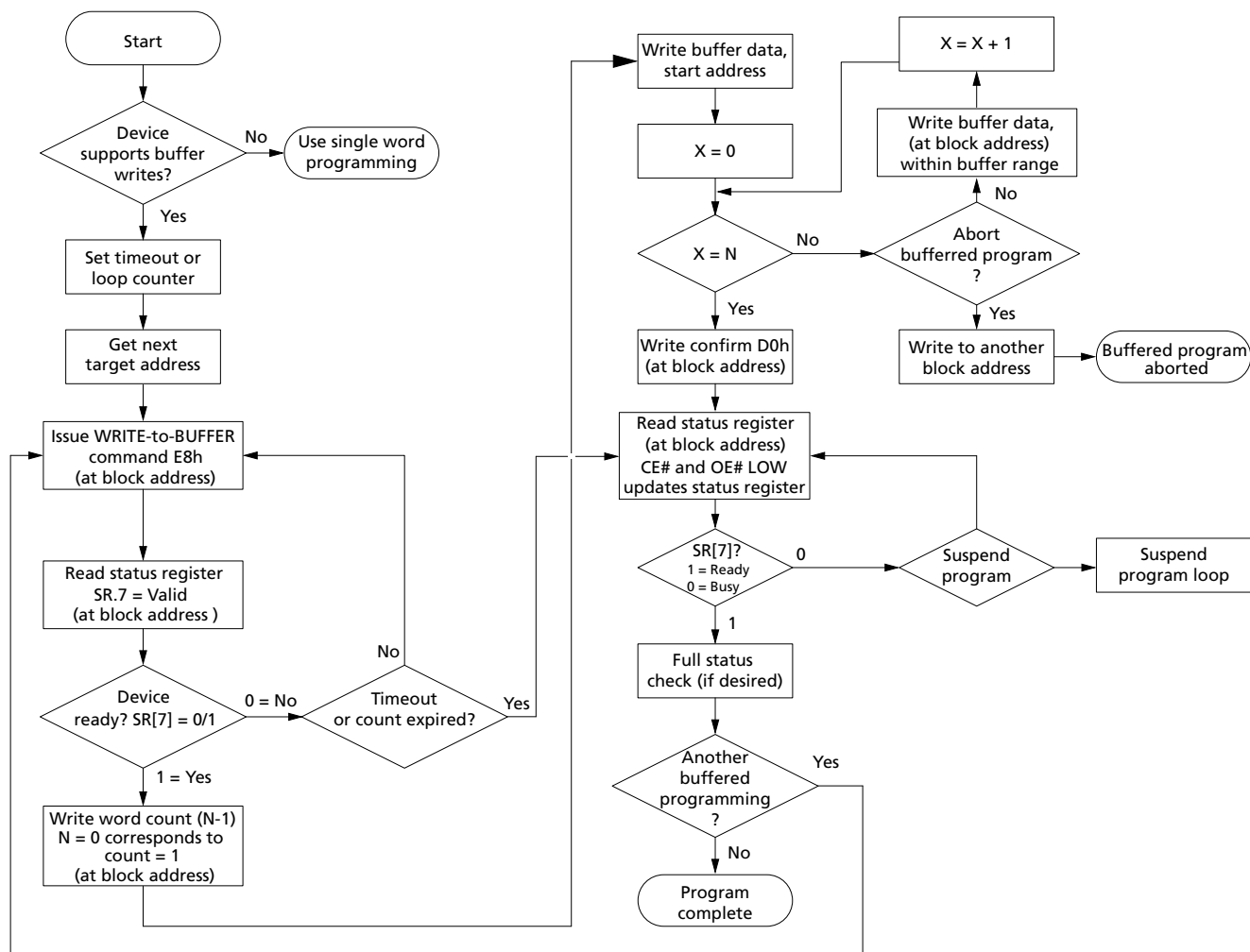
Notes:
1. Word count values on DQ0:DQ15 are loaded into the count register. Count ranges for this device are N = 0000h to 01FFh.
2. Device outputs the status register when read.
3. Write buffer contents will be programmed at the device start address or destination address.
4. Align the start address on a write buffer boundary for maximum programming performance; that is, A[9:1] of the start address = 0).
5. Device aborts the BUFFERED PROGRAM command if the current address is outside the original block address.
6. Status register indicates an improper command sequence if the BUFFERED PROGRAM command is aborted. Follow this with a CLEAR STATUS REGISTER command.
7. Device defaults to SR output data after Buffered Programming Setup Command (E8h) is issued . CE# or OE# must be toggled to update Status Register . Don't issue the Read SR command (70h); it is interpreted by the device as Buffer Word Count.
8. Full status check can be done after erase and write sequences complete. Write FFh after the last operation to reset the device to read array mode.

Figure 19: Buffered Enhanced Factory Programming (BEFP) Procedure

Setup Phase

Start

↓

Issue BEFP SETUP
Data = 0x80

↓

Issue BEFP CONFIRM
Data = 00D0h

↓

BEFP setup
delay

↓

Read status
register

↓

BEFP setup
done? → Yes (SR[7] = 0)

↓ No (SR[7] = 1)

SR error-handler
user-defined

↓

Exit

Program and Verify Phase

Read status
register

↓

Buffer ready? → No (SR[0] = 1)

↓ Yes (SR[0] = 0)

Write data
word to buffer

↓

Buffer full? → No

↓ Yes

Read status
register

↓

Program
done? → No (SR[0] = 1)

↓ Yes (SR[0] = 0)

Program
more data
? → Yes

↓ No

Write 0xFFFF
outside block

Exit Phase

Read status
register

↓

BEFP exited? → No (SR[7] = 0)

↓ Yes (SR[7] = 1)

Full status
register check
for errors

↓

Finish

Figure 20: Block Erase Procedure

```
                        ┌──────────────┐
                        │    Start     │
                        └──────┬───────┘
                               │
                               ▼
            ┌──────────────────────────────────┐
            │         Command Cycle            │
            │  - Issue ERASE command           │
            │  - Address = block to be erased  │
            │  - Data = 0x20                   │
            └──────────────┬───────────────────┘
                           │
                           ▼
            ┌──────────────────────────────────┐
            │         Confirm Cycle            │
            │  - Issue CONFIRM command         │
            │  - Address = block to be erased  │
            │  - Data = erase confirm (0xD0)   │
            └──────────────┬───────────────────┘
                           │
                           ▼
            ┌──────────────────────────────────┐
            │       Check Ready Status         │
            │  - READ STATUS REGISTER          │
            │    command not required          │
            │  - Perform READ operation        │
            │  - Read ready status on SR[7]    │
            └──────────────┬───────────────────┘
                           │
                           ▼
```

Check Ready Status → SR[7] = 1? — No → Suspend? — Yes → Erase Suspend (See Suspend/Resume Flowchart) → Errors? — Yes → Error Handler user-defined routine

Suspend? — No (returns to Check Ready Status)

Errors? — No (returns to Check Ready Status)

SR[7] = 1? — Yes → Read Status Register
- Toggle CE# or OE# to update status register
- See Status Register Flowchart

→ End

Figure 21: Program Suspend/Resume Procedure

```
                 ┌──────────────┐
                 │    Start     │
                 └──────┬───────┘
               Read  │  Status
                 ┌──────▼───────┐
                 │   Write 70h  │
                 │  Any Address │
                 └──────┬───────┘
            Program  │  Suspend
                 ┌──────▼───────┐
                 │   Write B0h  │
                 │  Any Address │
                 └──────┬───────┘
```

```
 SR.2 =
 1 = Suspended          0        Program
 0 = Completed    ───────────►   Completed
       │ 1
   Read │ Array
   Write FFh
   Any Address
```

Start → Read | Status → **Write 70h / Any Address** → Program | Suspend → **Write B0h / Any Address** → **Read Status Register / Initiate Read cycle to update the status register (Address = Block to suspend)** → **SR.7 = 1 = Ready / 0 = Busy** — 0 (loop back) — 1 →

SR.2 = 1 = Suspended / 0 = Completed — 0 → **Program Completed**; 1 → Read | Array → **Write FFh / Any Address** → **Read Array Data from a block other than from the one being programmed** → **Done Reading** — No (loop back) — Yes → Program | Resume → **Write D0h / Any Address** → **Program Resumed** → Read | Status → **Write 70h / Any Address**

Program Completed → Read | Array → **Write FFh** → **Read Array Data**

Figure 22: Erase Suspend/Resume Procedure

Note: 1. The ^{t}ERS/SUSP timing between the initial block erase or erase resume command and a subsequent erase suspend command should be followed.

Figure 23: Block Lock Operations Procedure

```
                          ┌──────────────┐
                          │    Start     │◄───────────────┐
                          └──────────────┘                │
                         Lock │ Setup                     │
                          ┌──────────────┐                │
                          │  Write 60h   │                │
                          │ Block Address│                │
                          └──────────────┘                │
                         Lock │ Confirm                   │
                          ┌──────────────┐                │
                          │Write 01h, D0h, 2Fh│           │
                          │ Block Address│                │
                          └──────────────┘                │
                         Read │ ID Plane                  │
           ┌─────────        ┌──────────────┐             │
           │                 │  Write 90h   │             │
           │                 └──────────────┘             │
           │                        │                     │
           │                 ┌──────────────┐             │
  Optional │                 │ Read Block   │             │
           │                 │ Lock Status  │             │
           │                 └──────────────┘             │
           │                        │                     │
           │                      ◇◇◇◇◇      No           │
           │                   ◇  Locking ◇──────────────┘
           │                    ◇ Change? ◇
           │                      ◇◇◇◇◇
           │              Read │ Yes  Array
           └────────────       ┌──────────────┐
                               │  Write FFh   │
                               │ Any Address  │
                               └──────────────┘
                                      │
                               ┌──────────────┐
                               │ Lock Change  │
                               │   Complete   │
                               └──────────────┘
```
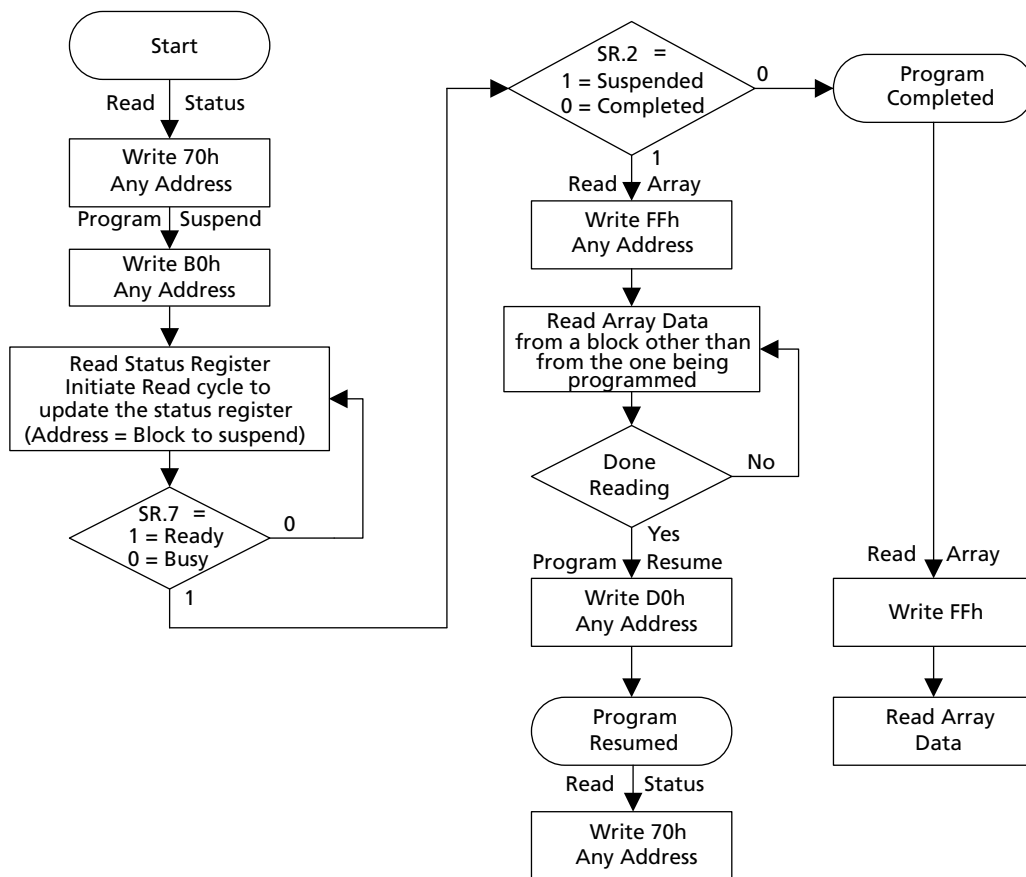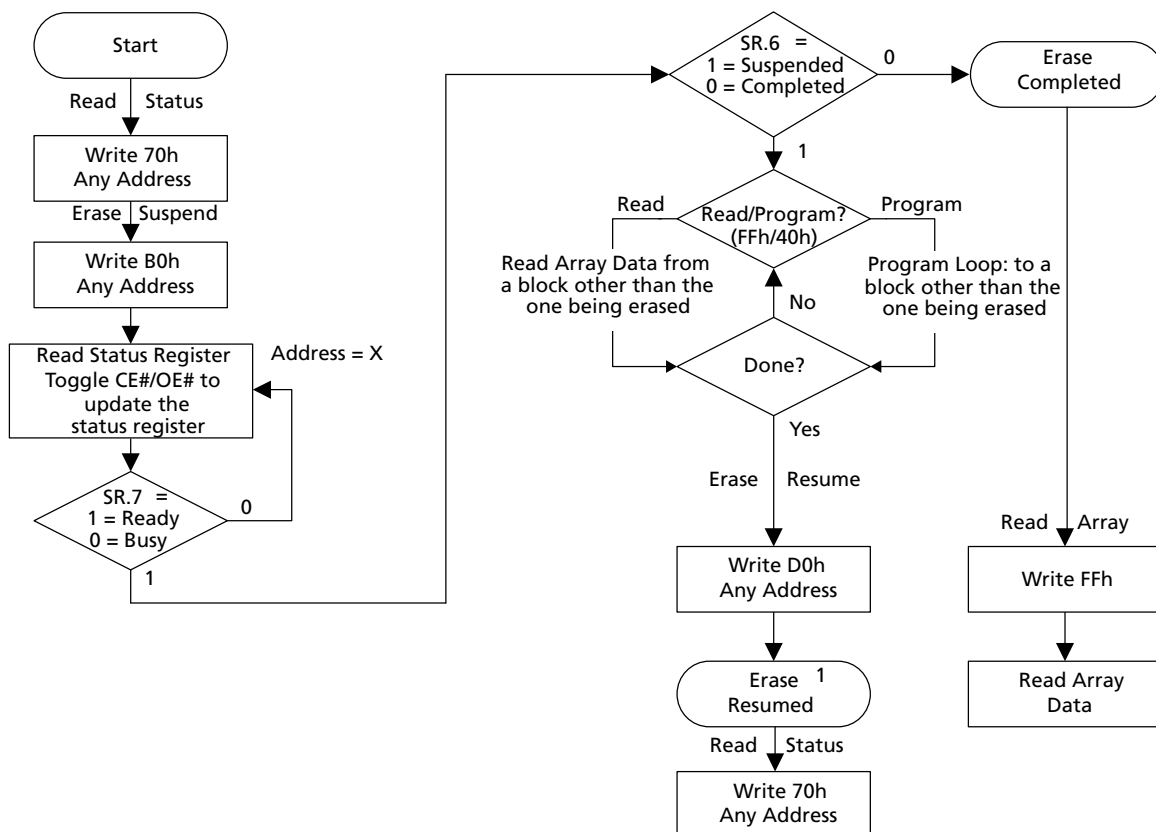
Figure 24: OTP Register Programming Procedure

Figure 25: Status Register Procedure

```
                        ╭─────────────╮
                        │    Start    │
                        ╰─────────────╯
                               │
                               ▼
              ┌────────────────────────────────────┐
              │          Command Cycle             │
              │ - Issue STATUS REGISTER command    │
              │ - Address =  any device address    │
              │ - Data = 0x70                      │
              └────────────────────────────────────┘
                               │
                               ▼
              ┌────────────────────────────────────┐
              │            Data Cycle              │
              │ - Read Status Register SR[7:0]     │
              └────────────────────────────────────┘
```

Set/Reset by device:

- SR[7] = 1 → No → End
- SR[7] = 1 → Yes
- SR[6] = 1 → Yes → Erase Suspend — See Suspend/Resume Flowchart
- SR[6] = 1 → No
- SR[2] = 1 → Yes → Program Suspend — See Suspend/Resume Flowchart
- SR[2] = 1 → No

- Set by device
- Reset by user
- See Clear Status Register Command

- SR[5] = 1 → Yes → SR[4] = 1 → No → Error Command sequence
- SR[4] = 1 → Yes → Error Erase failure
- SR[5] = 1 → No
- SR[4] = 1 → Yes → Error Program failure
- SR[4] = 1 → No
- SR[3] = 1 → Yes → Error $V_{PEN}/V_{PP} < V_{PENLK}/V_{PPLK}$
- SR[3] = 1 → No
- SR[1] = 1 → Yes → Error Block locked
- SR[1] = 1 → No → End

Power-Up and Power-Down

Power supply sequencing is not required if V_{PP} is connected to V_{CC} or V_{CCQ}. Otherwise, V_{CC} should attain V_{CCmin} before applying V_{CCQ} and V_{PP}. Device inputs should not be driven before supply voltage = V_{CCmin}.

Power supply transitions should only occur when RST# is low. This protects the device from accidental programming or erasure during power transitions.

Reset Specifications

Asserting RST# during a system reset is important with automated program/erase devices because systems typically expect to read from flash memory when coming out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization may not occur. This is because the flash memory may be providing status information, instead of array data as expected. Connect RST# to the same active low reset signal used for CPU initialization.
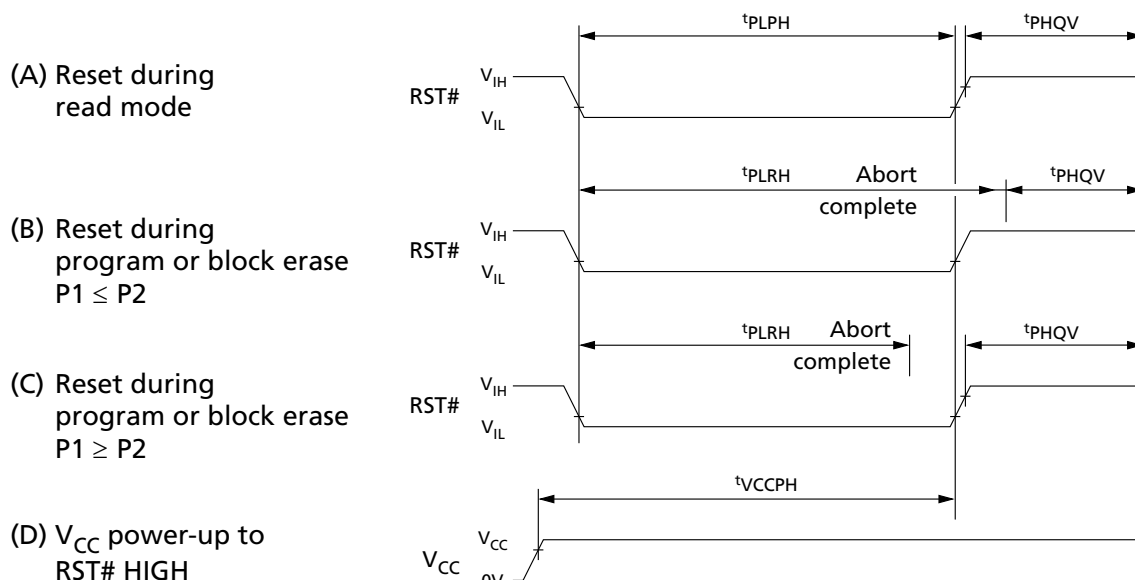
Also, because the device is disabled when RST# is asserted, it ignores its control inputs during power-up/down. Invalid bus conditions are masked, providing a level of memory protection.

Table 38: Power and Reset

Number	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RST# pulse width low	100	-	ns	1, 2, 3, 4
P2	t_{PLRH}	RST# low to device reset during erase	-	25	us	1, 3, 4, 7
		RST# low to device reset during program	-	25		1, 3, 4, 7
P3	t_{VCCPH}	V_{CC} Power valid to RST# de-assertion (high)	300	-		1, 4, 5, 6

Notes: 1. These specifications are valid for all device versions (packages and speeds).
2. The device may reset if t_{PLPH} is < $t_{PLPH\ MIN}$, but this is not guaranteed.
3. Not applicable if RST# is tied to Vcc.
4. Sampled, but not 100% tested.
5. When RST# is tied to the V_{CC} supply, device will not be ready until t_{VCCPH} after $V_{CC} \geq V_{CCMIN}$.
6. When RST# is tied to the V_{CCQ} supply, device will not be ready until t_{VCCPH} after $V_{CC} \geq V_{CCMIN}$.
7. Reset completes within t_{PLPH} if RST# is asserted while no erase or program operation is executing.

Figure 26: Reset Operation Waveforms

(A) Reset during read mode

(B) Reset during program or block erase P1 ≤ P2

(C) Reset during program or block erase P1 ≥ P2

(D) V_{CC} power-up to RST# HIGH

Power Supply Decoupling

Flash memory devices require careful power supply de-coupling. Three basic power supply current considerations are 1) standby current levels, 2) active current levels, and 3) transient peaks produced when CE# and OE# are asserted and deasserted.

When the device is accessed, many internal conditions change. Circuits within the device enable charge-pumps, and internal logic states change at high speed. All of these internal activities produce transient signals. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and correct decoupling capacitor selection suppress transient voltage peaks.

Because flash memory devices draw their power from VCC, VPP, and VCCQ, each power connection should have a 0.1 µF ceramic capacitor to ground. High-frequency, inherently low-inductance capacitors should be placed as close as possible to package leads.

Additionally, for every eight devices used in the system, a 4.7 µF electrolytic capacitor should be placed between power and ground close to the devices. The bulk capacitor is meant to overcome voltage droop caused by PCB trace inductance.

Absolute Maximum Ratings

Caution: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

Table 39: Absolute Maximum Ratings

Parameter	Maximum Rating	Notes
Temperature under bias	–40 °C to + 85 °C	-
Storage temperature	–65 °C to + 125 °C	-
Voltage on any signal (except V_{CC}, V_{PP} and V_{CCQ})	–2.0 V to + 4.0 V	1
V_{PP} voltage	–2.0 V to + 11.5 V	1, 2
V_{CC} voltage	–2.0 V to + 4.0 V	1
V_{CCQ} voltage	–2.0 V to + 5.6 V	1
Output short circuit current	100 mA	3

Notes: 1. Voltages shown are specified with respect to VSS. During infrequent non-periodic transitions, the level may undershoot to –2.0 V for periods less than 20 ns or overshoot to V_{CC} + 2.0 V or V_{CCQ} + 2.0 V for periods less than 20 ns.
2. Program/erase voltage is typically 1.7 V ~ 2.0 V. 9.0 V can be applied for 80 hours maximum total. 9.0 V program/erase voltage may reduce block cycling capability.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Conditions

Caution: Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 40: Operating Conditions

Symbol	Parameter		Min	Max	Unit	Notes
T_C	Operating Temperature		–40	+85	°C	1
V_{CC}	V_{CC} Supply Voltage		1.7	2.0	V	3
V_{CCQ}	I/O Supply Voltage	CMOS inputs	1.7	3.6		
		TTL inputs	2.4	3.6		
V_{PPL}	V_{PP} Voltage Supply (Logic Level)		0.9	3.6		2
V_{PPH}	Buffered Enhanced Factory Programming V_{PP}		8.5	9.5		
t_{PPH}	Maximum V_{PP} Hours	V_{PP} = V_{PPH}	-	80	Hours	
Block Erase Cycles	Main and Parameter Blocks	V_{PP} = V_{PPL}	100,000	-	Cycles	
	Main Blocks	V_{PP} = V_{PPH}	100,000	-		
	Parameter Blocks	V_{PP} = V_{PPH}	100,000	-		

Notes: 1. T_C = Case Temperature.
2. In typical operation VPP program voltage is V_{PPL}.

DC Current Characteristics

Table 41: DC Current Characteristics

Sym-bol	Parameter		CMOS Inputs (V$_{CCQ}$ = 1.7V - 3.6 V)		TTL Inputs (V$_{CCQ}$ = 2.4 V - 3.6 V)		Unit	Test Conditions		Notes
			Typ	Max	Typ	Max				
I$_{LI}$	Input Load Current		-	±1	-	±2	µA	V$_{CC}$ = V$_{CC}$Max V$_{CCQ}$ = V$_{CCQ}$Max V$_{IN}$ = V$_{CCQ}$ or V$_{SS}$		1, 6
I$_{LO}$	Output Leakage Current	DQ[15:0], WAIT	-	±1	-	±10	µA	V$_{CC}$ = V$_{CC}$Max V$_{CCQ}$ = V$_{CCQ}$Max V$_{IN}$ = V$_{CCQ}$ or V$_{SS}$		
I$_{CCS}$, I$_{CCD}$	V$_{CC}$ Standby, Power-Down	256-Mbit	65	210	65	210	µA	V$_{CC}$ = V$_{CC}$Max V$_{CCQ}$ = V$_{CCQ}$Max CE# = V$_{CCQ}$ RST# = V$_{CCQ}$ (for I$_{CCS}$) RST# = V$_{SS}$ (for I$_{CCD}$) WP# = V$_{IH}$		1. 2
		512-Mbit	130	420	130	420				
I$_{CCR}$	Average V$_{CC}$ Read Current	Asynchronous Single-Word f = 5 MHz (1 CLK)	26	31	26	31	mA	16-Word Read	V$_{CC}$ = V$_{CC}$Max CE# = V$_{IL}$ OE# = V$_{IH}$ Inputs: V$_{IL}$ or V$_{IH}$	1
		Page-Mode Read f = 13 MHz (17 CLK)	12	16	12	16	mA	16-Word Read		
		Synchronous Burst f = 52 MHz, LC=4	19	22	19	22	mA	8-Word Read		
			16	18	16	18	mA	16-Word Read		
			21	24	21	24	mA	Continuous Read		
I$_{CCW}$, I$_{CCE}$	V$_{CC}$ Program Current, V$_{CC}$ Erase Current		35	50	35	50	mA	V$_{PP}$ = V$_{PPL}$, Pgm/Ers in progress		1, 3, 5
			35	50	35	50		V$_{PP}$ = V$_{PPH}$, Pgm/Ers in progress		1, 3, 5
I$_{CCWS}$, I$_{CCES}$	V$_{CC}$ Program Suspend Current, V$_{CC}$ Erase Suspend Current	256-Mbit	65	210	65	210	µA	CE# = V$_{CCQ}$; suspend in progress		1, 3, 4
		512-Mbit	70	225	70	225				
I$_{PPS}$, I$_{PPWS}$, I$_{PPES}$	V$_{PP}$ Standby Current, V$_{PP}$ Program Suspend Current, V$_{PP}$ Erase Suspend Current		0.2	5	0.2	5	µA	V$_{PP}$ = V$_{PPL}$, suspend in progress		1, 3, 7
I$_{PPR}$	V$_{PP}$ Read		2	15	2	15	µA	V$_{PP}$ = V$_{PPL}$		1, 3
I$_{PPW}$	V$_{PP}$ Program Current		0.05	0.10	0.05	0.10	mA	V$_{PP}$ = V$_{PPL}$, program in progress		3
			0.05	0.10	0.05	0.10		V$_{PP}$ = V$_{PPH}$, program in progress		
I$_{PPE}$	V$_{PP}$ Erase Current		0.05	0.10	0.05	0.10	mA	V$_{PP}$ = V$_{PPL}$, erase in progress		3
			0.05	0.10	0.05	0.10		V$_{PP}$ = V$_{PPH}$, erase in progress		
I$_{PPBC}$	V$_{PP}$ Blank Check		0.05	0.10	0.05	0.10	mA	V$_{PP}$ = V$_{PPL}$		3
			0.05	0.10	0.05	0.10		V$_{PP}$ = V$_{PPH}$		

Notes: 1. All currents are RMS unless noted. Typical values at typical V$_{CC}$, T$_C$ = +25 °C.
2. I$_{CCS}$ is the average current measured over any 5 ms time interval 5 µs after CE# is deasserted.

3. Sampled, not 100% tested.

4. I_{CCES} is specified with the device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}.

5. I_{CCW}, I_{CCE} measured over typical or max times specified in Program and Erase Characteristics (page 94) .

6. if $V_{IN} > V_{CC}$ the input load current increases to 10uA max.

7. the I_{PPS},I_{PPWS},I_{PPES} Will increase to 200uA when Vpp/WP# is at V_{PPH}.

DC Voltage Characteristics

Table 42: DC Voltage Characteristics

Symbol	Parameter	CMOS Inputs ($V_{CC}Q = $ 1.7 V – 3.6 V)		TTL Inputs [1] ($V_{CC}Q = $ 2.4 V – 3.6 V)		Unit	Test Conditions	Notes
		Min	Max	Min	Max			
V_{IL}	Input Low Voltage	-0.5	0.4	-0.5	0.6	V		2
V_{IH}	Input High Voltage	$V_{CCQ} - 0.4$	$V_{CCQ} + 0.5$	2	$V_{CCQ} + 0.5$	V		
V_{OL}	Output Low Voltage	-	0.2	-	0.2	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min $I_{OL} = 100$ µA	-
V_{OH}	Output High Voltage	$V_{CCQ} - 0.2$	-	$V_{CCQ} - 0.2$	-	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min $I_{OH} = -100$ µA	-
V_{PPLK}	V_{PP} Lock-Out Voltage	-	0.4	-	0.4	V		3
V_{LKO}	V_{CC} Lock Voltage	1.0	-	1.0	-	V		-
V_{LKOQ}	V_{CCQ} Lock Voltage	0.9	-	0.9	-	V		-
V_{PPL}	V_{PP} Voltage Supply (Logic Level)	1.5	3.6	1.5	3.6	V		
V_{PPH}	Buffered Enhanced Factory Programming V_{PP}	8.5	9.5	8.5	9.5	V		

Notes: 1. Synchronous read mode is not supported with TTL inputs.

2. V_{IL} can undershoot to –1.0 V for duration of 2ns or less and V_{IH} can overshoot to $V_{CCQ} + $ 1.0 V for durations of 2ns or less.

3. $V_{PP} \leq V_{PPLK}$ inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.
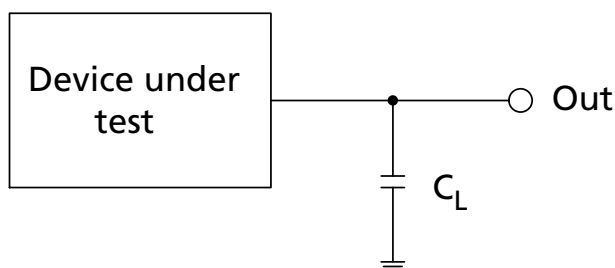
AC Test Conditions

Figure 27: AC Input/Output Reference Timing
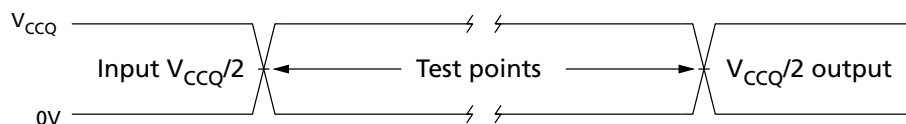
Note: 1. AC test inputs are driven at V_{CCQ} for Logic "1" and 0 V for Logic "0". Input/output timing begins/ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed occurs at $V_{CC} = V_{CCMin}$.

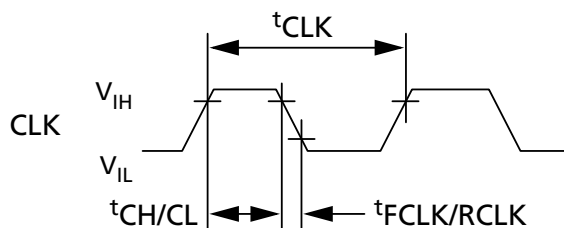**Figure 28: Transient Equivalent Load Circuit**

Notes: 1. See the Test Configuration Component Value For Worst Case Speed Conditions table for component values.
2. CL includes jig capacitance.

Table 43: Test Configuration: Worst Case Speed Condition

Test Configuration	C_L (pF)
V_{CCQ}Min Standard Test	30

Figure 29: Clock Input AC Waveform

Capacitance

Table 44: Capacitance

Parameter	Signal	Density	Min	Typ	Max	Unit	Condition	Notes
Input Capacitance	Address, Data, CE#, WE#, OE#, RST#, CLK, ADV#, WP#	256Mb	3	7	8	pF	Typ temp = 25 °C, Max temp = 85 °C, V_{CC} = (0 V - 2.0 V), V_{CCQ} = (0 V - 3.6 V), Discrete silicon die	1
		256Mb/ 256Mb	6	14	16			
Output Capacitance	Data, WAIT	256Mb	3	5	7			
		256Mb/ 256Mb	6	10	14			

Note: 1. Sampled, but not 100% tested.

AC Read Specifications

Table 45: AC Read Specifications

Number	Symbol	Parameter		Min	Max	Unit	Note
Asynchronous Specifications							
R1	t_{AVAV}	Read cycle time	Easy BGA/QUAD+	100	-	ns	-
			TSOP	110		ns	-
R2	t_{AVQV}	Address to output valid	Easy BGA/QUAD+	-	100	ns	-
			TSOP		110	ns	-
R3	t_{ELQV}	CE# low to output valid	Easy BGA/QUAD+	-	100	ns	-
			TSOP		110	ns	-
R4	t_{GLQV}	OE# low to output valid		-	25	ns	1, 2
R5	t_{PHQV}	RST# high to output valid		-	150	ns	1
R6	t_{ELQX}	CE# low to output in low-Z		0	-	ns	1, 3
R7	t_{GLQX}	OE# low to output in low-Z		0	-	ns	1, 2, 3
R8	t_{EHQZ}	CE# high to output in high-Z		-	20	ns	1, 3
R9	t_{GHQZ}	OE# high to output in high-Z		-	15	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change		0	-	ns	
R11	t_{EHEL}	CE# pulse width high		17	-	ns	1
R12	t_{ELTV}	CE# low to WAIT valid		-	17	ns	
R13	t_{EHTZ}	CE# high to WAIT high-Z		-	20	ns	1, 3
R15	t_{GLTV}	OE# low to WAIT valid		-	17	ns	1
R16	t_{GLTX}	OE# low to WAIT in low-Z		0	-	ns	1, 3
R17	t_{GHTZ}	OE# high to WAIT in high-Z		-	20	ns	
Latching Specifications							
R101	t_{AVVH}	Address setup to ADV# high		10	-	ns	1
R102	t_{ELVH}	CE# low to ADV# high		10	-	ns	
R103	t_{VLQV}	ADV# low to output valid	Easy BGA/QUAD+	-	100	ns	
			TSOP	-	110	ns	
R104	t_{VLVH}	ADV# pulse width low		10	-	ns	
R105	t_{VHVL}	ADV# pulse width high		10	-	ns	
R106	t_{VHAX}	Address hold from ADV# high		9	-	ns	1, 4
R108	t_{APA}	Page address access		-	25	ns	1
R111	t_{PHVH}	RST# high to ADV# high		30	-	ns	
Clock Specifications							

Table 45: AC Read Specifications (Continued)

Number	Symbol	Parameter		Min	Max	Unit	Note
R200	f_{CLK}	CLK frequency	Easy BGA/QUAD+	-	52	MHz	1, 3, 5
			TSOP	-	40	MHz	
R201	t_{CLK}	CLK period	Easy BGA/QUAD+	19.2	-	ns	
			TSOP	25	-	ns	
R202	$t_{CH/CL}$	CLK high/low time	Easy BGA/QUAD+	5	-	ns	
			TSOP	9			
R203	$t_{FCLK/RCLK}$	CLK fall/rise time		0.3	3	ns	
Synchronous Specifications[5]							
R301	$t_{AVCH/L}$	Address setup to CLK	-	9	-	ns	1, 6
R302	$t_{VLCH/L}$	ADV# low setup to CLK	-	9	-	ns	
R303	$t_{ELCH/L}$	CE# low setup to CLK	-	9	-	ns	
R304	t_{CHQV} / t_{CLQV}	CLK to output valid	Easy BGA/QUAD+	-	17	ns	
			TSOP	-	20	ns	1, 6
R305	t_{CHQX}	Output hold from CLK	-	3	-	ns	1, 6
R306	t_{CHAX}	Address hold from CLK	-	10	-	ns	1, 4, 6
R307	t_{CHTV}	CLK to WAIT valid	Easy BGA/QUAD+	-	17	ns	1, 6
			TSOP	-	20		
R311	t_{CHVL}	CLK Valid to ADV# Setup	-	3	-	ns	1
R312	t_{CHTX}	WAIT Hold from CLK	Easy BGA/QUAD+	3	-	ns	1, 6
			TSOP	5	-		

Notes:
1. See on page for timing measurements and max allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
5. Synchronous read mode is not supported with TTL level inputs.
6. Applies only to subsequent synchronous reads.

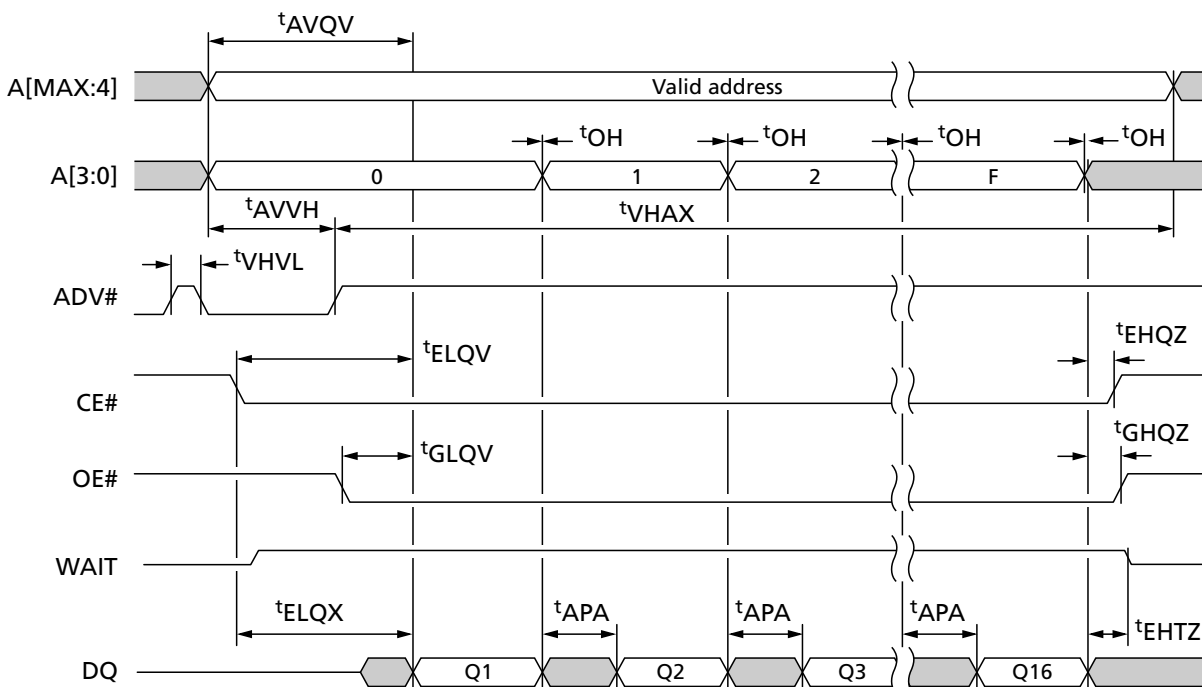**Figure 30: Asynchronous Single Word Read (ADV# LOW)**
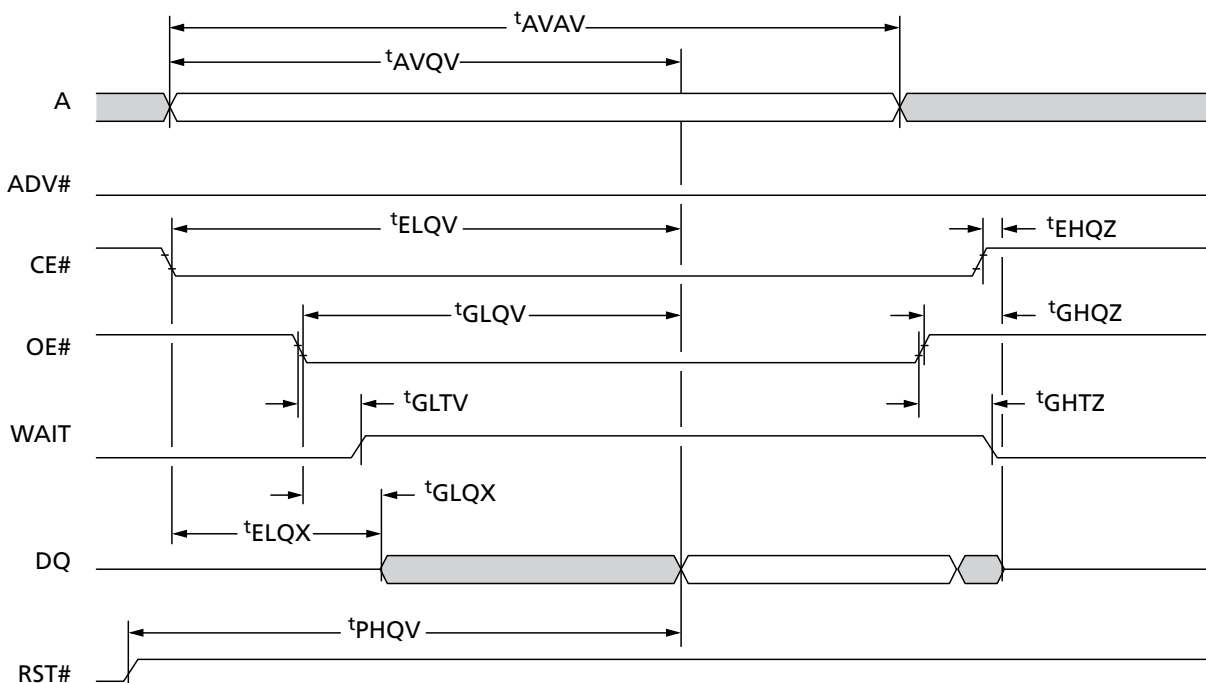
Note: 1. WAIT shown deasserted during asynchronous read mode (RCR.10=0, WAIT asserted low).
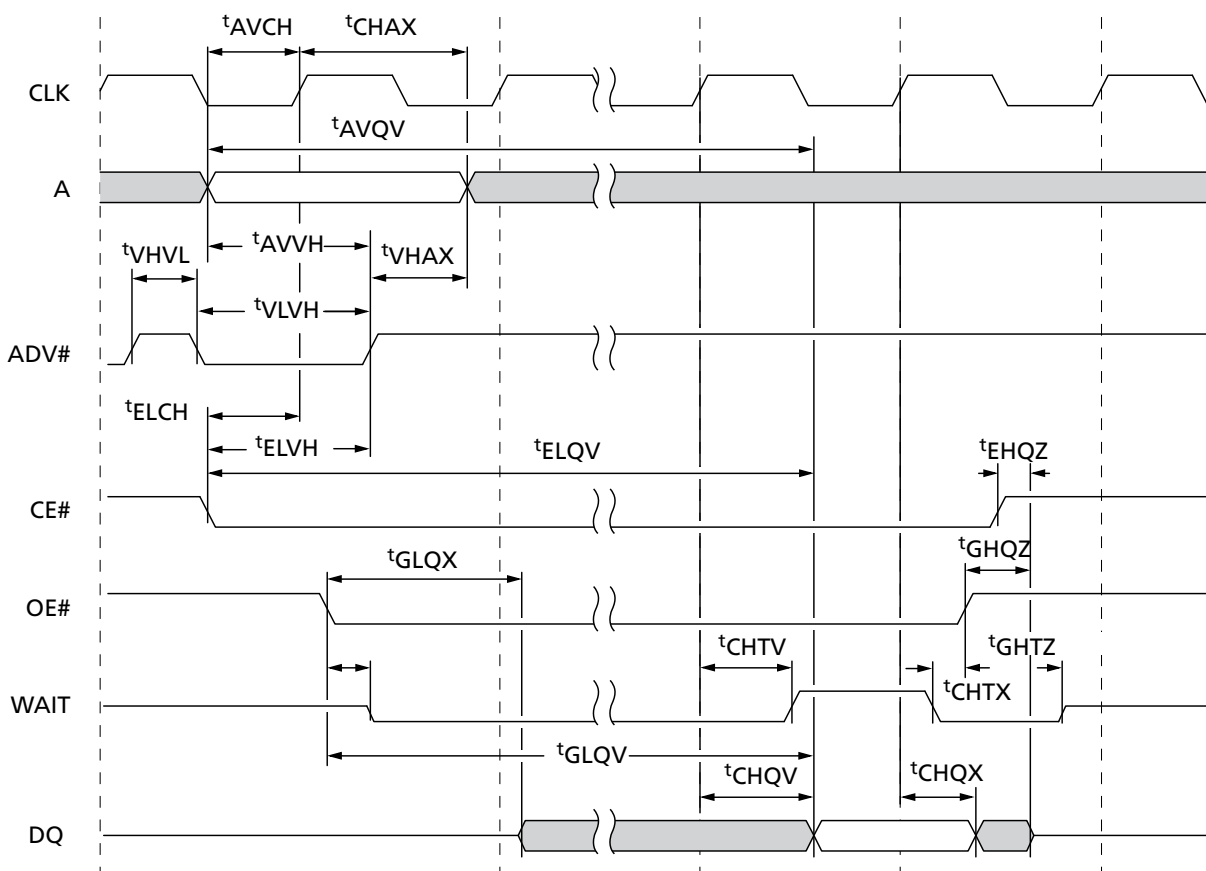
Figure 31: Asynchronous Single Word Read (ADV# Latch)
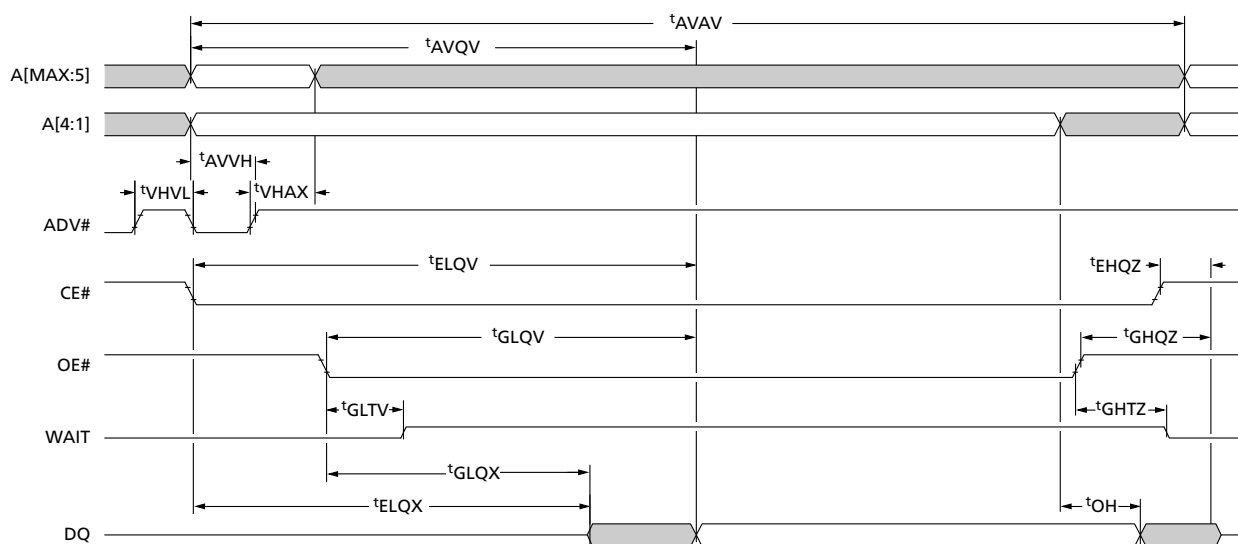
Note: 1. WAIT shown deasserted during asynchronous read mode (RCR.10=0, WAIT asserted low).

**Figure 32: Asynchronous Page Mode Read**

Note: 1.   WAIT shown deasserted during asynchronous read mode (RCR.10=0, WAIT asserted low).

Figure 33: Synchronous Single Word Array or Nonarray Read

Notes: 1. WAIT is driven per OE# assertion during synchronous array or non-array read, and can be configured to assert either during or one data cycle before valid data.
2. This diagram illustrates the case in which an n-word burst is initiated to the flash memory array and it is terminated by CE# deassertion after the first word in the burst.

Figure 34: Continuous Burst Read with Output Delay (ADV# LOW)
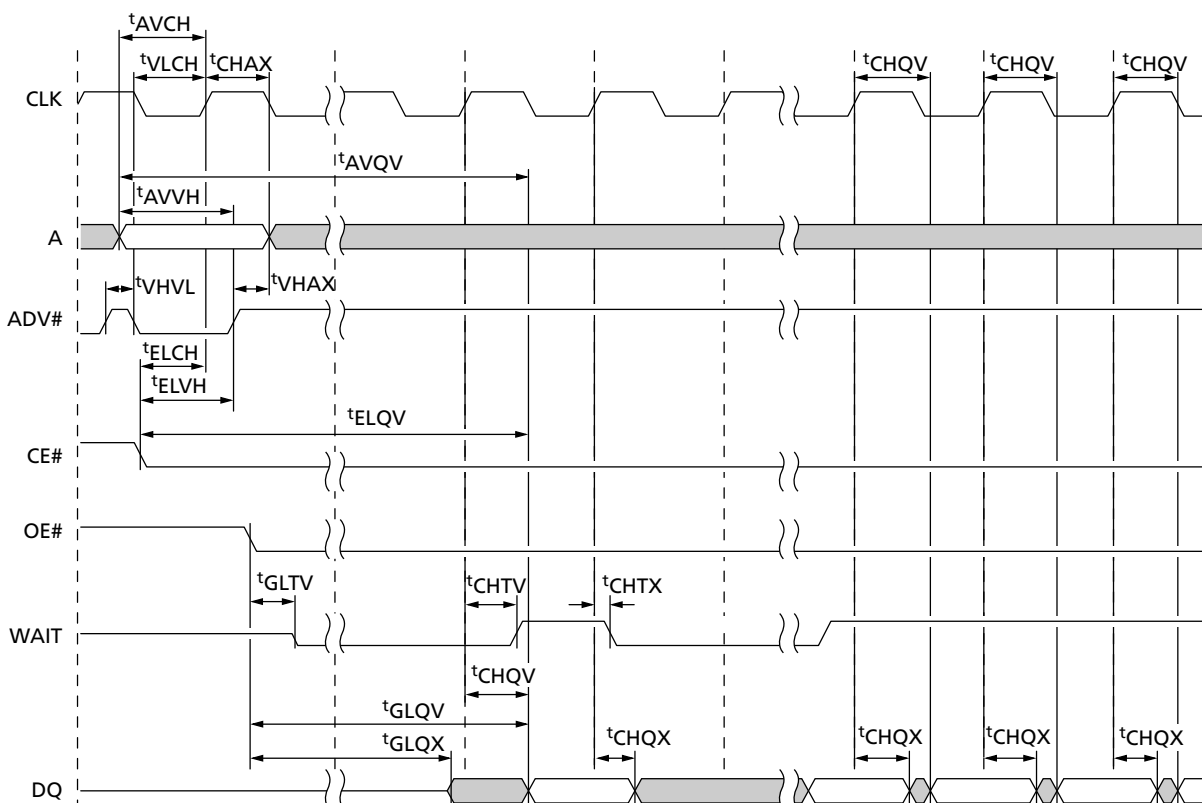
Notes: 1. WAIT is driven per OE# assertion during synchronous array or non-array read, and can be configured to assert either during or one data cycle before valid data.
2. At the end of Word Line; the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 4-word boundary aligned.

Figure 35: Synchronous Burst Mode 4-Word Read
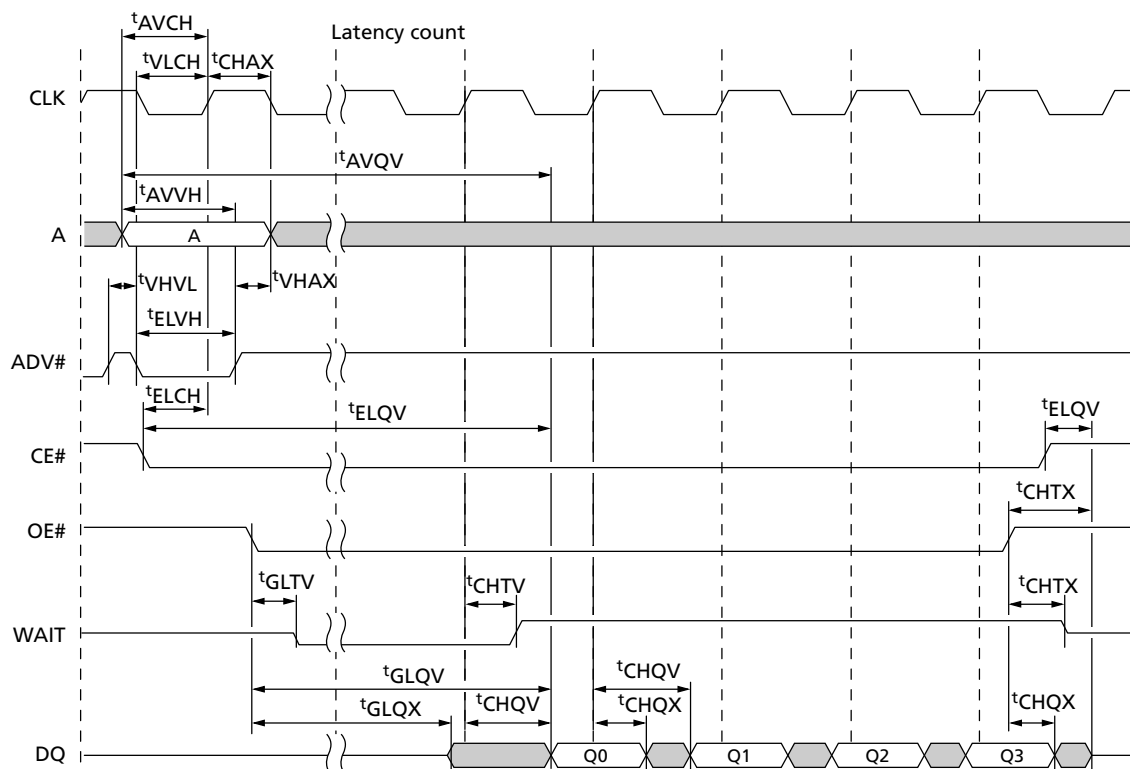
Note: 1.   WAIT is driven per OE# assertion during synchronous array or non-array read. WAIT asserted during initial latency and deasserted during valid data (RCR.10 = 0, WAIT asserted low).

AC Write Specifications

Table 46: AC Write Specifications

Number	Symbol	Parameter	Min	Max	Unit	Notes
W1	t_{PHWL}	RST# high recovery to WE# low	150	-	ns	1, 2, 3
W2	t_{ELWL}	CE# setup to WE# low	0	-	ns	1, 2, 3
W3	t_{WLWH}	WE# write pulse width low	50	-	ns	1, 2, 4
W4	t_{DVWH}	Data setup to WE# high	50	-	ns	1, 2, 12
W5	t_{AVWH}	Address setup to WE# high	50	-	ns	1, 2
W6	t_{WHEH}	CE# hold from WE# high	0	-	ns	
W7	t_{WHDX}	Data hold from WE# high	0	-	ns	
W8	t_{WHAX}	Address hold from WE# high	0	-	ns	
W9	t_{WHWL}	WE# pulse width high	20	-	ns	1, 2, 5
W10	t_{VPWH}	V_{PP} setup to WE# high	200	-	ns	1, 2, 3, 7
W11	t_{QVVL}	V_{PP} hold from Status read	0	-	ns	
W12	t_{QVBL}	WP# hold from Status read	0	-	ns	1, 2, 3, 7
W13	t_{BHWH}	WP# setup to WE# high	200	-	ns	
W14	t_{WHGL}	WE# high to OE# low	0	-	ns	1, 2, 9
W16	t_{WHQV}	WE# high to read valid	$t_{AVQV} + 35$	-	ns	1, 2, 3, 6, 10
Write to Asynchronous Read Specifications						
W18	t_{WHAV}	WE# high to Address valid	0	-	ns	1, 2, 3, 6, 8
Write to Synchronous Read Specifications						
W19	$t_{WHCH/L}$	WE# high to Clock valid	19	-	ns	1, 2, 3, 6, 10
W20	t_{WHVH}	WE# high to ADV# high	19	-	ns	
W28	t_{WHVL}	WE# high to ADV# low	7	-	ns	
Write Specifications with Clock Active						
W21	t_{VHWL}	ADV# high to WE# low	-	20	ns	1, 2, 3, 11
W22	t_{CHWL}	Clock high to WE# low	-	20	ns	

Notes:
1. Write timing characteristics during erase suspend are the same as write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Thus, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever occurs first) to CE# or WE# low (whichever occurs last). Thus, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
6. t_{WHVH} or $t_{WHCH/L}$ must be met when transiting from a write cycle to a synchronous burst read.
7. V_{PP} and WP# should be at a valid level until erase or program success is determined.
8. This specification is only applicable when transiting from a write cycle to an asynchronous read. See spec W19 and W20 for synchronous read.
9. When doing a Read Status operation following any command that alters the Status Register, W14 is 20 ns.

10. Add 10 ns if the write operation results in a RCR or block lock status change, for the subsequent read operation to reflect this change.

11. These specs are required only when the device is in a synchronous mode and clock is active during address setup phase.

12. This specification must be complied with by customer's writing timing. The result would be unpredictable if any violation to this timing specification.
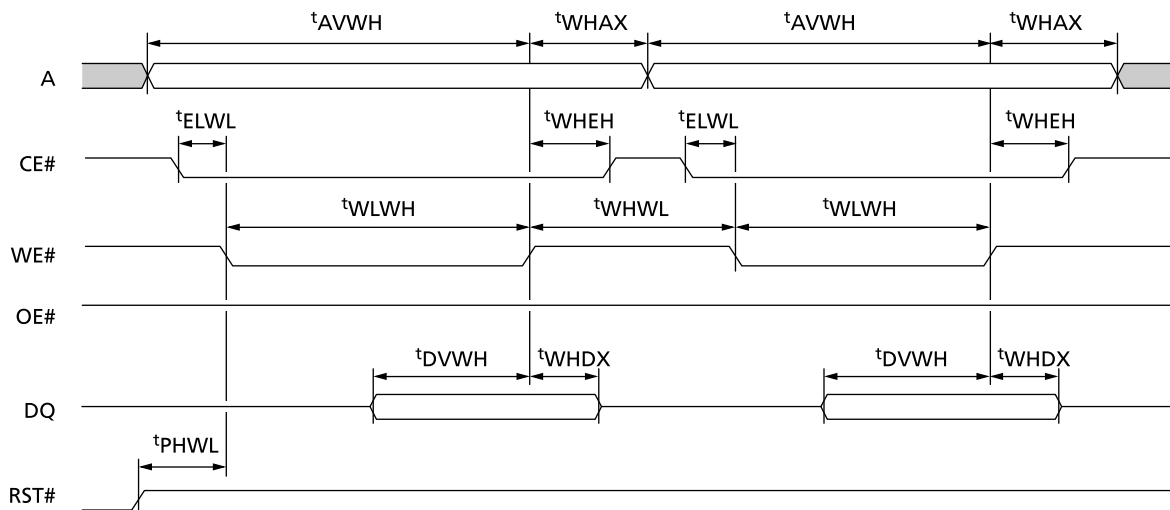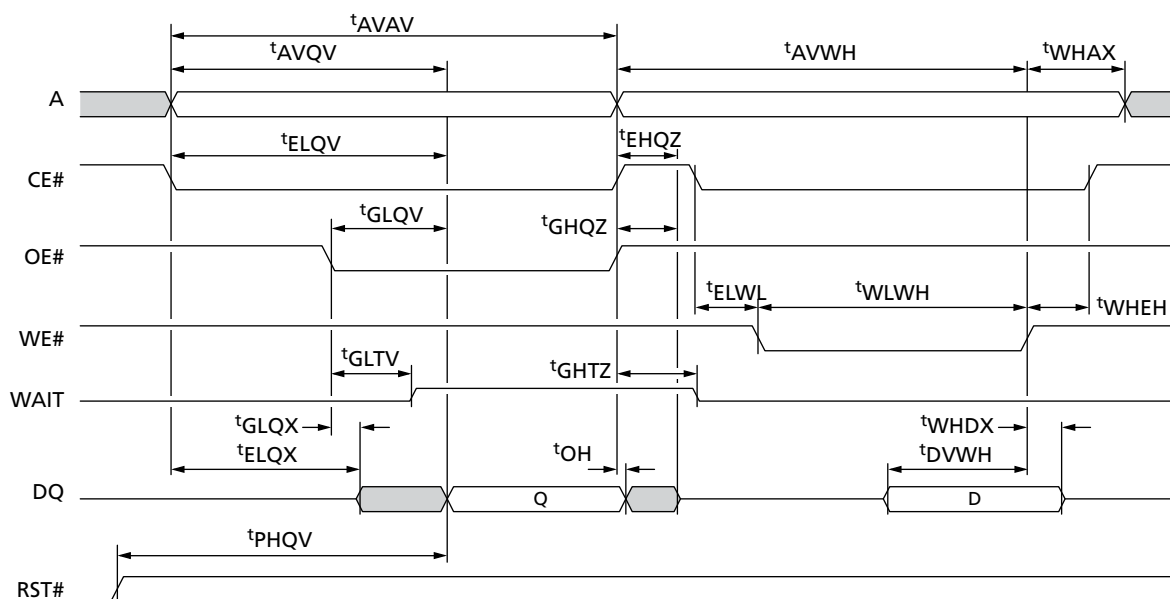
Figure 36: Write to Write Timing

Figure 37: Asynchronous Read to Write Timing

Note: 1. WAIT deasserted during asynchronous read and during write. WAIT High-Z during write per OE# deasserted.

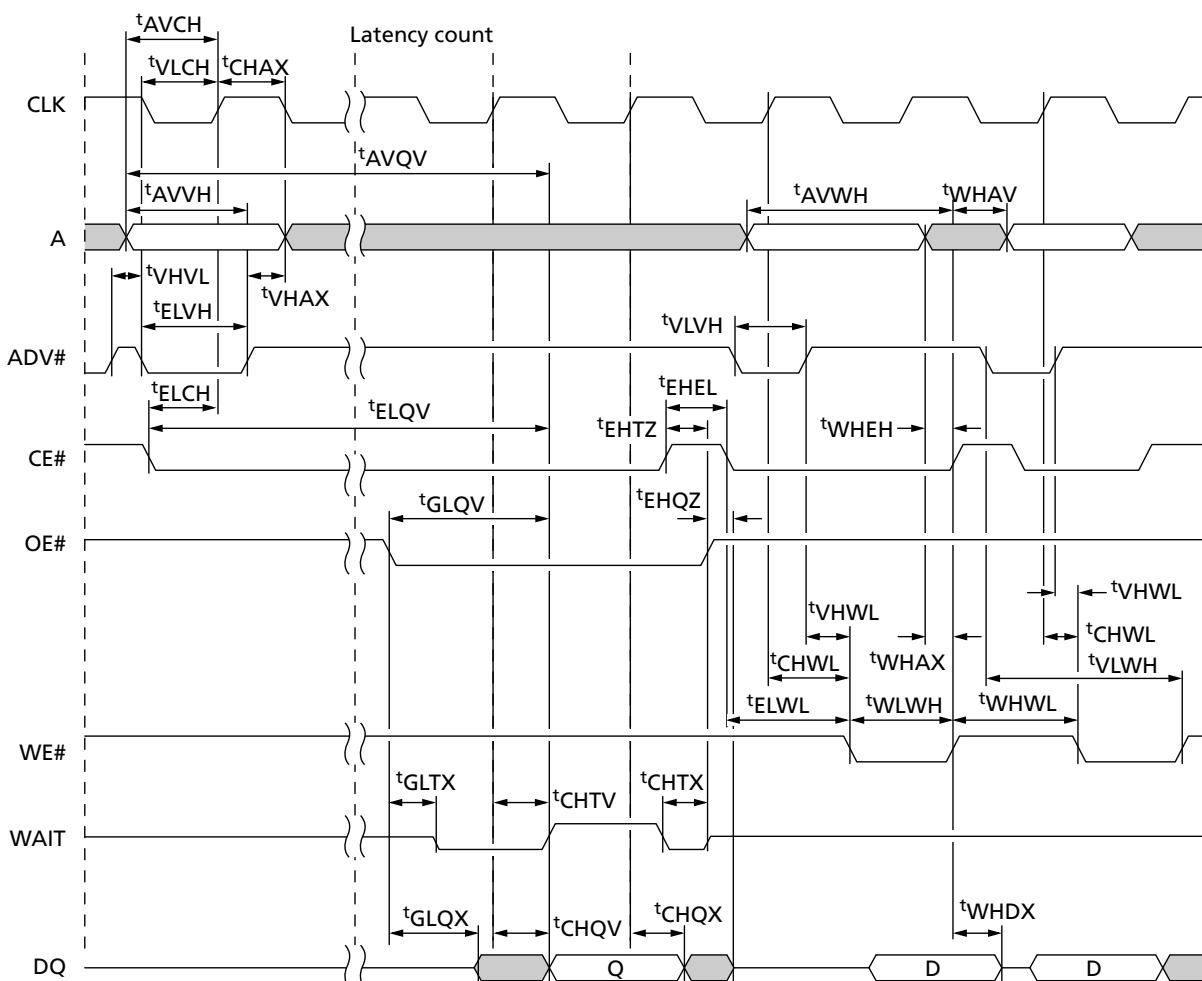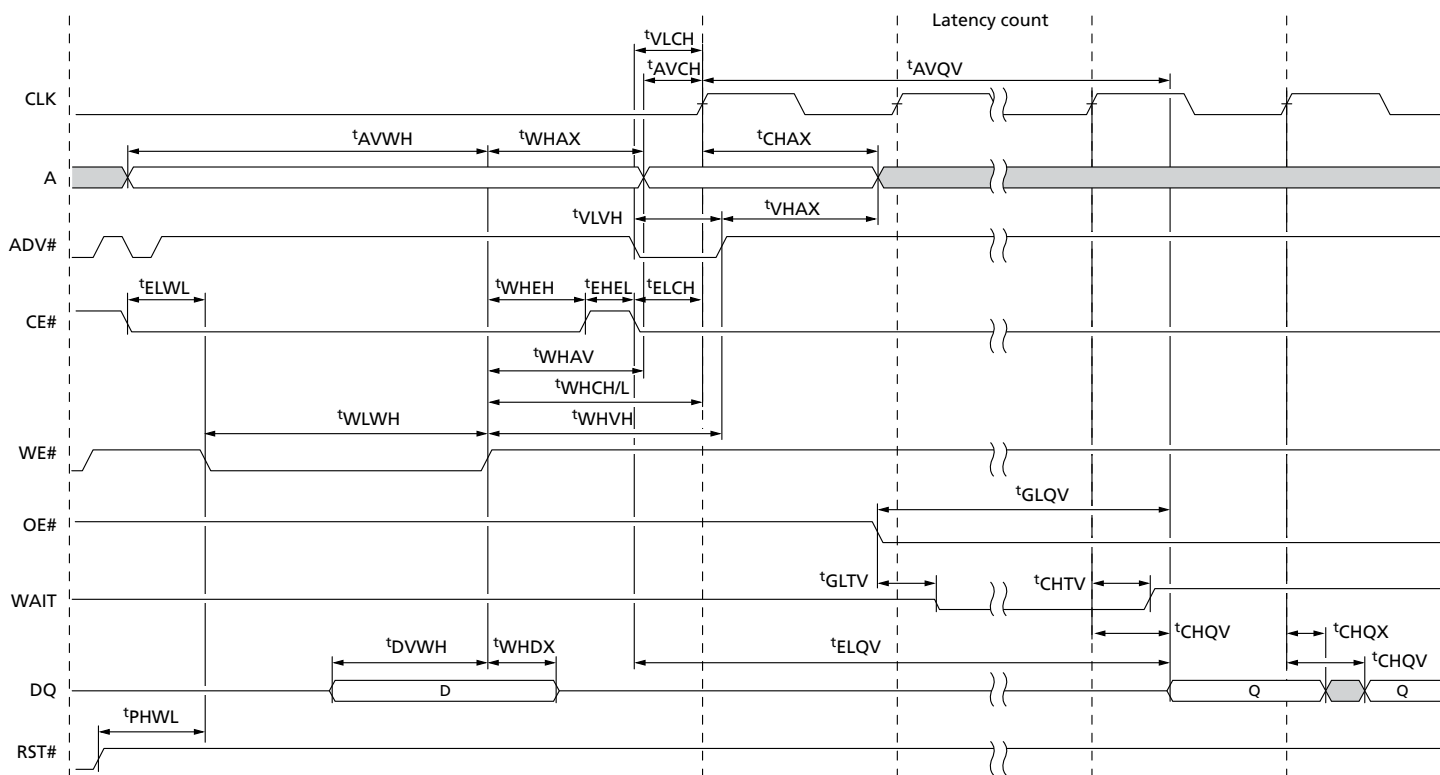**Figure 38: Write to Asynchronous Read Timing**
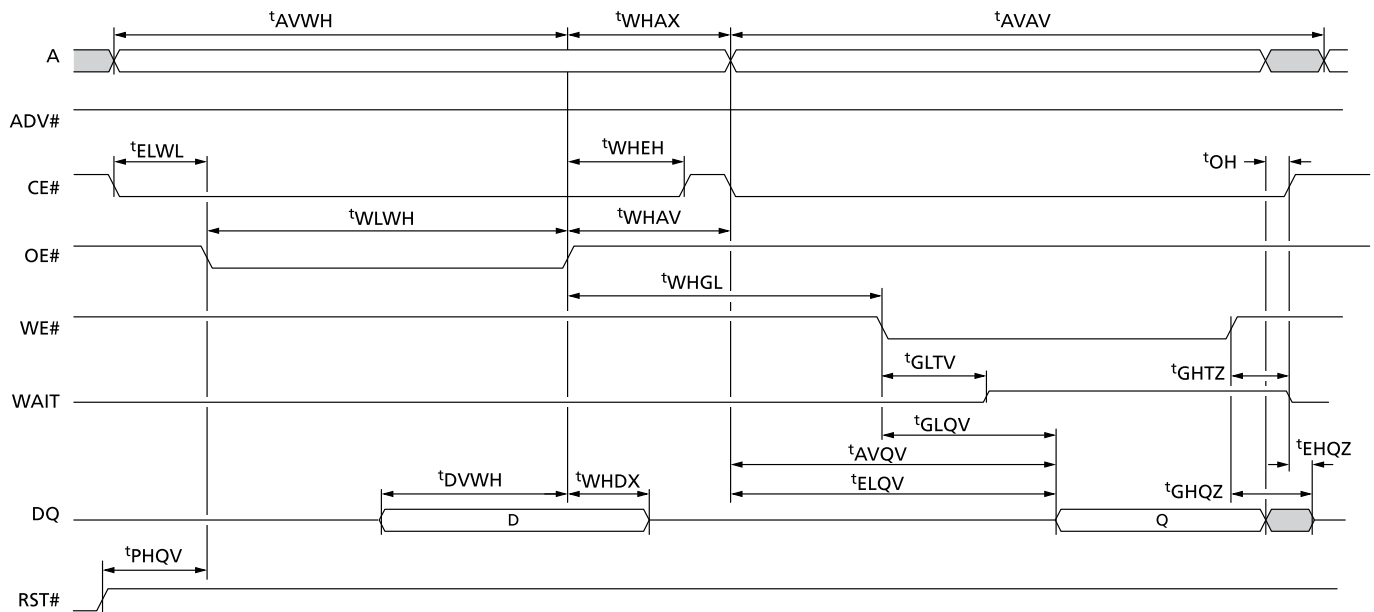
Figure 39: Synchronous Read to Write Timing

Note: 1.   WAIT shown deasserted and High-Z per OE# deassertion during write operation (RCR.
            10=0, WAIT asserted low). Clock is ignored during write operation.

Figure 40: Write to Synchronous Read Timing

Note: 1. WAIT shown deasserted and High-Z per OE# deassertion during write operation (RCR. 10=0, WAIT asserted low).

Program and Erase Characteristics

Table 47: Program and Erase Specifications

Number	Symbol	Parameter		V_{PPL}			V_{PPH}			Unit	Notes
				Min	Typ	Max	Min	Typ	Max		
Conventional Word Programming											
W200	$t_{PROG/W}$	Program Time	Single word	-	270	456	-	270	456	µs	1
Buffered Programming											
W250	t_{PROG}	Program Time	Aligned 32-Word, BP time (32 words)	-	310	716	-	310	716	µs	1
			Aligned 64-Wd, BP time (64 words)	-	310	900	-	310	900		
			Aligned 128-Wd, BP time (128 words)	-	375	1140	-	375	1140		
			Aligned 256-Wd, BP time (256 words)	-	505	1690	-	505	1690		
			one full buffer, BP time (512 words)	-	900	3016	-	900	3016		
Buffered Enhanced Factory Programming											
W451	$t_{BEFP/B}$	Program	Single byte	n/a	n/a	n/a	-	0.5	-	µs	1, 2
W452	$t_{BEFP/Setup}$		BEFP Setup	n/a	n/a	n/a	5	-	-		1
Erase and Suspend											
W500	$t_{ERS/PB}$	Erase Time	32-KByte Parameter	-	0.8	4.0	-	0.8	4.0	s	1
W501	$t_{ERS/MB}$		128-KByte Main	-	0.8	4.0	-	0.8	4.0		
W600	$t_{SUSP/P}$	Suspend Latency	Program suspend	-	25	30	-	25	30	µs	
W601	$t_{SUSP/E}$		Erase suspend	-	25	30	-	25	30		
W602	$t_{ERS/SUSP}$		Erase to Suspend	-	500	-	-	500	-		1, 3
Blank Check											
W702	$t_{BC/MB}$	blank check	Main Array Block	-	3.2	-	-	3.2	-	ms	

Notes: 1. Typical values measured at T_C = +25 °C and nominal voltages. Performance numbers are valid for all speed versions. Excludes system overhead. Sampled, but not 100% tested.
2. Averaged over entire device.
3. W602 is the typical time between an initial block erase or erase resume command and the a subsequent erase suspend command. Violating the specification repeatedly during any particular block erase may cause erase failures.

Revision History

Rev. A – 10/12

- Initial Micron brand release

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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