

# LC05111CMT



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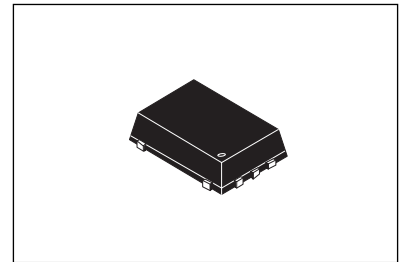
CMOS LSI

## 1-Cell Lithium-Ion Battery Protection IC with integrated Power MOS FET

### Overview

The LC05111CMT is a protection IC for 1-cell lithium-ion secondary batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over-charging, over-discharging, over-current discharging and over-current charging.

A battery protection system can be made by only LC05111CMT and few external parts.



WDFN6 2.6x4.0, 0.65P, Dual Flag

### Feature

- Charge-and-discharge power MOSFET are integrated at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$   
ON resistance (total of charge and discharge) 11.2m $\Omega$  (typ)
- Highly accurate detection voltage/current at  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.7\text{V}$ 
  - Over-charge detection  $\pm 25\text{mV}$
  - Over-discharge detection  $\pm 50\text{mV}$
  - Charge over-current detection  $\pm 0.7\text{A}$
  - Discharge over-current detection  $\pm 0.7\text{A}$
- Delay time for detection and release (fixed internally)
- Discharge/Charge over-current detection is compensated for temperature dependency of power FET
- 0V battery charging : "Permission"
- Auto wake-up function battery charging : "Permission"
- Over charge detection voltage : 4.0V to 4.5V (5mV steps)
- Over charge release hysteresis : 0V to 0.3V (100mV steps)
- Over discharge detection voltage : 2.2V to 2.7V (50mV steps)
- Over discharge release hysteresis at Auto wake-up : 0V to 0.6V (200mV steps)
- Over discharge release hysteresis : 0V to 0.075V (25mV steps)
- Discharge over current detection : 2.0A to 8.0A (0.5A steps)
- Charge over current detection : -8.0A to -2.0A (0.5A steps)

### Typical Applications

- Lithium ion battery protection

### ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

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## Specifications

**Absolute Maximum Ratings** at Ta = 25°C

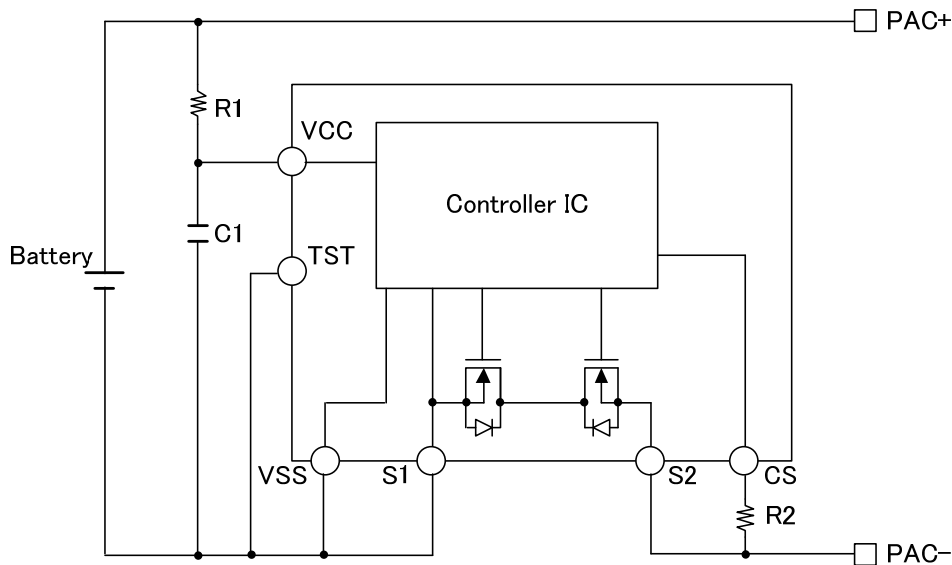
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V <sub>CC</sub>	Between PAC+ and V <sub>CC</sub> : R1=680Ω	-0.3 to +12.0	V
S1 - S2 voltage	VS1-S2		24.0	V
CS terminal Input voltage	CS		V <sub>CC</sub> -24.0	V
Charge or discharge current	BAT-, PAC-		10.0	A
TST Input voltage	TST		-0.3 to +7.0	V
Storage temperature	Tstg		-55 to +125	°C
Current between S1 and S2(DC)	ID	V <sub>CC</sub> = 3.7V	10.0	A
Current between S1 and S2 (continuous pulse)	IDP	Pulse Width<10μs, duty cycle<1%	35	A
Operating ambient temperature	Topr		-40 to +85	°C
Allowable power dissipation	Pd	Glass epoxy four-layer board. Board size 27.4mm x 3.1mm x 0.8mm	450	mW
Junction temperature	Tj		125	°C

Caution 1) Absolute maximum ratings represent the values which cannot be exceeded even for a moment.

Caution 2) If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## Example of Application Circuit



Components	Recommended value	MAX	unit	Description
R1	680	1k	Ω	
R2	1k	2k	Ω	
C1	0.1μ	1.0μ	F	

\* We don't guarantee the characteristics of the circuit shown above.

\* TST pin would be better to be connected to VSS pin, though it is connected to VSS with internal resistor (100kΩ typ).

\* Battery voltage drop occurs, a current of about 60uA flow period of 1.5V-1.3V.

**Electrical Characteristics**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Detection voltage							
Over-charge detection voltage	Vov	R1=680Ω	25°C	Vov_set -25	Vov_set	Vov_set +25	mV
			-30 to 70°C	Vov_set -30	Vov_set	Vov_set +30	
Over-charge release voltage	Vovr	R1=680Ω	25°C	Vovr_set -40	Vovr_set	Vovr_set +40	mV
			-30 to 70°C	Vovr_set -70	Vovr_set	Vovr_set +70	
Over-discharge detection voltage	Vuv	R1=680Ω	25°C	Vuv_set -50	Vuv_set	Vuv_set +50	mV
			-30 to 70°C	Vuv_set -80	Vuv_set	Vuv_set +80	
Over-discharge release voltage	Vuvr	R1=680Ω CS=0V	25°C	Vuvr_set -100	Vuvr_set	Vuvr_set +100	mV
			-30 to 70°C	Vuvr_set -120	Vuvr_set	Vuvr_set +120	
Over-discharge release voltage2	Vuvr2	R1=680Ω CS=open	25°C	Vuvr2_set -100	Vuvr2_set	Vuvr2_set +100	mV
			-30 to 70°C	Vuvr2_set -120	Vuvr2_set	Vuvr2_set +120	
Discharge over-current detection current	loc	R2=1kΩ	25°C VCC=3.7V	loc_set -0.7	loc_set	loc_set +0.7	A
			-30 to 70°C VCC=2.6 to 4.3V	loc_set -1.2	loc_set	loc_set +1.2	
Discharge over-current release current	locr	R2=1kΩ	25°C VCC=3.7V	(loc_set-0.7)	(loc_set)	(loc_set+0.7)	A
			-30 to 70°C VCC=2.6 to 4.3V	(loc_set-1.2)	(loc_set)	oc_set+1.2)	
Discharge over-current detection current(Short circuit)	loc2	R2=1kΩ	25°C VCC=3.7V	loc2_set*0.8	loc2_set	loc2_set*1.2	A
Charge over-current detection current	loch	R2=1kΩ	25°C VCC=3.7V	loch_set -0.7	loch_set	loch_set +0.7	A
			-30 to 70°C VCC=2.6 to 4.3V	loch_set -1.2	loch_set	loch_set +1.2	
Charge over-current release current	lochr	R2=1kΩ	25°C VCC=3.7V	loch_set -0.7	loch_set	loch_set +0.7	A
			-30 to 70°C VCC=2.6 to 4.3V	loch_set -1.2	loch_set	loch_set +1.2	
Input voltage							
Operating Voltage for 0V charging	Vchg	VCC-CS VCC-GND =0V	25°C			1.4	V
Current consumption							
Operating current	icc	At normal state	25°C VCC=3.7V		3	6	μA
Stand-by current	lstb	At Stand-by state Auto wake-up =enable	25°C VCC=2.0V			0.95	μA

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resistance							
ON resistance 1 of integrated power MOS FET	Ron1	V <sub>CC</sub> =3.1V I=±2.0A	25°C	10.4	13	18.2	mΩ
ON resistance 2 of integrated power MOS FET	Ron2	V <sub>CC</sub> =3.7V I=±2.0A	25°C	9.6	12	15.6	mΩ
ON resistance 3 of integrated power MOS FET	Ron3	V <sub>CC</sub> =4.0V I=±2.0A	25°C	9.2	11.6	15	mΩ
ON resistance 4 of integrated power MOS FET	Ron4	V <sub>CC</sub> =4.5V I=±2.0A	25°C	8.8	11.2	14	mΩ
Internal resistance (V <sub>CC</sub> -CS)	Rcsu	V <sub>CC</sub> =V <sub>uv</sub> _set CS=0V	25°C		300		kΩ
Internal resistance (V <sub>SS</sub> -CS)	Rcsd	V <sub>CC</sub> =3.7V CS=0.1V	25°C		15		kΩ

### Detection and Release delay time

Over-charge detection delay time	Tov		25°C	0.8	1	1.2	sec
			-30 to 70°C	0.6	1	1.5	
Over-charge release delay time	Tovr		25°C	12.8	16	19.2	ms
			-30 to 70°C	9.6	16	24	
Over-discharge detection delay time	Tuv		25°C	16	20	24	ms
			-30 to 70°C	12	20	30	
Over-discharge release delay time	Tuvr		25°C	0.9	1.1	1.3	ms
			-30 to 70°C	0.6	1.1	1.5	
Discharge over-current detection delay time 1	Toc1	V <sub>CC</sub> =3.7V	25°C	9.6	12	14.4	ms
			-30 to 70°C	7.2	12	18	
Discharge over-current release delay time 1	Tocr1	V <sub>CC</sub> =3.7V	25°C	3.2	4	4.8	ms
			-30 to 70°C	2.4	4	6	
Discharge over-current detection delay time 2 (Short circuit)	Toc2	V <sub>CC</sub> =3.7V	25°C	280	400	560	μs
			-30 to 70°C	180	400	800	
Charge Over-current detection delay time	Toch	V <sub>CC</sub> =3.7V	25°C	12.8	16	19.2	ms
			-30 to 70°C	9.6	16	24	
Charge Over-current release delay time	Tochr	V <sub>CC</sub> =3.7V	25°C	3.2	4	4.8	ms
			-30 to 70°C	2.4	4	6	

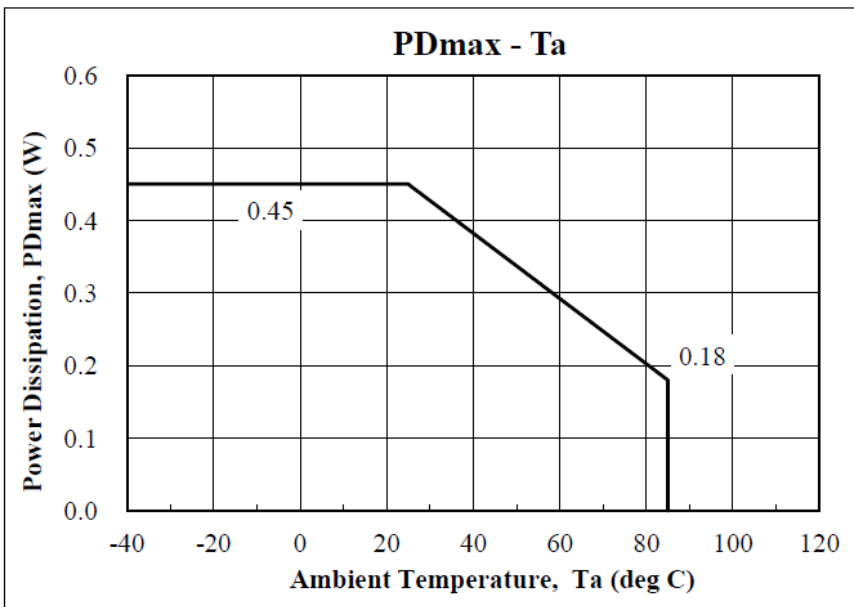
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# LC05111CMT

## SELECTION GUIDE

Device	Vov(V)	Vovr(V)	Vuv(V)	Vuvr(V)	Vuvr2(V)	AWUP	loc(A)	loch(A)	loc2(A)	0Vcharge
LC05111C01MTTTG	4.425	4.225	2.500	2.500	2.900	enable	6.00	4.00	17.5	enable
LC05111C02MTTTG	4.280	4.180	2.700	2.700	2.900	enable	6.00	3.50	21.5	enable
LC05111C03MTTTG	4.425	4.225	2.600	2.600	3.000	enable	6.00	4.00	17.5	enable
LC05111C04MTTTG	4.375	4.175	2.400	2.400	2.800	enable	6.15	6.25	17.5	enable
LC05111C05MTTTG	4.425	4.225	2.300	2.300	2.700	enable	4.00	4.00	17.5	enable
LC05111C06MTTTG	4.425	4.225	2.400	2.400	2.800	enable	6.00	4.00	17.5	enable
LC05111C07MTTTG	4.425	4.225	2.500	2.520	2.900	enable	5.00	5.00	17.5	enable
LC05111C08MTTTG	4.430	4.430	2.400	2.450	2.800	enable	5.00	5.00	17.5	enable
LC05111C09MTTTG	4.400	4.200	2.400	2.400	3.000	enable	6.00	4.00	17.5	enable
LC05111C10MTTTG	4.280	4.080	2.600	2.600	3.000	enable	6.00	4.00	17.5	enable
LC05111C11MTTTG	4.310	4.110	2.500	2.500	2.900	enable	2.00	2.00	17.5	enable
LC05111C12MTTTG	4.450	4.450	2.600	2.600	3.000	enable	4.0	3.0	15.0	enable

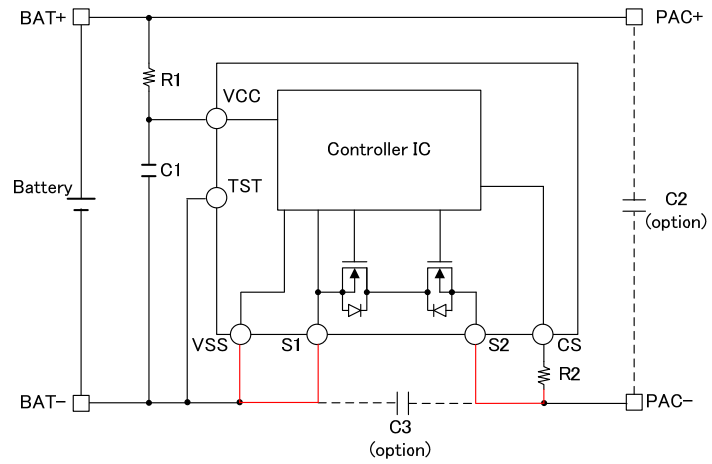
## Pdmax-Ta graph



# LC05111CMT

## Recommended board layout

Board schematic



Board size L=27.4mm W=3.1 mm H=0.8mm glass-epoxy 4layers



## LC05111CMT

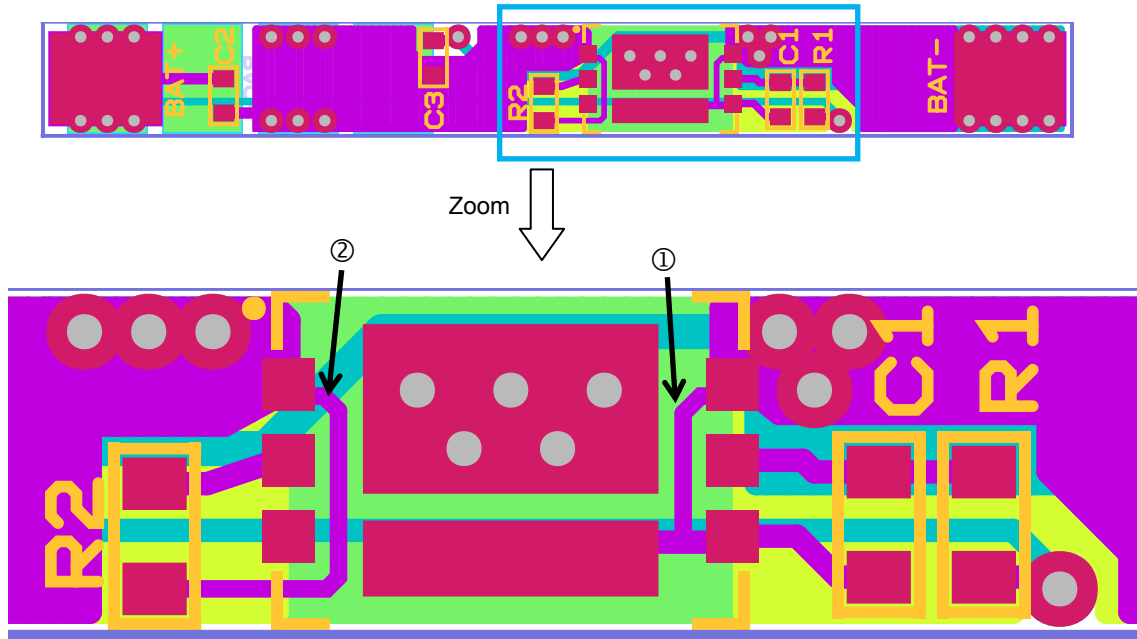
### Note

- ① Please connect the VSS line to a pin of S1 directly.
- ② Please connect the resistance of R2 to a pin of S2 directly.

It can perform the detection of the overcurrent exactly by performing these.

It can get rid of influence of the wiring impedance caused by a severe electric current flowing through S1 and S2.

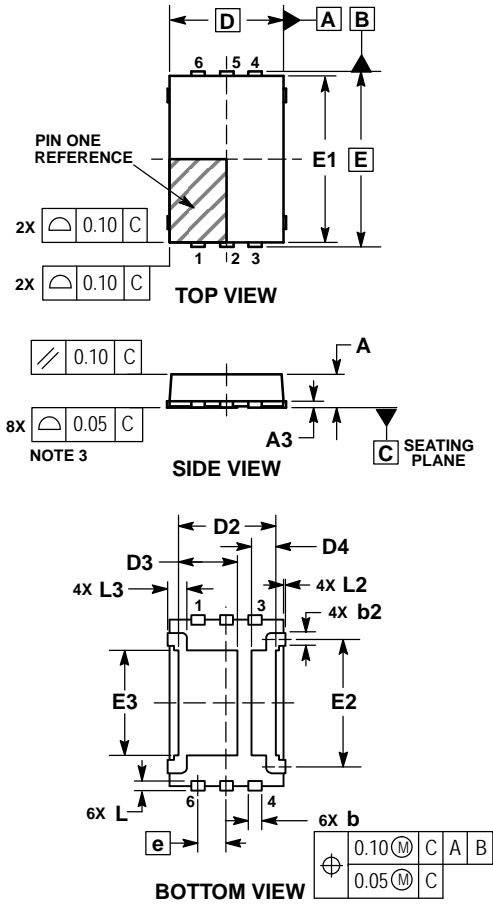
Red line of schematic is very important line.



Package Dimensions

unit : mm

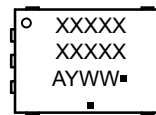
WDFN6 2.6x4.0, 0.65P, Dual Flag  
CASE 511BZ  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. PROFILE TOLERANCE APPLIES TO THE EXPOSED PADS AS WELL AS THE LEADS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.80
A3	0.10	0.25
b	0.25	0.40
b2	0.15	0.30
D	2.60 BSC	
D2	2.075	2.375
D3	1.20	1.50
D4	0.40	0.70
E	4.00 BSC	
E1	3.80 REF	
E2	2.95	3.05
E3	2.25	2.55
e	0.65 BSC	
L	0.12	0.32
L2	---	0.10
L3	---	0.55

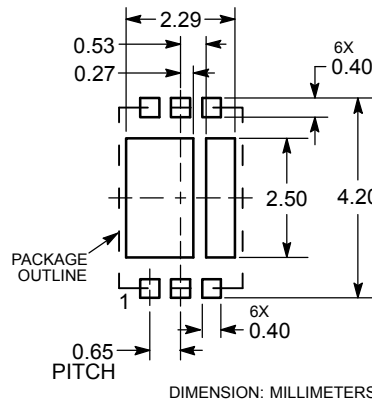
GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)  
\*This information is generic. Please refer to device data sheet for actual part marking.

RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

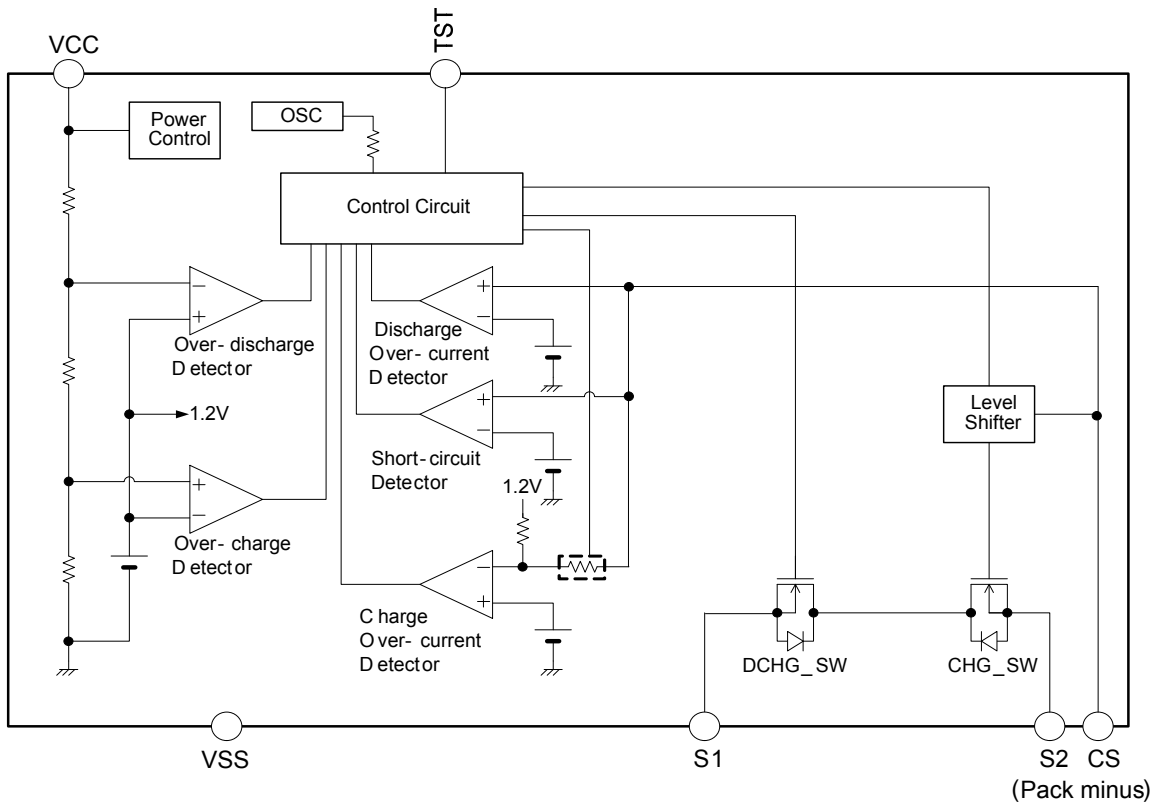


# LC0511CMT

## Pin Functions

Pin No.	Symbol	Pin Function	Description
1	S2	Charger minus voltage input pin	
2	CS	Charger minus voltage input pin	
3	TST	Package trimming Terminal	Connected to GND by internal 100kΩ resistor
4	VSS	Negative power input	
5	VCC	VCC terminal	
6	S1	Negative power input	
7	Drain	<b>Drain of FET</b>	Exposed pad
8	Sub	<b>IC Sub (VSS)</b>	Exposed pad

## Block Diagram



## (1) Normal mode

- LC05111CMT controls charging and discharging by detecting cell voltage (VCC) and controls S2-S1 current. In case that cell voltage is between over-discharge detection voltage (Vuv) and over-charge detection voltage (Vov), and S2-S1 current is between charge over-current detection current (Ioch) and discharge over-current detection current (Ioc), internal power MOS FETs as CHG\_SW, DCHG\_SW are all turned ON.

This is the normal mode, and it is possible to be charged and discharged.

## (2) Over-charging mode

- Internal power MOS FET as CHG\_SW will be turned off if cell voltage will get equal to or higher than over-charge detection voltage (Vov) over the delay time of over-charging (Tov).

This is the over-charging detection mode.

- The recovery from over-charging will be made after the following three conditions are all satisfied.
  - a. Charger is removed from IC.
  - b. Cell voltage will get lower than over-charge release voltage (Vovr) over the delay time of over-charging release (Tovr) due to discharging through load.

Consequently, internal power MOS FET as CHG\_SW will be turned on and normal mode will be resumed.

- In over-charging mode, discharging over-current detection is made only when CS pin will get higher than discharging over-current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG\_SW FET.

If CS pin voltage will get higher than discharging over-current detection current 2 (Ioc2) over the delay time of discharging over-current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG\_SW is turned off.(short-circuit detection mode)

After detecting short-circuit, CS pin will be pulled down to Vss by internal resistor Rcsd.

The recovery from short circuit detection in over-charging mode will be made after the following two conditions are satisfied.

- a. Load is removed from IC.
- b. CS pin voltage will get equal to or lower than discharging over-current detection current 2 (Ioc2) due to CS pin pulled down through Rcsd.

Consequently, internal power MOS FET as DCHG\_SW will be turned on, and over-charging detection mode will be resumed.

## (3) Over-discharging mode

- If cell voltage will get lower than over-discharge detection voltage (Vuv) over the delay time of over-discharging (Tuv), discharging will be shut off, because internal power FETs as DCHG\_SW is turned off.

This is the over-discharging mode.

After detecting over-discharging, CS pin will be pulled up to Vcc by internal resistor Rcsu and the bias of internal circuits will be shut off. (Stand-by mode)

In stand-by mode, operating current is suppressed under 0.95uA (max).

- The recovery from stand-by mode will be made by internal circuits biased after the following two conditions are satisfied.
  - a. Charger is connected.
  - b. VCC level rise more than Over-discharge release voltage2(Vuvr2) without charger.(Auto wake-up function)
- If CS pin voltage will get lower than charger detecting voltage (Vchg) by connecting charger under the condition that cell voltage is lower than over-discharge detection voltage, internal power MOS FET as DCHG\_SW is turned on and power dissipation in power MOS FETs is suppressed.

\*In case that charging current is low enough, ripple current will be appeared at S2 terminal when CS pin voltage is near by the threshold of charger detecting voltage (Vchg).

It is caused that the two modes, charger detected and charger not detected (charging through parasitic diodes of DCHG\_SW, is alternately appeared.

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- By continuing to be charged, if cell voltage will get higher than over-discharge detection voltage ( $V_{uvr}$ ) over the delay time of over-discharging ( $T_{uvr}$ ), internal power MOS FETs as DCHG\_SW is turned on and normal mode will be resumed.
- In over-discharge detection mode, charging over-current detection does not operate.  
By continuing to be charged, charging over-current detection starts to operate after cell voltage goes up more than over-discharge release voltage ( $V_{uvr}$ ).

#### (4) Discharging over-current detection mode 1

- Internal power MOS FET as DCHG\_SW will be turned off and discharging current will be shut off if CS pin voltage will get equal to or higher than discharging over-current detection current ( $I_{oc}$ ) over the delay time of discharging over-current ( $T_{oc1}$ ).  
This is the discharging over-current detection mode 1.  
In discharging over-current detection mode 1, CS pin will be pulled down to  $V_{ss}$  with internal resistor  $R_{csd}$ .
- The recovery from discharging over-current detection mode will be made after the following two conditions are satisfied.
  - a. Load is removed from IC.
  - b. CS pin voltage will get equal to or lower than discharging over-current release current ( $I_{ocr}$ ) over the delay time of discharging over-current release ( $T_{ocr1}$ ) due to CS pin pulled down through  $R_{csd}$ .

Consequently, internal power MOS FET as DCHG\_SW will be turned on, and normal mode will be resumed.

#### (5) Discharging over-current detection mode 2 (short circuit detection)

- Internal power MOS FET as DCHG\_SW will be turned off and discharging current will be shut off if CS pin voltage will get equal to or higher than discharging over-current detection current2 ( $I_{oc2}$ ) over the delay time of discharging over-current 2 ( $T_{oc2}$ ).  
This is the short circuit detection mode.
- In short circuit detection mode, CS pin will be pulled down to  $V_{ss}$  by internal resistor  $R_{csd}$ .  
The recovery from short circuit detection mode will be made after the following two conditions are satisfied.
  - a. Load is removed from IC.
  - b. CS pin voltage will get equal to or lower than discharging over-current release current ( $I_{ocr}$ ) over the delay time of discharging over-current release ( $T_{ocr1}$ ) due to CS pin pulled down through  $R_{csd}$ .

Consequently, internal power MOS FET as DCHG\_SW will be turned on, and normal mode will be resumed.

#### (6) Charging over-current detection mode

- Internal power MOS FET as CHG\_SW will be turned off and charging current will be shut off if CS pin voltage will get equal to or lower than charging over-current detection current ( $I_{och}$ ) over the delay time of charging over-current ( $T_{och}$ ).  
This is the charging over-current detection mode.
- The recovery from charging over-current detection mode will be made after the following two conditions is satisfied.
  - a. Charger is removed from IC and CS pin will get higher by load connected.
  - b. CS pin voltage will get equal to or higher than charging over-current release current ( $I_{ochr}$ ) over the delay time of charging over-current release ( $T_{ochr}$ ).

Consequently, internal power MOS FET as CHG\_SW will be turned on, and normal mode will be resumed.

\*Internal current flows out through CS and S2 terminals.

After charger is removed, it flows through parasitic diode of CHG\_SW FET.

Therefore, CS pin voltage will go up more than charging over-current release current ( $I_{ochr}$ ).

So CS pin voltage is not an indispensable condition for recovery from charging over-current detection.

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### (7) Available Voltage for 0V charging

It is the function that the voltage of a connected battery can charge from the state that became 0V by self-discharge. The 0V battery charge start battery charger voltage (Vchg), it fix a gate of the charge system order FET to the VDD terminal voltage when it connect a battery charger of the above-mentioned voltage to PAC+ terminal between PAC- terminals.

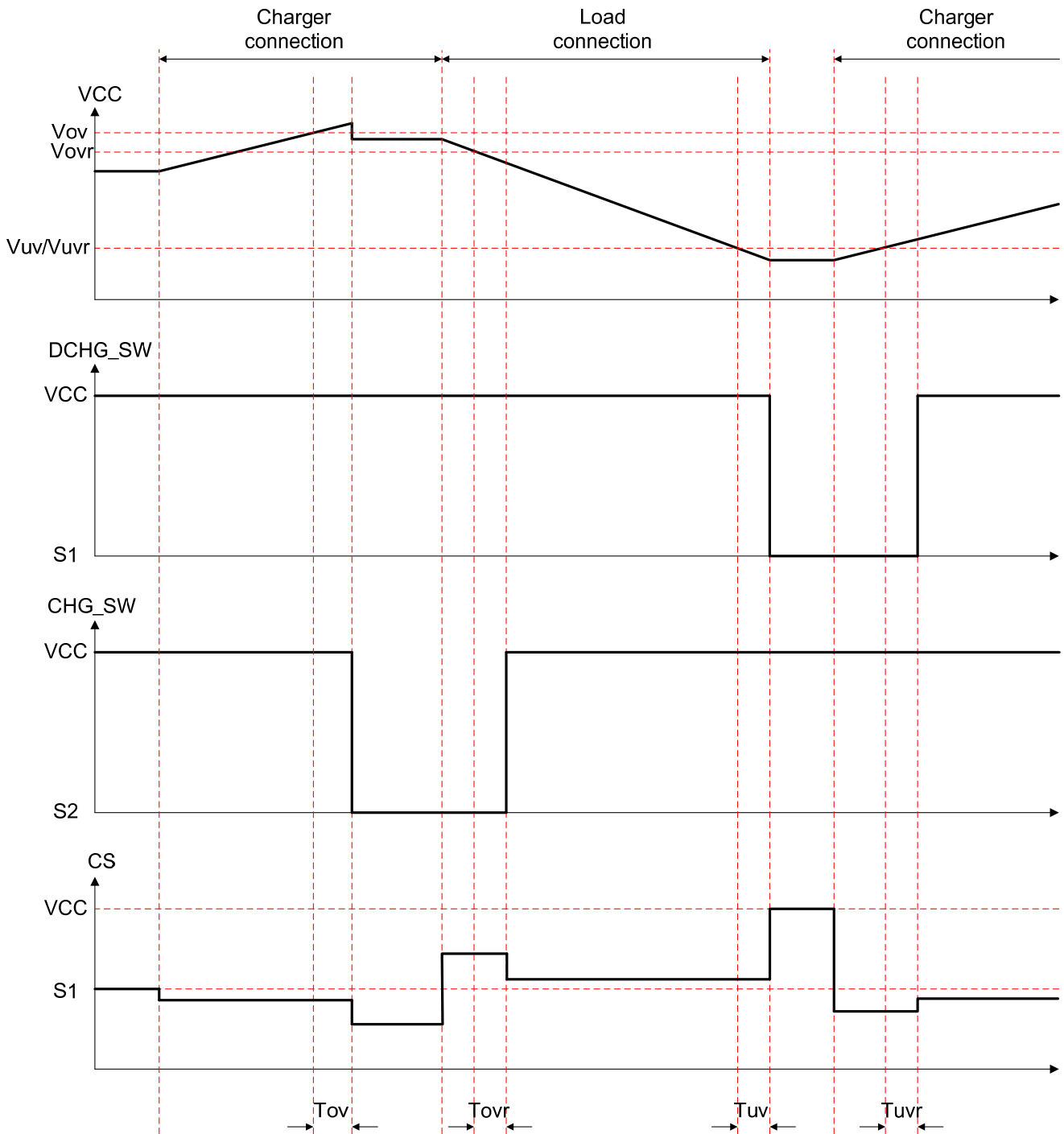
Gate-source voltage of the charge control FET becomes equal to the turn-on voltage or more due to the charger voltage, the charging control FET.

To start charging row is turned on.

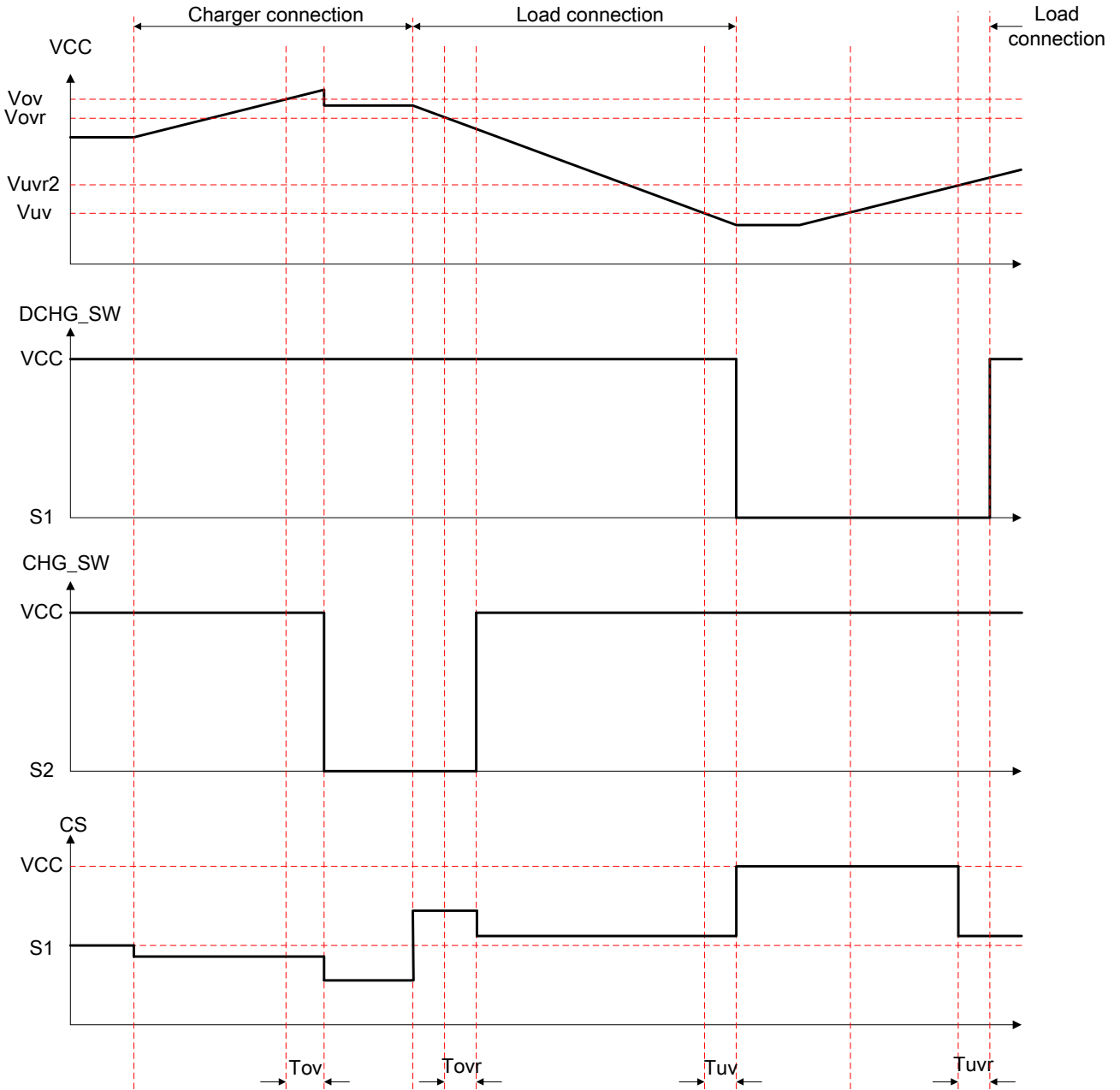
Discharge control FET is off at this time, the charge current flows through the internal parasitic diode in the discharging control FET. It is the normal state battery voltage becomes the overdischarge release voltage (Vuvr) or more.

Timing Chart

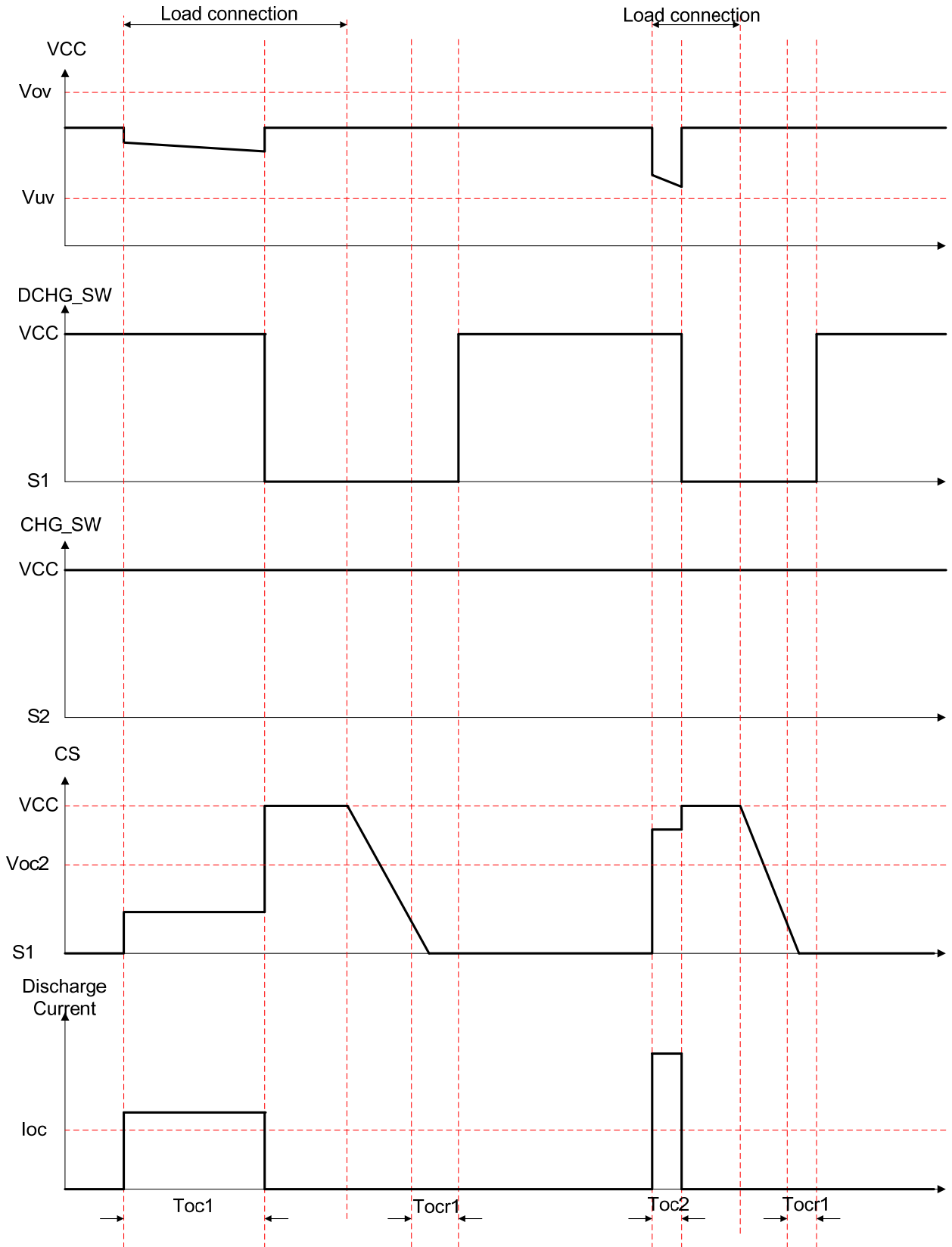
Over-charge detection/release, Over-discharge detection/release (connect charger)



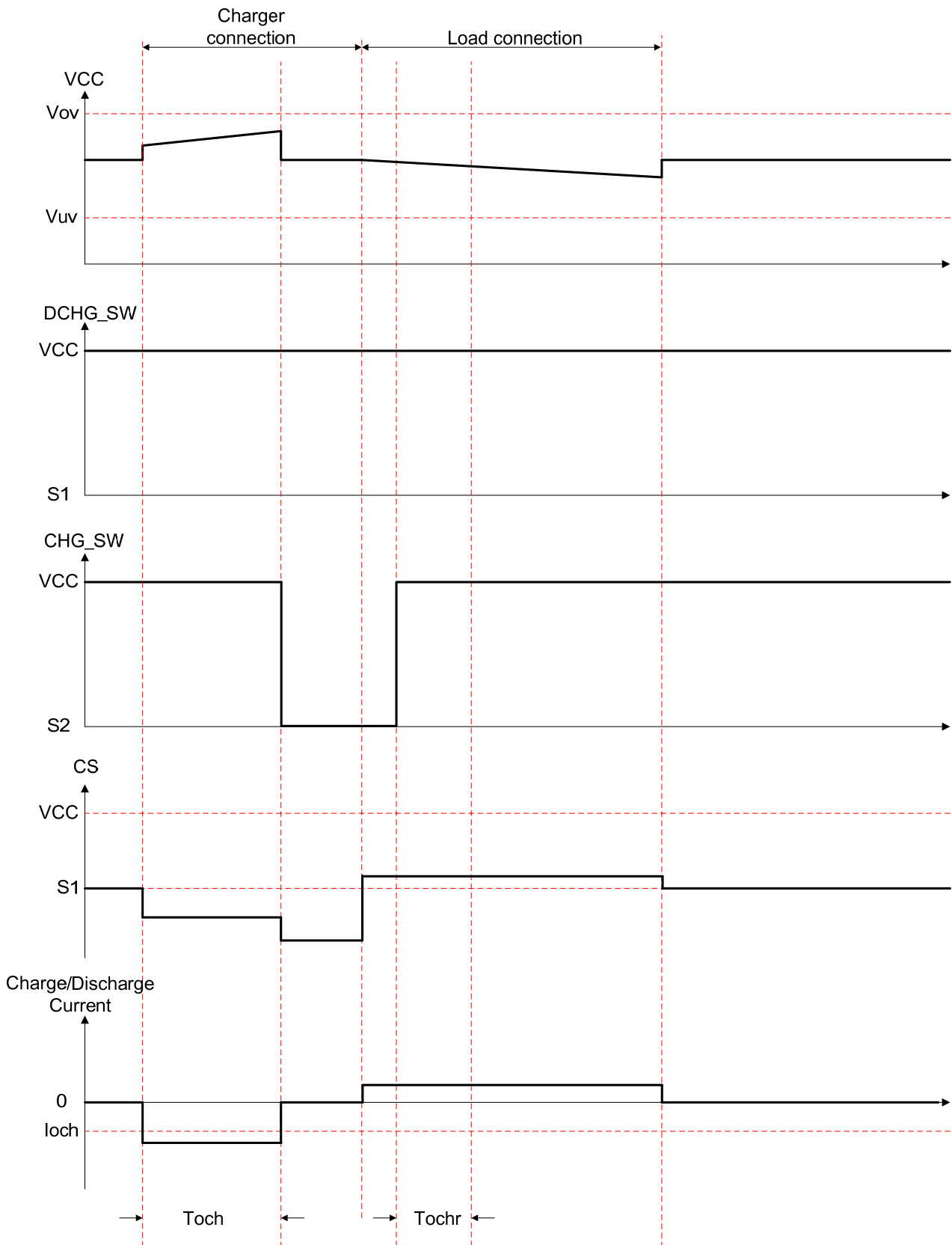
Over-charge detection/release, Over-discharge detection/release (non connect charger)



Discharge over-current detection1, Discharge over-current detection2  
(Short circuit)



Charge over-current detection





**ORDERING INFORMATION**

Device	Package	Shipping (Qty / Packing)
LC05111C01MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C02MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C03MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C04MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C05MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C06MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C07MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C08MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C09MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C10MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C11MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel
LC05111C12MTTTG	WDFN6 2.6x4.0, 0.65P, Dual Flag (Pb-Free / Halogen Free)	4000 / Tape & Reel

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- Консультации по применению компонента;
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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