

512 K (32 K x 16) Static RAM

Features

- Pin-and function-compatible with CY7C1020CV33
- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 60 \text{ mA @ } 10 \text{ ns}$
- Low CMOS standby power
 - $I_{SB2} = 3 \text{ mA}$
- 2.0 V Data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin TSOP II packages

Functional Description

The CY7C1020DV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has

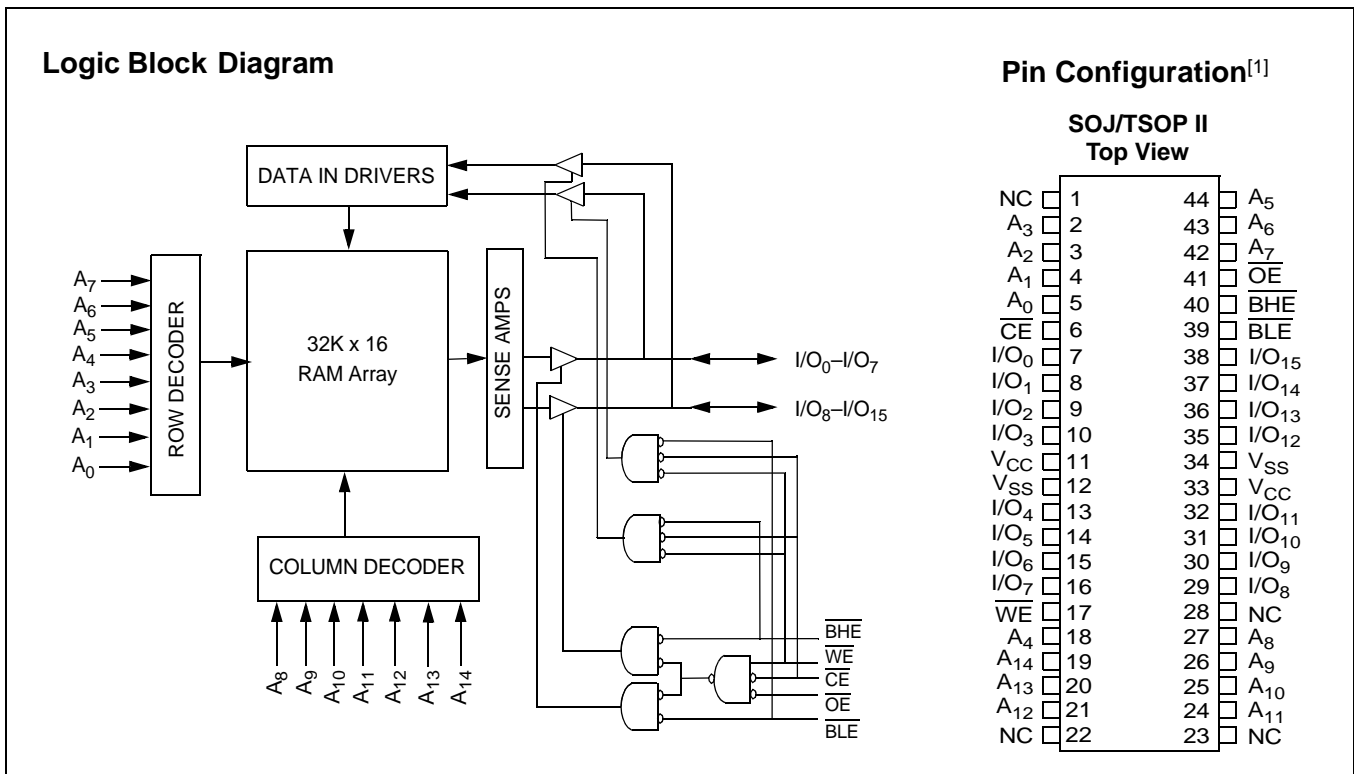
an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking chip enable (CE) and write enable (WE) inputs LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₄). If byte high enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₄).

Reading from the device is accomplished by taking chip enable (CE) and output enable (OE) LOW while forcing the write enable (WE) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If byte high enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1020DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin TSOP II packages.



Notes

1. NC pins are not connected on the die.

Selection Guide

| | -10 (Industrial) | Unit |
|------------------------------|-------------------------|-------------|
| Maximum access time | 10 | ns |
| Maximum operating current | 60 | mA |
| Maximum CMOS standby current | 3 | mA |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} to Relative GND^[2] ... -0.5 V to +4.6 V
 DC voltage applied to outputs in High-Z State^[2] -0.5 V to V_{CC} + 0.5 V

DC input voltage^[2] -0.5 V to V_{CC} + 0.5 V
 Current into outputs (LOW) 20 mA
 Static discharge voltage > 2001 V (per MIL-STD-883, Method 3015)
 Latch-up current > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} | Speed |
|--------------|----------------------------|-----------------------|--------------|
| Industrial | -40 °C to +85 °C | 3.3 V ± 0.3 V | 10 ns |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -10 (Industrial) | | Unit |
|------------------|---------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-----------------------|-------------|
| | | | Min. | Max. | |
| V _{OH} | Output HIGH voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | | V |
| V _{OL} | Output LOW voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | V |
| V _{IH} | Input HIGH voltage | | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW voltage ^[2] | | -0.3 | 0.8 | V |
| I _{IX} | Input Load current | GND ≤ V _I ≤ V _{CC} | -1 | +1 | μA |
| I _{OZ} | Output leakage current | GND ≤ V _I ≤ V _{CC} , Output Disabled | -1 | +1 | μA |
| I _{CC} | V _{CC} operating supply current | V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} | 100 MHz | 60 | mA |
| | | | 83 MHz | 55 | mA |
| | | | 66 MHz | 45 | mA |
| | | | 40 MHz | 30 | mA |
| I _{SB1} | Automatic CE Power-down Current—TTL Inputs | Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX} | | 10 | mA |
| I _{SB2} | Automatic CE Power-down Current—CMOS Inputs | Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0 | | 3 | mA |

Notes

2. V_{IL}(min.) = -2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.

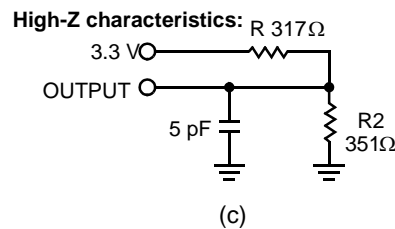
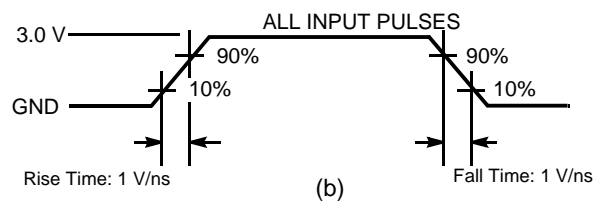
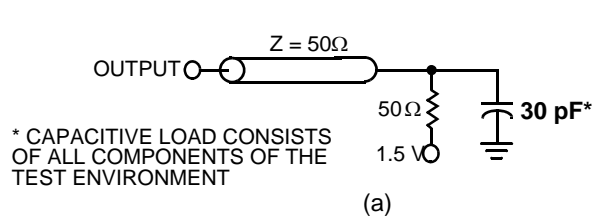
Capacitance^[3]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|-----------------------------------------------------------|------|------|
| C _{IN} | Input capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 3.3 V | 8 | pF |
| C _{OUT} | Output capacitance | | 8 | pF |

Thermal Resistance^[3]

| Parameter | Description | Test Conditions | SOJ | TSOP II | Unit |
|-----------------|------------------------------------------|-------------------------------------------------------------------------|-------|---------|------|
| Θ _{JA} | Thermal resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 59.52 | 53.91 | °C/W |
| Θ _{JC} | Thermal resistance (Junction to Case) | | 36.75 | 21.24 | °C/W |

AC Test Loads and Waveforms^[4]



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

Switching Characteristics Over the Operating Range ^[5]

| Parameter | Description | -10 (Industrial) | | Unit |
|-----------------------------------|--------------------------------------------------|------------------|------|---------|
| | | Min. | Max. | |
| Read Cycle | | | | |
| $t_{power}^{[6]}$ | V_{CC} (typical) to the first access | 100 | | μ S |
| t_{RC} | Read cycle time | 10 | | ns |
| t_{AA} | Address to data valid | | 10 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | | ns |
| t_{ACE} | \overline{CE} LOW to data valid | | 10 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | | 5 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z ^[7] | 0 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[7, 8] | | 5 | ns |
| t_{LZCE} | \overline{CE} LOW to Low-Z ^[7] | 3 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High-Z ^[7, 8] | | 5 | ns |
| $t_{PU}^{[9]}$ | \overline{CE} LOW to Power-up | 0 | | ns |
| $t_{PD}^{[9]}$ | \overline{CE} HIGH to Power-down | | 10 | ns |
| t_{DBE} | Byte enable to data valid | | 5 | ns |
| t_{LZBE} | Byte enable to low-Z | 0 | | ns |
| t_{HZBE} | Byte disable to high-Z | | 5 | ns |
| Write Cycle^[10] | | | | |
| t_{WC} | Write cycle time | 10 | | ns |
| t_{SCE} | \overline{CE} LOW to write end | 8 | | ns |
| t_{AW} | Address set-up to write end | 8 | | ns |
| t_{HA} | Address hold from write end | 0 | | ns |
| t_{SA} | Address set-up to write start | 0 | | ns |
| t_{PWE} | \overline{WE} pulse width | 7 | | ns |
| t_{SD} | Data set-up to write end | 5 | | ns |
| t_{HD} | Data hold from write end | 0 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[7] | 3 | | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[7, 8] | | 5 | ns |
| t_{BW} | Byte enable to end of write | 7 | | ns |

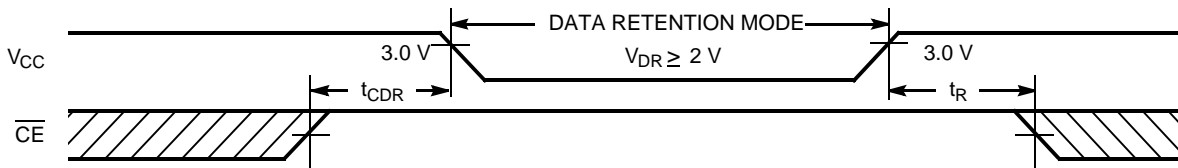
Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed
7. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Data Retention Characteristics (Over the Operating Range)

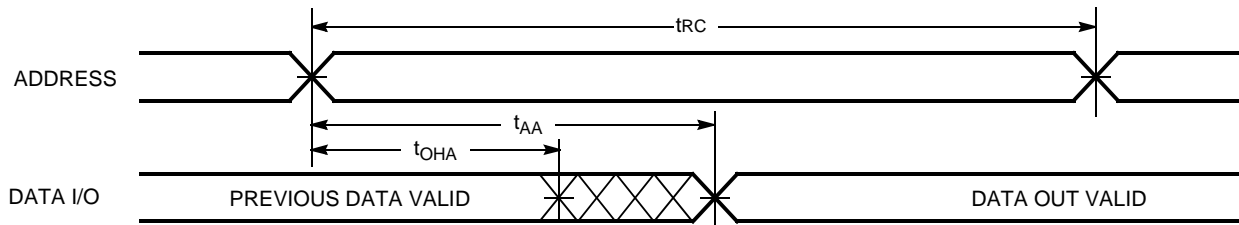
| Parameter | Description | Conditions | Min. | Max. | Unit |
|-----------------|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------|------|
| V_{DR} | V_{CC} | | 2.0 | | V |
| I_{CCDR} | Data retention current | $V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | | 3 | mA |
| $t_{CDR}^{[3]}$ | Chip deselect to data retention time | | 0 | | ns |
| $t_R^{[11]}$ | Operation recovery time | | t_{RC} | | ns |

Data Retention Waveform

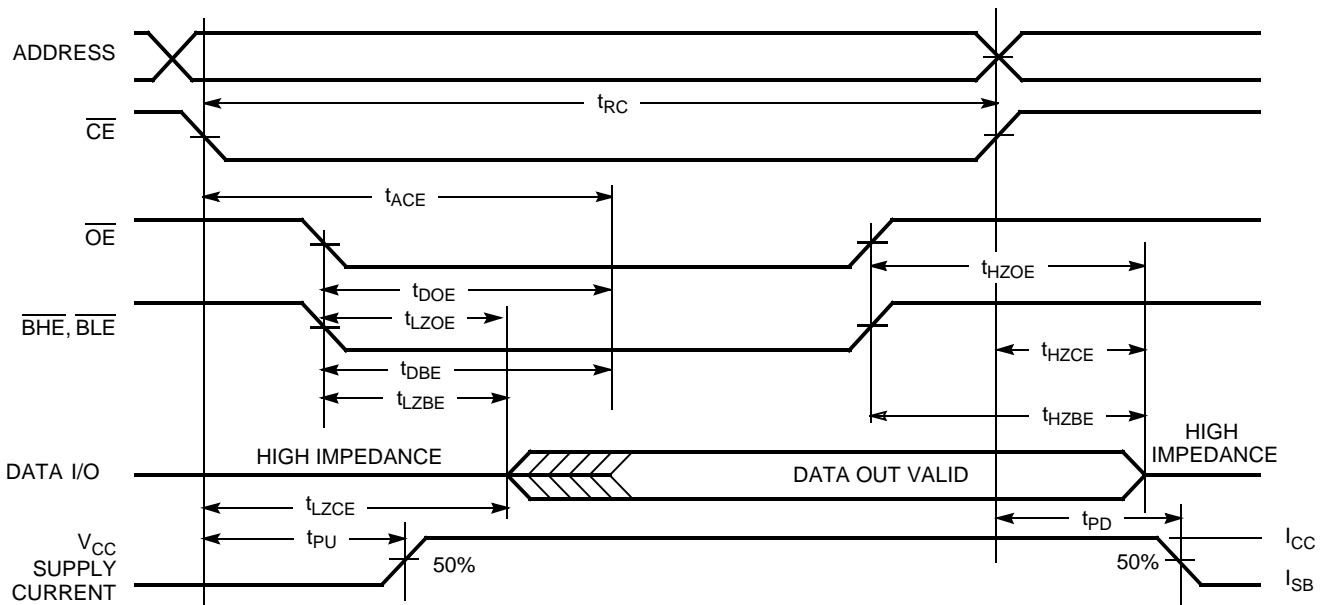


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled)^[12, 13]



Read Cycle No. 2 (OE Controlled)^[13, 14]

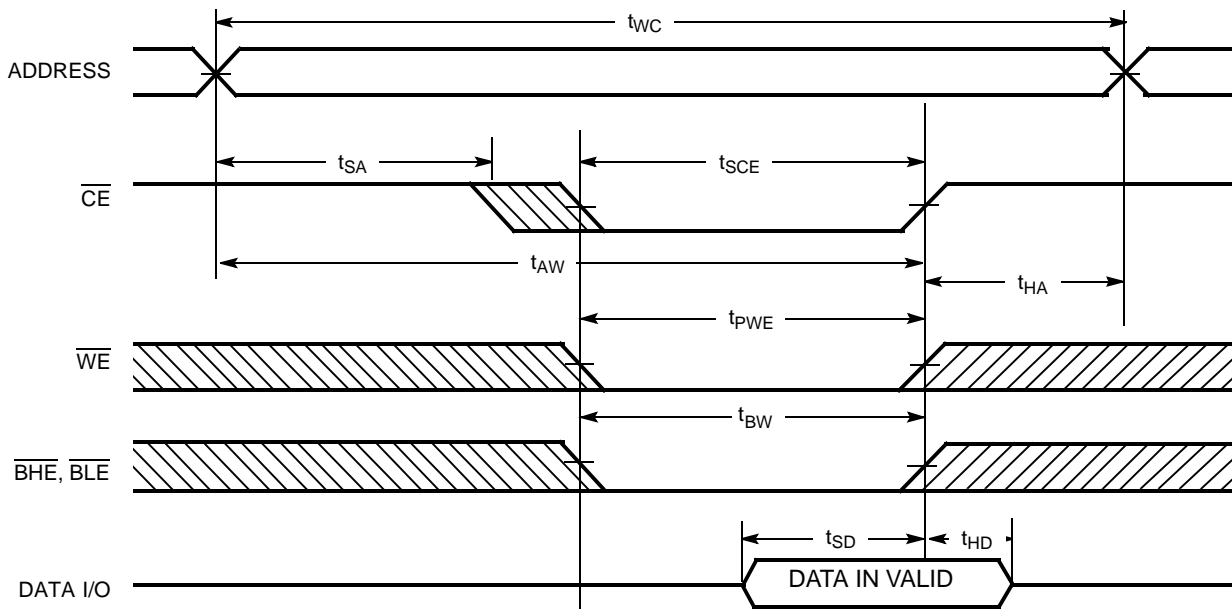


Notes:

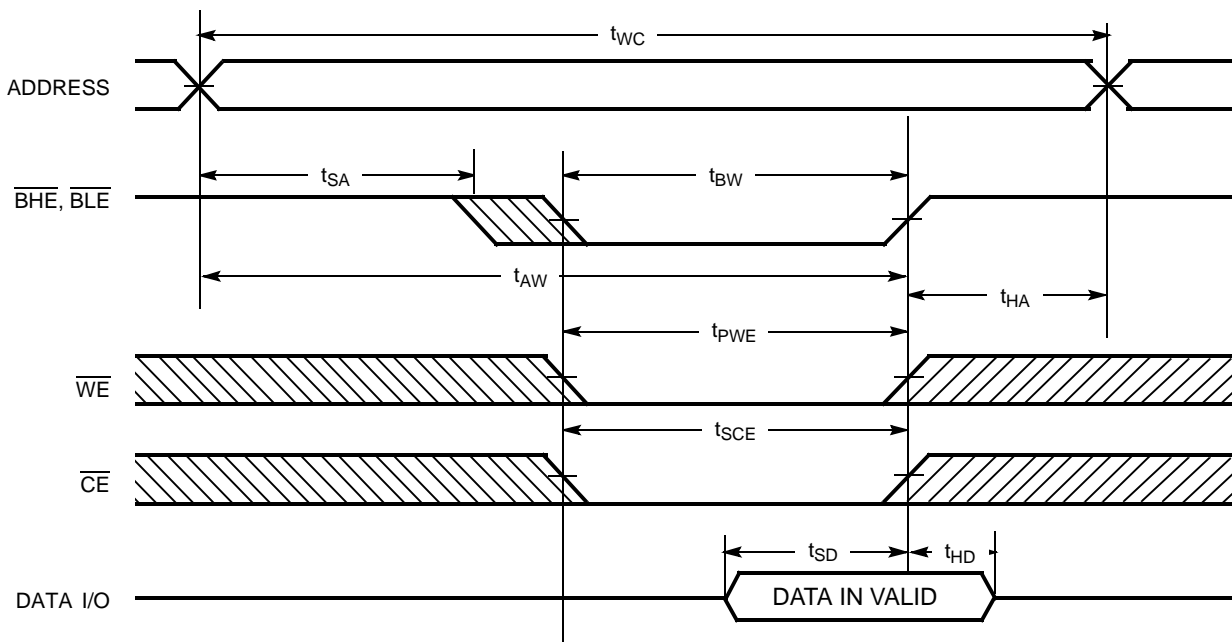
- 11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 50\ \mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 50\ \mu\text{s}$.
- 12. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or $\overline{BLE} = V_{IL}$.
- 13. \overline{WE} is HIGH for Read cycle.
- 14. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[15, 16]



Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



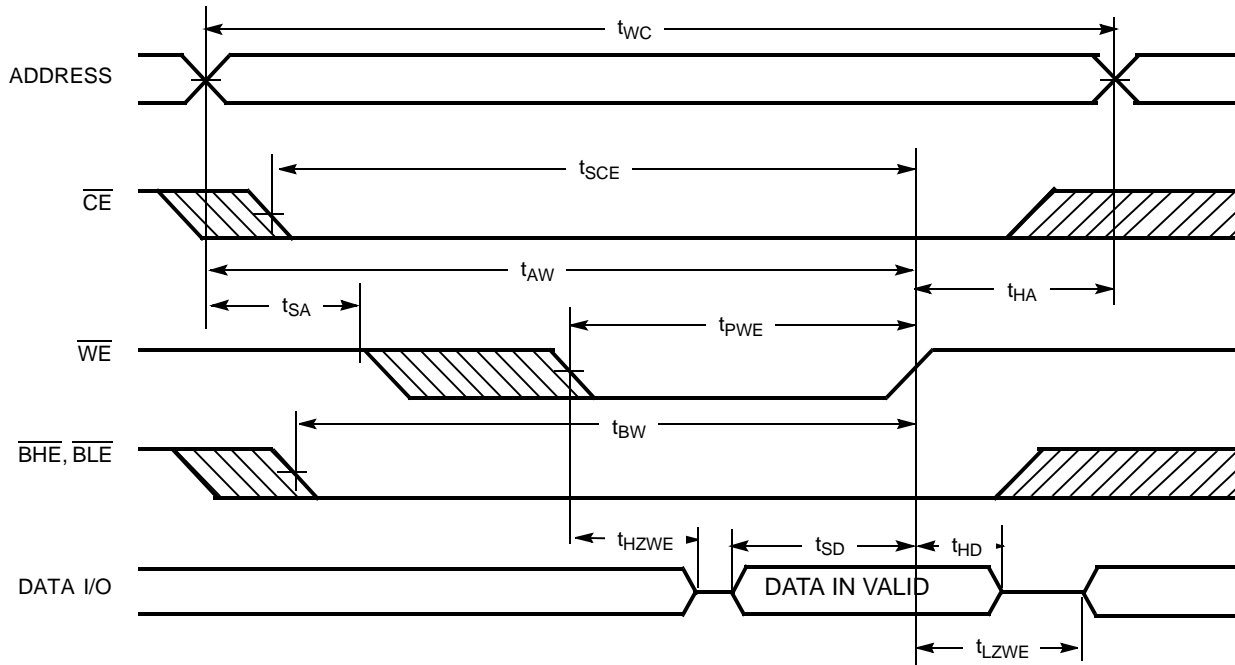
Notes:

15. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.

16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



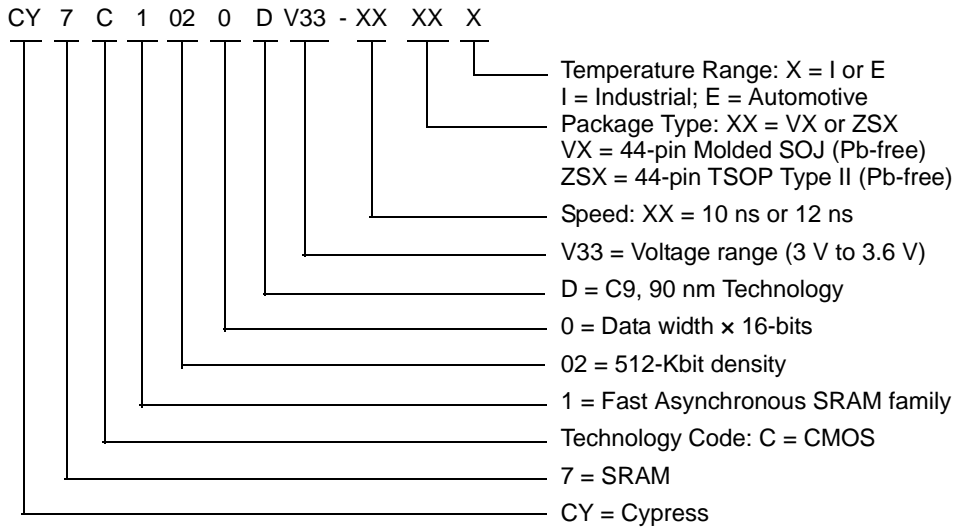
Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------|
| H | X | X | X | X | High-Z | High-Z | Power-down | Standby (I_{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read—All bits | Active (I_{CC}) |
| | | | L | H | Data Out | High-Z | Read—Lower bits only | Active (I_{CC}) |
| | | | H | L | High-Z | Data Out | Read—Upper bits only | Active (I_{CC}) |
| L | X | L | L | L | Data In | Data In | Write—All bits | Active (I_{CC}) |
| | | | L | H | Data In | High-Z | Write—Lower bits only | Active (I_{CC}) |
| | | | H | L | High-Z | Data In | Write—Upper bits only | Active (I_{CC}) |
| L | H | H | X | X | High-Z | High-Z | Selected, Outputs Disabled | Active (I_{CC}) |
| L | X | X | H | H | High-Z | High-Z | Selected, Outputs Disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------------|--------------|-------------------------------|-----------------|
| 10 | CY7C1020DV33-10ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | Industrial |

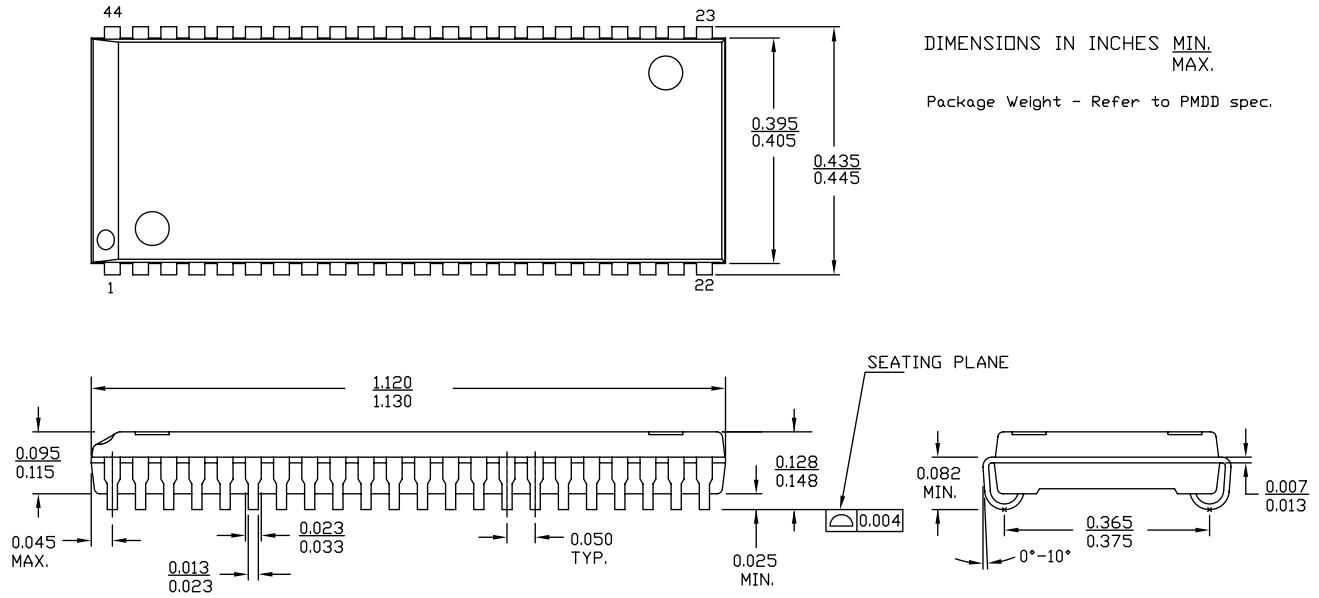
Ordering Code Definitions



Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

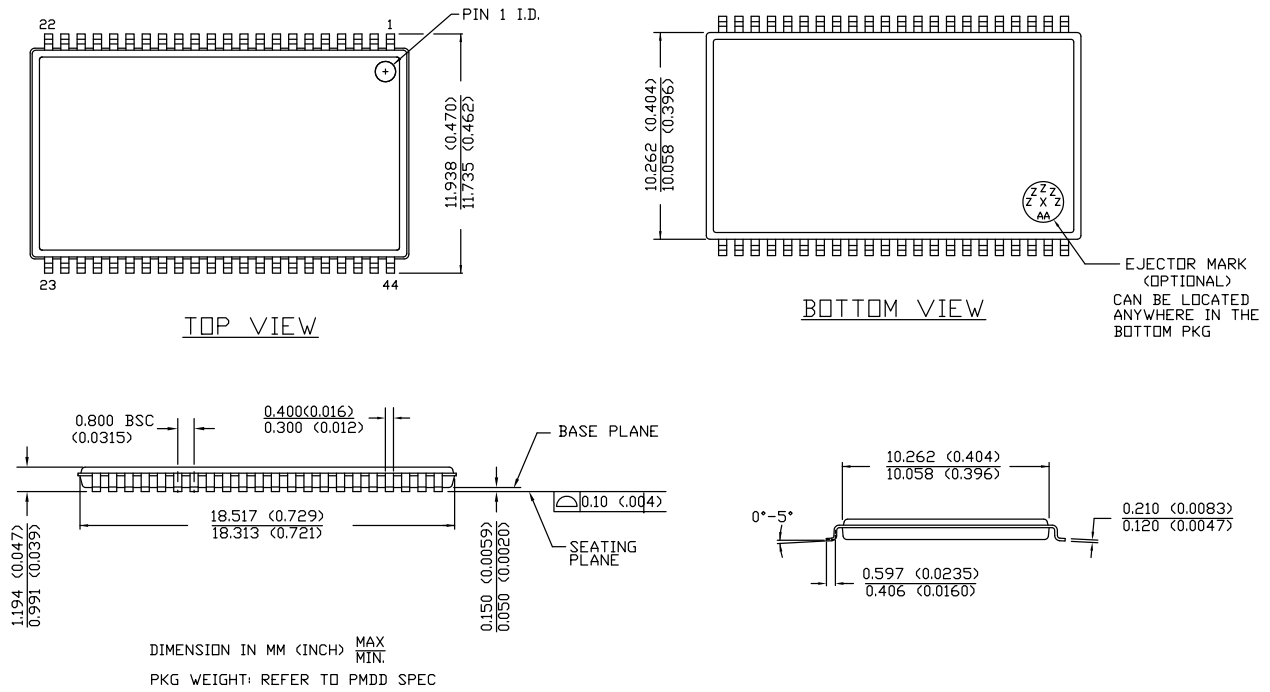
Figure 1. 44-pin (400-Mil) Molded SOJ (51-85082)



51-85082 *E

Package Diagrams (continued)

Figure 2. 44-Pin Thin Small Outline Package Type II (51-85087)



51-85087 *E

Acronyms

| Acronym | Description |
|-------------------------|-----------------------------------------|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degrees Celsius |
| μA | microamperes |
| mA | milliamperes |
| MHz | megahertz |
| ns | nanoseconds |
| pF | picofarads |
| V | volts |
| Ω | ohms |
| W | watts |

Document History Page

| Document Title: CY7C1020DV33, 512 K (32 K x 16) Static RAM | | | | |
|------------------------------------------------------------|---------|------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Document Number: 38-05461 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 201560 | See ECN | SWI | Advance Information data sheet for C9 IPP |
| *A | 233695 | See ECN | RKF | DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information |
| *B | 262950 | See ECN | RKF | Changed I/O ₁ – I/O ₁₆ to I/O ₀ – I/O ₁₅ Added Data Retention Characteristics table Added T _{power} spec in Switching Characteristics table Added 44-SOJ package diagram Shaded Ordering Information |
| *C | 307596 | See ECN | RKF | Reduced Speed bins to –8 and –10 ns |
| *D | 560995 | See ECN | VKN | Converted from Preliminary to Final Removed Commercial operating range Removed 8 ns speed bin Added Automotive information Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information table Changed Overshoot spec from V _{CC} +2 V to V _{CC} +1 V in footnote #4 |
| *E | 2898399 | 03/24/2010 | AJU | Updated Package Diagrams |
| *F | 3109992 | 12/14/2010 | AJU | Added Ordering Code Definitions . |
| *G | 3424450 | 10/28/2011 | TAVA | Updated footnotes Updated Selection Guide , Operating Range , Electrical Characteristics Over the Operating Range , Switching Characteristics Over the Operating Range ^[5] , Data Retention Characteristics (Over the Operating Range) , Switching Waveforms , and Ordering Information . Updated Package Diagrams Added Acronyms , and Document Conventions |
| *H | 3861347 | 01/08/2013 | TAVA | Updated Ordering Information (Updated part numbers). Updated Package Diagrams : spec 51-85082 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *D to *E. |

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.