LVPECL Frequency-Programmable Crystal Oscillator

IDT8N3S270

DATA SHEET

General Description

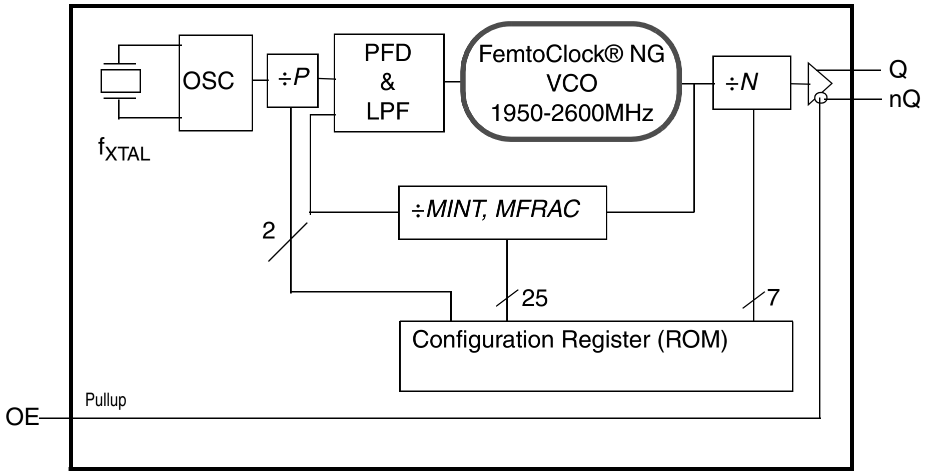
The ICS8N3S270 is a Frequency-Programmable Crystal Oscillator with very flexible frequency programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 6-lead ceramic 5mm x 7mm x 1.55mm package.

The device can be factory programmed to any frequency in the range from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz and supports a very high degree of frequency precision of 218Hz or better. The extended temperature range supports wireless infrastructure, telecommun- ication and networking end equipment requirements.

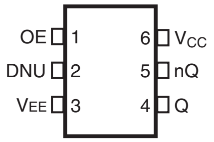
Features

- Fourth generation FemtoClock® NG technology
- Factory-programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Frequency programming resolution is 218Hz and better
- One 2.5V or 3.3V LVPECL clock output
- Output enable control (positive polarity), LVCMOS/LVTTL compatible
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.24ps (typical), integer PLL feedback configuration
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): 0.27ps (typical), integer PLL feedback configuration
- 2.5V or 3.3V supply
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) 6-pin ceramic package

Block Diagram



Pin Assignment



IDT8N3S270
6-lead ceramic 5mm x 7mm x 1.55mm package body
CD Package
Top View

Pin Description and Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE	Input	Pullup	Output enable pin. See Table 3A for function. LVCMOS/LVTTL interface levels.
2	DNU			Do not use (factory use only).
3	V_{EE}	Power		Negative power supply.
4, 5	Q, nQ	Output		Differential clock output. LVPECL interface levels.
6	V_{CC}	Power		Positive power supply.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OE			5.5		pF
R_{PULLUP}	Input Pullup Resistor				50		kΩ

Function Tables

Table 3A. OE Configuration

Input	
OE	Output Enable
0	Outputs Q, nQ are in high-impedance state.
1 (default)	Outputs are enabled.

NOTE: OE is an asynchronous control.

Table 3B. Output Frequency Range

15.476MHz to 866.67MHz
975MHz to 1,300MHz

NOTE: Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.

Principles of Operation

The block diagram consists of the internal 3RD overtone crystal and oscillator which provide the reference clock f_{XTAL} of either 114.285MHz or 100MHz. The PLL includes the FemtoClock NG VCO along with the Pre-divider (*P*), the feedback divider (*M*) and the post divider (*N*). The *P*, *M*, and *N* dividers determine the output frequency based on the f_{XTAL} reference. The feedback divider is fractional supporting a huge number of output frequencies. The configuration of the feedback divider to integer-only values results in an improved output phase noise characteristics at the expense of the range of output frequencies. Internal registers are used to hold one factory pre-set *P*, *M*, and *N* configuration setting. The *P*, *M*, and *N* frequency configuration supports an output frequency range from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator.

The output frequency is determined by the 2-bit pre-divider (*P*), the feedback divider (M) and the 7-bit post divider (*N*). The feedback divider (*M*) consists of both a 7-bit integer portion (*MINT*) and an 18-bit fractional portion (*MFRAC*) and provides the means for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[MINT + \frac{MFRAC + 0.5}{2^{18}} \right]$$

Frequency Configuration

An order code is assigned to each frequency configuration programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information on programming cababilities of the device for custom frequency and pull-range configurations, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	49.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			123	148	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			119	143	mA

Table 4C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.8$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.6$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4D. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.8$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVCMOS/LVTTL DC Characteristic, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = V_{IN} = 3.465V	-0.3		0.8	V
			V_{CC} = V_{IN} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

AC Electrical Characteristics

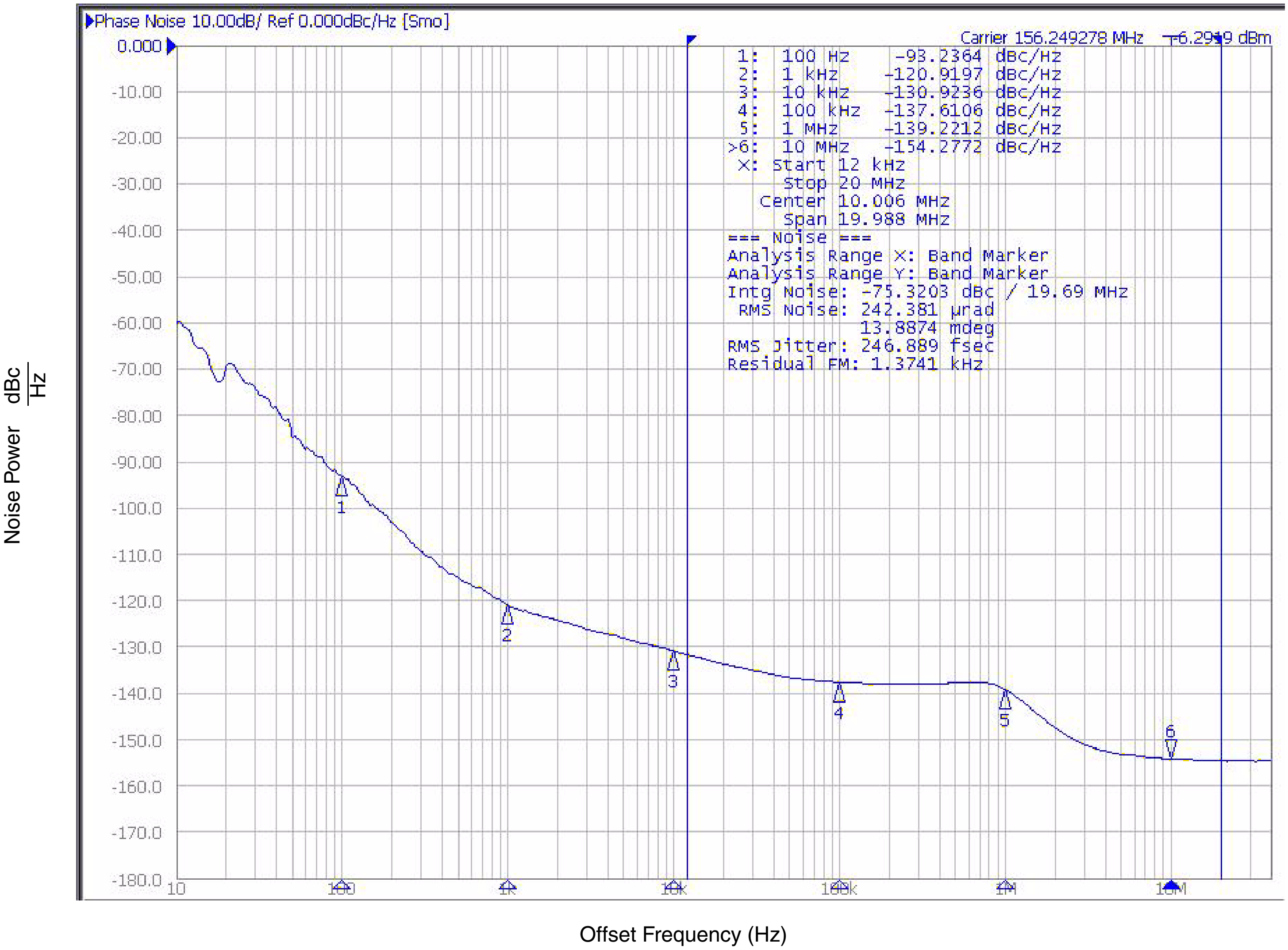
Table 5. AC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ		15.476		866.67	MHz
			975		1,300	MHz
f_I	Initial Accuracy	Measured @ 25°C			±10	ppm
f_S	Temperature Stability	Option code = A or B			±100	ppm
		Option code = E or F			±50	ppm
		Option code = K or L			±20	ppm
f_A	Aging	Frequency drift over 10 year life			±3	ppm
		Frequency drift over 15 year life			±5	ppm
f_T	Total Stability	Option code A, B (10 year life)			±113	ppm
		Option code E, F (10 year life)			±63	ppm
		Option code K, L (10 year life)			±33	ppm
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 1				30	ps
tjit(per)	RMS Period Jitter; NOTE 1			1.9	2.8	ps
tjit(Ø)	RMS Phase Jitter (Random); Fractional PLL feedback and f_{XTAL} = 100MHz (2xxx order codes)	17MHz ≤ f_{OUT} ≤ 1300MHz, NOTE 2, 3, 4		0.497	0.882	ps
	RMS Phase Jitter (Random); Integer PLL feedback and f_{XTAL} = 100MHz (1xxx order codes)	500MHz ≤ f_{OUT} ≤ 1300MHz, NOTE 2, 3, 4		0.232	0.322	ps
		125MHz ≤ f_{OUT} < 500MHz, NOTE 2, 3, 4		0.250	0.384	ps
		17MHz ≤ f_{OUT} < 125MHz, NOTE 2, 3, 4		0.275	0.405	ps
		f_{OUT} = 156.25MHz, NOTE 2, 3, 4		0.242	0.311	ps
		f_{OUT} = 156.25MHz, NOTE 2, 3, 5		0.275	0.359	ps
	RMS Phase Jitter (Random) Fractional PLL feedback and f_{XTAL} = 114.285MHz (0xxx order codes)	17MHz ≤ f_{OUT} ≤ 1300MHz, NOTE 2, 3, 4		0.474	0.986	ps
Φ_N(100)	Single-side band phase noise, 100Hz from Carrier	156.25MHz		-92		dBc/Hz
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	156.25MHz		-120		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier	156.25MHz		-131		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier	156.25MHz		-138		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier	156.25MHz		-139		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier	156.25MHz		-154		dBc/Hz
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		450	ps
odc	Output Duty Cycle		47		53	%
$t_{STARTUP}$	Device startup time after power up				20	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Refer to the phase noise plot.
NOTE 3: Please see the FemtoClockNG Ceramic 5x7 Modules Programming guide for more information on PLL feedback modes and the optimum configuration for phase noise. Integer PLL feedback is the default operation for the dddd = 1xxx order codes.
NOTE 4: Integration range: 12kHz - 20MHz.
NOTE 5: Integration range: 1kHz - 40MHz.

Typical Phase Noise at 156.25MHz (12kHz - 20MHz)



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Phase Noise 10.00dB/ Ref 0.000dBc/Hz [Smo]
                                Carrier 156.249278 MHz   -6.2919 dBm
 1:  100 Hz     -93.2364 dBc/Hz
 2:  1 kHz     -120.9197 dBc/Hz
 3:  10 kHz    -130.9236 dBc/Hz
 4:  100 kHz   -137.6106 dBc/Hz
 5:  1 MHz     -139.2212 dBc/Hz
>6:  10 MHz    -154.2772 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -75.3203 dBc / 19.69 MHz
 RMS Noise: 242.381 µrad
            13.8874 mdeg
RMS Jitter: 246.889 fsec
Residual FM: 1.3741 kHz
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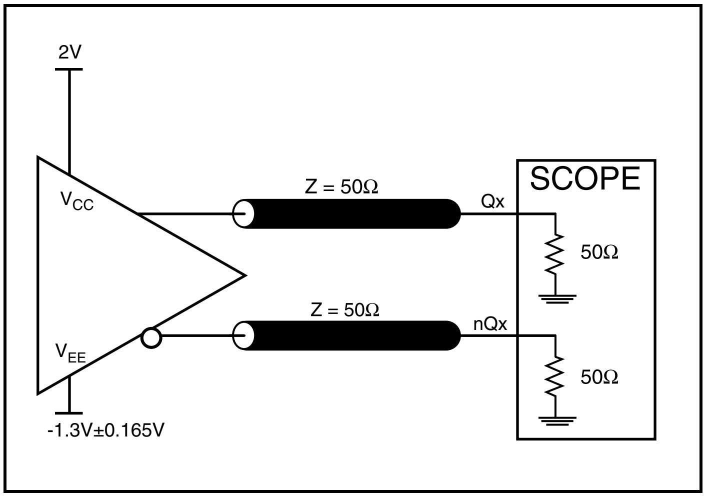
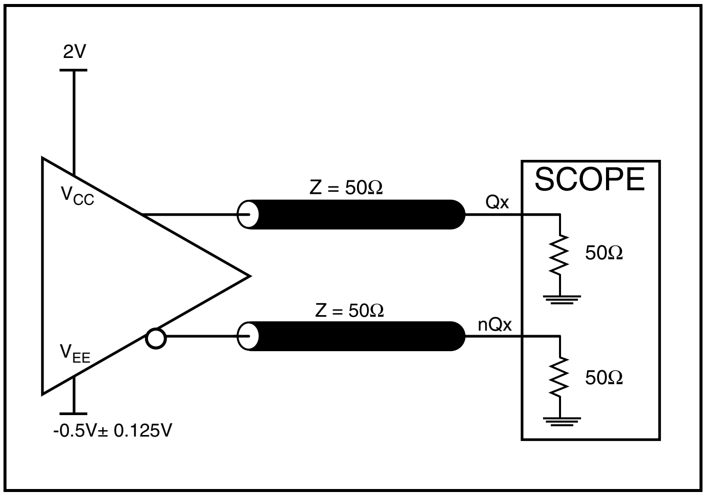
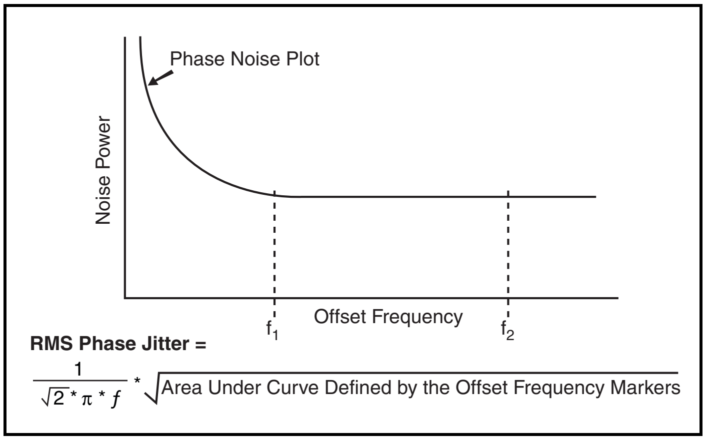
Parameter Measurement Information



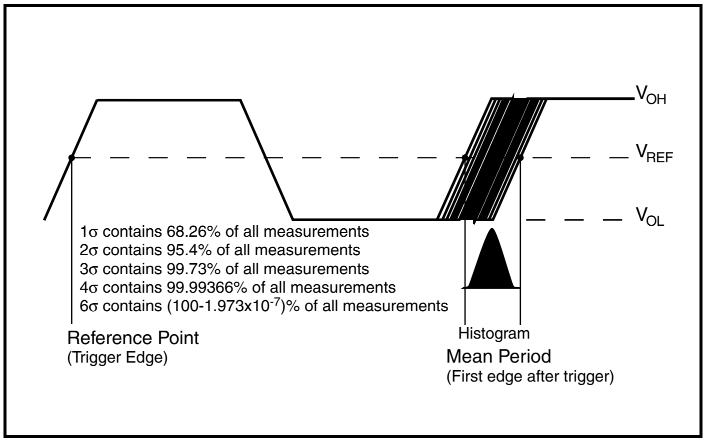
3.3V LVPECL Output Load AC Test Circuit



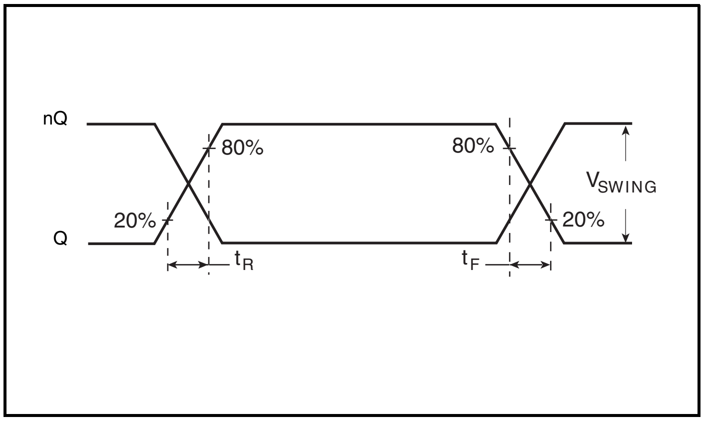
2.5V LVPECL Output Load AC Test Circuit



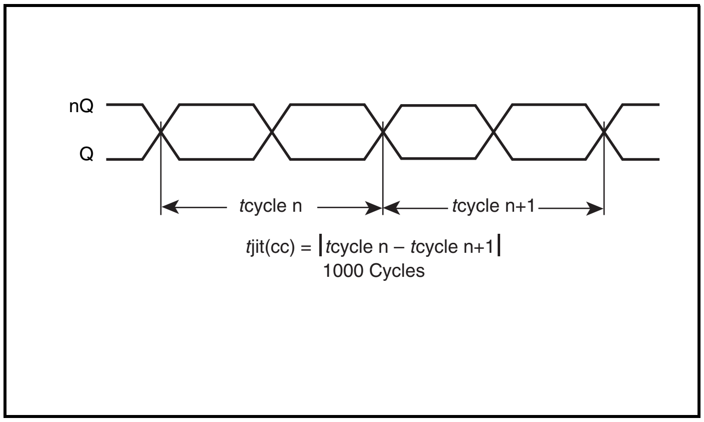
RMS Phase Jitter



Period Jitter

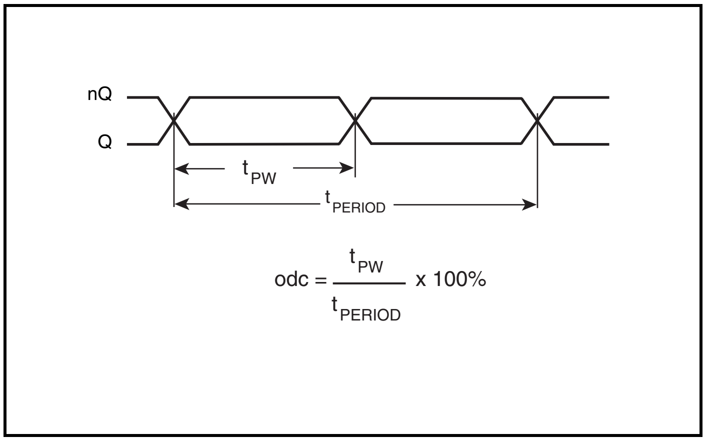


Output Rise/Fall Time



Cycle-to-Cycle Jitter

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Applications Information

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

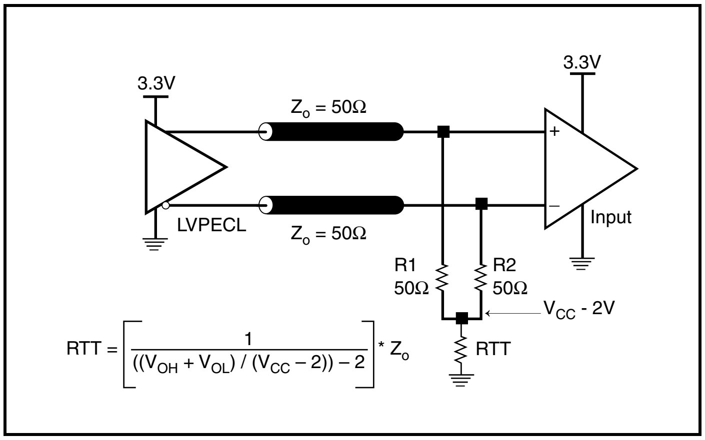


Figure 1A. 3.3V LVPECL Output Termination

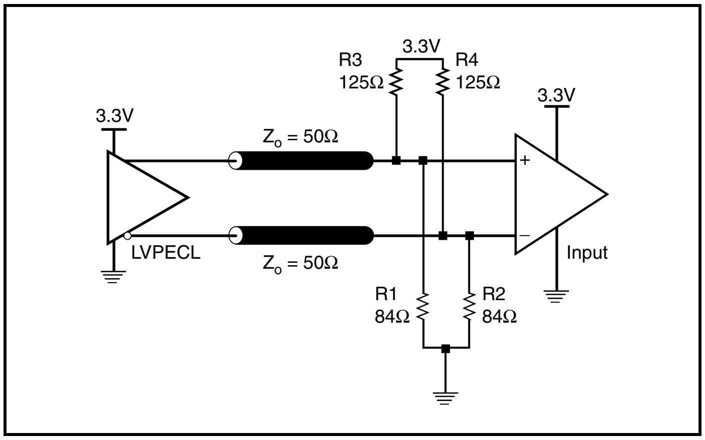


Figure 1B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 2A and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C.*

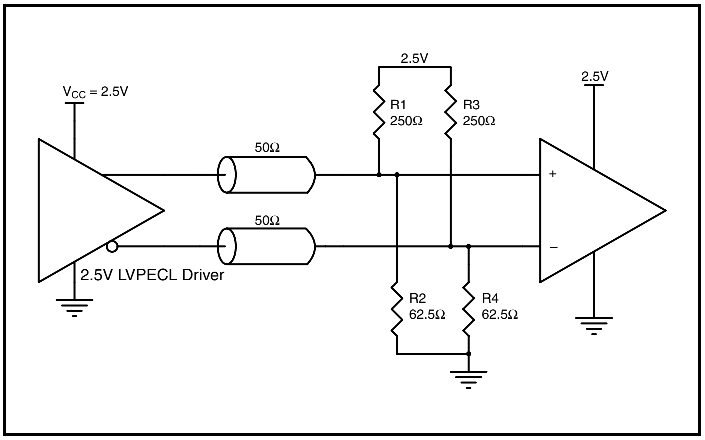


Figure 2A. 2.5V LVPECL Driver Termination Example

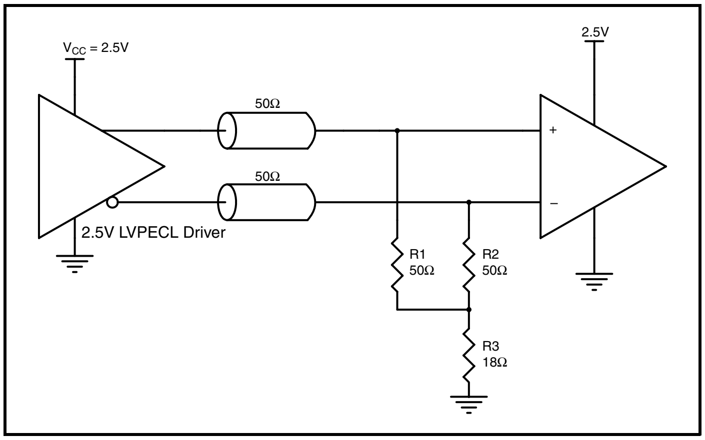


Figure 2B. 2.5V LVPECL Driver Termination Example

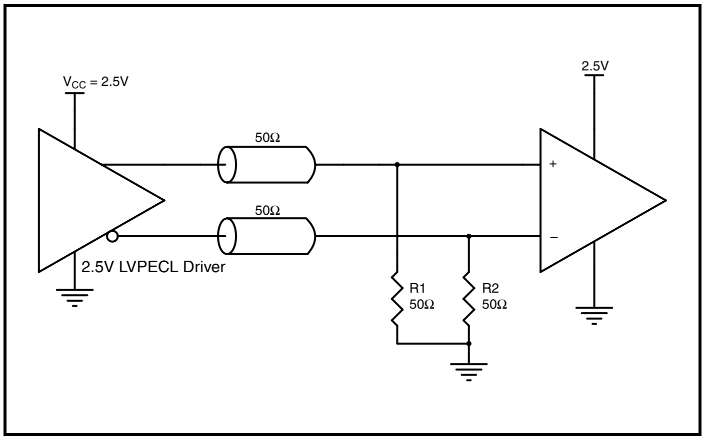


Figure 2C. 2.5V LVPECL Driver Termination Example

Schematic Layout

Figure 3 shows an example of IDT8N3270 application schematic. In this example, the device is operated at V_{CC} = 3.3V. As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

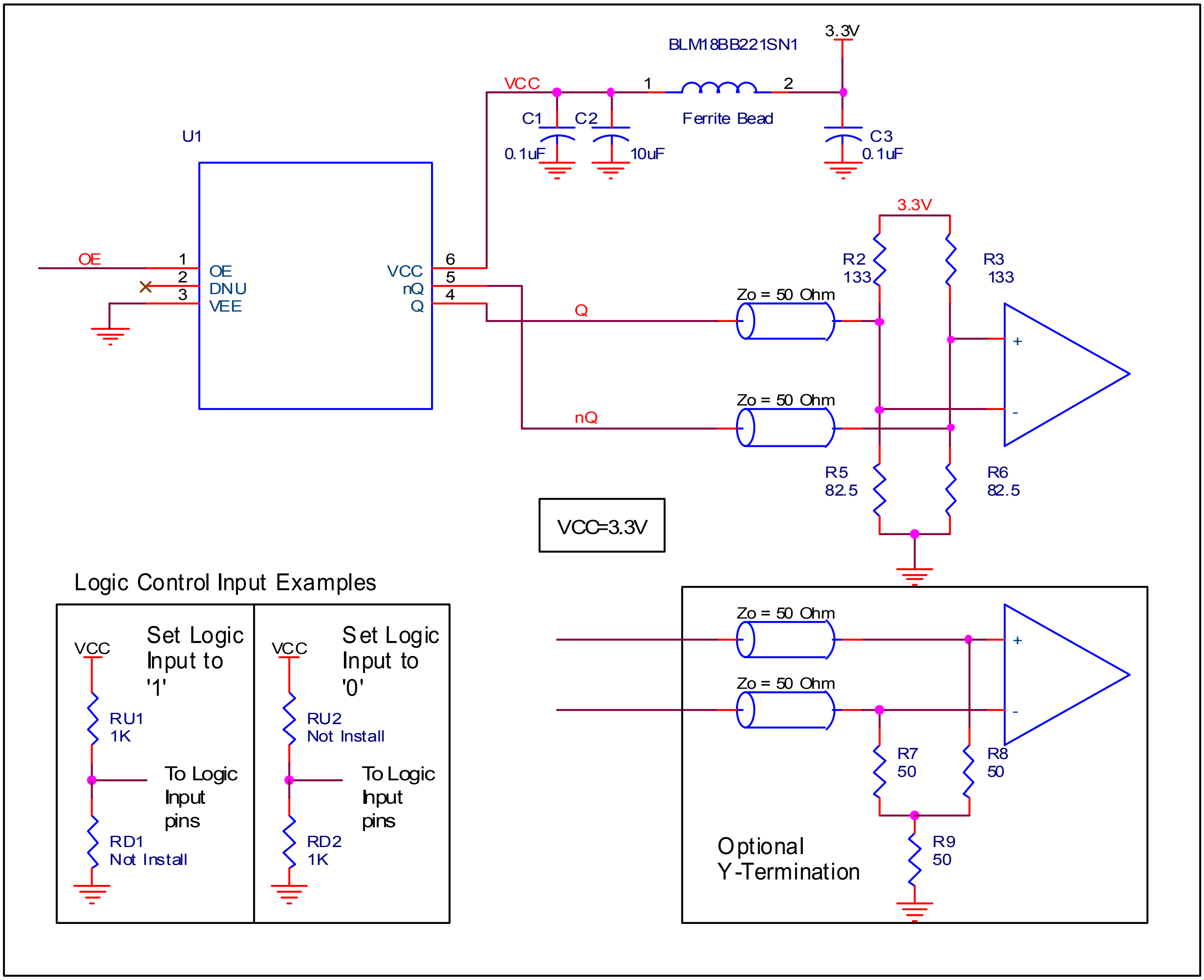


Figure 3. IDT8N3S270 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N3S270.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8N3S270 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 148mA = **512.82mW**
- Power $(outputs)_{MAX}$ = **32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 512.82mW + 32mW = **544.82mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.545W * 49.4°C/W = 111.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 6 Lead Ceramic 5mm x 7mm Package, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4.*

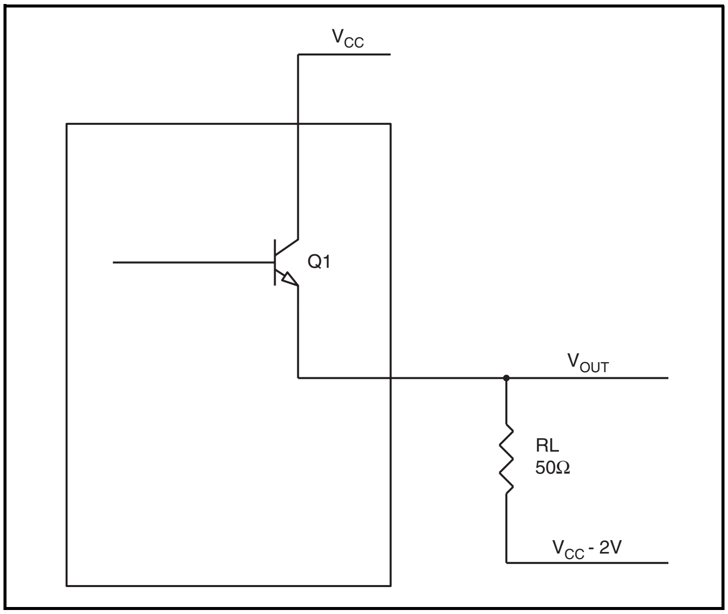


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.6V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50\Omega] * 1.6V = \mathbf{12.8mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **32mW**

Reliability Information

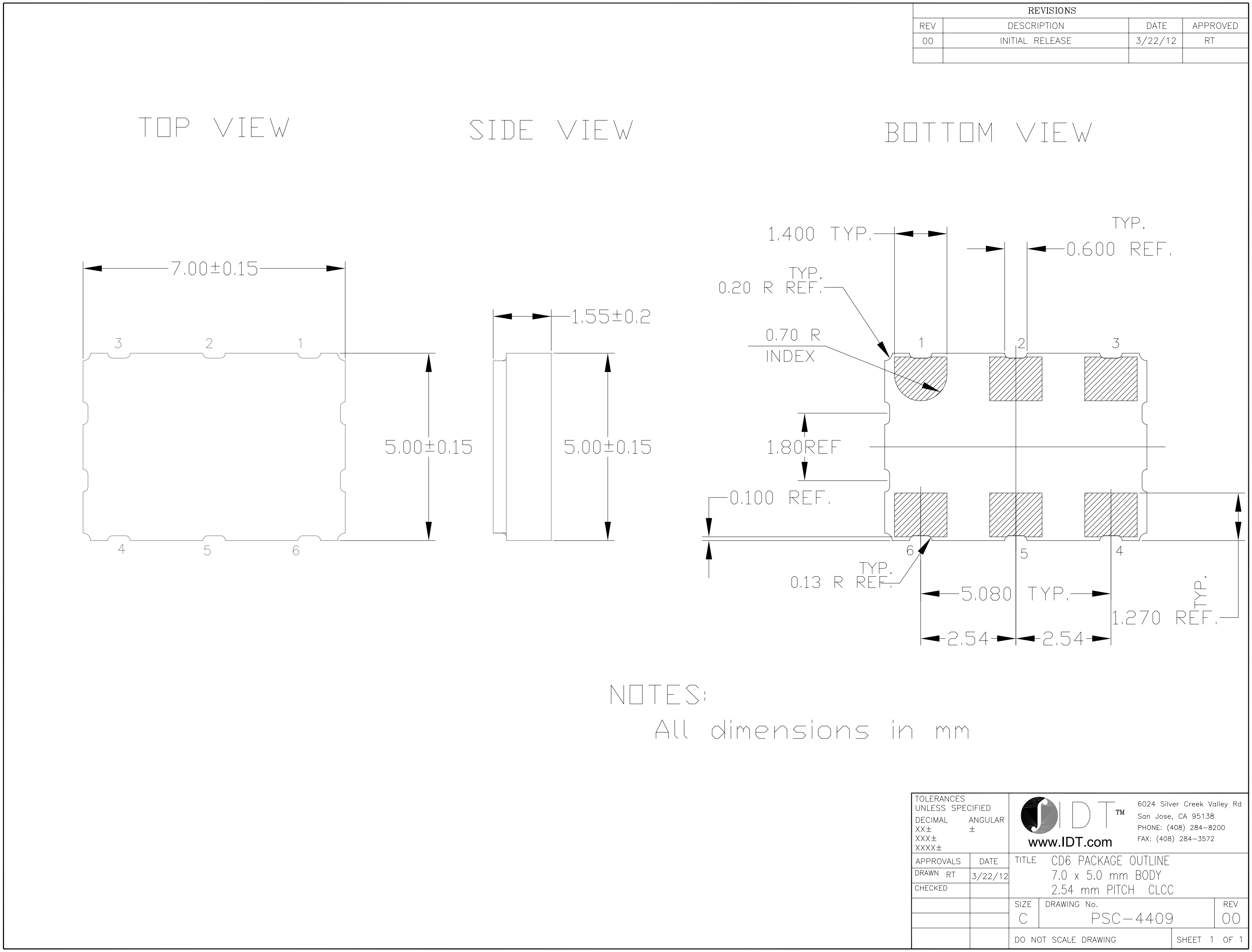
Table 7. θ_{JA} vs. Air Flow Table for a 6-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	42.1°C/W

Transistor Count

The transistor count for IDT8N3S270 is: 47,511

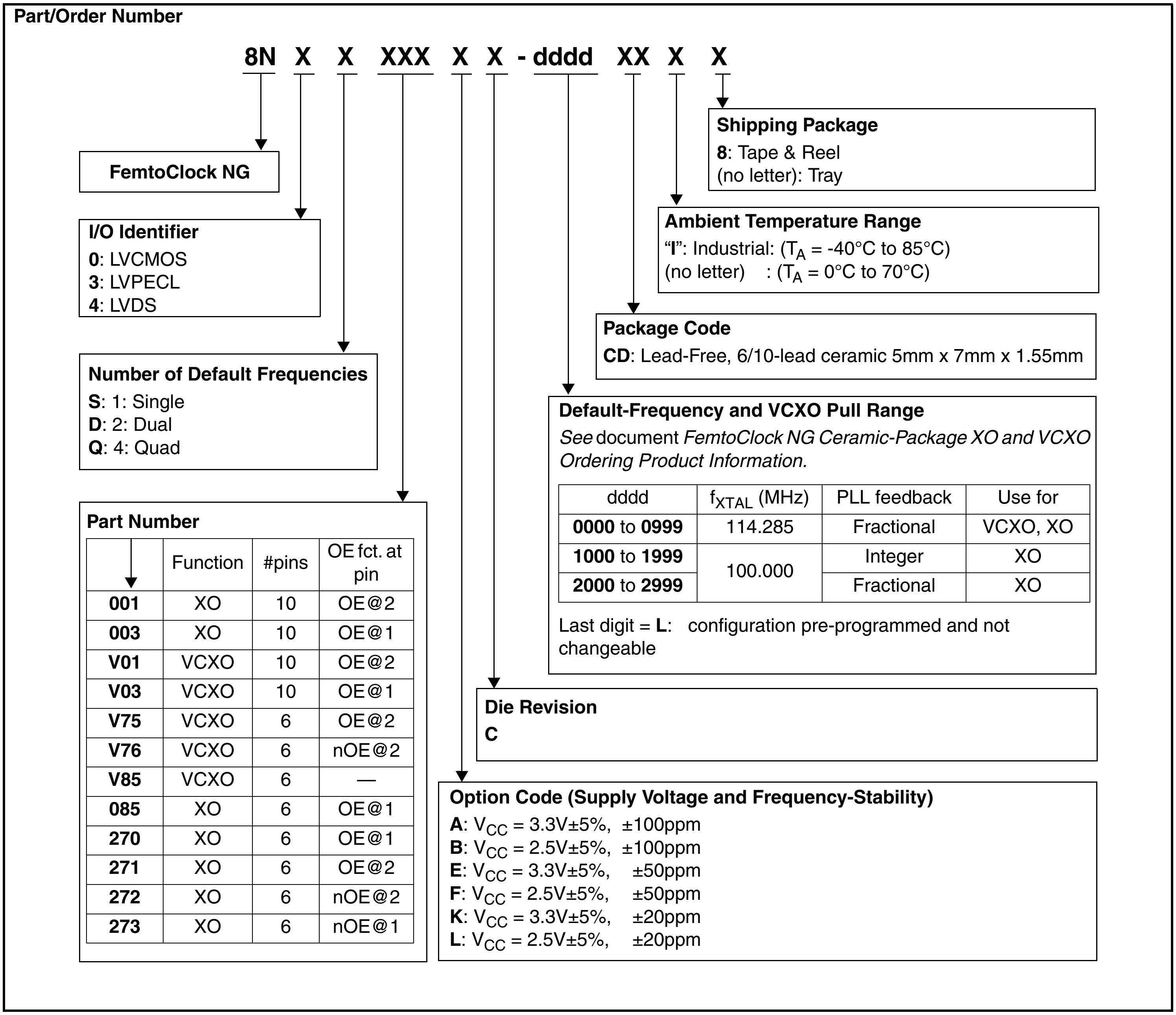
Package Outline and Package Dimensions



Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. The table below specifies the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N3QV01FG-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ±50ppm crystal frequency accuracy, contains a 114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 6-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of minimum ±100ppm.

Other default frequencies and order codes are available from IDT on request. For more information on available default frequencies, see the *FemtoClock N Ceramic-Package XO and VCXO Ordering Product Information* document.



Part/Order Number

8N X X XXX X X - dddd XX X X

FemtoClock NG

I/O Identifier

0: LVCMOS
3: LVPECL
4: LVDS

Number of Default Frequencies

S: 1: Single
D: 2: Dual
Q: 4: Quad

Part Number

↓	Function	#pins	OE fct. at pin
001	XO	10	OE@2
003	XO	10	OE@1
V01	VCXO	10	OE@2
V03	VCXO	10	OE@1
V75	VCXO	6	OE@2
V76	VCXO	6	nOE@2
V85	VCXO	6	—
085	XO	6	OE@1
270	XO	6	OE@1
271	XO	6	OE@2
272	XO	6	nOE@2
273	XO	6	nOE@1

Option Code (Supply Voltage and Frequency-Stability)

A: V_{CC} = 3.3V±5%, ±100ppm
B: V_{CC} = 2.5V±5%, ±100ppm
E: V_{CC} = 3.3V±5%, ±50ppm
F: V_{CC} = 2.5V±5%, ±50ppm
K: V_{CC} = 3.3V±5%, ±20ppm
L: V_{CC} = 2.5V±5%, ±20ppm

Die Revision

C

Default-Frequency and VCXO Pull Range

See document *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information.*

dddd	f_{XTAL} (MHz)	PLL feedback	Use for
0000 to **0999**	114.285	Fractional	VCXO, XO
1000 to **1999**	100.000	Integer	XO
2000 to **2999**		Fractional	XO

Last digit = **L**: configuration pre-programmed and not changeable

Package Code

CD: Lead-Free, 6/10-lead ceramic 5mm x 7mm x 1.55mm

Ambient Temperature Range

"**I**": Industrial: (T_A = -40°C to 85°C)
(no letter) : (T_A = 0°C to 70°C)

Shipping Package

8: Tape & Reel
(no letter): Tray

Table 8. Device Marking

Marking	Industrial Temperature Range (T_A = -40°C to 85°C)	Commercial Temperature Range (T_A = 0°C to 70°C)
	IDT8N3S270**y**C-**dddd**CDI	IDT8N3S270**y**C-**dddd**CD
	y = Option Code, **dddd**=Default-Frequency and VCXO Pull Range	

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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