



# PMPB50ENE

30 V, N-channel Trench MOSFET

26 April 2018

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Extended temperature range  $T_j = 175\text{ }^{\circ}\text{C}$
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Tin-plated 100 % solderable side pads for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Trench MOSFET technology

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

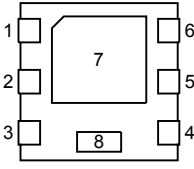
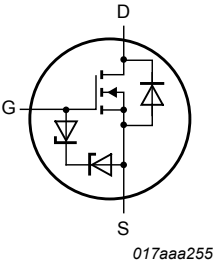
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	30	V
$V_{GS}$	gate-source voltage			-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-	6.9	A
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5.1\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$		-	30	43	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view <b>DFN2020MD-6 (SOT1220)</b></p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB50ENE	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB50ENE	3U

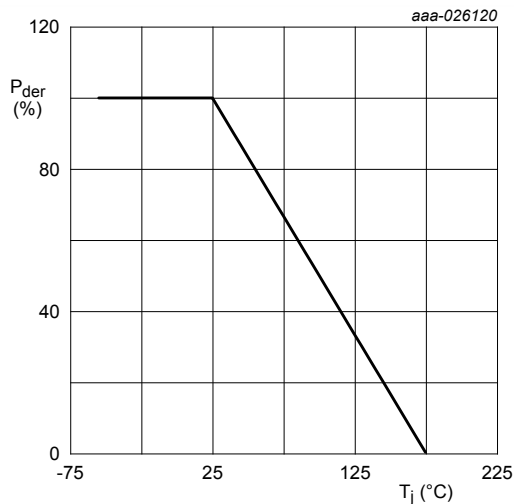
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

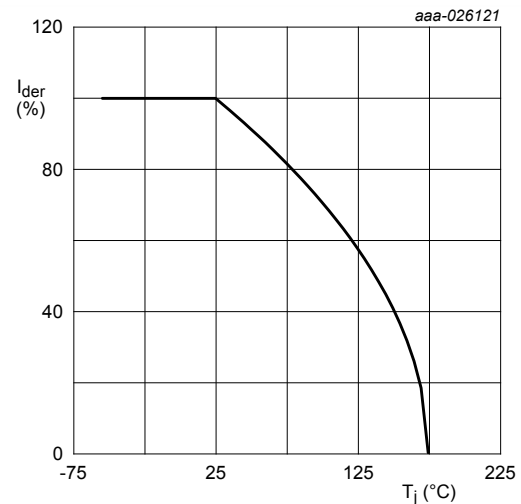
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	30	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	6.9	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	5.1	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	3.2	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	20	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[1]	-	1.9	mW
		T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	3.8	W
		T <sub>sp</sub> = 25 °C		-	11	W
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>amb</sub>	ambient temperature			-55	175	°C
T <sub>stg</sub>	storage temperature			-65	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	2	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

**Fig. 1. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

**Fig. 2. Normalized continuous drain current as a function of junction temperature**

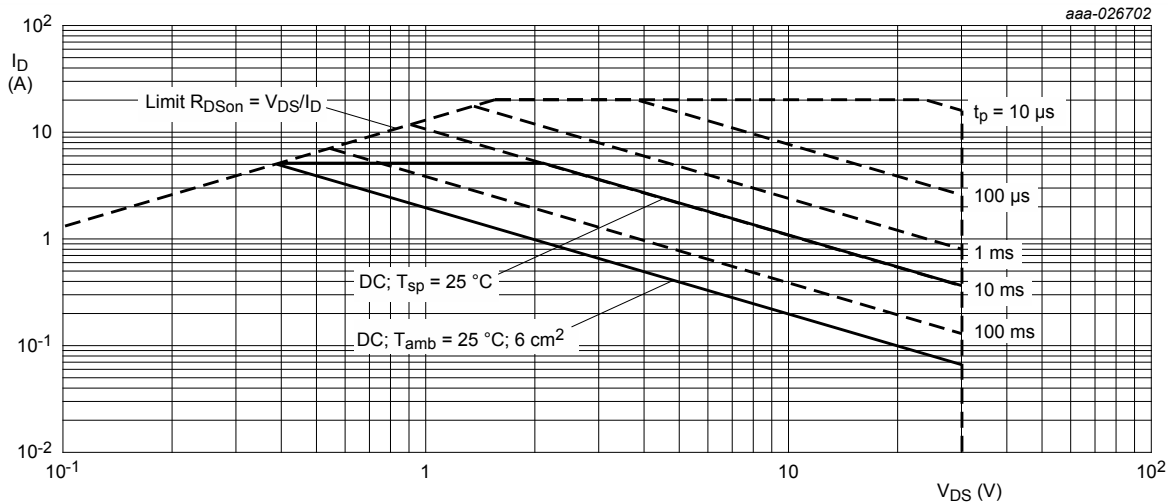


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	238	274	K/W
			[2]	-	67	77	K/W
		in free air; $t \leq 5$ s	[2]	-	35	40	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	11	14	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

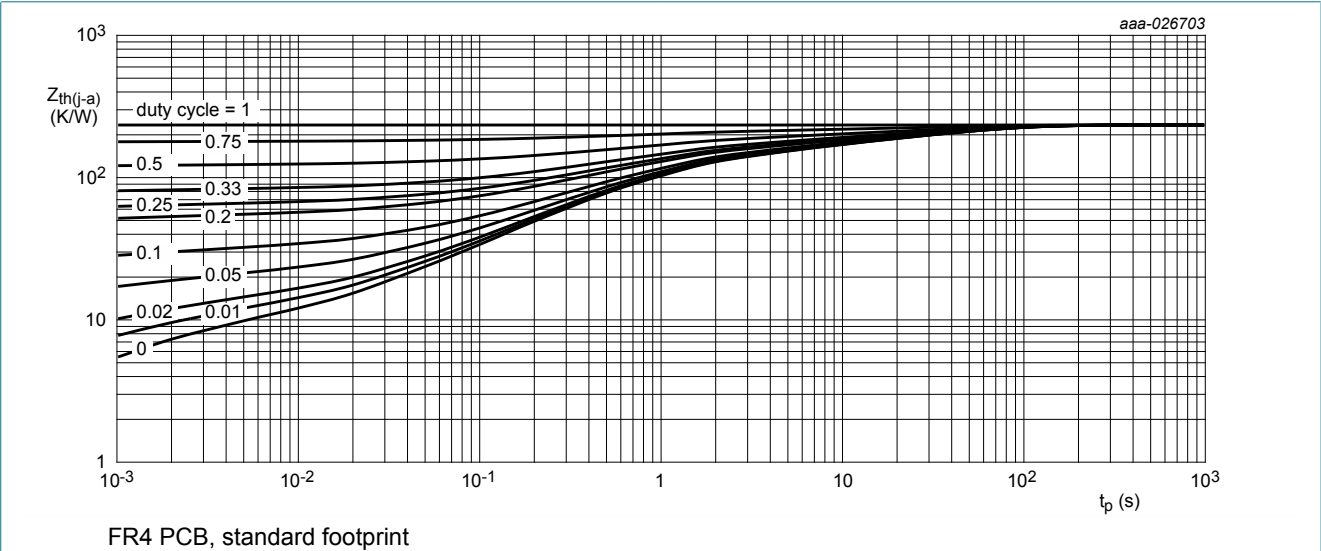


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

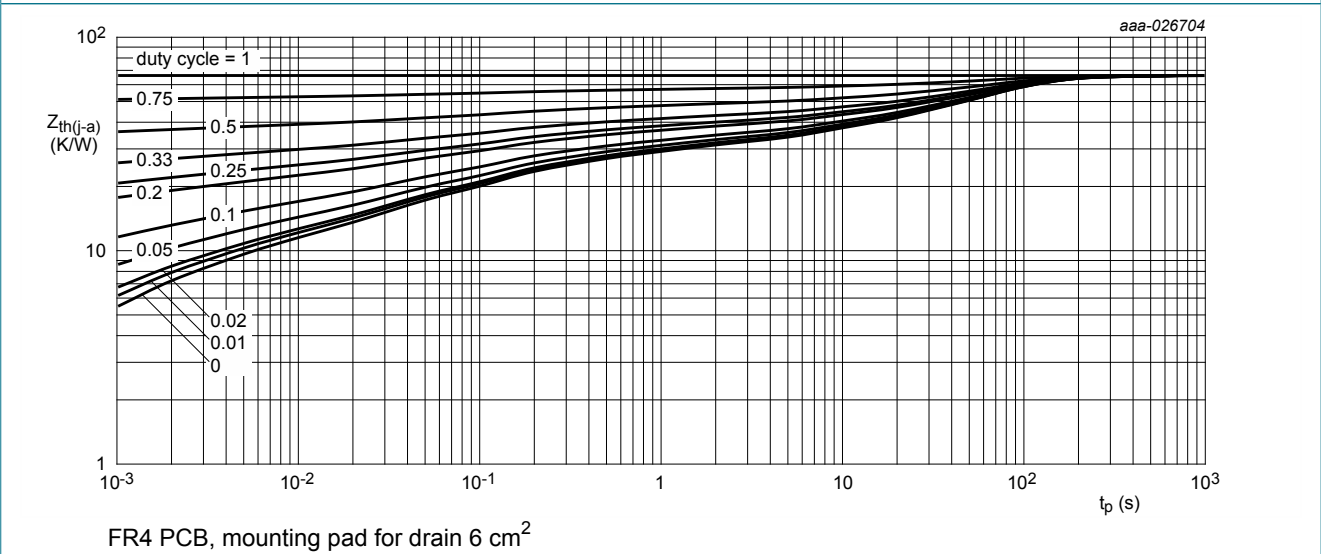


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		30	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		1	1.5	2.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	200	nA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-200	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5.1 A; T <sub>j</sub> = 25 °C		-	30	43	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5.1 A; T <sub>j</sub> = 175 °C		-	54	78	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 4.2 A; T <sub>j</sub> = 25 °C		-	39	60	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 5.1 A; T <sub>j</sub> = 25 °C		-	13	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	6.6	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 5.1 A; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C		-	6	10	nC
Q <sub>GS</sub>	gate-source charge			-	0.7	-	nC
Q <sub>GD</sub>	gate-drain charge			-	1.3	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 15 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	271	-	pF
C <sub>oss</sub>	output capacitance			-	58	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	43	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 5.1 A; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	4	-	ns
t <sub>r</sub>	rise time			-	24	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	17	-	ns
t <sub>f</sub>	fall time			-	6	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 2 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.8	1.2	V

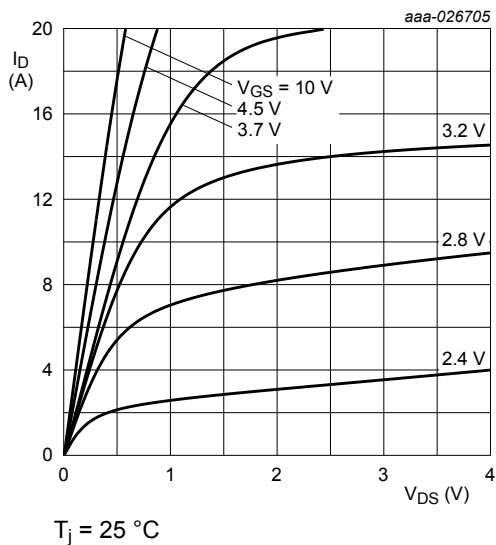


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

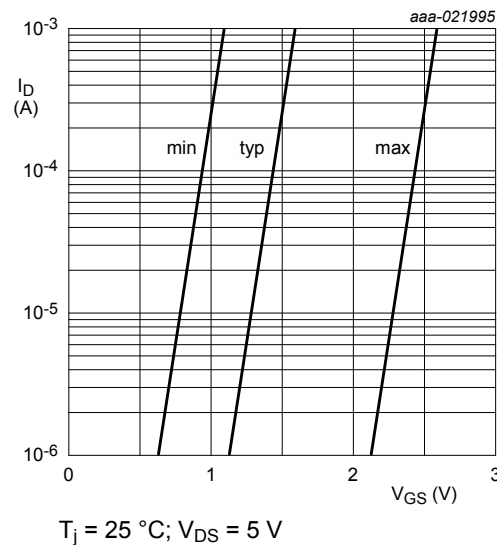


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

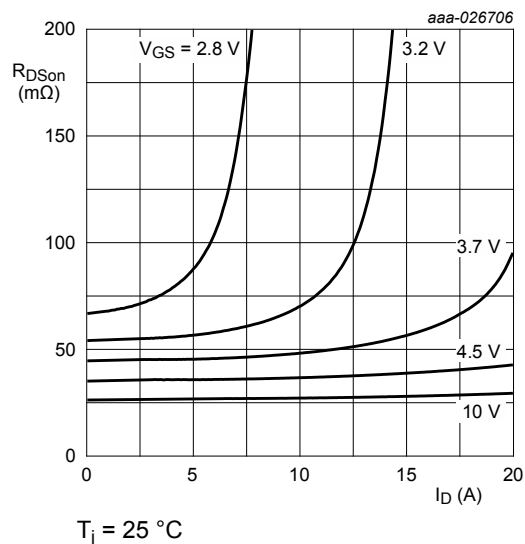


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

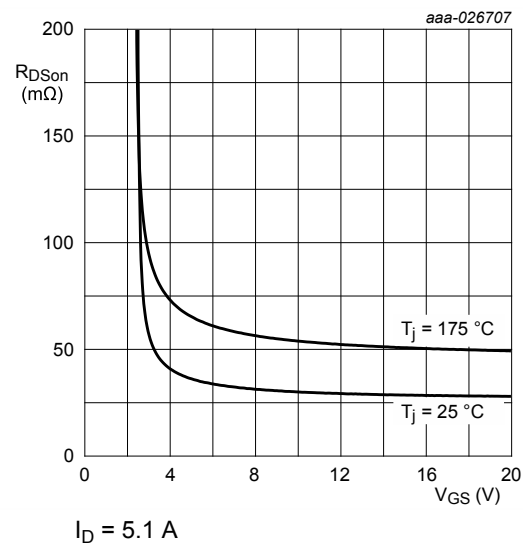


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

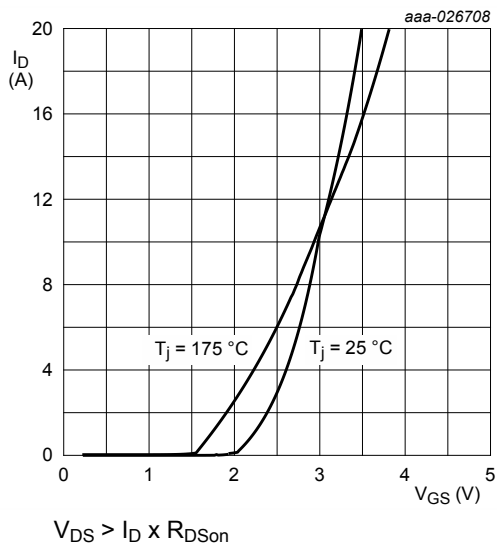


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

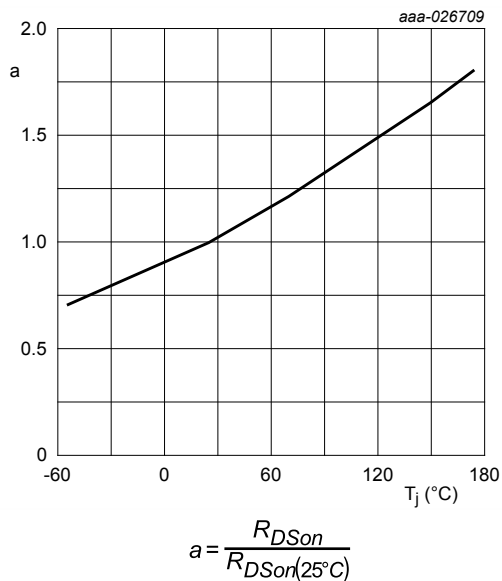


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

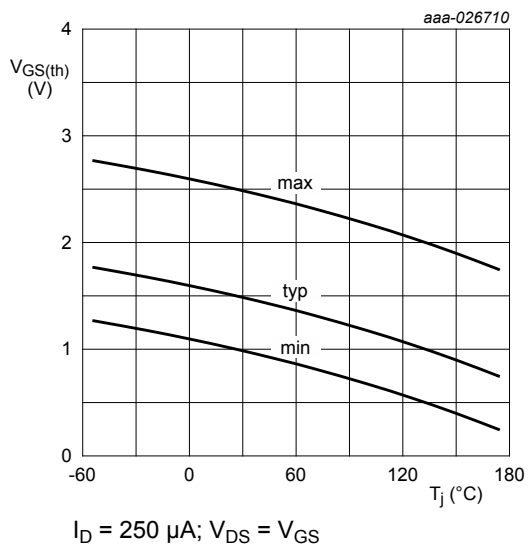


Fig. 12. Gate-source threshold voltage as a function of junction temperature

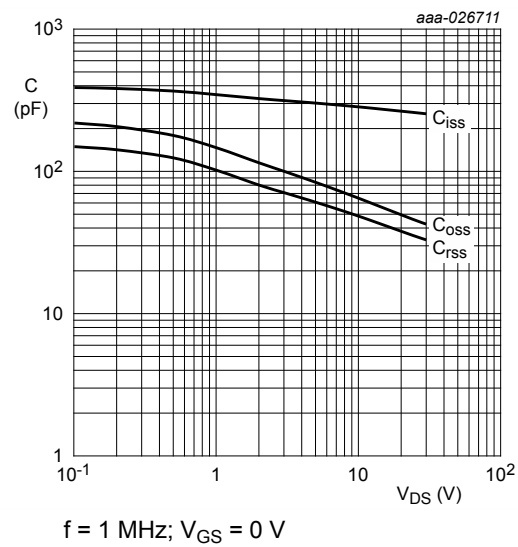


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



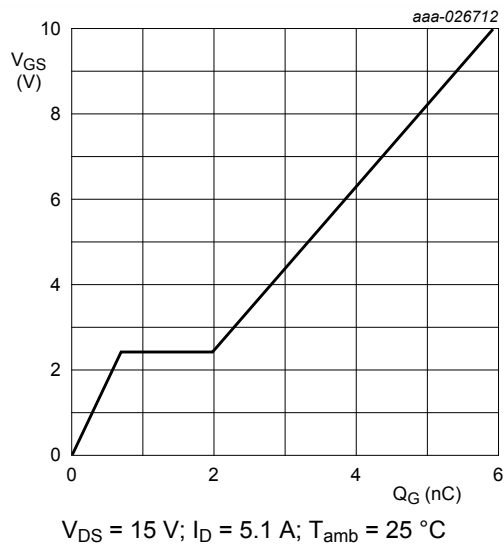


Fig. 14. Gate-source voltage as a function of gate charge; typical values

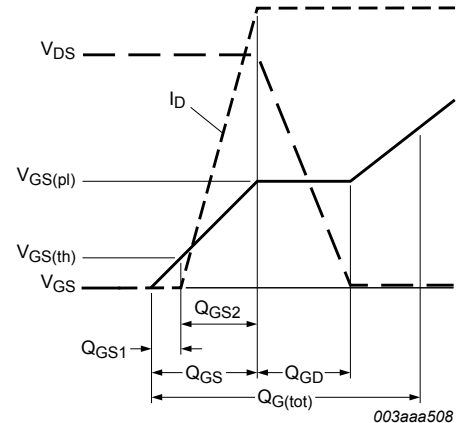


Fig. 15. Gate charge waveform definitions

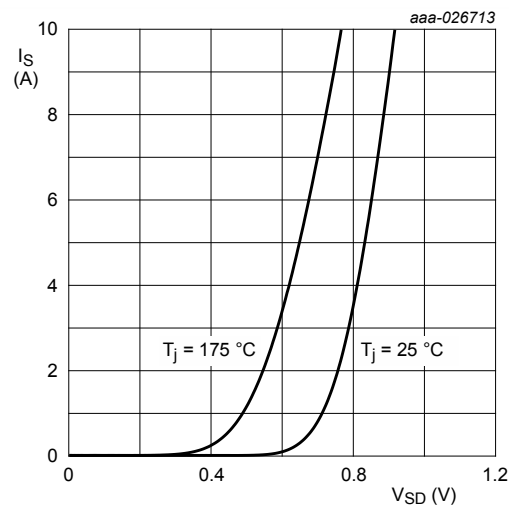


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

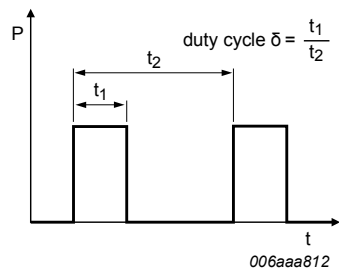


Fig. 17. Duty cycle definition

12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

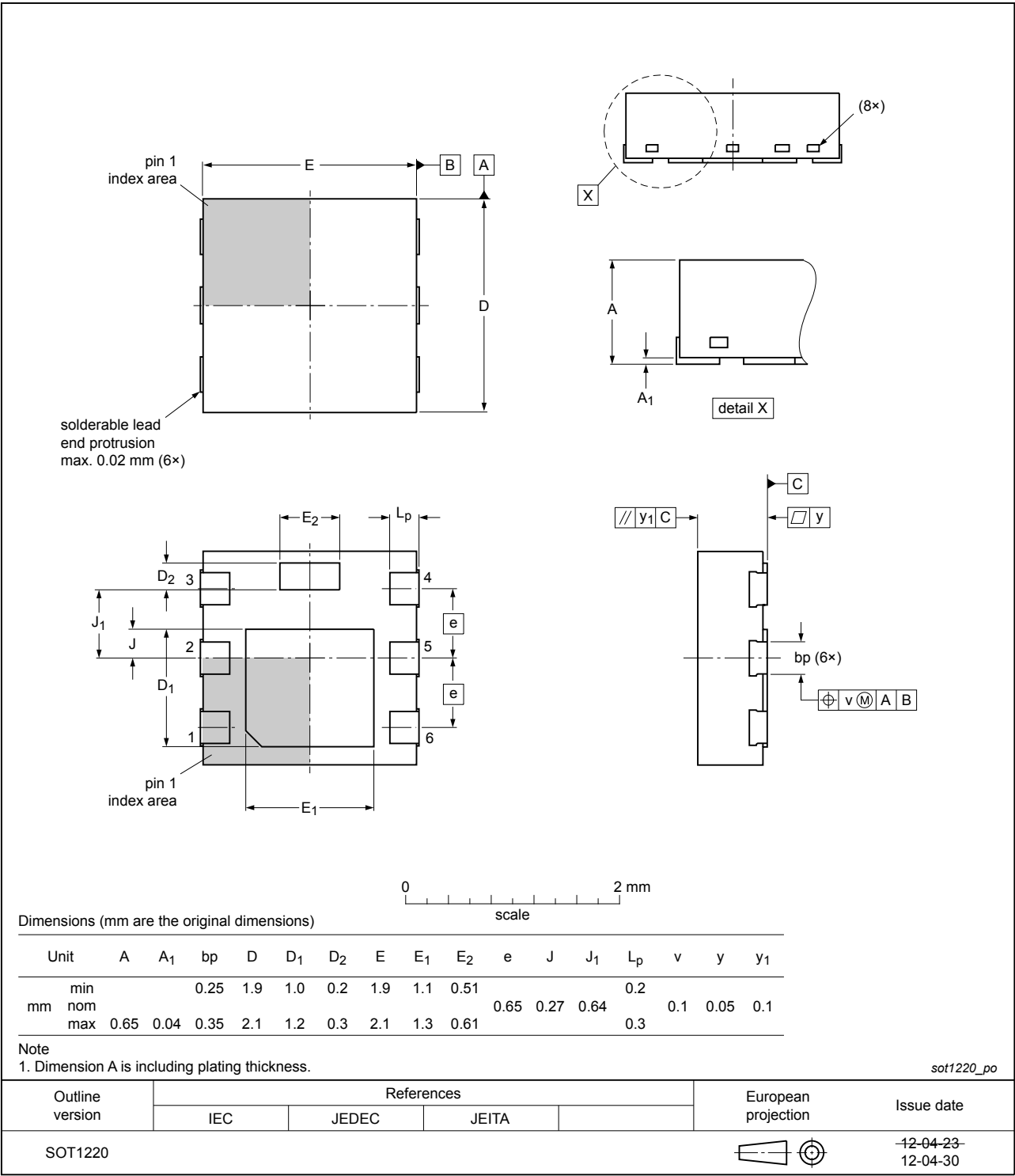
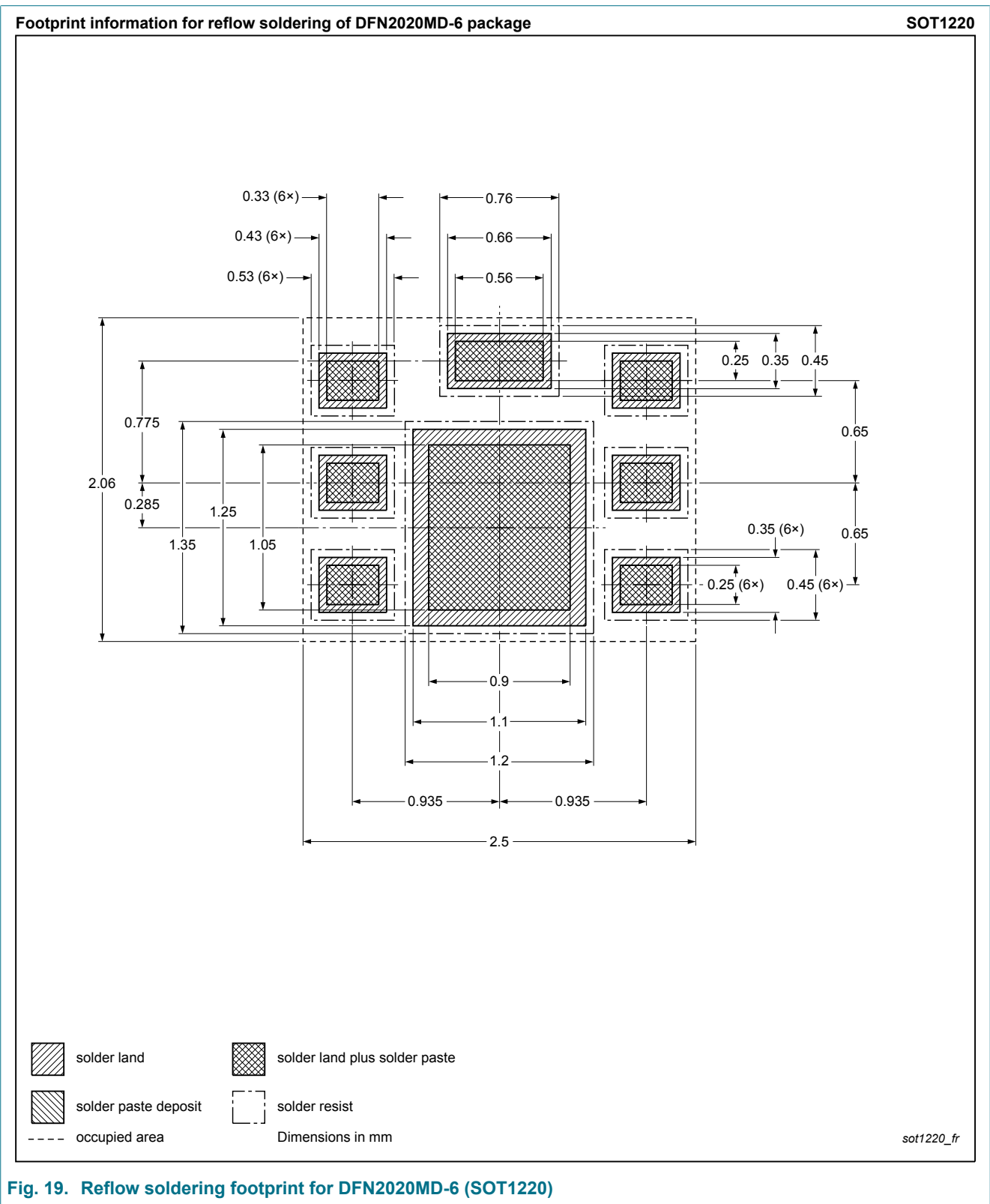


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

13. Soldering



## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB50ENE v.1	20180426	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 26 April 2018



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