



STD5N95K3, STF5N95K3 STP5N95K3, STU5N95K3

N-channel 950 V, 3 Ω, 4 A, DPAK, TO-220, TO-220FP, IPAK
Zener-protected SuperMESH3™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _w
STD5N95K3	950 V	< 3.5 Ω	4 A	90 W
STF5N95K3	950 V	< 3.5 Ω	4 A	25 W
STP5N95K3	950 V	< 3.5 Ω	4 A	90 W
STU5N95K3	950 V	< 3.5 Ω	4 A	90 W

- 100% avalanche tested
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitances
- Zener-protected

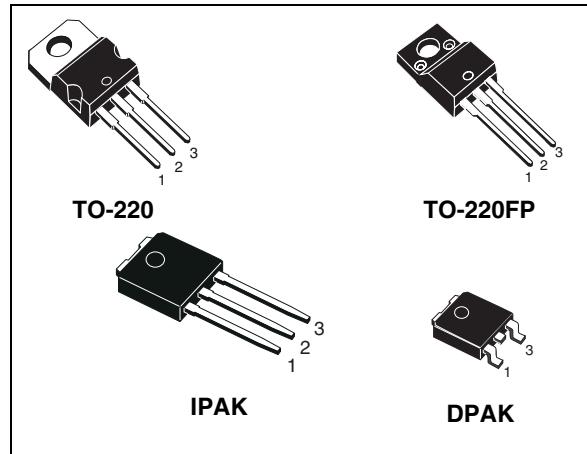


Figure 1. Internal schematic diagram

AM01476v1

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD5N95K3	5N95K3	DPAK	Tape and reel
STF5N95K3	5N95K3	TO-220FP	Tube
STP5N95K3	5N95K3	TO-220	Tube
STU5N95K3	5N95K3	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
V_{GS}	Gate- source voltage	30				V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	$4^{(1)}$	4		A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	3	$3^{(1)}$	3		A
$I_{DM}^{(2)}$	Drain current (pulsed)	16	$16^{(1)}$	16		A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	90	25	90		W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4				A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	100				mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	5				V/ns
V_{ISO}	Insulation withstand voltage (AC)		2500			
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150				°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 4\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	TO-220FP	IPAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.39	5	1.39		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50	100			°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max			50		°C/W
T_J	Maximum lead temperature for soldering purpose	300				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	950			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V; V _{DS} =0			10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2 A		3	3.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	460 38 1	-	pF pF pF
C _{o(tr)⁽¹⁾}	Equivalent capacitance time related	V _{DS} = 0 to 760 V, V _{GS} = 0	-	970	-	pF
C _{o(er)⁽²⁾}	Equivalent capacitance energy related	V _{DS} = 0 to 760 V, V _{GS} = 0	-	15	-	pF
R _g	Gate input resistance	f=1 MHz open drain	-	5.5	-	Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 760 V, I _D = 4 A, V _{GS} = 10 V <i>(see Figure 20)</i>	-	19 4.7 12	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$, $I_D = 2 \text{ A}$,		17		ns
t_r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$	-	7	-	ns
$t_{d(off)}$	Turn-off-delay time	(see Figure 19)		32	-	ns
t_f	Fall time			18		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$		410		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	3.5		μC
I_{RRM}	Reverse recovery current	(see Figure 21)		17		A
t_{rr}	Reverse recovery time	$I_{SD} = 4 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$		516		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	4.1		μC
I_{RRM}	Reverse recovery current	(see Figure 21)		16		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

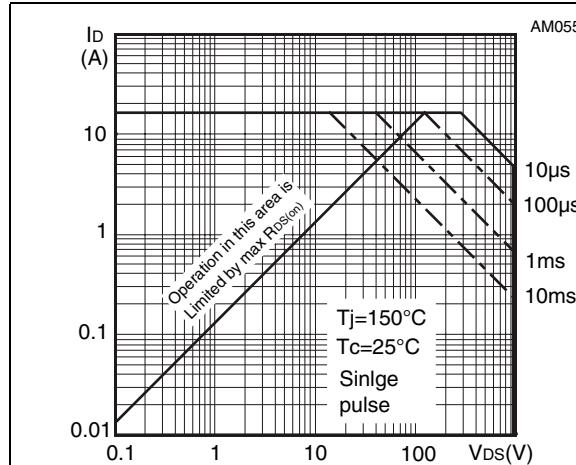


Figure 3. Thermal impedance for TO-220

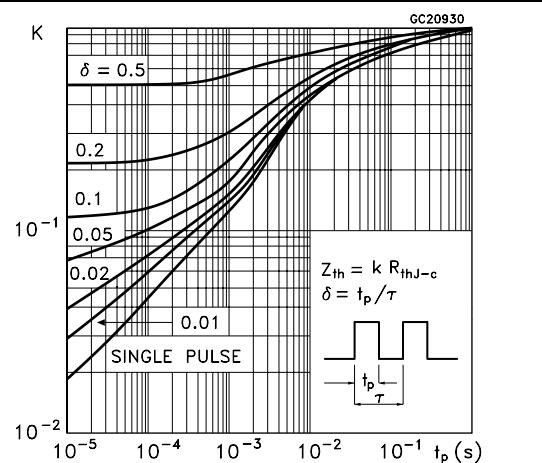


Figure 4. Safe operating area for TO-220FP

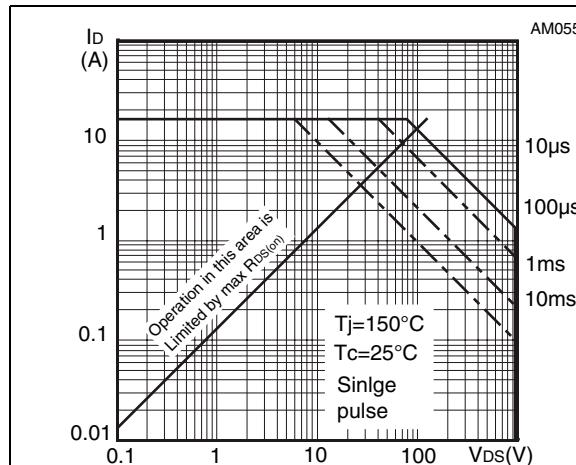


Figure 5. Thermal impedance for TO-220FP

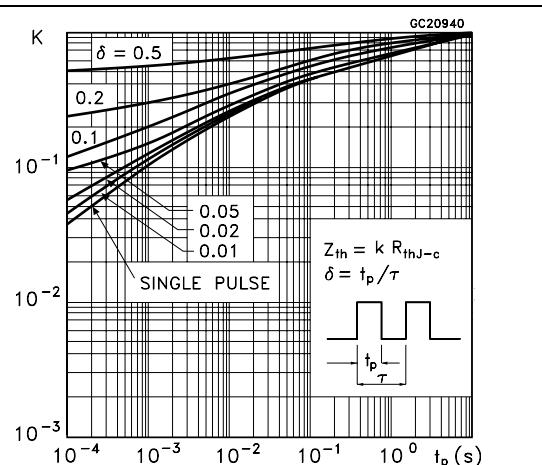


Figure 6. Safe operating area for IPAQ, DPAK

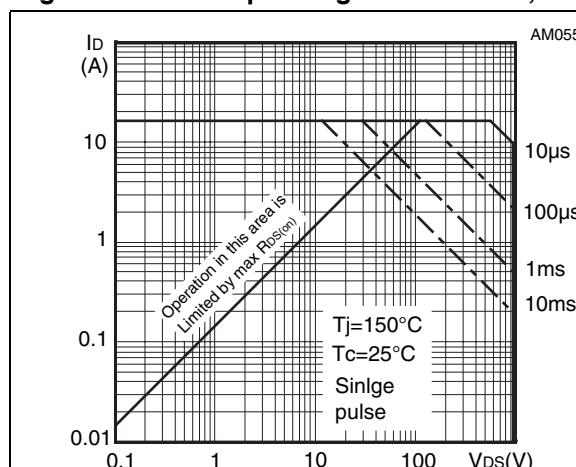


Figure 7. Thermal impedance for IPAQ, DPAK

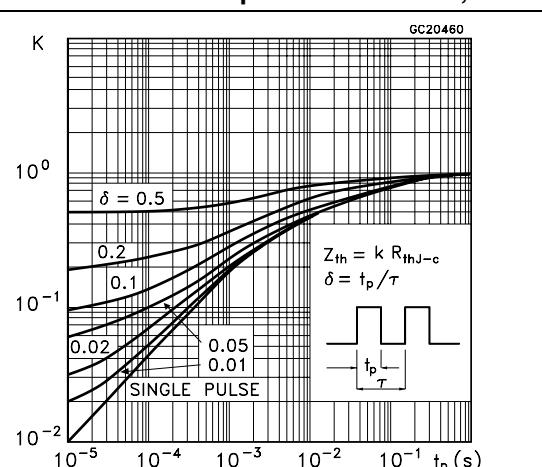


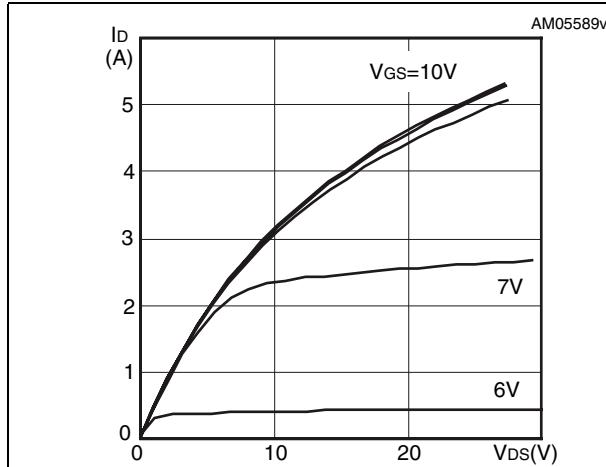
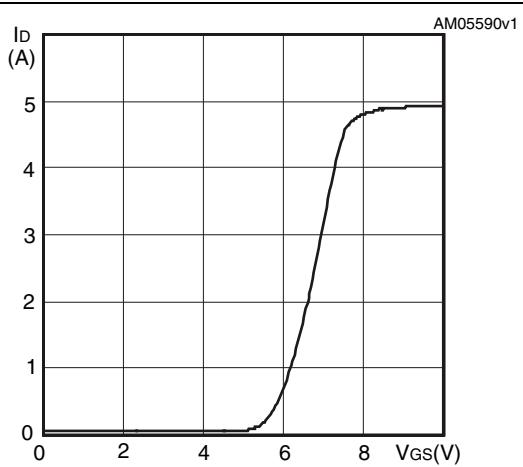
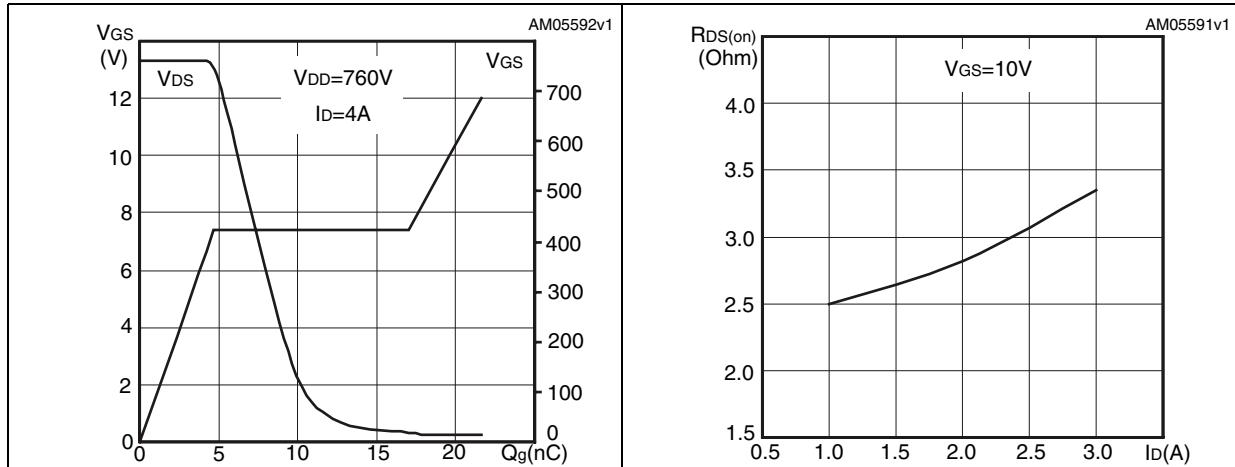
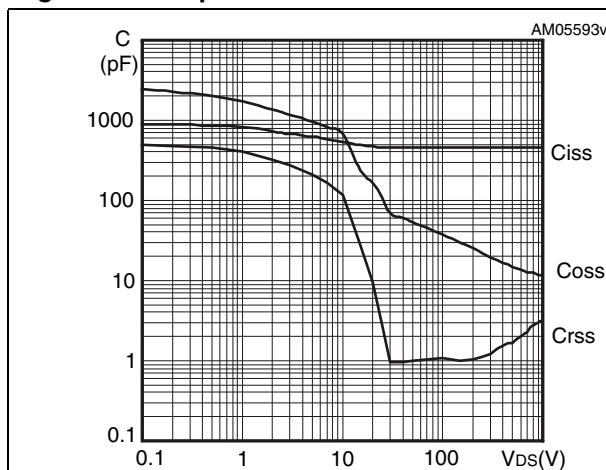
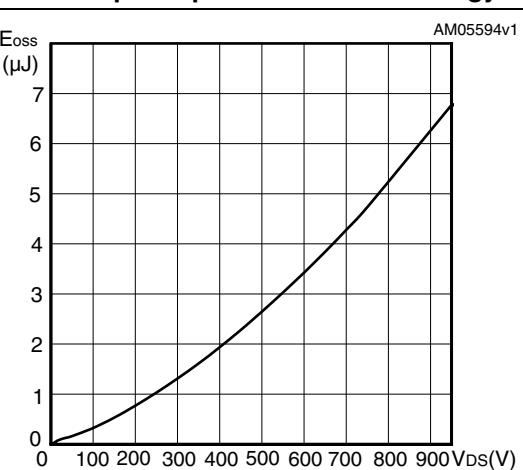
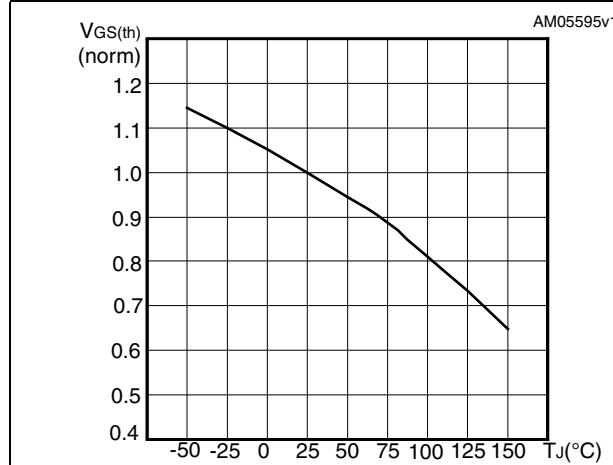
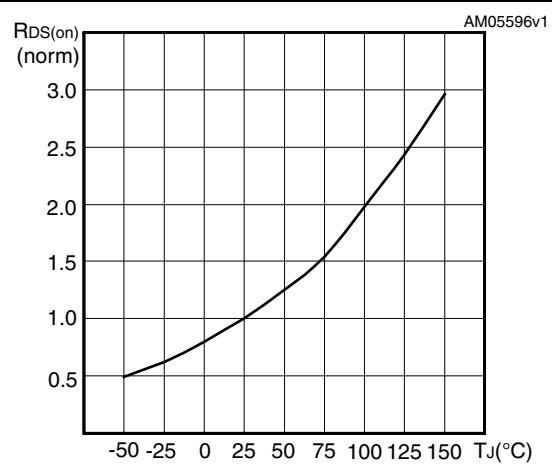
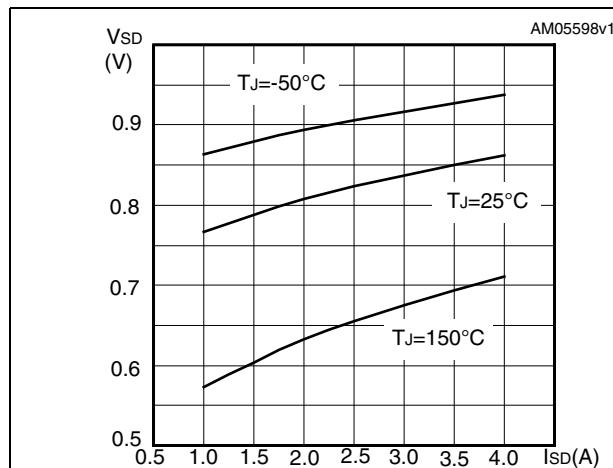
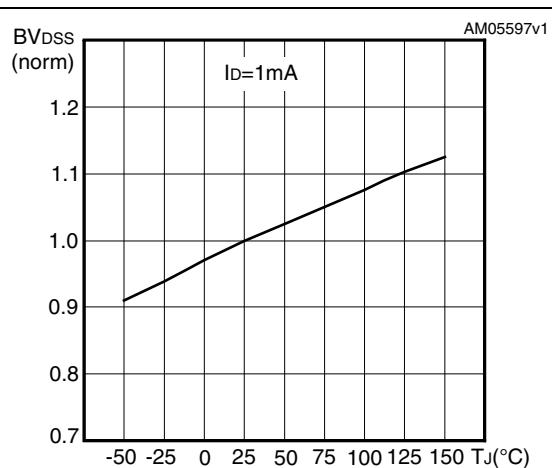
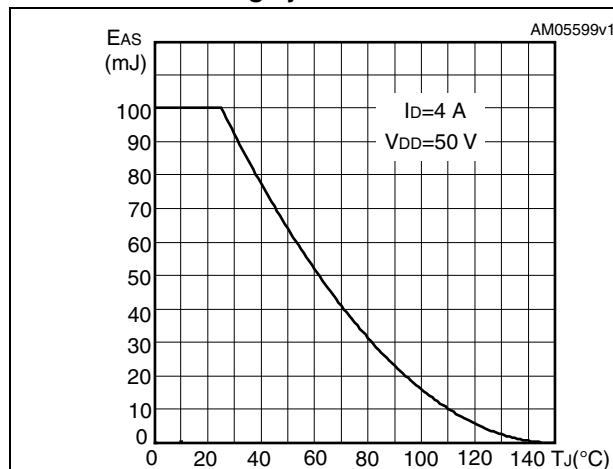
Figure 8. Output characteristics**Figure 9. Transfer characteristics****Figure 10. Gate charge vs gate-source voltage** **Figure 11. Static drain-source on resistance****Figure 12. Capacitance variations****Figure 13. Output capacitance stored energy**

Figure 14. Normalized gate threshold voltage vs temperature**Figure 15. Normalized on resistance vs temperature****Figure 16. Source-drain diode forward characteristics****Figure 17. Normalized B_{VDSS} vs temperature****Figure 18. Maximum avalanche energy vs starting T_j**

3 Test circuits

Figure 19. Switching times test circuit for resistive load

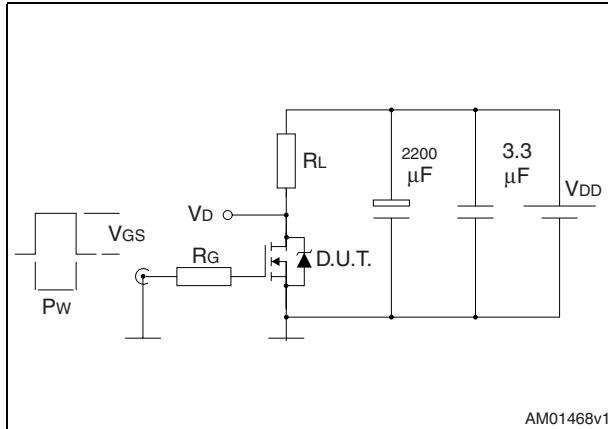


Figure 20. Gate charge test circuit

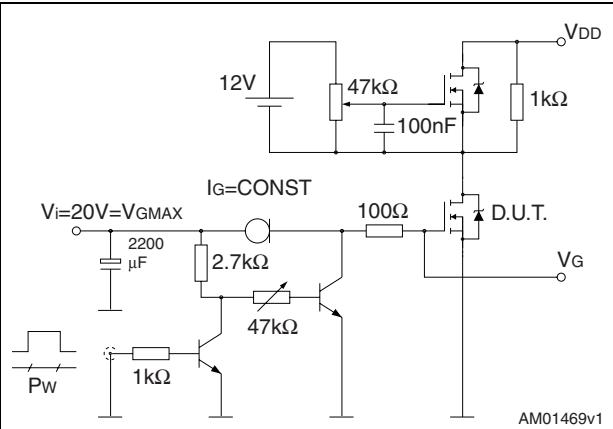


Figure 21. Test circuit for inductive load switching and diode recovery times

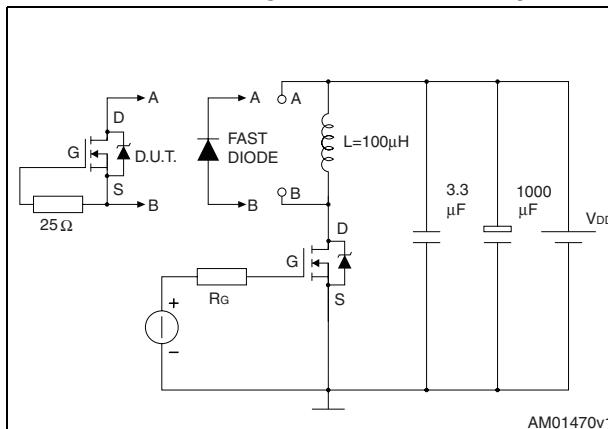


Figure 22. Unclamped inductive load test circuit

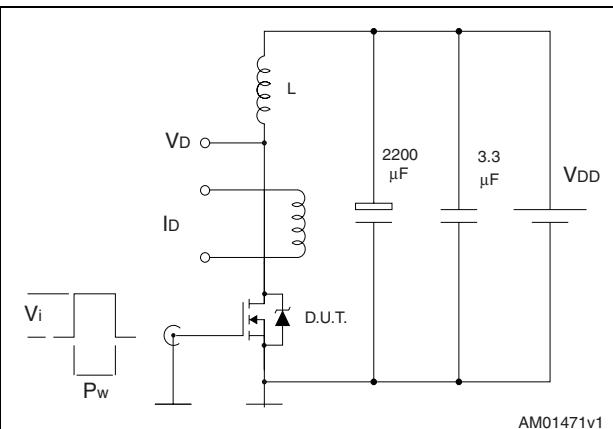


Figure 23. Unclamped inductive waveform

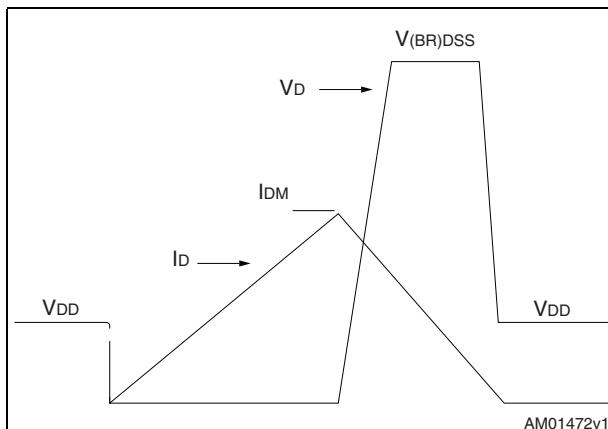
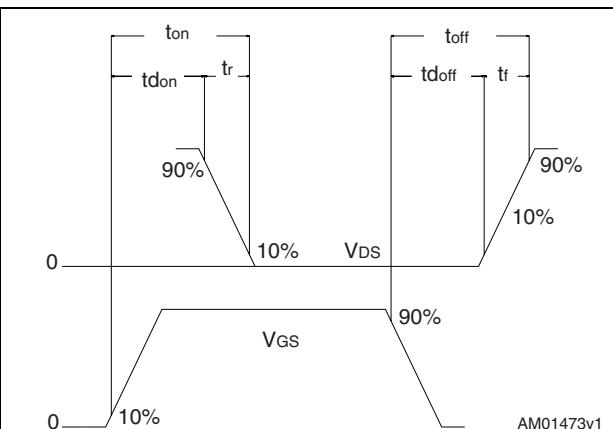


Figure 24. Switching time waveform

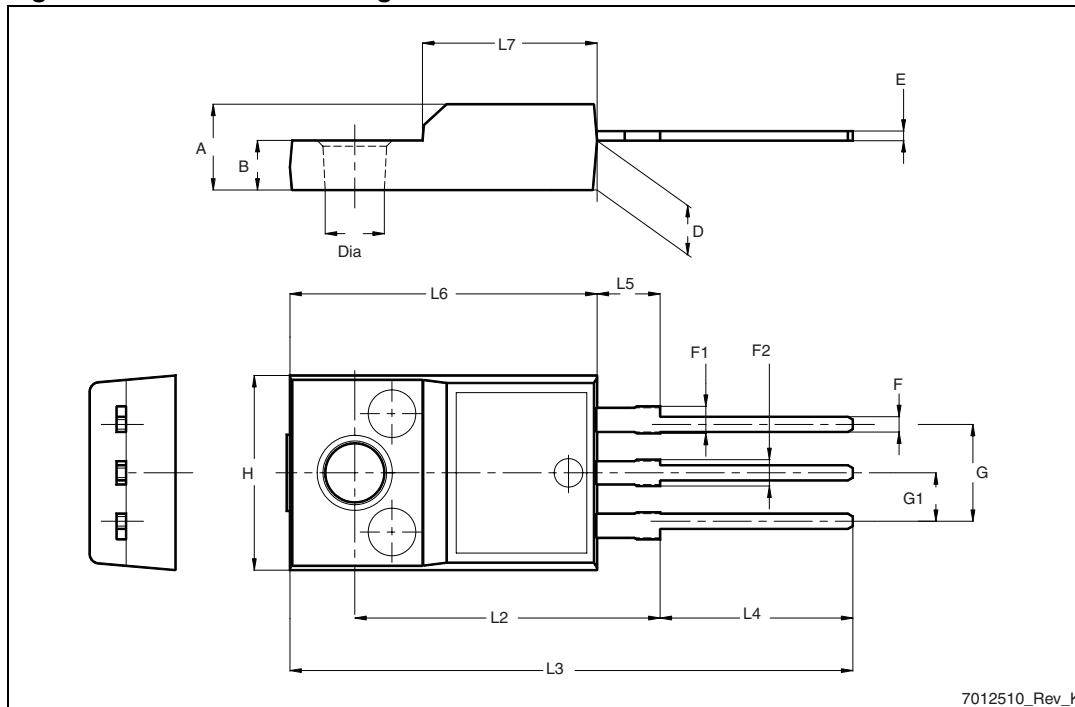


4 Package mechanical data

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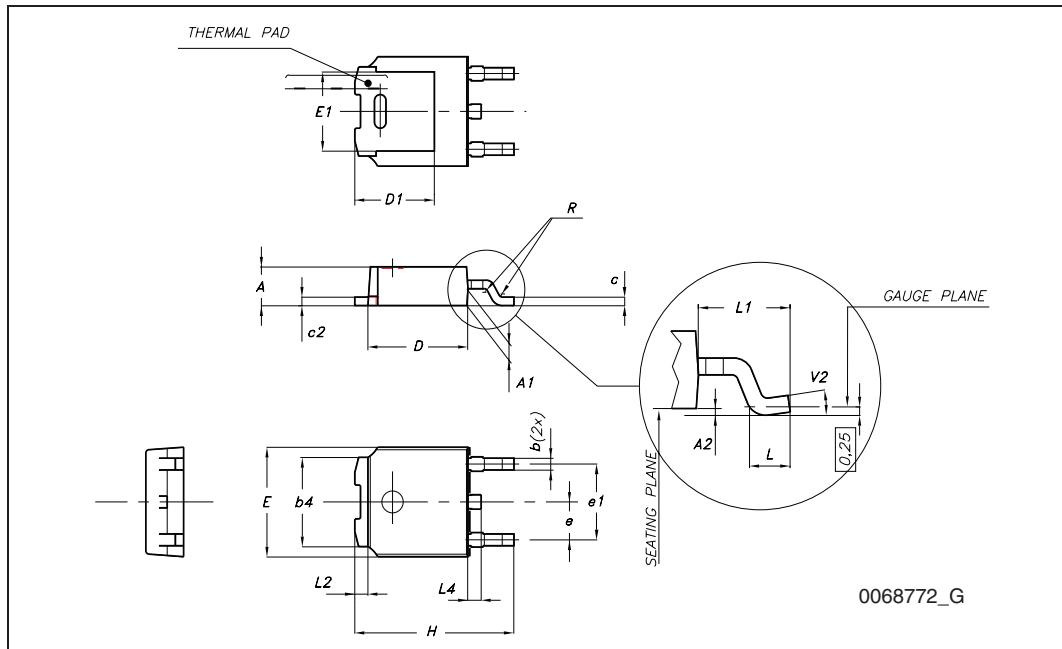
Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

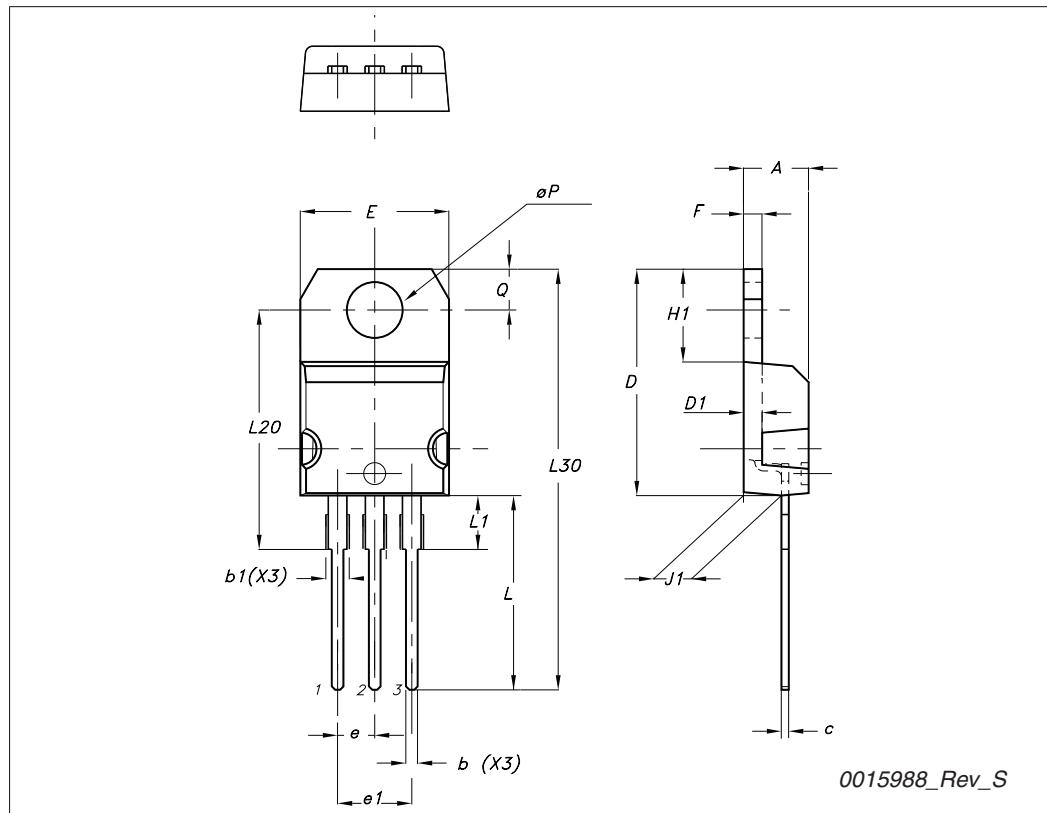
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



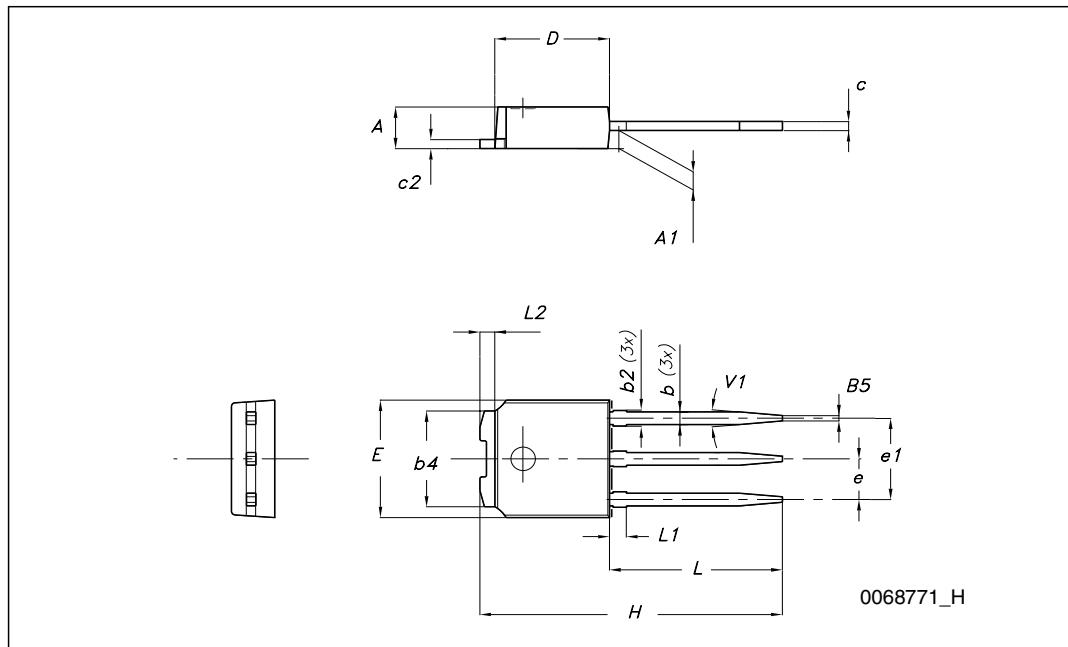
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
$\varnothing P$	3.75		3.85
Q	2.65		2.95



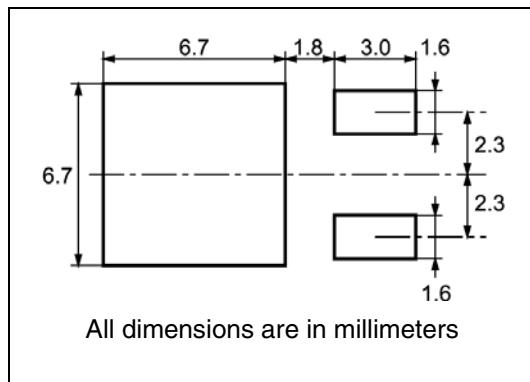
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



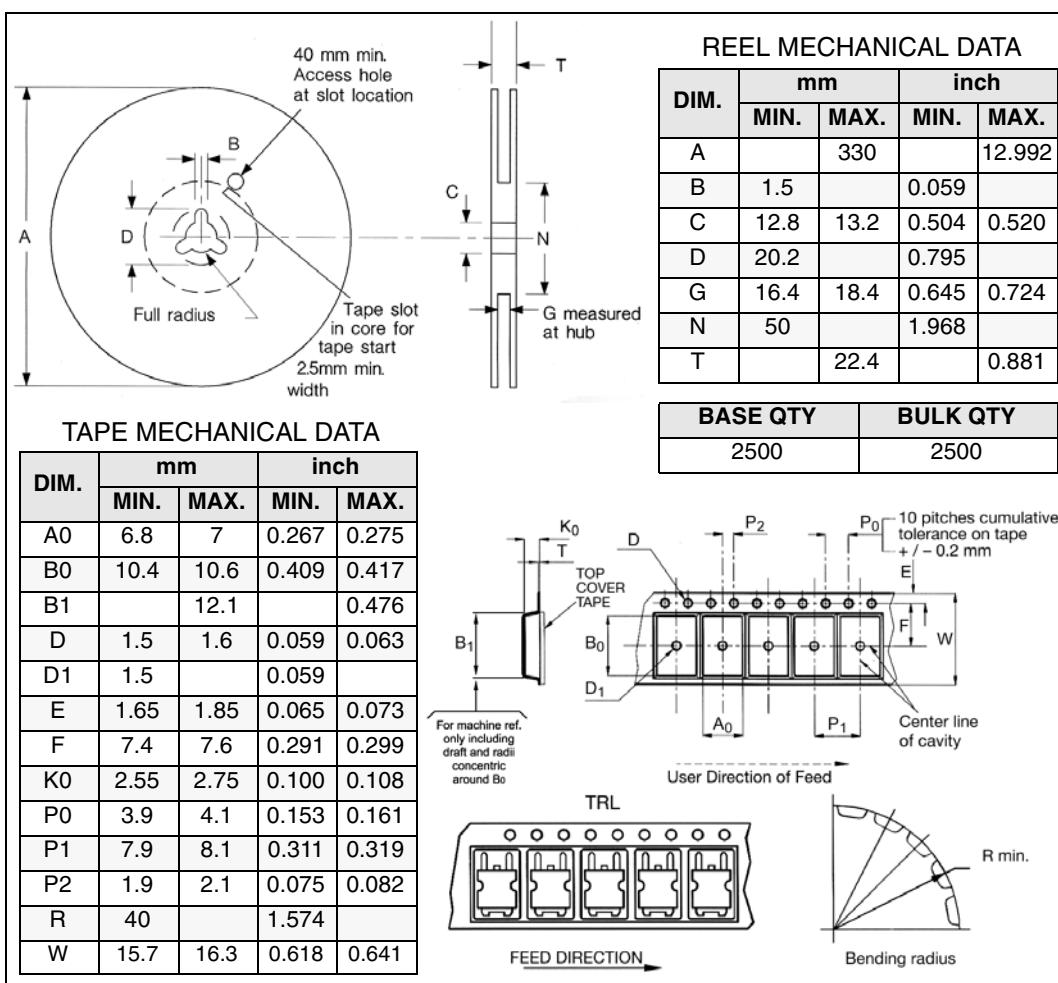
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-May-2009	1	First release
11-Dec-2009	2	Document status promoted from preliminary data to datasheet

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- Техническая поддержка проекта;
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