LTC2207, LTC2206, LTC2205, LTC2204, LTC2203, LTC2202, LTC2201 16-Bit/14-Bit 10Msps to 105Msps ADCs

DESCRIPTION

Demonstration circuit 919A supports members of a family of 16-bit/14-bit 10Msps to 105Msps ADCs. Each assembly features one of the following devices: LTC®2207, LTC2206, LTC2205, LTC2204, LTC2203, LTC2202, or LTC2201 high speed, high dynamic range ADCs.

Other members of this family include the LTC2208/LTC2208-14 16-bit/14-bit 130Msps ADC with LVDS outputs. These 9mm × 9mm QFN devices are supported by Demonstration circuit 854 (CMOS outputs) or by Demonstration circuit 996 (LVDS outputs).

Several versions of the 919A demo board supporting a single-ended clock input, specifically targeted for use with the 25Msps LTC2203, 20Msps LTC2201 and 10Msps LTC2202 A/D converters, are listed in Table 1. LTC2204, LTC2205, LTC2206 and LTC2207 have differential clock inputs but use a single-ended clock input for evaluation with the DC input on the DC919A board. Depending on the required sample rate and input frequency, the DC919A is supplied with the appropriate ADC and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies from DC to 70MHz or from 1MHz to 70MHz if using the transformer coupled input. For higher input frequencies, contact the factory for support.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC919A Variants

DC919 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
919A-A	LTC2207	16-Bit	105Msps	DC - 70MHz
919A-B	LTC2206	16-Bit	80Msps	DC - 70MHz
919A-C	LTC2205	16-Bit	65Msps	DC - 70MHz
919A-D	LTC2204	16-Bit	40Msps	DC -70MHz
919A-E	LTC2203	16-Bit	25Msps	DC - 70MHz
919A-F	LTC2202	16-Bit	10Msps	DC - 70MHz
919A-G	LTC2207-14	14-Bit	105Msps	DC -70MHz
919A-H	LTC2206-14	14-Bit	80Msps	DC - 70MHz
919A-I	LTC2205-14	14-Bit	65Msps	DC - 70MHz
919A-J	LTC2201	16-Bit	20Msps	DC - 70MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on Sampling Rate and the A/D Converter Provided, this Supply Must Provide Up to 500mA.	Optimized for 3.3V [3.15V ↔ 3.45V Min/Max]
Analog Input Range	Depending on PGA Pin Voltage	$1.5V_{P-P}$ to $2.25V_{P-P}$
Logic Input Voltages	Minimum Logic High	2.4V
	Maximum Logic Low	0.8V
Logic Output Voltage (74VCX245 Output Buffer, V_{CC} = 2.5V)	Minimum Logic High at –1.6mA	2.3V (33Ω Series Terminations)
	Maximum Logic Low at 1.6mA	0.7V (33Ω Series Terminations)
Sampling Frequency (Convert Clock Frequency)	See Table 1	

PERFORMANCE SUMMARY (T_A = 25°C)

Convert Clock Level	50Ω Source Impedance, AC-Coupled or Ground Referenced (Convert Clock Input Is Capacitor Coupled on Board and Terminated with 50Ω.)	$2V_{P-P}$ ↔ $2.5V_{P-P}$ Sine Wave or Square Wave
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 919A is easy to set up to evaluate the performance of the LTC2207, LTC2206, LTC2205, LTC2204, LTC2203, or LTC2202 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow this procedure:

Setup

If a DC718 QuikEval™ II Data Analysis and Collection System was supplied with the DC919A demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC919A to a PC.

DC919A Demonstration Circuit Board Jumpers

The DC919A demonstration circuit board should have the following jumper settings as default: (as per Figure 1)

JP1: Output clock polarity: GND

JP2: SENSE: VDD, (Internal reference)

JP3: PGA: GND 2.25V range

JP4: RAND: GND Not randomized

JP5: SHDN: GND Not shutdown

JP6: DITH: GND No internal dithering

Applying Power and Signals to the DC919A Demonstration Circuit

If a DC718 is used to acquire data from the DC919A, the DC718 must FIRST be connected to a powered USB port or provided an external 6V to 9V BEFORE applying 3.3V across the pins marked "+3.3V" and "PWR GND" on the DC919A. The DC919A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC718 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub in which case it must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

Encode Clock

NOTE: This is a logic compatible input, contrary to the majority of Linear Technology ADC demo boards. It is not terminated with 50Ω.

Apply an encode clock to the SMA connector on the DC919A demonstration circuit board marked "J3 ENCODE INPUT".

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. A low jitter 3.3V oscillator with direct connection through a barrel is recommended.

If using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$ or 13dBm, filtered and terminated with a 50Ω thru-terminator. If a generator with 50Ω output impedance is connected via a cable, it is recommended that a thru-terminator be used. However, below 15MHz, it is recommended that a square wave drive be used.

If a sinusoidal ground referenced signal, or an AC-coupled signal is used, 1.5V to 1.7V DC bias must be introduced via a bias tee.

DC919A has provision for a popular surface mount oscillator form and some population options to select this as the clock source. (Please see schematic.)

If only sinusoidal or clipped sinusoid signal sources are available as the clock source for scenarios involving sampling rates less than 15Msps to 20Msps, it is recommended

QUICK START PROCEDURE

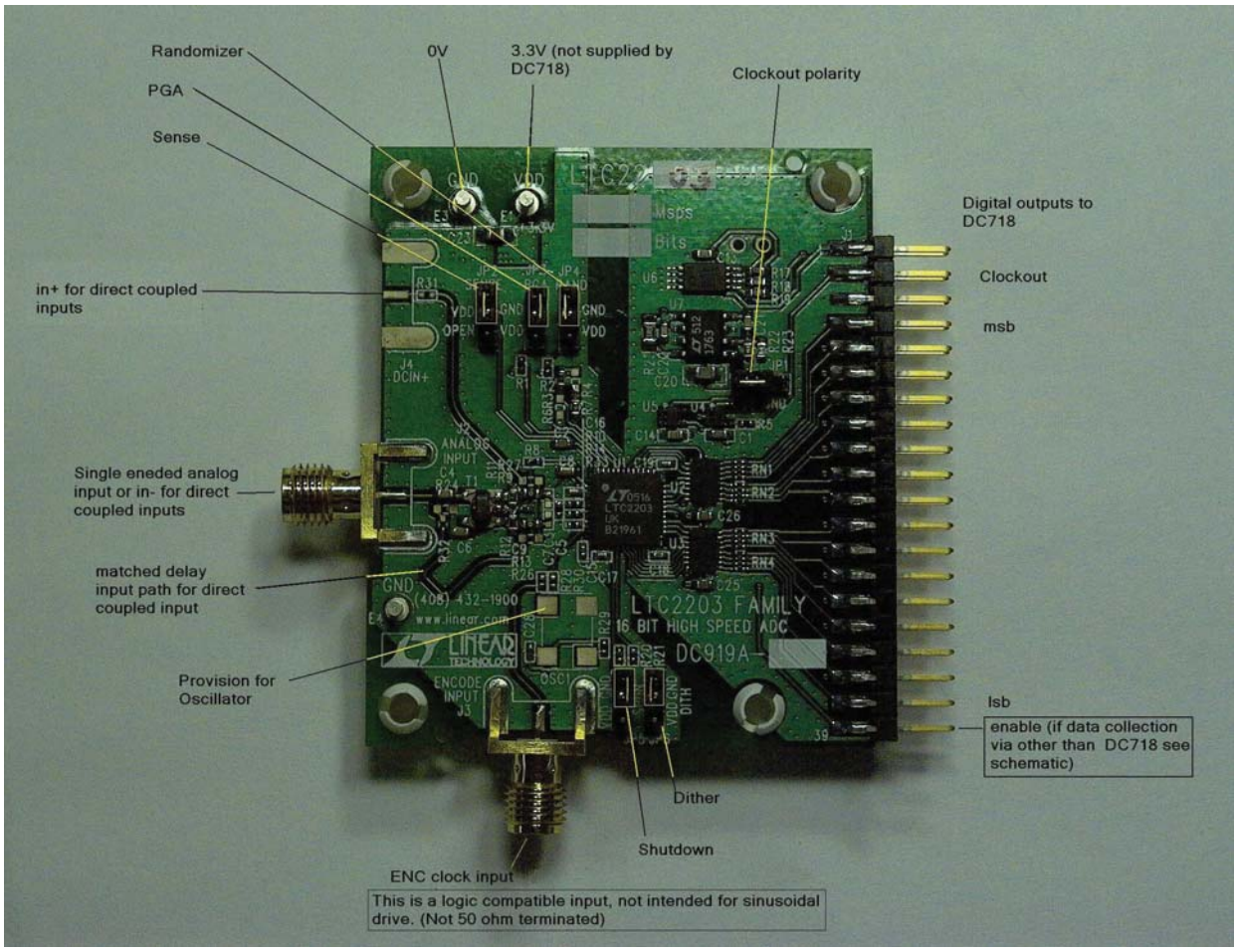


Figure 1. DC919A Setup

that a divide by 4 or divide by 8 be used. If the converter is to be used at very low sampling rates approaching the minimum, a higher divide ratio may be required. This is especially important if undersampling.

If you want to use these converters at less than the minimum sampling rate, it is recommended that you run the ADC above the minimum rate, and decimate. If oversampling low frequencies, the use of a sinusoid is potentially acceptable, but it must be very clean or the low dV/dt will result in a great sensitivity to wideband noise in the clock driver.

The use of a divider may require a bandpass filter prior to the divider in order to achieve best SNR as the divider can exaggerate phase noise if it is sensitive to GHz frequencies. Contact Linear Technology for recommendations or in some cases, available clock sources or dividers.

Most generators require filtering or they will compromise both the SNR and the SFDR of the ADCs.

Generally data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input. In the case of the LTC2203/LTC2202/LTC2201 we use a divide by 4.

This demo board is, populated by default for the DC input path. There is a transformer mounted at T1, but C4, C6, R9 and R13 are not populated. If a single-ended AC input is required, the DC input paths must be disconnected by removing R26, 27, 31 and 32, and the above components installed.

QUICK START PROCEDURE

If the transformer input is required, C4 and C6 should be 0.1µF X5R 0402, R9 and R13 should be 10Ω 0402 resistors.

Note that this transformer (ETC1-1T) is poor below 1MHz.

Reduced amplitude signals can be applied to 300kHz. Applications below 300kHz must be driven directly via DC inputs.

As there are a significant number of these boards that are customized, please confirm the population of your board. The schematic below shows the default population, the photograph shows the population of a transformer coupled version. This board may also be populated with LTC2204-2207 for DC drive applications, in which case, R33 is a 0.1µF capacitor.

Apply the analog input signal of interest to the SMA connector on the DC919A demonstration circuit board marked "J2 ANALOG INPUT". These inputs are capacitive coupled to a Flux coupled transformers ETC1-1T. In some cases, where these devices are to be used in undersampling scenarios, this transformer should be replaced with an ETC1-1-13 Balun.

The DC919A can be modified for direct DC drive from a suitable differential signal source.

This may be done by yourself or at special request when you order the demo board.

If the DC input paths are populated with low value (5.1Ω) resistors at both ends of these transmission lines, you must provide a reasonably well balanced differential drive with 1.25V common mode.

The spacing of these SMA connectors (0.8") allows them to be mated directly with demo boards for devices such as the LT1993, LT1994, LT5514 and others.

It is not recommended to drive this ADC in a single-ended fashion into a single DC input.

An internally generated conversion clock output is available on pin 3 of J1 and the data samples are available on Pins 7 to 37 of J1 which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40-pin ribbon cable or collected by the DC718 QuikEval II Data Acquisition Board using the PScope™ System Software provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

If data is to be collected by a logic analyzer, pin 40 must be strapped to OVDD or 2.5V.

(Please see schematic.)

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC919A demonstration circuit is properly connected to the DC718, PScope should automatically detect the DC919A, and configure itself accordingly. If necessary, the procedure below explains how to manually configure PScope.

Under the configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options:

User configure

16-Bit (or 14-Bit if using -14 versions)

Alignment: Left-16

Bipolar (2's complement)

Positive clock edge

Type: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC718 Quick Start Guide and in the online help available within the PScope program itself.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs should be optimized for different analog input frequencies. At this point in time, the circuit in Figure 3 for input frequencies below 70MHz. For input frequencies from 70MHz to 140MHz, the circuit in Figure 2 is used. These two input networks cover a

QUICK START PROCEDURE

broad bandwidth and are not optimized for operation at a specific input frequency.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

Narrow band high-Q filters may produce poor SNR results with Dither enabled. 10% bandpass would be preferred over 5% bandpass on the analog input. The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband.

In cases with long transmission lines, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

For advice on drive circuits or for input frequencies greater than 70MHz contact the factory for support.

For input frequencies less than 5MHz, or greater than 150MHz, other input networks may be more appropriate. Please consult the factory for suggestions on drivers and networks if your signal sources extend outside these ranges, or if you experience difficulties driving these suggested networks.

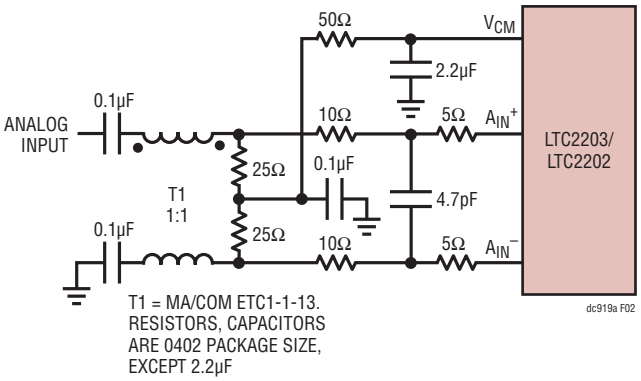


Figure 2. Analog Front End Circuit For 70MHz+

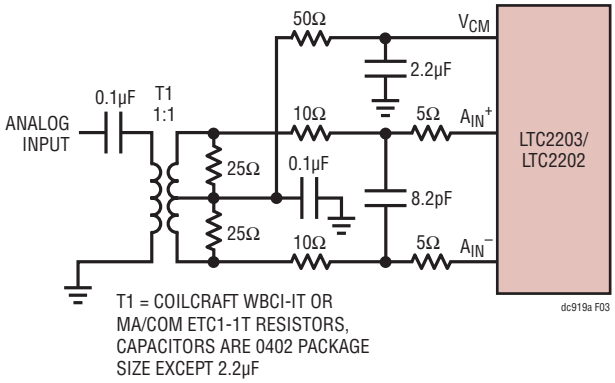
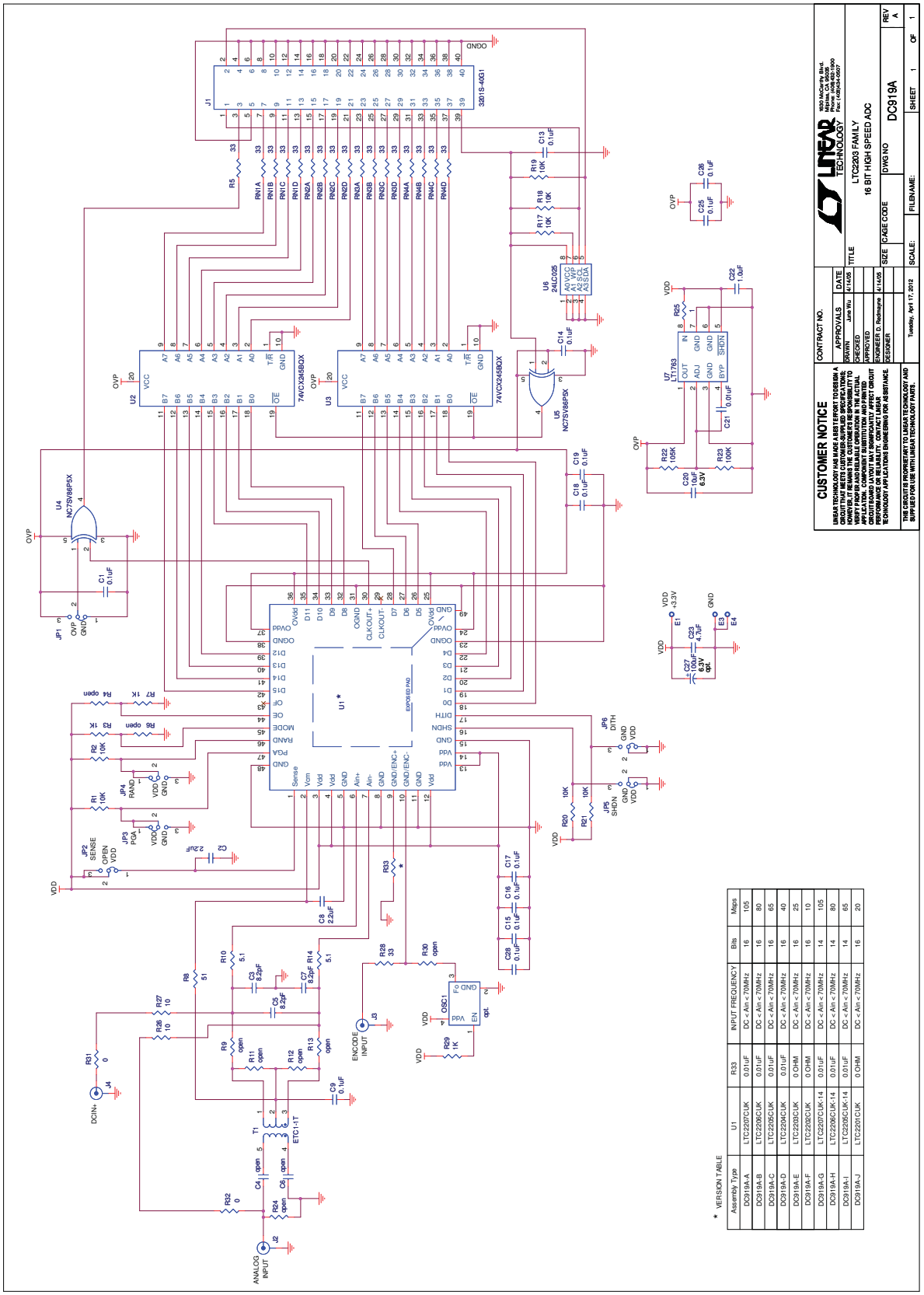


Figure 3. Analog Front End Circuit for 1MHz < A_{IN} < 70MHz

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	5	C1, C13, C14, C25, C26	CAP., X7R, 0.1µF, 25V, 10% 0603	TDK, C1608X7R1E104K
2	0	C4, C6 (OPEN)	CAP., 0603	
3	2	C8, C2	CAP., X5R, 2.2µF, 6.3V, 10% 0603	TDK, C1608X5R0J225K
4	3	C3, C5, C7	CAP., C0G, 8.2pF, 50V, 5% 0402	AVX, 04025A8R2JAT
5	7	C9, C15-C19, C28	CAP., X5R, 0.1µF, 10V, 10% 0402	TDK, C1005X5R1A104K
6	1	C20	CAP., X5R, 10µF, 6.3V, 10% 0805	TDK, C2012X5R0J106K
7	1	C21	CAP., X7R, 0.01µF, 50V, 10% 0603	TDK, C1608X7R1H103K
8	1	C22	CAP., X7R, 1.0µF, 16V, 10% 0603	TDK, C1608X7R1C105K
9	1	C23	CAP., X5R, 4.7µF, 10V, 10% 0805	TDK, C2012X5R1A475K
10	0	C27 (OPT)	CAP., 100µF, 6.3V 6032	
11	3	E1, E3, E4	TESTPOINT, TURRET, 0.061"	MILL-MAX, 2308-2-00-44
12	6	JP1-JP6	0.079 SINGLE ROW HEADER, 3-PIN	SAMTEC, TMM103-02-L-S
13	6	JP1-JP6	SHUNT	SAMTEC, 2SN-BK-G
14	1	J1	CON, HDR, 0.1 × 0.1 CNTRS, 40-PIN	SAMTEC, TSW-120-07-L-D
15	3	J2, J3, J4	CON., SMA 50Ω EDGE-LANCH	CONNEX, 132357
16	0	OSC1 (OPT)		
17	4	RN1, RN2, RN3, RN4	RES ARRAY, 33Ω, 5%, 0402	VISHAY, CRA04S0803330JRT7
18	4	R1, R2, R20, R21	RES., CHIP, 10k, 1/16W, 5% 0402	AAC, CR05-103JM
19	2	R3, R7	RES., CHIP, 1k, 1/16W, 5% 0603	AAC, CR16-102JM
20	0	R4, R6, R9, R11-R13, R24, R30 (OPEN)	RES., CHIP, 0603	
21	2	R26, R27	RES., CHIP, 10Ω, 1/16W, 5% 0603	AAC, CR16-100JM
22	2	R5, R28	RES., CHIP, 33Ω, 1/16W, 5% 0402	VISHAY, CRCW0402330JRT6
23	1	R8	RES., CHIP, 51Ω, 1/16W, 5% 0402	AAC, CR05-510JM
24	1	R29	RES., CHIP, 1k, 1/16W, 5% 0402	AAC, CR05-102JM
25	2	R10, R14	RES., CHIP, 5.1Ω, 1/16W, 5% 0402	AAC, CR05-5R1JM
26	2	R31, R32	RES., CHIP, 0Ω, 1/16W, 0402	AAC, CJ05-000M
28	2	R12, R11	RES., CHIP, 24.9Ω, 1/16W, 1% 0603	VISHAY, CRCW060324R9FRT6
29	3	R17, R18, R19	RES., CHIP, 10k, 1/16W, 5% 0603	AAC, CR16-103JM
30	1	R22	RES., CHIP, 105k, 1/16W, 1% 0603	AAC, CR16-1053FM
31	1	R23	RES., CHIP, 100k, 1/16W, 5% 0603	AAC, CR16-104JM
32	1	R25	RES., CHIP, 1Ω, 1/8W, 5% 0805	AAC, CR10-1R0JM
33	1	T1	TRANSFORMER, 1:1, ETC1-1T	M/A-COM, ETC1-1T
34	2	U3, U2	I.C., 74VCX245BQX, DQFN20	FAIRCHILD, 74VCX245BQX
35	2	U4, U5	I.C., NC7SV86 SC70-5	FAIRCHILD, NC7SV86P5X
36	1	U6	I.C., 24LC025, TSSOP-8	MICROCHIP, 24LC025 I /ST
37	1	U7	I.C., LT1763, SO8	LINEAR TECH., LT1763CS8
38	4	(STAND-OFF)	STAND-OFF, NYLON 0.25" tall	KEYSTONE, 8831(SNAP ON)

SCHEMATIC DIAGRAM



* VERSION TABLE

Assembly Type	U1	R33	INPUT FREQUENCY	Bits	Msps
DC919A-A	LTC2207CUK	0.01uF	DC < Ain < 70MHz	16	105
DC919A-B	LTC2206CUK	0.01uF	DC < Ain < 70MHz	16	80
DC919A-C	LTC2205CUK	0.01uF	DC < Ain < 70MHz	16	65
DC919A-D	LTC2204CUK	0.01uF	DC < Ain < 70MHz	16	40
DC919A-E	LTC2203CUK	0 OHM	DC < Ain < 70MHz	16	25
DC919A-F	LTC2202CUK	0 OHM	DC < Ain < 70MHz	16	10
DC919A-G	LTC2207CUK-14	0.01uF	DC < Ain < 70MHz	14	105
DC919A-H	LTC2206CUK-14	0.01uF	DC < Ain < 70MHz	14	80
DC919A-I	LTC2205CUK-14	0.01uF	DC < Ain < 70MHz	14	65
DC919A-J	LTC2201CUK	0 OHM	DC < Ain < 70MHz	16	20

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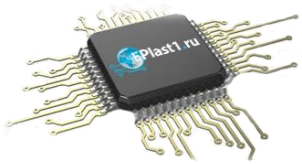

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