Brief Description

The ASI4U is a next-generation CMOS integrated circuit for AS-i networks. This low-level field bus AS-i (Actuator Sensor Interface) was designed for easy, safe, and cost-effective interconnection of sensors, actuators, and switches. It transports both power and data over the same two-wire unshielded cable.

The ASI4U is used as part of a master or slave node and functions as an interface to the physical bus. It provides the power supply, physical data transfer, and communication protocol handling. The ASI4U is fully compliant with the *AS-Interface Complete Specification V3.0*. It is function and pin compatible with the A²SI IC.

All configuration data are stored in an internal EEPROM that can be easily programmed by a stationary or handheld programming device. The special AS-i safety option assures short response times for security-related events.

Features

- Compliant with *AS-Interface Complete Specification V3.0*
- Universal application: slaves, masters, repeaters, and bus-monitors
- Floating AS-i transmitter and receiver for highly symmetrical high-power applications
- On-chip electronic inductor with current drive capability of 55 mA
- Two configurable LED outputs to support all *AS-Interface Complete Specification V3.0* status indication modes
- Several data pre-processing functions, including configurable data input filters and bit-selective data inverting
- Additional addressing channel for easy wireless module setup
- Support of 8 and 16 MHz crystals by automatic frequency detection
- Special AS-i safety option
- Clock watchdog for high system security

Related Products

- SAP5 Universal AS-Interface IC

Benefits

- Flexible, separated I/O pins
- Flexible AS-i Bus adoption (isolated transceiver)
- Very small package SSOP28 (ASI4U and ASI4U-F)
- High ambient temperature applications (ASI4U-E)

Physical Characteristics

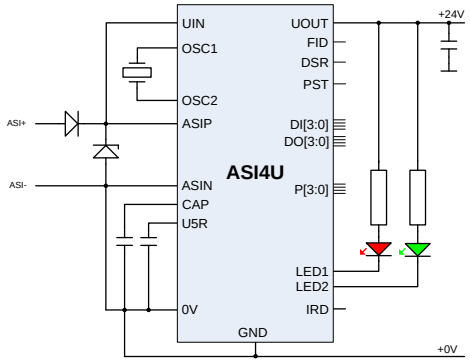
- ASI4U operational temperature: -25 to +85 °C
- ASI4U-F operational temperature: -40 to +85 °C
- ASI4U-E operational temperature: -25 to +105 °C
- RoHS-conformant package: SSOP28 (ASI4U and ASI4U-F) / SOP28 (ASI4U-E)

Available Support

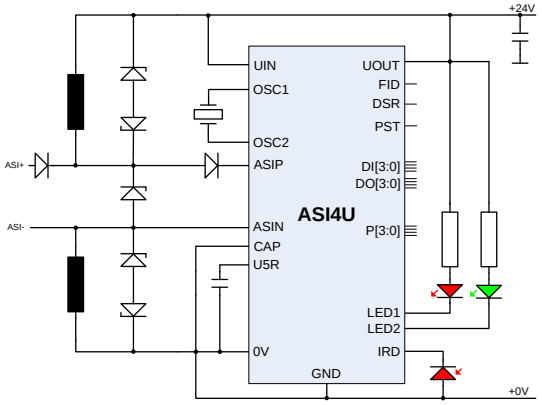
- IDT AS-Interface Programmer Kit V2.0
- IDT ASI4U Evaluation Board V2.0

ASI4U Basic Application Circuits

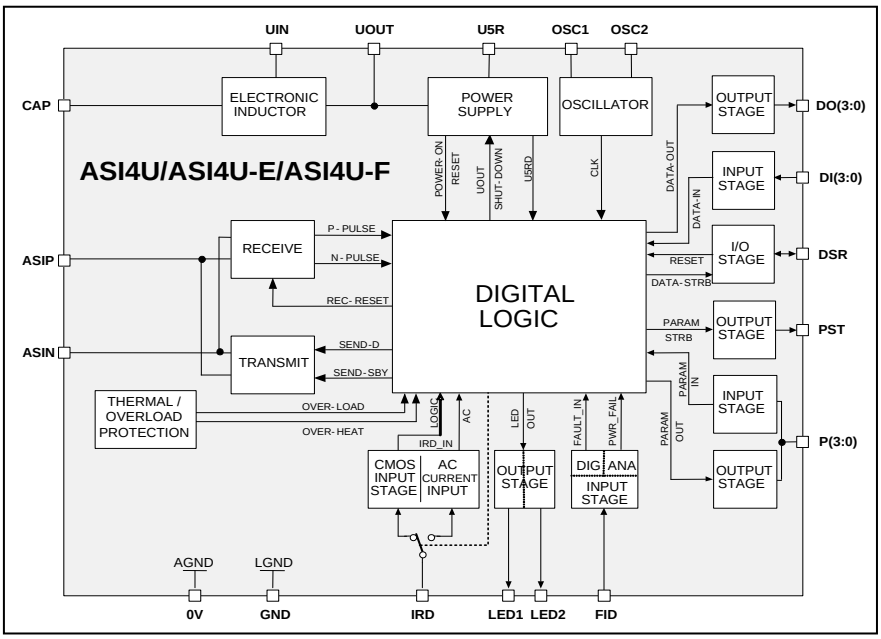
Standard Application



Extended Power Application with IR-Addressing Option



ASI4U Block Diagram



Typical Applications

- AS-i Master Modules
- AS-i Slave Modules
- AS-i Safety Modules

Ordering Information

Ordering Code	Type	Package	T_a [°C]	RoHS Conform	Packaging	Minimum Order
ASI4UE-G1-ST	Standard	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-SR	Standard	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-G1-SR-7	Standard	SSOP28	-25 to 85	Y	Tape & Reel 7” (500 parts/reel)	500
ASI4UE-G1-MT	Master	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-MR	Master	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-E-G1-ST	Standard	SOP28	-25 to 105	Y	Tube (27 parts/tube)	270
ASI4UE-E-G1-SR	Standard	SOP28	-25 to 105	Y	Tape & Reel (1000 parts/reel)	1000
ASI4UE-F-G1-ST	Standard	SSOP28	-40 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-F-G1-SR	Standard	SSOP28	-40 to 85	Y	Tape & Reel (1500 parts/reel)	1500

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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1 Important Safety Advice

Important Safety Notice: This IDT product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high-reliability applications, such as military, medical life-support, or life-sustaining equipment, are specifically not recommended without additional mutually agreed upon processing by IDT for such applications.

1.1. AS-i-Safety Applications

The ASI4U/ASI4U-E/ASI4U-F is designed to allow replacement of IDT's A²SI ICs in existing board layouts and applications (also see section 1.2 for important restrictions). However, since the ASI4U/ASI4U-E/ASI4U-F provides additional data preprocessing functions at the data input channel, the fault reaction time of an AS-i Safety module could increase by 40ms if some of the new features become activated by intention, by accident, or hardware fault.

IDT strongly recommends the use of the Safety Mode feature of the ASI4U/ASI4U-E/ASI4U-F if it is replacing the A²SI in existing ASI-Safety designs. The same fault reaction times as with the A²SI are guaranteed only in this Safety Mode. For compatibility with the modified data input routing in Safety Mode, the user must adapt the safety code table stored in the external microcontroller. Only safety code sequences that contain the value **1110** are permitted.

If the IC is operated in Safety Mode, the user must ensure that the Synchronous Data I/O Mode as well as the data input filters remain disabled by appropriate EEPROM configuration.

Application of the ASI4U/ASI4U-E/ASI4U-F in Standard Mode (no Safety Mode enabled) for AS-i Safety products is possible if an additional fault reaction time of 40ms is taken into account.

The user must also adhere to the additional security advice provided in *Production and Repair of AS-i Safety Slaves*, which is available on the IDT web page www.IDT.com (see section 8).

1.2. Repair of ASI-Safety Modules

Important: If an A²SI-based ASI-Safety module must be repaired, replacing the A²SI IC with the newer ASI4U/ASI4U-E/ASI4U-F is **explicitly prohibited**. This is to prevent safety-relevant deviations of module properties that can result from the different data input paths and the possible increase in fault reaction time discussed in section 1.1.

The user must also adhere to the additional security advice provided in *Production and Repair of AS-i Safety Slaves*, which is available on the IDT web page www.IDT.com.

2 General Device Specifications

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 2.1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to conditions rated as the absolute maximum for extended periods might affect device reliability.

2.1. Absolute Maximum Ratings (Non-Operating)

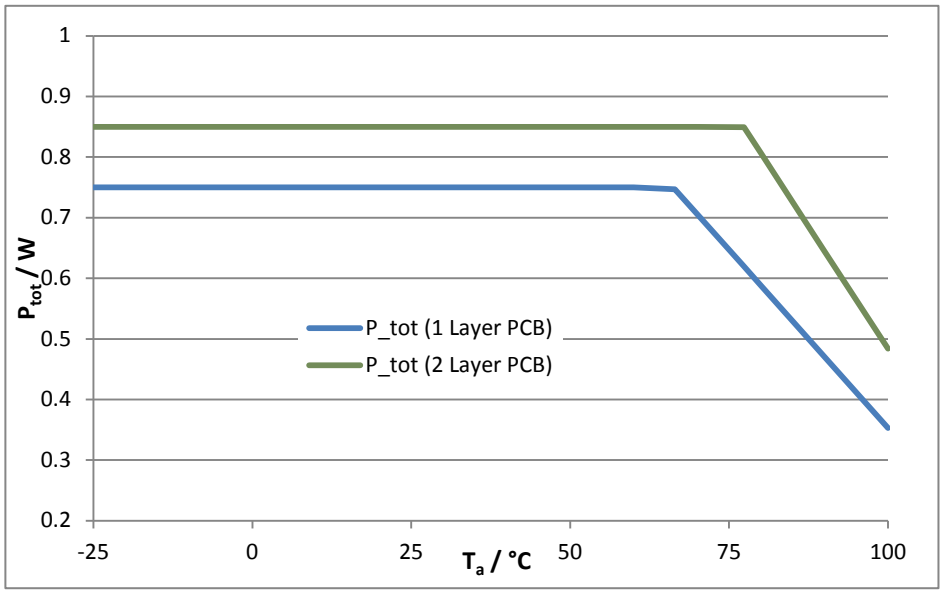
Table 2.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Voltage reference	V_{0V}, V_{GND}		0	0	V
Voltage difference between ASIP and ASIN (V_{ASIP} - V_{ASIN}) [1)]	$V_{ASIP-ASIN}$		-0.3	40	V
Pulse voltage between ASIP and ASIN (V_{ASIP} - V_{ASIN})	$V_{ASIP-ASIN_P}$	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Pulse voltage between ASIP and 0V (V_{ASIP} – V_{0V}) [2)]	V_{ASIP}	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Voltage between ASIN and 0V (V_{ASIN} – V_{0V}) [2)]	V_{ASIN}		-6.0	6.0	V
Power supply input voltage	V_{UIN}		-0.3	40	V
Pulse voltage at power supply input	V_{UIN_P}	Pulse width ≤ 50µs Repetition rate ≤ 0.5Hz	-0.3	50	V
Voltage at DI3, DI2, DI1, DI0, DO3, DO2, DO1, DO0, P3, P2, P1, P0, DSR, PST, LED1, LED2, FID, IRD, and UOUT pins	$V_{inputs1}$		-0.3	V_{UOUT} + 0.3	V
Voltage at OSC1, OSC2, CAP, and U5R pins	$V_{inputs2}$		-0.3	7	V
Input current into any pin except supply pins	I_{in}	Latch-up resistance, reference to pin 0V	-50	50	mA
Humidity – non-condensing	H	Level 4 according to JEDEC-020D standard			
Electrostatic discharge – Human Body Model (HBM1)	V_{HBM1}	C = 100pF charged to V_{HBM1} with resistor R = 1.5kΩ in series	3500		V
Electrostatic discharge – Human Body Model (HBM2)	V_{HBM2}	C = 100pF charged to V_{HBM2} with resistor R = 1.5kΩ in series	2000		V

Parameter	Symbol	Conditions	Min	Max	Unit
Electrostatic discharge – Equipment Discharge Model (EDM)	V_{EDM}	C = 200pF charged to V_{EDM} with no resistor in series	400		V
Storage temperature	T_{STG}		-55	125	°C
Soldering temperature Sn/Pb	T_{Lead}	JEDEC-J-STD-020D		240	°C
Soldering temperature 100%Sn	T_{Lead}	JEDEC-J-STD-020D		260	°C
Total power dissipation [6)]	P_{tot}			0.85	W
Thermal resistance of SSOP 28 package (ASI4U and ASI4U-F)	R_{thj}	Single layer board P_{tot} = 0.5W Air velocity = 0m/s at maximum value Air velocity = 2.5m/s at minimum value	40	80	K/W
Thermal resistance of SOP 28 package (ASI4U-E)			60	80	K/W

1) Reverse polarity protection must be performed externally.
2) VASIP-ASIN and VASIP-ASIN_P must not be exceeded.
3) Valid for ASIP-ASIN only.
4) Valid for all pins except ASIP-ASIN.
5) Valid for ASIP-ASIN only.
6) At the maximum operating temperature, the maximum total power dissipation allowed depends on additional the thermal resistance from the package to the ambient air and on the operational ambient temperature as shown in Figure 2.1

Figure 2.1 $P_{tot} = f(T_a)$



2.2. Operating Conditions

Table 2.2 Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX.	UNIT
Positive supply voltage for IC operation [1)]	V_{UIN}	DC parameter: $V_{UINmin} = V_{UOUTmin} + V_{DROPmax}$ $V_{UINmax} = V_{UOUTmax} + V_{DROPmin}$	16	33.1	V
Negative supply voltage	V_{0V}, V_{GND}		0	0	V
DC voltage at ASIP [2)]	V_{ASIP}	Relative to V_{0V}	16	33.1	V
DC voltage at ASIN [2)]	V_{ASIN}	Relative to V_{0V}	-4	4	V
Operating current	I_{UIN}	V_{UIN} = 30V f_c = 8.000 MHz; no load at any pin; transmitter turned off; digital State Machine is in idle state		6	mA
Maximum output sink current at DO0, DO1, DO2, DO3, and DSR pins	I_{CL1}			10	mA
Maximum output sink current at P0, P1, P2, P3, and PST pins	I_{CL2}			10	mA
Ambient temperature range, operating range	T_a	ASI4U	-25	85	°C
		ASI4U-E	-25	105	°C
		ASI4U-F	-40	85	°C

1) Below V_{UINmin}, the power supply block might not be able to provide the specified output currents at UOUT and U5R.
2) Outside the maximum and minimum limits, the send current shape and send current amplitude cannot be guaranteed.

Table 2.3 Crystal Frequency

PARAMETER	SYMBOL	CONDITIONS	NOMINAL	UNIT
Crystal frequency [1)]	f_c		8.000/16.000	MHz

1) The IC automatically detects whether the crystal frequency is 8.000MHz or 16.000MHz and controls the internal clock circuit accordingly. The frequency detection is locked as soon as one AS-i telegram has been correctly received **at any input channel**. It can be reset by a power-on reset only.
Note: In Slave Mode, the locking occurs if a Master Call has been received. In the Master, Repeater, or Monitor Modes, a Master Call or a Slave Response that has been received on any input channel triggers the frequency locking.

The ASI4U/ASI4U-E/ASI4U-F supports an integrated clock watchdog. If no crystal or clock oscillation is recognized for 150µs, the IC generates a RESET event until clock oscillation is available. More detailed oscillator pin definitions can be found in section 4.10.

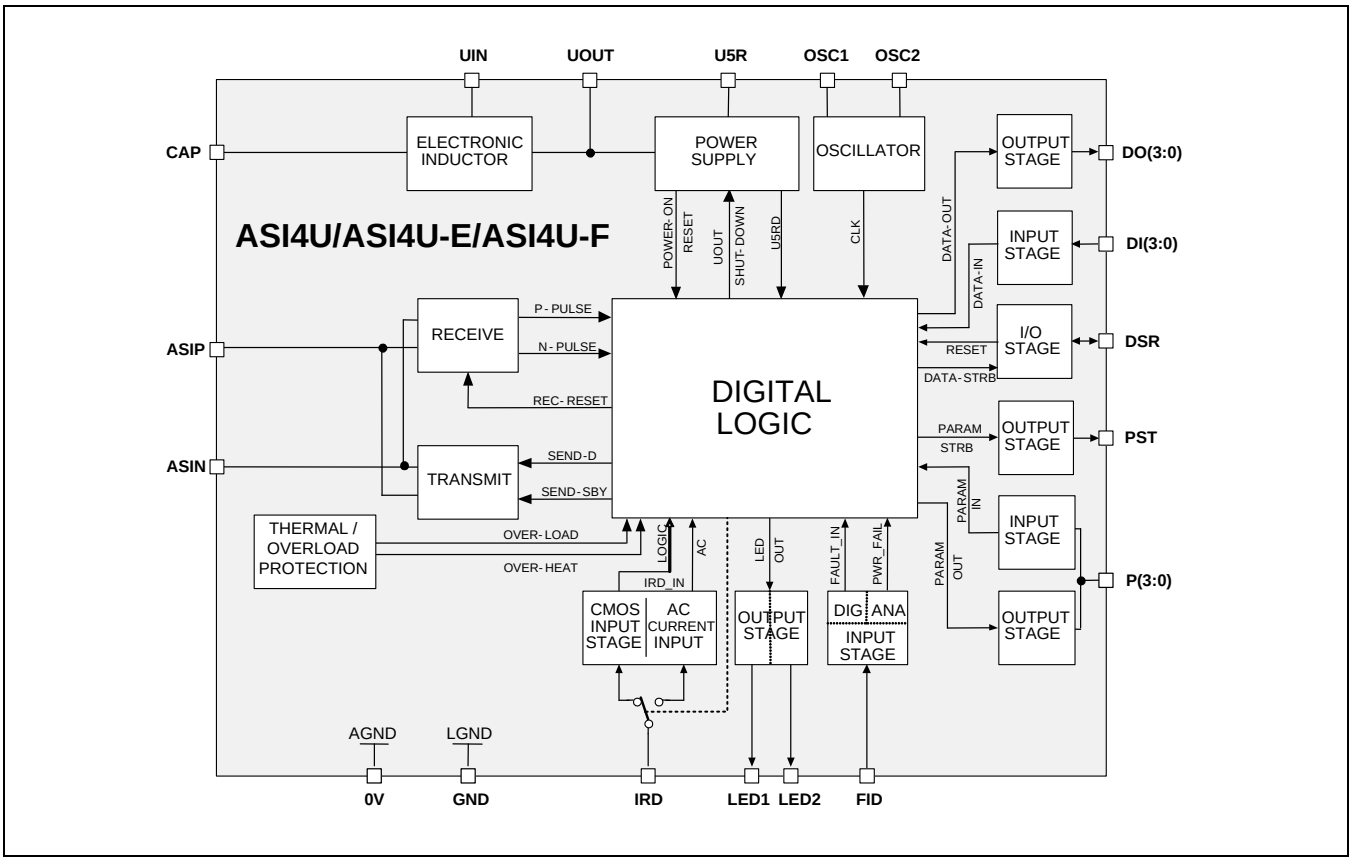
2.3. Quality Standards

The quality of the ASI4U/ASI4U-E/ASI4U-F is ensured according to the IDT quality standards. Functional device parameters are valid for device operating conditions specified in section 2.2. Unless otherwise stated, production device tests are performed at T_a = +25°C within the recommended ranges of (V_{ASIP} - V_{ASIN}) and (V_{IN} - V_{0V}). Additional sample base testing is done at +85°C and -25°C (-40°C for the ASI4U-F).

3 Basic Functional Description

3.1. Functional Block Diagram

Figure 3.1 ASI4U Functional Block Diagram



Following device functions are associated with the different blocks of the IC:

RECEIVE The RECEIVE block converts the analog telegram waveform from the AS-i bus to a digital pulse-coded signal that can be processed further by a digital UART circuit.

The RECEIVE block is directly connected to the ASIP and ASIN pins, which connect to the AS-i line. It converts the differential AS-i telegram to a single-ended signal and removes the DC offset by high-pass filtering. To adapt quickly to changing signal amplitudes in telegrams from different network users, the amplitude of the first telegram pulse is measured by a 3-bit flash ADC and the threshold of a positive and a negative comparator is set accordingly to about 50% of the measured level. The comparators generate the P-pulse and N-pulse signals.

TRANSMIT The TRANSMIT block transforms a digital response signal to a correctly shaped send current signal that is applied to the AS-i bus. Due to the inductive network behavior of the network, the changing send current induces voltage pulses on the network line that overlay the DC operating voltage. The voltage pulses must have $\sin^2$-wave shapes; therefore the send current shape must follow the integral of the $\sin^2$-wave function.

DIGITAL LOGIC The DIGITAL LOGIC block contains the UART, Main State Machine, EEPROM memory and other control logic. EEPROM write access and other I/O operations of the Main State Machine are supported in Slave Mode only (see description of general IC operational modes below). In Master Mode, the IC is basically equivalent to a physical layer transceiver.

If Slave Mode is activated, the UART demodulates the received telegrams, verifies telegram syntax and timing, and controls a register interface to the Main State Machine. After reception of a correct telegram, the UART generates appropriate Receive Strobe signals that tell the Main State Machine to start further processing. The Main State Machine decodes the telegram information and starts respective I/O processes or EEPROM access. A second register interface is used to send data back to the UART for construction of a telegram response. The UART modulates the response data into a Manchester-II-coded bit stream that is used to control the TRANSMIT unit.

ELECTRONIC INDUCTOR The ELECTRONIC INDUCTOR block is basically a gyrator circuit. It provides an inductive behavior between the IC's UIN and UOUT pins while the inductance is controlled by the capacitor on the CAP pin. The inductor decouples the power regulator of the IC as well as the external load circuit from the AS-i bus, and this prevents cross talk or switching noise from disturbing the telegram communication on the bus.

The *AS-Interface Complete Specification V3.0* describes the input impedance behavior of a slave module by an equivalent circuit that consists of a resistance (R), an inductance (L), and a capacitance (C) in parallel. For example, a slave module in Extended Address Mode must have R > 13.5kΩ, L > 13.5mH and C < 50pF. The electronic inductor of the ASI4U/ASI4U-E/ASI4U-F delivers values that are well within the required ranges for output currents up to 55mA. More detailed parameters can be found in section 4.18.2.

The electronic inductor requires an external capacitor of at least 10µF at the UOUT pin for stability.

POWER SUPPLY The POWER SUPPLY block consists of a bandgap-referenced 5V regulator and other reverence voltage and bias current generators for internal use. The 5V regulator requires an external capacitor at pin U5R of at least 1µF for stability. It can source up to 4mA for external use; however, the power dissipation and the resulting device heating become a major concern if too much current is drawn from the regulator.

OSCILLATOR The OSCILLATOR block supports direct connection to 8.000 MHz or 16.000 MHz crystals with a dedicated load capacity of 12pF and parasitic pin capacities of up to 8pF. The IC automatically detects the oscillation frequency of the connected crystal and controls the internal clock generator circuit accordingly.

After power-on reset, the IC is set to 16.000 MHz operation by default. After approximately 200µs, it will either switch to 8.000 MHz operation or remain in the 16.000 MHz mode. The frequency detection is active until the first AS-i telegram has been successfully received in order to ensure that the IC has found the correct clock frequency setting. The detection result is locked thereafter to increase resistance against burst or other interferences.

The oscillator unit also contains a clock watchdog circuit that can generate an unconditional IC reset if there has been no clock oscillation for more than approximately 20µs. This is to prevent the IC from unpredictable behavior if a clock signal is no longer available.

THERMAL/OVERLOAD PROTECTION The IC is self-protected against overheating and short-circuiting of the UOUT pin toward IC ground.

If the silicon die temperature rises above approximately 140°C for more than 2 seconds, the IC detects overheating, switches off the electronic inductor, performs an IC reset, and sets all analog blocks to power down mode. Although the 5V regulator is turned off in this state, there will still remain a voltage of approximately 3V to 3.5V available at U5R that is derived from the internal start circuitry. The overheating protection state can only be de-activated by power-cycling the AS-i voltage.

Short-circuiting the UOUT pin toward IC ground causes the same IC behavior as overheating.

IRD CMOS / AC CURRENT INPUT The IRD pin is the input for the additional addressing channel in Slave Mode (see section 3.2 for a description of general IC operational modes) or the direct AS-i transmitter input in Master Mode. In Slave Mode, the IRD pin can be operated either in CMOS Mode or AC Current Input Mode. The latter is provided for direct connection of a photodiode. More detailed information can be found in section 4.3.

FID DIGITAL / ANALOG STAGE The FID pin can be set to the Digital CMOS Mode or Analog Voltage Input Mode. In Slave Mode, it is set to CMOS operation; in Master Mode, it works in Analog Mode and functions as the input for the power fail comparator.

INPUT STAGE All digital inputs, except the oscillator pins, have high voltage capabilities and partial Schmitt trigger and pull-up features. For more details, see section 4.4.

OUTPUT STAGE All digital output stages, except for the oscillator pins, have high voltage capabilities and are implemented as NMOS open-drain buffers. Each pin can sink up to 10mA of current.

3.2. General Operational Modes

The ASI4U/ ASI4U-E/ASI4U-F provides two main operational modes and two additional sub-operational modes. The two main operation modes are Slave Mode and Master Mode. Sub-operation modes are Repeater Mode and Monitor Mode. The latter were derived from Master Mode for providing different output signals at the Parameter Port.

The active operational mode is selected by programming the *Master_Mode* and *Repeater_Mode* flags in the “Firmware Area” block of the EEPROM (also see Table 3.4). The EEPROM is read at every initialization of the IC. Online mode switching is not provided. Table 3.1 gives the bit configurations for the operational modes.

Table 3.1 Assignment of Operational Modes

SELECTED OPERATIONAL MODE	MASTER MODE FLAG	REPEATER MODE FLAG
Slave Mode	0	0
Master Mode	1	0
Repeater Mode	1	1
Monitor Mode	0	1

In Slave Mode, the IC operates as a full-feature AS-i slave IC according to the *AS-Interface Complete Specification V3.0*.

In Master Mode, the IC translates a digital output signal from the master control logic (e.g., a programmable logic controller or microcontroller) to a correctly shaped, analog AS-i pulse sequence and vice versa. Every AS-i telegram received is checked for consistency with the AS-Interface communication protocol specifications, and if no errors were found, an appropriate Receive Strobe signal is generated.

Master Mode and Monitor Mode differ in the kind of telegrams signaled. In Master Mode, a single Receive Strobe signal is provided validating every correctly received Slave Response; in Monitor Mode, two different Receive Strobe signals are available indicating every correctly received Master and Slave telegram separately. The Monitor Mode is intended for use in intelligent slaves and bus monitors that provide their own telegram decoding mechanisms but do not check for correct telegram timing or syntax.

The Repeater Mode is specifically provided for AS-i bus repeater applications.

3.3. Slave Mode

The Slave Mode is the most complex operational mode of the IC. The IC supports all mandatory AS-i Slave functions and also a variety of additional features that make AS-i slave module design very easy and flexible.

3.3.1. AS-Interface Communication Channel

In Slave Mode, the ASI4U can work on two different communication channels: the AS-i channel and the IRD channel. The AS-i channel is directly connected to the AS-i bus via the ASIP and ASIN pins. A receiver and a transmitter unit are connected in parallel to the pins. This allows fully bi-directional communication through ASIP and ASIN.

The ASI4U/ASI4U-E/ASI4U-F is the first IC that supports floating operation of the AS-i receiver and transmitter (within specified limits) relative to IC ground. Previously, the ASIN pin always had to be on the same potential as the IC ground (see Figure 3.2 for an example), preventing full symmetrical input circuits with external coils. Figure 3.3 illustrates the new enhanced functionality. The relation Z1/Z2 is a measure of the symmetry of the AS-i module input relative to machine ground. The application in Figure 3.3 is more symmetrical since Z1 and Z2 are more equal than in the conventional solution. Note: This is not a complete application circuit.

Figure 3.2 Conventional Application for AS-i IC with One External Coil

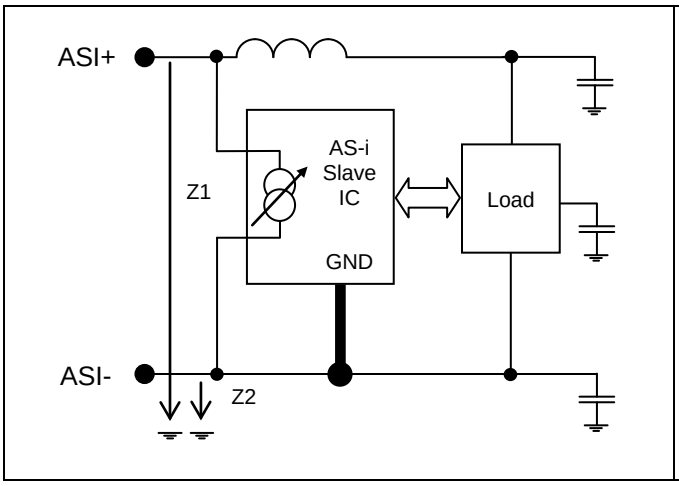
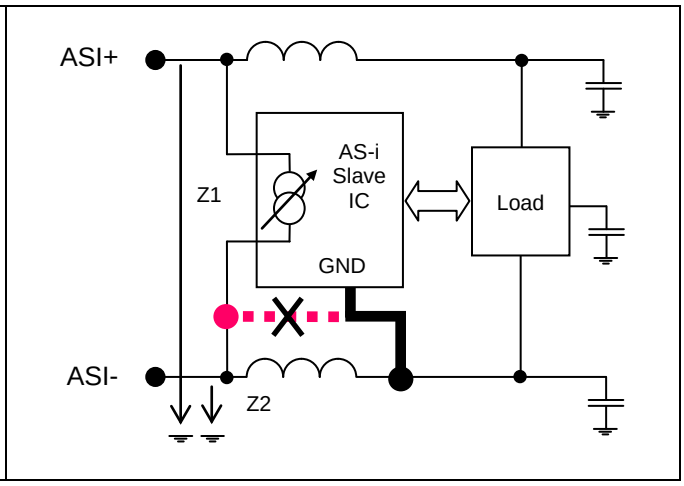


Figure 3.3 Application for AS-i IC with Two External Coils



3.3.2. IRD Communication Channel

In addition to the AS-Interface communication channel, the ASI4U can also operate on a second input channel: the IRD Input Channel or Addressing Channel. In this mode, the IRD pin is the input for an AS-i signal in Manchester-II-coded format. The signal can be either an AC-current signal generated by a photodiode or a 5V-CMOS signal. The IC automatically detects the type of the signal and switches the input path accordingly.

The output pin in IRD Communication Mode is LED1. It transmits the slave response as an inverted Manchester-II-coded AS-i signal. A red LED connected to LED1 can form the response transmitter in an optical communication system, or LED1 can be directly connected to external circuitry.

Activation of the IRD communication channel is achieved by a transmission referred to as a “Magic Sequence” that is sent in advance of the desired communication. The construction of a Magic Sequence is described in detail in section 4.3. The IRD communication mode is deactivated by an IC reset, except in a special case described in section 4.3.

3.3.3. Parameter Port Pins

The ASI4U features a 4-bit-wide parameter port and a related parameter strobe signal on the PST pin. There is a defined phase relation between a parameter output event, the parameter input sampling, and the activation of the PST signal, so it can be used to trigger external logic or a microcontroller to process the received parameter data or to provide new input data for the AS-i slave response.

Version 3.0 of the *AS-Interface Complete Specification* defines a bidirectional mode for parameter data. The ASI4U/ASI4U-E/ASI4U-F supports this feature, which can be activated by special EEPROM setting.

See section 4.6 for further details.

3.3.4. Data Port Pins

An important feature of the ASI4U/ASI4U-E/ASI4U-F is the 8-bit wide data port that consists of a 4-bit-wide input section and a 4-bit-wide output section. The input and output sections work independently from each other allowing a maximum of 8 devices (4 input and 4 output devices) to be connected to the ASI4U/ASI4U-E/ASI4U-F. For special applications (compatibility), the Multiplex Mode can be activated, which limits the output activation to a specific time frame. With this feature, a 4-bit wide bi-directional data I/O port can be achieved by external connection of the corresponding data input and output pins.

The data port is accompanied by the data strobe signal on the DSR pin. There is a defined phase relation between a data output event, the input data sampling, and the activation of the DSR signal, so it can be used to trigger external logic or a microcontroller to process the received data or to provide new input data for the AS-i slave response. See section 4.7 for further details.

3.3.5. Data Input Inversion

By default, the logic signal (HIGH/LOW) that is present at the data input pins during the input sampling phase is transferred without modification to the send register, which is interfaced by the UART so that the signal directly becomes part of the slave response.

Some applications function with inverted logic levels. To avoid additional external inverters, the input signal can be inverted by the ASI4U/ASI4U-E/ASI4U-F before the signal is transferred to the send register. The inversion of the input signals can either be done bit-selectively or jointly for all data input pins. See section 4.7.2.

3.3.6. Data Input Filtering

To prevent input signal bouncing being transferred to the AS-Interface Master, the data input signals can be digitally filtered. Filter times can be configured in seven steps from 128µs up to 8.192ms. When the AS-i Cycle Mode is activated, the filter time is determined by the actual AS-i cycle time. For more detailed information, refer to section 4.7.2.

The filter function can be enabled bit-selectively. Activation of the filters can be done jointly either by EEPROM configuration or by the logic state of the parameter port pin P2. See section 4.7.2.

3.3.7. Fixed-Data Output Driving

The fixed-data output-driving feature is intended to facilitate board-level design for similar products that do not require the full data output port width. The user can select one or more bits from the data output port to be driven by a distinct logic level instead of by the data that was sent by the master. The distinct output data is stored in the EEPROM and can be set during final module configuration. With this feature, it is possible to signal the actual IC profile to external circuitry and to allow reuse of some types of board designs for different product applications.

See section 4.7.3.

3.3.8. Synchronous Data I/O Mode

Version 3.0 of the *AS-Interface Complete Specification* defines a synchronous data I/O feature that allows a number of slaves in the network to switch their outputs at the same time and to have their inputs sampled jointly. This feature is especially useful if more than 4-bit wide data are to be provided synchronously to an application.

The synchronization point is defined as the data exchange event of the slave with the lowest address in the network. This definition relies on the cyclical slave polling with incrementing slave addresses each cycle, which is one of the basic communication principles of AS-i. The IC always monitors the data communication and detects the change from a higher to a lower slave address. If such a change has been recognized, the IC assumes that the slave with the lower address has the lowest address in the network.

There are some special procedures that become active during the start of synchronous I/O mode operation and if more than three consecutive telegrams have been sent to the same slave address. This is described in more detail in section 4.7.4.

3.3.9. 4 Input / 4 Output Processing in Extended Address Mode

Version 3.0 of the *AS-Interface Complete Specification* also supports 4-bit wide output data in Extended Address Mode. Up to *AS-Interface Complete Specification V2.11*, it was only possible to send three data output bits from the master to the slave in Extended Address Mode because telegram bit I3 was used to select between the A and B slave types for extended slave addressing (up to 62 slaves per network). In Normal Address Mode, bit I3 carries output data for pin D3.

The version 3.0 definition introduces a multiplexed data transfer so that all 4-bits of the data output port can be used again. A first AS-i cycle transfers the data for a 2-bit output nibble only, while the second AS-i cycle transfers the data for the contrary 2-bit nibble. Nibble selection is done by the remaining third bit. To ensure continuous alternation of bit information I2 and thus continued data transfer to both nibbles, a special watchdog was implemented that observes the state of the I2 bit. The watchdog can be activated or deactivated by EERPOM setting. It provides a watchdog filter time of about 327ms.

The multiplexed transfer increases the refresh time per output by a factor of two; however, some applications can tolerate this increase for the benefit of less external circuitry and better slave address efficiency. The sampling cycle of the data inputs remains unchanged since the meaning of the I3 bit was not changed in the slave response with the definition of the Extended Address Mode.

For more detailed information, see section 4.7.5.

3.3.10. AS-i Safety Mode

The enhanced data input features described in previous sections require additional registers in the data input path that store the input values for a specific time before they transfer them to the AS-i transmitter. This causes a time delay in the input path that could lead to a delayed “turn off” event if the registers are activated by intention or unintentionally in AS-i Safety applications.

To safely exclude an activation of the enhanced data I/O features in AS-i Safety applications, the IC provides a special Safety Mode that is strongly recommended for AS-i Safety communication purposes. See section 4.7.6 for further details.

3.3.11. Enhanced LED Status Indication

ASI4U now supports enhanced status indication by two LED outputs. A special mode for direct application of dual LEDs and the respective different signaling modes are also implemented. Compared to the A²SI, the former U5RD pin was reassigned as LED2 pin. Thus, compatibility to existing A²SI board layouts is still guaranteed. However, it will require keeping the LED2 pin disabled (default state at delivery) in order to avoid short-circuiting U5R to ground. More detailed information on the different signaling schemes and their activation can be found in section 4.9.

3.3.12. Communication Monitor/Watchdog

Data and parameter communication are continuously observed by a communication monitor. If neither *Data_Exchange* nor *Write_Parameter* calls were addressed to and received by the IC within a time frame of approximately 41ms, a *No Data/Parameter Exchange* status is detected and signaled at LED1.

If the respective flags are set in the EEPROM, the communication monitor can also act as communication watchdog that initiates a complete IC reset after expiration of the watchdog timer. The watchdog mode can also be activated and deactivated by a signal at parameter port pin P0. See section 4.15 for more detailed information.

3.3.13. Write Protection of *ID_Code_Extension_1*

As defined in the *AS-Interface Complete Specification V3.0,* the ASI4U/ASI4U-E/ASI4U-F also supports write protection for *ID_Code_Extension_1*. This feature allows the activation of new manufacturer-protected slave profiles and is enabled by an EEPROM setting. For more details, see section 4.17.

3.3.14. Summary of Master Calls

Table 3.2 and the diagram on the following page show the complete set of Master calls that are decoded by the ASI4U/ASI4U-E/ASI4U-F in Slave Mode. The "Enter Program Mode" call is intended for programming of the IC by the slave manufacturer only. It becomes deactivated as soon as the *Program_Mode_Disable* flag is set in the “Firmware Area” block of the EEPROM.

Important note regarding full compliance with the *AS-Interface Complete Specification*: In order to achieve full compliance to the *AS-Interface Complete Specification*, the *Program_Mode_Disable* flag must be set by the manufacturer of AS-i slave modules during the final manufacturing and configuration process and before an AS-i slave device is delivered to field application users.

Table 3.2 ASI4U Master Calls and Related Slave Responses

		Master Request														Slave Response						
Instruction	**MNE**	**ST**	**CB**	**A4**	**A3**	**A2**	**A1**	**A0**	**I4**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**	**SB**	**I3**	**I2**	**I1**	**I0**	**PB**	**EB**
Data Exchange	DEXG	0	0	A4	A3	A2	A1	A0	0	D3 ~Sel	D2	D1	D0	PB	1	0	D3 E3	D2 E2	D1 E1	D0 E0	PB	1
Write Parameter	WPAR	0	0	A4	A3	A2	A1	A0	1	P3 ~Sel	P2	P1	P0	PB	1	0	P3 I3	P2 I2	P1 I1	P0 I0	PB	1
Address Assignment	ADRA	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	PB	1	0	0	1	1	0	0	1
Write Extented ID Code_1	WID1	0	1	0	0	0	0	0	0	ID3	ID2	ID1	ID0	PB	1	0	0	0	0	0	0	1
Delete Address	DELA	0	1	A4	A3	A2	A1	A0	0	0 Sel	0	0	0	PB	1	0	0	0	0	0	0	1
Reset Slave	RES	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	0	0	PB	1	0	0	1	1	0	0	1
Read IO Configuration	RDIO	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	0	PB	1	0	IO3	IO2	IO1	IO0	PB	1
Read ID Code	RDID	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	0	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_1	RID1	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	0	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read ID Code_2	RID2	0	1	A4	A3	A2	A1	A0	1	0 Sel	0	1	1	PB	1	0	ID3	ID2	ID1	ID0	PB	1
Read Status	RDST	0	1	A4	A3	A2	A1	A0	1	1 ~Sel	1	1	0	PB	1	0	S3	S2	S1	S0	PB	1
Broadcast (Reset)	BR01	0	1	1	1	1	1	1	1	0	1	0	1	1	1	--- no slave response ---						
Enter Program Mode	PRGM	0	1	0	0	0	0	0	1	1	1	0	1	1	1	--- no slave response ---						

Note: In Extended Address Mode, the "Select Bit" defines whether the A-Slave or B-Slave is being addressed. Depending on the type of master call, bit I3 carries the select bit information (Sel = A-Slave) or the inverted select bit information (~Sel = B-Slave).

B-Slave with Profile 0.A (green shaded)	ASI Master Request (black/green)	ASI Slave Response (blue)	No Slave Response (blue shaded)

ADR != 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3	I3=Sel	(Slave Address != 0) AND (Progam Mode not activated)							
000	Sel=0	Data_Exchange /Sel D2 D1 D0							
001	Sel=1	Data_Exchange D3 D2 D1 D0			D3 D2 D1 D0				
010	Sel=0	Write_Parameter /Sel P2 P1 P0							
011	Sel=1	Write_Parameter P3 P2 P1 P0			P3 P2 P1 P0				
100	Sel=0	Delete_Addr x0							
101	Sel=1	Delete_Addr x0							
110	Sel=0	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	
111	Sel=1	Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6		Rd_Status <S3:S0>	

ADR == 0	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		(Slave Address == 0) AND (Progam Mode not activated)							
000									
001				Address_Assignment A4 A3 A2 A1 A0					
010					0x6				
011									
100				Write_Var_Ext_Code1 ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>		Broadcast		
111						Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	

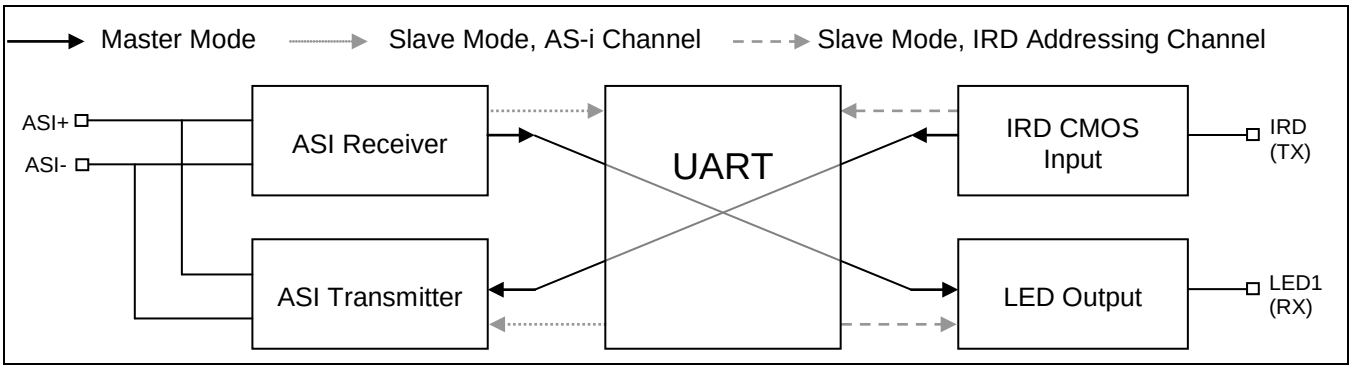
	I2 I1 I0	000	001	010	011	100	101	110	111
CB I4 I3		Progam Mode activated							
000									
001		Data_Exchange - - - -			I3 I2 I1 I0	(EEPROM READ ACCESS)			
010									
011		Write_Parameter I3 I2 I1 I0			I3 I2 I1 I0	(EEPROM WRITE ACCESS)			
100				Write_Var_ID_Code ID3 ID2 ID1 ID0					
101					0x0				
110		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	Broadcast	Rd_Status <S3:S0>	reserved
111		Rd_IO_Cfg <I3:I0>	Read_ID <I3:I0>	Read_ID_1<I3:I0>	Read_ID_2 <I3:I0>	Reset_Slave 0x6	EnterPmode	Rd_Status <S3:S0>	reserved

3.4. Master Mode

Master Mode and the related Repeater and Monitor Modes differ completely in their functional properties from the Slave Mode. While the IC can autonomously perform different tasks in Slave Mode, it will only act as a physical layer transceiver in the Master, Repeater, and Monitor Modes.

The basic property of these modes is a modulation/demodulation of AS-i signals to Manchester-II code and vice versa. The following figure shows the different data path configurations.

Figure 3.4 Data Path in the Master, Repeater, and Monitor Modes



Master Mode, Repeater Mode, and Monitor Mode differ from each other in the kind of signals that are available at the data I/O and parameter port pins of the IC. The signal assignments in Table 3.3 are provided:

Table 3.3 Signal Assignments for Data I/O and Parameter Port Pins

PIN	MASTER MODE	REPEATER MODE	MONITOR MODE
P0	Receive Clock	Hi-Z	Receive Clock
P1	Power Fail	Hi-Z	Power Fail
P2	Receive Strobe – Slave Telegram	Hi-Z	Receive Strobe – Slave Telegram
P3	Hi-Z	Hi-Z	Receive Strobe – Master Telegram
DI0	Inverting of IRD input signal. If these two are on different levels, the IRD input signal is inverted before further processing; otherwise it is directly forwarded to the UART.		
DI1			
DI2	Inverting of LED output signal. If these two inputs are on different levels, the LED output signal is inverted after processing; otherwise it is directly forwarded to the LED1 output.		
DI3			
DO0	Hi-Z	Hi-Z	Pulse Code Error
DO1	Hi-Z	Hi-Z	No Information Error
DO2	Hi-Z	Hi-Z	Parity Bit Error
DO3	Hi-Z	Hi-Z	Manchester-II-Code Error at IRD Input

More detailed signal descriptions can be found in sections 4.6, 4.7, and 4.12.

3.5. EEPROM

The ASI4U provides an on-chip EEPROM with typical write times of 12.5ms and read times of 110ns. For security reasons, the memory area is structured in two independent data blocks and a single bit *Security* flag.

The data blocks are named the “User Area” and “Firmware Area.” The Firmware Area block contains all manufacturing-related configuration data (e.g., selection of operational modes, ID codes). It can be protected against undesired data modification by setting the *Program_Mode_Disable* flag to 1.

The User Area contains only data that is relevant for changes in the final application (i.e., field installation of the slave module). The environment, where modifications of the user data might become necessary, can sometimes be rough and unpredictable. In order to ensure a write access cannot result in an undetected corruption of EEPROM data, additional security is provided when programming the User Area.

Any write access to the User Area (by the calls *Address_Assignment* or *Write_ID_Code1*) is accompanied by two write steps to the *Security* flag, one before and one after the actual modification of user data.

The following procedure is executed when writing to the *User Area* of the EEPROM:

1. The *Security* flag is programmed to 1.
2. The content of the *Security* flag is read back, verifying it was programmed to 1.
3. The user data is modified.
4. A read back of the written data is performed.
5. If the read back has proven successful programming of the user data, the *Security* flag is programmed back to 0.
6. The content of the *Security* flag is read back, verifying it was programmed to 0.

In addition to a read out of the data areas, the *Security* flag of the EEPROM is also read and evaluated during IC initialization. If the value of the *Security* flag equals 1 (e.g., due to an undesired interruption of a User Area write access), the entire User Area data is treated as corrupted and the Slave Address is set to 0_{HEX} in the corresponding volatile shadow registers during initialization. Then the programming of the User Area data can be repeated.

Table 3.4 EEPROM Contents

User Area Firmware Area

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
0	0 to 3	*A0 to A3*	Slave address low nibble
1	0	*A4*	Slave address high nibble
2	0 to 2	*ID1_Bit0 to ID1_Bit2*	*ID_Code_Extension_1*
2	3	*ID1_Bit3*	*ID_Code_Extension_1*, A/B slave selection in extended address mode
3 to 7			Not implemented
8	0 to 3	*ID_Bit0 to ID_Bit3*	*ID_Code*
9	0 to 3	*ID2_Bit0 to ID2_Bit3*	*ID_Code_Extension_2*
A	0 to 3	*IO_Bit0 to IO_Bit3*	*IO_Code*

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
B	0	*Multiplex_Data*	Multiplexed bi-directional Data Port mode
	1	*Multiplex_Parameter*	Multiplexed bi-directional Parameter Port mode
	2	*P0_Watchdog_Activation*	Watchdog can be activated/deactivated by the logic value at parameter pin P0. *Watchdog_Active* must **not** be set.
	3	*Watchdog_Active*	Communication watchdog is continuously activated.
C	0	*Master_Mode*	If set, Firmware Area cannot be accessed.
	1	*Program_Mode_Disable*	If set, Firmware Area is protected against overriding.
	2	*Repeater_Mode*	If set, Firmware Area cannot be accessed.
	3	*Invert_Data_In*	All Data Port inputs are inverted.
D	0 to 3	*DI_Invert_Configuration*	Enables separate input data inverting for selected DI pins. *Invert_Data_In* must **not** be set.
E	0 to 3	*DI_Filter_Configuration*	Enables anti-bouncing filters for selected DI pins
F	0 to 2	*DI_Filter_Time_Constant*	Defines a time constant for the input filter. For coding rules, see section 4.7.2.
	3	*P1_Filter_Activation*	If flag is set, the logic value at the parameter pin P1 determines whether the filter function is active or inactive (see section 4.6.2.) If flag is not set, *DI_Filter_Configuration* activates the filter function.
10	0 to 3	*Data_Out_Configuration*	Defines whether the corresponding Data Port output pin is driven by the Data Output Register (sensitive to the *Data_Exchange* command) or the *Data_Out_Value* register (EEPROM configured).
11	0 to 3	*Data_Out_Value*	Stores static Data Port output value if selected by *Data_Out_Configuration*

ASI4U Internal EEPROM Address [hex]	Bit Position	EEPROM Cell Content	EEPROM Register Content
12	0	*Enhanced_Status_Indication*	If set, Enhanced Status Indication Mode according to the *AS-Interface Complete Specification* is activated. **Activates LED2 output! For compatibility to A²SI board layouts, this flag must not be set (= 0).**
	1	*Dual_LED_Mode*	If set, LED1 and LED2 output signals are controlled to comply with the dual LED indication configurations of AS-i. Generated signals also depend on the value of the *Enhanced_Status_Indication* flag. Direct connection of a dual LED is supported. **Activates LED2 output! For compatibility to A²SI board layouts, this flag must not be set (= 0).**
	2	*FID_Invert*	The FID input value is inverted before further processing.
	3	*Safety_Mode*	If set, the ASI4U/ASI4U-E/ASI4U-F Safety Mode is enabled and a special data input routing is activated.
13	0	*Synchronous_Data_IO*	Enables Synchronized Data I/O Mode
	1	*P2_Sync_Data_IO_Activation*	If flag is set, the logic value at the parameter pin P2 determines whether the Synchronous Data IO Mode is active or inactive. If flag is not set, the Synchronous Data IO Mode is always active if it was enabled by the *Synchronous_Data_IO* flag.
	2	*Ext_Addr_4I/4O_Mode*	Enables 4 Input / 4 Output support in Extended Address Mode.
	3	*ID_Code1_Protect*	If flag is set, *ID_Code_Extension_1* is write-protected for user access. In Extended Address Mode, only bits 2 to 0 are blocked. Bit 3 is used for A/B slave selection and must remain user accessible.
14	0 to 3	*ID1_Bit0* to *ID1_Bit3*	*Protected_ID_Code_Extension_1* If the *ID_Code1_Protect* flag is set, a *Read_ID_Code_1* request will be answered with the data stored in this register.
15	0 to 3	Trim Area; accessible by IDT only	
16	0 to 3		
17	0 to 3		

4 Detailed Functional Description

4.1. AS-i Receiver

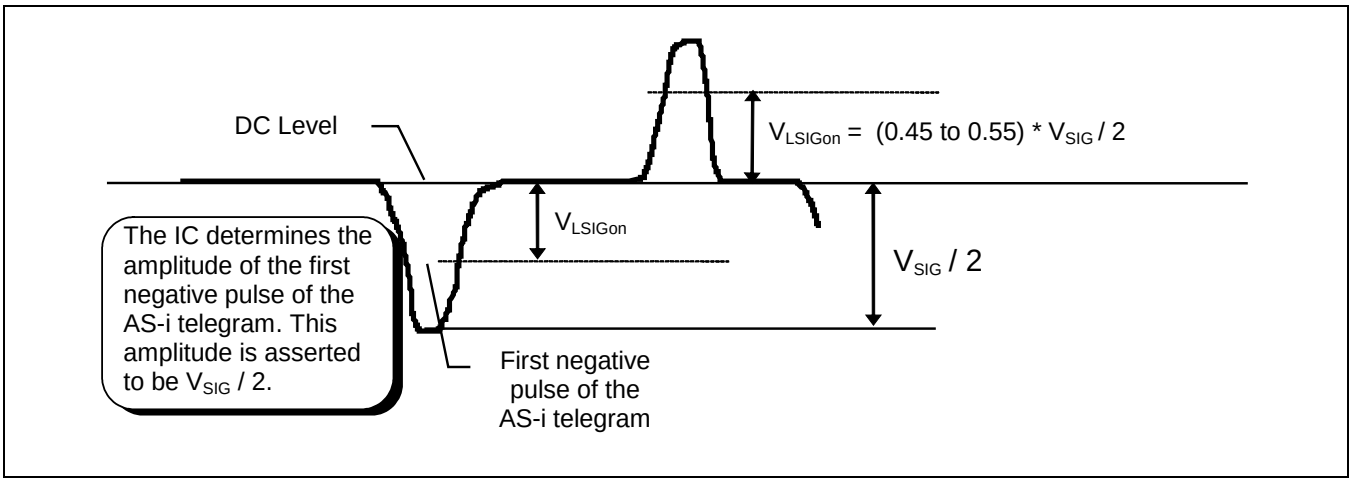
The receiver detects (telegram) signals on the AS-i line, converts them to digital pulses, and forwards them to the UART for further processing. The receiver is internally connected between the ASIP and ASIN pins. It supports floating (ground free) input signals within the voltage limits of ASIP and ASIN given in Table 2.2.

Functionally, the receiver removes the DC value of the input signal, band-pass filters the AC signal, and extracts the digital output signals from the $\sin^2$-shaped input pulses via a set of comparators. The amplitude of the first pulse determines the threshold level for all subsequent pulses. This amplitude is digitally filtered to guarantee stable conditions and to suppress burst spikes. This approach combines a fast adaptation to changing signal amplitudes with a high detection safety. The comparators are reset after every detection of a telegram pause at the AS-i line. When the receiver is turned on, the transmitter is turned off to reduce the power consumption.

Table 4.1 Receiver Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
AC signal peak-peak amplitude (between ASIP and ASIN)	V_{SIG}		3	8	V_{PP}
Receiver comparator threshold level (refer to Figure 4.1)	V_{LSIGon}	Related to 1st pulse amplitude	45	55	%

Figure 4.1 Simplified Receiver Comparator Threshold Setup



4.2. AS-i Transmitter

The transmitter draws a modulated current between ASIP and ASIN to generate the communication signals. The shape of the current corresponds to the integral of a $\sin^2$-function. The transmitter comprises a current DAC and a high current driver. The driver requires a small bias current to flow. The bias current is ramped up slowly for a specific time before the transmission starts so that any false voltage pulses on the AS-i line are avoided.

Table 4.2 Transmitter Current Amplitude

PARAMETER	SYMBOL	MIN	MAX	UNIT
Modulated transmitter peak current swing (between ASIP and ASIN)	I_{SIG}	55	68	mA_P

To support high symmetry extended power applications as shown in Figure 5.2, the transmitter is designed to allow input voltages different from IC ground at the ASIN pin. The limits given in Table 2.2 apply. When the transmitter is turned on, the receiver is turned off to reduce the power consumption.

4.3. Addressing Channel Input IRD

4.3.1. General Slave Mode Functionality

To ease the configuration process for slave modules in the field application, a secondary command input channel is provided on the IRD pin, which is referred to as the Addressing Channel.

If the channel is activated for communication, the IRD pin receives Manchester-II-coded (AS-i) master telegrams, while the LED1 pin returns slave response telegrams in Manchester-II format.

Applying a Magic Sequence at the IRD input activates the Addressing Channel. It does not matter whether the IC is communicating via the AS-i input channel or staying in idle mode. As long as the initialization process is finished and the IC is operating in Slave Mode, a correctly received Magic Sequence will reset the data and parameter outputs; generate appropriate data strobe and parameter strobe signals; reset the *Data_Exchange_Disable* flag; and activate the Addressing Channel.

The Magic Sequence requires the reception of four consecutive correct AS-i telegrams in Manchester-II format within a timeframe of 8.192ms (– 6.25%). The telegrams will neither be answered nor otherwise internally processed. They are only checked for correct syntax (number of bits, correct start bit, end bit, and parity) and timing (compliance to standard AS-i telegram timing).

To avoid invalid activation of the Addressing Channel by undesired cross coupling of signals from the AS-i line to the IRD input, **two additional security features** are implemented.

1. The ASI4U/ASI4U-E/ASI4U-F resets the Magic Sequence telegram counter if more than 5 but less than 14 telegram bits were correctly received. Pulse signals that lead to detection of a communication error before the 6th telegram bit will not reset the Magic Sequence counter in order to avoid blocking the IRD activation due to signal bouncing effects.
2. The ASI4U/ASI4U-E/ASI4U-F resets the Magic Sequence telegram counter if a telegram that was received at the IRD input correlates to the AS-i line input signal in terms of telegram reception time <u>and</u> content.

Note: The UART processes both input channels (AS-i line and the IRD Addressing Channel) in parallel and generates *Receive_Strobe* signals after every correctly received Master telegram. A telegram correlation between both channels is found if *Receive_Strobe* signals from both input channels arrive at a time frame ≤ 3µs *and* the telegram contents are equal.

The Addressing Channel generally becomes **deactivated** by an **IC reset.**

If the IC is locked to the Addressing Channel and AC Current Input Mode (see descriptions further below) is active, there are **four special IC functions** that are implemented to support existing handheld programming devices (from the company Pepperl+Fuchs):

1. The IC does not leave the Addressing Channel Mode after the reception of a *Reset_Slave* or *Broadcast_Reset* call if the *Data_Exchange_Disable* flag is cleared (0). This is always the case if the ASI4U/ASI4U-E/ASI4U-F has performed data or parameter communication before the reset so that the handheld has been operating in Data or Parameter Mode.
2. The IC does not leave the Addressing Channel during an IC reset that was caused by an expired Communication Watchdog.

   See section 4.15 for detailed descriptions of the Communication Monitor and Communication Watchdog.
3. Software controlled IC resets (resets through *Reset_Slave* or *Broadcast_Reset* calls) are performed slightly differently than resets in normal slave IC operation.

   The IC still resets the data and parameter outputs immediately after reception of the calls, and Data Strobe and Parameter Strobe signals are generated. However, the *IC initialization procedure is postponed for 2.048ms* (-6.25%), keeping the IC blocked to any further telegram inputs at the Addressing Channel or the AS-i line input. This is to avoid an immediate reactivation of the Addressing Channel after IC initialization since the handheld programming device always sends five subsequent *Broadcast_Reset* calls. The ASI4U would otherwise process the first reset call from the handheld correctly but misinterpret the four remaining calls as a new Magic Sequence.
4. The UART is constantly set to Synchronous Receive Mode. This is because the signal sequence that is generated by the handheld programming device exhibits an additional signal transition in a time frame of 3 bit-times after the end of the transmitted master call.

4.3.2. AC Current Input Mode

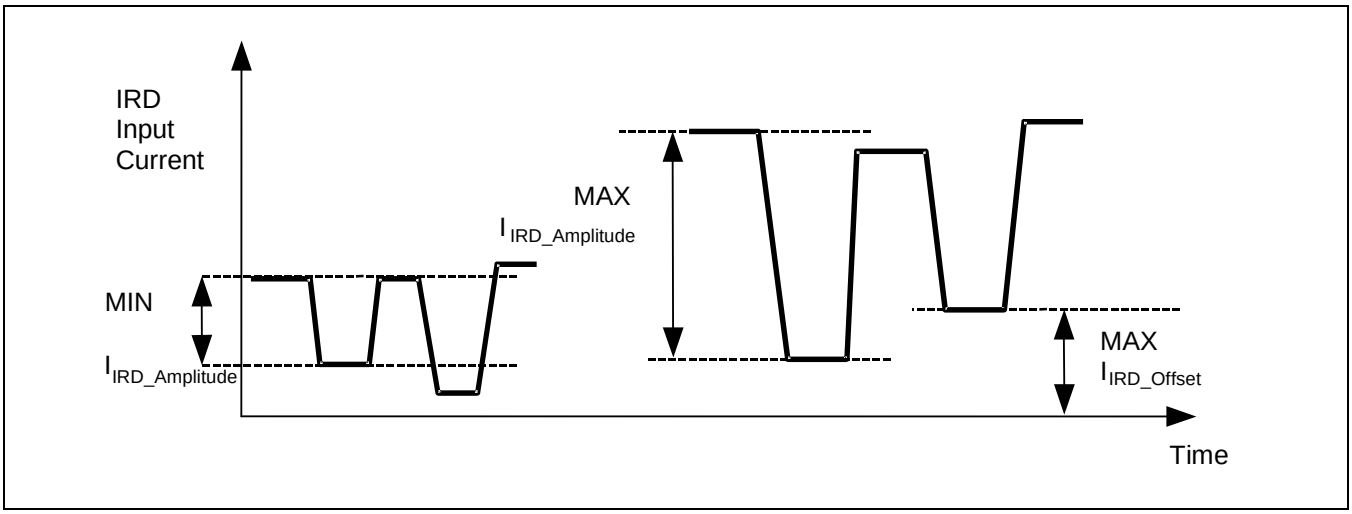
The IRD input allows direct connection of a photodiode (referenced to 0V pin) and senses the generated photo current. A valid input signal must have a specified current amplitude (range) and must not exceed a specified offset current value, which are given in Figure 4.2 and Table 4.3

In contrast to A²SI versions, the IRD input of the ASI4U/ASI4U-E/ASI4U-F covers the entire input current range by a single amplifying stage with continuous (logarithmical) gain adaptation. This avoids cyclical gain switching, and the IC can react more safely and without delay on different input signal amplitudes.

Table 4.3 IRD AC Current Input Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Input current offset	I_{IRD_Offset}			10	µA
Input current amplitude	$I_{IRD_Amplitude}$		25	100	µA

Figure 4.2 Addressing Channel Input (IRD), Photo-Current Waveforms



The TEMIC TEMD5000 photodiode is suggested for optimal performance.

4.3.3. CMOS Input Mode

In addition to the AC Current Input Mode, the IRD input can also operate in CMOS Input Mode. Mode switching is only possible as long as the IC has not already locked to the Addressing Channel by reception of a Magic Sequence. The input mode that led to the activation of the Addressing Channel will remain locked until the Addressing Channel is deactivated (by an IC reset).

The CMOS Input Mode is entered if the IRD input voltage is **above 2.5V** (logic HIGH) for more than 7.680ms (-6.66%). It is exited if the IRD input voltage is **below 1.0V** (logic LOW) for more than 7.680ms (-6.66%). The initial input mode after IC initialization is determined at the end of the initialization phase and depends on the value of the IRD input signal at that time.

Table 4.4 IRD Current/Voltage Mode Switching

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Minimum IRD input voltage to activate CMOS Input Mode of IRD pin	V_{IRD_VM}		2.5		V
Maximum IRD input voltage to activate AC Current Input Mode of IRD pin	V_{IRD_CM}			1.0	V
Filter time constant for IRD input mode switching	$t_{IRD_Mode_Filter}$		7.68	8.192	ms

The following input levels apply in CMOS Input Mode:

Table 4.5 IRD CMOS Input Mode Levels

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Input voltage range	V_{IRD_IN}		-0.3	V_{Uout}	V
Voltage range for input LOW level	V_{IRD_IL}		0	1.0	V
Voltage range for input HIGH level	V_{IRD_IH}		2.5	V_{Uout}	V
Rise or fall time [1)]	t_r or t_f			100	ns
1) In Master Mode, the rise/fall time of the IRD input signal should be as low as possible in order to avoid jitter on the AS-i line.					

4.3.4. Master, Repeater, and Monitor Modes

In the Master, Repeater, and Monitor Modes, the IRD input is always configured in CMOS Input Mode. The input levels specified in Table 4.5 apply.

The expected polarity of the Manchester-II-coded bit stream at the IRD pin depends on the values of the DI0 and DI1 pins.

Table 4.6 Polarity of Manchester-II Signal at IRD in Master Mode

INPUT VALUES AT DI0 AND DI1	DESCRIPTION
Equal (“11” or “00”)	The Manchester-II signal is active LOW (default logic output value at no communication is 1). This mode is compatible with the A²SI IRD input.
Unequal (“01” or “10”)	The Manchester-II signal is active HIGH (default logic output value at no communication is 0).

Note: The complemented definition was chosen to retain backward compatibility to A²SI-based AS-i Master designs.

4.4. Digital Inputs – DC Characteristics

The following pins contain digital high voltage input stages:

Input-only pins: **DI0, DI1, DI2, DI3, and FID**

I/O pins: **P0, P1, P2, P3, DSR, PST, and LED2**

Note: PST and LED2 are inputs for test purposes only.

Table 4.7 DC Characteristics of Digital High Voltage Input Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Voltage range for input LOW level	V_{IL}		0	2.5	V
Voltage range for input HIGH level	V_{IH}		3.5	V_{UOUT}	V
Hysteresis for switching level	V_{HYST}		0.25		V
Current range for input LOW level [1)]	I_{IL}		-10	-3	µA
Current range for input HIGH level	I_{IH}	$V_0 \geq V_{U5R}$	-10	10	µA
Capacitance at pin DSR [2)]	C_{DL}			10	pF

1) The pull-up current is driven by a current source connected to U5R. It stays almost constant for input voltages ranging from 0 to 3.8V. The current source is disabled at the FID pin in the Master, Repeater, and Monitor Modes to provide a straight analog signal input for the Power Fail comparator.

2) The internal pull-up current is sufficient to avoid accidental triggering of an IC reset if the DSR pin remains unconnected. For external loads at DSR, a pull-up resistor is required to ensure $V_{IH} \geq 3.5V$ in less than 35µs after the beginning of a DSR = low pulse. The pull-up resistor value depends on the parasitic components in the user's application.

4.5. Digital Outputs - DC Characteristics

The following pins contain digital high-voltage open-drain output stages:

Output-only pins **DO0, DO1, DO2, DO3, and LED1**

I/O pins **P0, P1, P2, P3, DSR, PST, and LED2**

Note: PST and LED2 are inputs for test purposes only.

Table 4.8 DC Characteristics of Digital High Voltage Output Pins

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Voltage range for output LOW level	V_{OL1}	I_{OL1} = 10mA	0	1	V
Voltage range for output LOW level	V_{OL2}	I_{OL2} = 2mA	0	0.4	V
Output leakage current	I_{OH}	$V_{0H} \geq V_{U5R}$	-10	10	µA
Voltage range for output HIGH level (external applied voltage)	V_{OH}			V_{UOUT}	V

4.6. Parameter Port and PST Pin

4.6.1. Slave Mode

The parameter port is configured for continuous bi-directional operation. Every pin contains an NMOS open-drain output driver plus a high-voltage, high-impedance digital input stage. Received parameter output data is stored in the Parameter Output Register and subsequently forwarded to the open-drain output drivers. A specific time $t_{PI\text{-}latch}$ (given in Table 4.9) after new output data has arrived at the port, the corresponding inputs are sampled.

The input value either results from a wired AND combination of the parameter output value and the signals driven to the port by external sources (*Multiplex_Parameter* =0) or simply represents the externally driven input signals (*Multiplex_Parameter* =1). For further explanation, see also Figure 4.3 and section 4.6.2.

The availability of new parameter output data is signaled by the *Parameter Strobe (PST)* signal.

In addition to the basic I/O function, the first parameter output event after an IC reset has an additional meaning. It enables the data output at the Data Port (see sections 4.7 and 4.11).

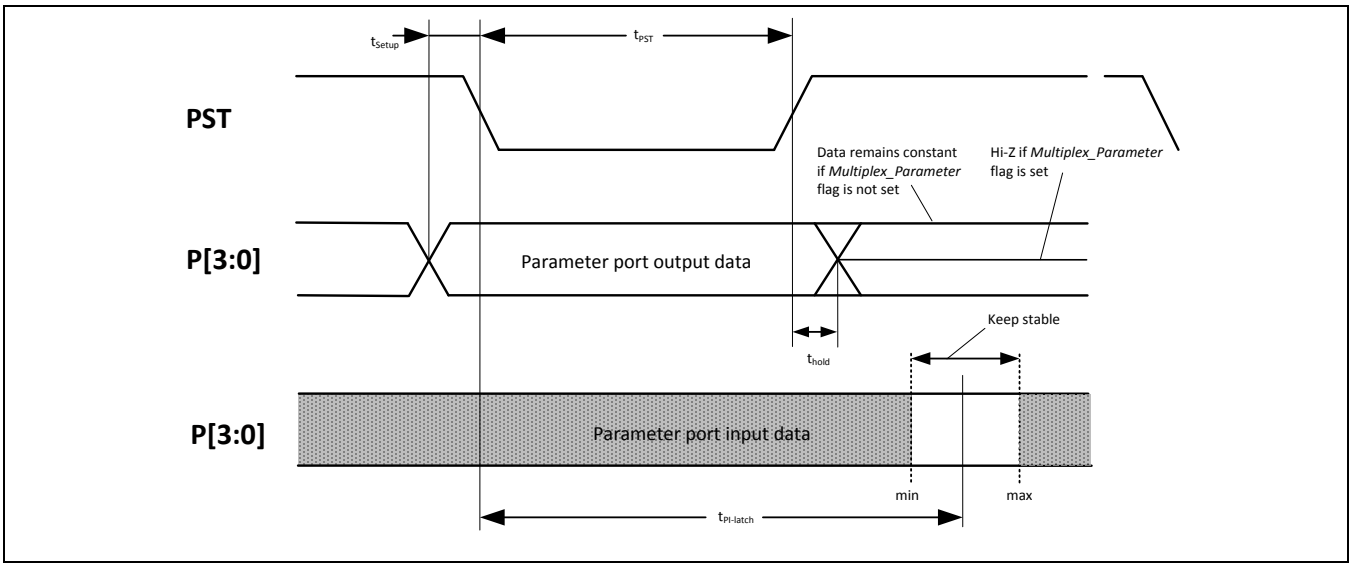
Any IC reset or the reception of a *Delete_Address* call sets the Parameter Output Register to F_{HEX} and forces the parameter output drivers to the high impedance state. Simultaneously a Parameter Strobe is generated, having the same t_{setup} timing and t_{PST} pulse width as is used when new output data is driven.

Table 4.9 Timing Parameter Port

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Output data is valid LOW before PST-H/L [1)]	t_{setupL}		0.1	0.6	µs
Output driver is at high impedance state before PST-H/L [1)]	t_{setupH}		0.1	0.6	µs
Output driver is at high impedance state after PST-H/L [1), 2)]	t_{hold}		0.1	0.6	µs
Pulse width of Parameter Strobe (PST) [3)]	t_{PST}		5	6	µs
Acceptance of input data [4)]	$t_{PI\text{-}latch}$		11	13.5	µs

1) The designed value is 0.5µs.
2) t_{hold} is only valid if the *Multiplex_Parameter* flag is set in the Firmware Area block of the EEPROM.
3) The timing of the resulting voltage signal also depends on the external pull up resistor.
4) The parameter input data must be stable within the period defined by minimum and maximum values of $t_{PI\text{-}latch}$.

Figure 4.3 Timing Diagram Parameter Ports P[3:0] and PST



4.6.2. Parameter Multiplex Mode

The *AS-Interface Complete Specification V3.0* defines a Parameter Multiplex Mode. This added feature allows bi-directional data transfer through the parameter port. The bi-directionality is achieved by turning the Parameter Output Drivers off after the Parameter Strobe period and before the input sampling event. By turning off its output drivers during the Parameter Strobe pulse, an external microcontroller can read the data from the Parameter Port of the ASI4U/ASI4U-E/ASI4U-F, prepare new return data, and place it to the port immediately after the Parameter Strobe signal.

The Parameter Multiplex Mode becomes activated by setting the corresponding *Multiplex_Parameter* flag (=1) in the EEPROM.

To keep full compatibility to A²SI-based applications, this flag should be kept as zero (=0). The A²SI did not allow real bi-directional parameter data transfer since it was not able to turn the output drivers off. The return value to a *Write_Parameter* call was always a wired AND combination of the output signal of the IC and the signal driven to the port by the external logic.

4.6.3. Special Function of P0, P1 and P2

If the *Watchdog_Active* flag is <u>not set</u> (=0) but the *P0_Watchdog_Activation* flag is set (= 1, in the Firmware Area block of the EEPROM), the value of the *Parameter Port* signal P0 determines whether the communication watchdog is enabled or disabled. In compliance with *Slave Profile 7D-5*, the behavior is defined as follows:

INPUT VALUE AT P0	STATE OF COMMUNICATION WATCHDOG
LOW level (=0)	Disabled
HIGH level (=1)	Enabled

If the *P1_Filter_Activation* flag is set in the EEPROM, the activation of the data input filters depends on the value of the *Parameter Port* signal P1. The following coding applies:

INPUT VALUE AT P1	DATA INPUT FILTER FUNCTION
LOW level (=0)	Activated
HIGH level (=1)	Deactivated

For further details, refer to section 4.7.

If the *Synchronous_Data_I/O_Mode* flag is set in the EEPROM, the value of the parameter port P2 activates or deactivates the *Synchronous Data I/O Mode* of the ASI4U/ASI4U-E/ASI4U-F. The following coding applies:

INPUT VALUE AT P2	SYNCHRONOUS DATA I/O MODE
LOW level (=0)	Activated
HIGH level (=1)	Deactivated

For further details, refer to section 4.7.

The processed values of P0, P1, and P2 result from a wired-AND combination between the corresponding output value and the input value driven by an external signal source.

4.6.4. Master, Repeater, and Monitor Modes

In the Master, Repeater, and Monitor Modes, the Parameter Port is configured differently than in Slave Mode. The pins serve as output channels for additional support signals or become set to the high impedance state. There is no input function associated with the Parameter Port pins.

The following support signals are provided at the Parameter Port in the Master, Repeater, and Monitor Modes.

Table 4.10 Parameter Port Output Signals in Master, Repeater, and Monitor Modes

PIN	MASTER MODE	REPEATER MODE	MONITOR MODE
P0	Receive Clock	Hi-Z	Receive Clock
P1	Power Fail	Hi-Z	Power Fail
P2	Receive Strobe – Slave Telegram	Hi-Z	Receive Strobe – Slave Telegram
P3	Hi-Z	Hi-Z	Receive Strobe – Master Telegram

Receive Clock is provided to simplify external processing of Manchester-II-coded output data at the LED1 pin. The availability of a new AS-i telegram bit at LED1 is signaled by a rising edge of the receive clock so that the received data can simply be clocked into a shift register. The output signal is active HIGH.

Power Fail signals a breakdown of the AS-i supply voltage. The output signal is active HIGH. For further information regarding the *Power Fail* function, refer to section 4.8.

Receive Strobe – Slave Telegram is generated after every correctly received AS-i slave telegram. The output signal is active HIGH.

Receive Strobe – Master Telegram is generated after every correctly received AS-i master telegram. The output signal is active HIGH.

The generated pulse width is 1.0µs for both *Receive Strobe* signals at the output drivers (Hi-Z time). The resulting signal pulse width depends on the external pull-up resistor and the load circuit.

4.7. Data Port and DSR Pin

4.7.1. Slave Mode

The data port is divided into 4 output and 4 input pins. This makes it possible to control a maximum of 8 binary devices (4 input + 4 output devices) by a single AS-i Slave IC. Compatibility to multiplexed bi-directional operation, as it is defined in some I/O configurations for AS-i Slaves, can be achieved by external connection of corresponding DI and DO pins and setting *Multiplex_Data* flag =1 in the Firmware Area block of the EEPROM.

Every output pin (DO0, DO1, DO2, DO3) contains an NMOS open-drain output driver; every input pin (DI0, DI1, DI2, DI3) contains a high-voltage, high-impedance input stage. Received output data is stored at the Data Output Register and subsequently forwarded to the DO pins. A specified time ($t_{DI\text{-}latch}$) after new output data has been written to the port, the DI pins are sampled.

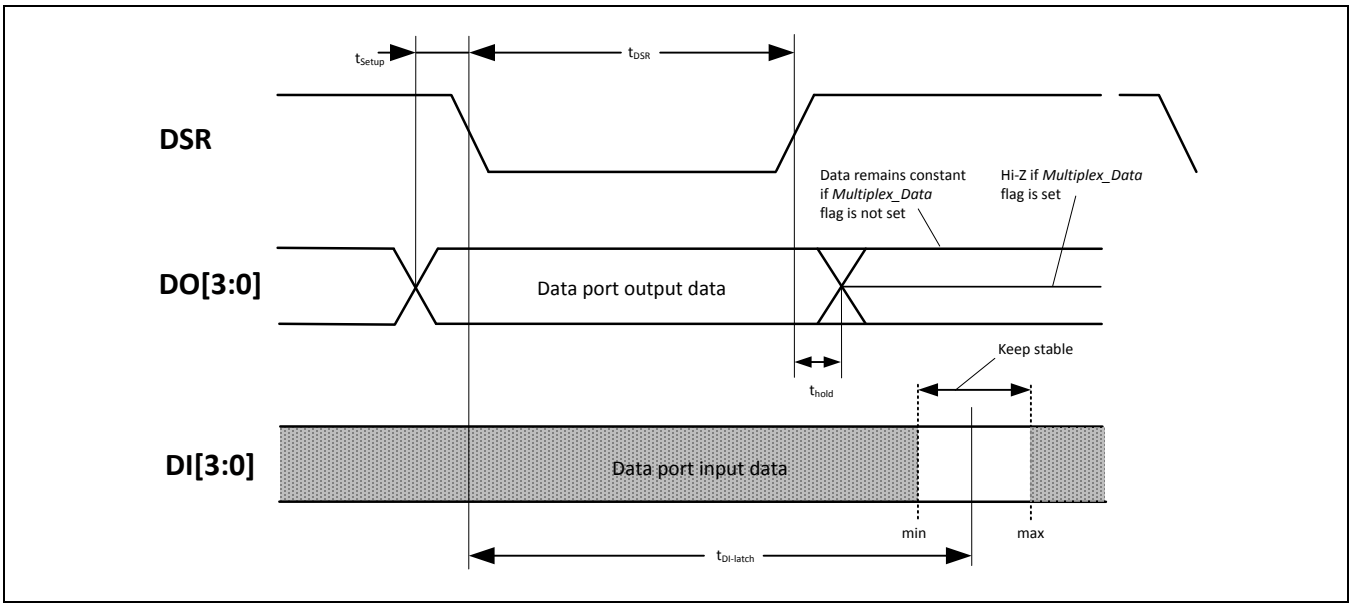
The availability of new output data is signaled by the Data Strobe (DSR) signal as shown in Figure 4.4. The DSR pin has an additional reset input function, which is described further in section 4.11.

Table 4.11 Timing Data Port Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Output data is valid LOW before DSR-H/L [1)]	t_{setupL}		0.1	0.6	µs
Output driver is at high impedance state before DSR-H/L [2)]	t_{setupH}		0.1	0.6	µs
Output driver is at high impedance state after DSR-H/L [1), 2)]	t_{hold}		0.1	0.6	µs
Pulse width of Data Strobe (DSR) [3)]	t_{DSR}		5	6	µs
Acceptance of input data [4)]	$t_{DI\text{-}latch}$		11	13.5	µs

1) The designed value is 0.5µs.
2) Parameter is only valid if *Multiplex_Data* flag is set in the Firmware Area block of the EEPROM.
3) The timing of the resulting voltage signal also depends on the external pull-up resistor.
4) The input data must be stable within the period defined by minimum and maximum values of $t_{DI\text{-}latch}$.

Figure 4.4 Timing Diagram Data Ports DO[3:0], DI[3:0] and DSR

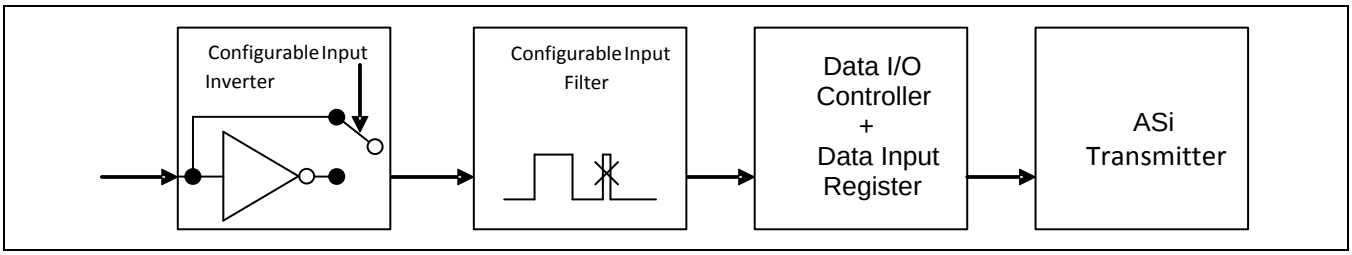


Any IC reset or the reception of a *Delete_Address* call changes the Data Output Register to F_{HEX} and forces the data output drivers to a high impedance state. Simultaneously, a *Data Strobe* is generated, having the same t_{setup} timing and t_{DSR} pulse width as is used when new output data is driven. All Data Port operations as well as the generation of a slave response to *Data_Exchange* (DEXG) requests depend on the value of the *Data_Exchange_Disable* flag. It becomes set during IC reset or after a *Delete_Address* call prohibiting any data port activity after IC initialization or address assignment, as long as the external circuitry was not pre-conditioned by dedicated parameter output data. The *Data_Exchange_Disable* flag is cleared while processing a *Write_Parameter* (WPAR) request. Consequently the AS-i master must send a WPAR call in advance of the first *Data_Exchange* (DEXG) request in order to enable Data Port operation at the slave.

4.7.2. Input Data Pre-processing

In addition to the standard input function, the Data Port offers different data pre-processing features that can be activated by setting corresponding flags in the Firmware Area of the EEPROM. The data path is structured as shown in Figure 4.5.

Figure 4.5 Input Path at Data Port



Joint Input Inverting

The input values of all four data input channels are inverted when the *Invert_Data_In* flag is set. Any configurations made in the *DI_Invert_Configuration* register are ignored. The feature is kept for compatibility with A²SI product versions.

- **Selective Input Inverting** If the *Invert_Data_In* flag is not set, inverting of input data can be configured individually for every *Data Port* input channel by setting the corresponding flag in the *DI_Invert_Configuration* register. The index of the DI channel corresponds to the bit position within the register; e.g., the data at input channel **DI0** is inverted if **bit 0** of the *DI_Invert_Configuration* register is set and similarly input channel **DI3** is inverted if **bit 3** is set.
- **Selective Input Filtering** A digital anti-bouncing filter is provided at every *Data Input* channel to keep undesired signal bouncing at the DI pins away from the AS-i Master. If activated, a signal transition at a given DI pin is passed to the Data Input Register only if the new value has remained constant for a specific time. The filter time can be adjusted jointly for all input channels in seven steps by programming the *DI_Filter_Time_Constant* register in the Firmware Area block of the EEPROM. The coding given in Table 4.12 applies.

Figure 4.6 Principles of Input Filtering

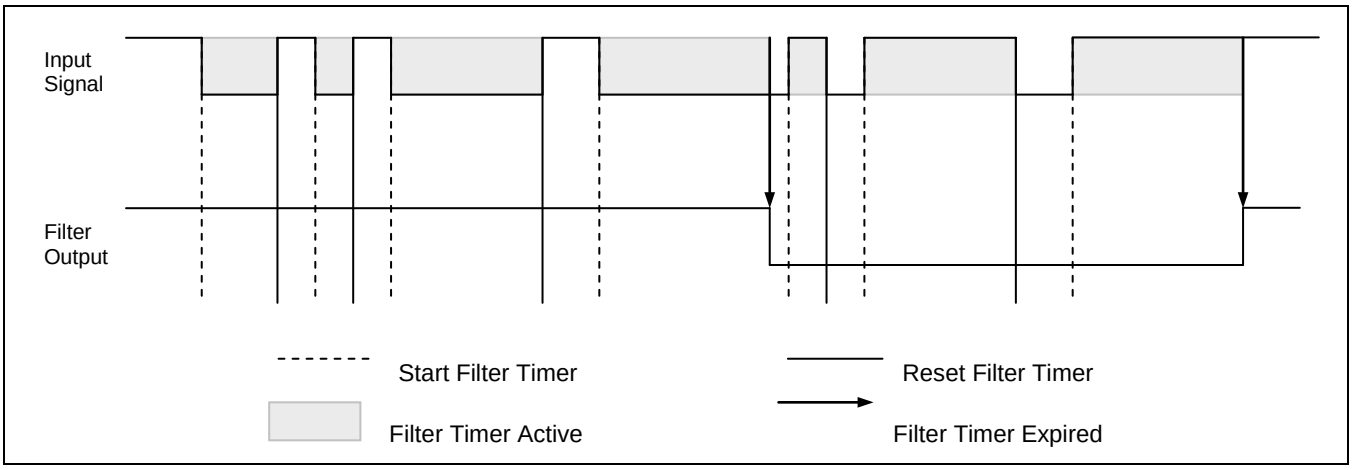
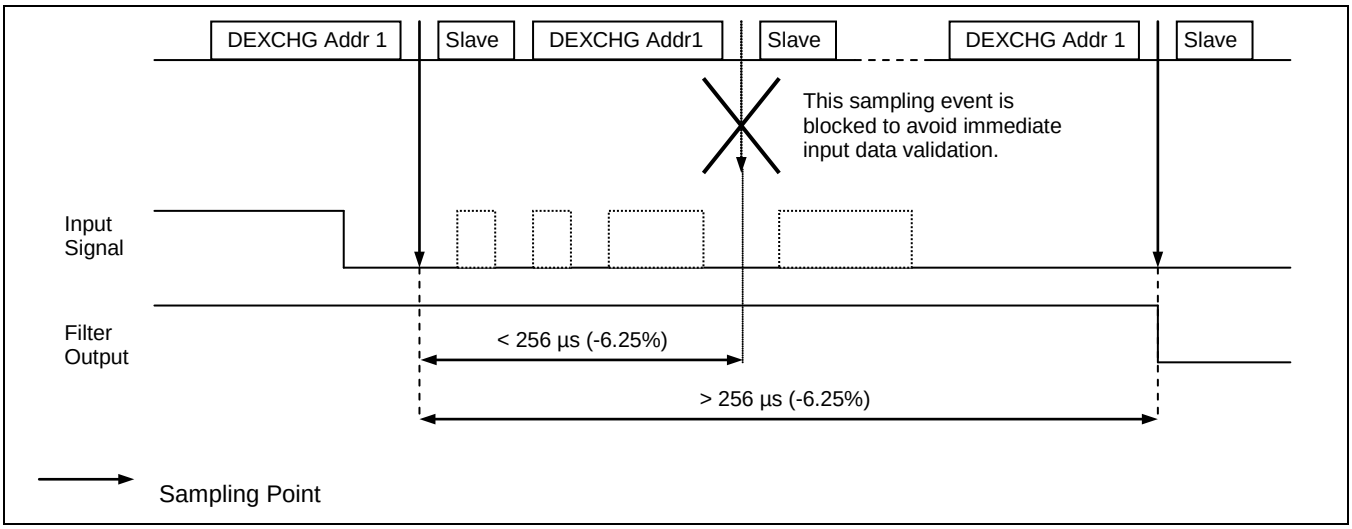


Table 4.12 Data Input Filter Time Constants

	DI_Filter_Time_Constant (Tolerance = - 6.25%)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Corresponding input filter time constant	128µs	256µs	512µs	1024µs	2048µs	4096µs	8192µs	AS-i cycle

If AS-i Cycle Mode is selected, a new input value is returned to the master if equal input data has been sampled for two consecutive *Data_Exchange* cycles. As long as the condition is not true, previous valid data is returned. To suppress undesired input data validation in the case of immediately repeated *Data_Exchange* calls (e.g., AS-i Masters immediately repeat one *Data_Exchange* request if no valid slave response was received on the first request), input data sampling is blocked for 256µs (-6.25%) after every sampling event in AS-i Cycle Mode.

Figure 4.7 Principle of AS-i Cycle Input Filtering (Example for Slave with Address 1)



The *DI_Filter_Configuration* register provides channel-selective enabling of input filters; just as the *DI_Invert_Configuration* register allows individual inverting of the four Data Port input channels. Again, the index of the DI channel corresponds to the bit position within the register; e.g., data at input channel **DI0** is filtered if **bit 0** of the *DI_Filter_Configuration* register is set and similarly input channel **DI3** is filtered if **bit 3** is set.

In general, the *Data Input Filters* become active if the corresponding bit in the *DI_Filter_Configuration* Register is set.

- They are initialized with “0” and the filter timer is reset after the initialization phase of the IC. (The first is because an AS-i Master interprets data inputs at “0” to be inactive.)
- If the *P1_Filter_Activation* flag is set to “1,” the filters will also start to run after the initialization phase; however, the data to construct the slave response is taken from either the actual Data Input values or the filtered values, depending on the state of Parameter Port P1.

Table 4.13 Input Filter Activation by Parameter Port Pin P1

***P1_Filter_Activation* FLAG**	**PARAMETER PORT P1**	**DATA INPUT FILTER FUNCTION**
0	Don’t care	ON, active filters depend on *DI_Filter_Configuration*
1	1	OFF
1	0	ON, active filters depend on *DI_Filter_Configuration*

If the IC is operated in Parameter Multiplex Mode (see descriptions in section 4.6.1 and subsequent sections) while the *P1_Filter_Activation* flag is set, the Parameter Multiplex Mode remains disabled for parameter port pin P1. This is to avoid erroneous deactivation of the input filters if no external driver is connected.

Input data inverting and input data filtering are independent features that can be combined as required by the application. Programming the following EEPROM flags or registers activates them:

Table 4.14 EEPROM Configuration for Different Input Modes

<table>
<tr><th rowspan="2">EEPROM FLAG OR REGISTER NAME</th><th colspan="4">INPUT MODE</th></tr>
<tr><th>Standard Input</th><th>Joint Input Inverting</th><th>Selective Input Inverting</th><th>Selective Input Filtering</th></tr>
<tr><td>Invert_Data_In</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Input inverting is additionally possible</td></tr>
<tr><td>DI_Invert_Configuration</td><td>0_{HEX}</td><td>“Don’t care”</td><td>1_{HEX} to F_{HEX}</td></tr>
<tr><td>DI_Filter_Configuration</td><td>0_{HEX}</td><td colspan="3" rowspan="2">Input filtering is also possible</td><td>1_{HEX} to F_{HEX}</td></tr>
<tr><td>DI_Filter_Time_Constant</td><td>“Don’t care”</td><td>0_{HEX} to 7_{HEX}</td></tr>
</table>

4.7.3. Fixed Output Data Driving

In addition to the standard output function, the Data Output Port provides an additional function to drive a fixed output value that is stored in the Firmware Area block of the EEPROM. This feature is basically meant to support signaling of different Firmware Area setups to outside slave module circuitry. It presumes the application does not require all four Data Output pins.

The EEPROM *Data_Out_Configuration* register is used to determine whether the corresponding Data Port output signal is sensitive to *Data_Exchange* calls, or if the driven Data Output value is taken from the corresponding bit in the *Data_Out_Value* register, also located in the Firmware Area of the EEPROM.

The index of the DO signal corresponds to the bit position in the *Data_Out_Configuration* and *Data_Out_Value* registers. The fixed output driving capability is activated if the particular *Data_Out_Configuration* bit is set to “1.” The standard output mode is activated if *Data_Out_Configuration* is programmed to 0_{HEX}, which is the default state of the register.

4.7.4. Synchronous Data I/O Mode

As defined in the *AS-Interface Complete Specification*, a master successively polls the network incrementing the slave addresses from the lowest to the highest. Hence, data input and output operations normally take place at different times in different slaves. To support applications that require simultaneous Data I/O operations on a given number of slaves in the network, a Synchronous Data I/O Mode is provided.

The feature is enabled if the *Synchronous_Data_IO* flag is set in the Firmware Area of the EEPROM (=1). Activation of the feature also depends on the value of the *P2_Sync_Data_IO_Activation* flag. The following coding applies:

Table 4.15 Activation States of Synchronous Data IO Mode

***Synchronous_Data_IO* FLAG**	***P2_Sync_Data_IO_Activation* FLAG**	**INPUT VALUE AT P2**	**SYNCHRONOUS DATA I/O MODE**
0	Don't care	Don't care	Deactivated
1	0	Don't care	Activated
1	1	Low level (= 0)	Activated
1	1	High level (= 1)	Deactivated

The Parameter Port signal **P2 is sampled at the rising edge of the Data Strobe** (LOW/HIGH transition) signal to determine the Data I/O behavior at the next Data Output event.

If the IC is operated in Parameter Multiplex Mode (see section 4.6.1*)* while the *Synchronous_Data_IO* flag **and** *P2_Sync_Data_IO_Activation* flag are set, the Parameter Multiplex Mode remains disabled for Parameter Port pin P2. This is to avoid erroneous deactivation of the Synchronous Data IO Mode if no external driver is connected.

Once activated, input data sampling as well as output data driving events are moved to different times **synchronized** to the polling cycle of the AS-i network. Nevertheless, the communication principles between master and slave remain unchanged compared to regular operation. The following rules apply:

- Data I/O is triggered by the DEXG call to the slave with the lowest slave address in the network. Based on the fact that a master is calling slaves successively with rising slave addresses, the ASI4U/ ASI4U-E/ASI4U-F considers the trigger condition to be true if the slave address of a received DEXG call is less than the slave address of the previous (correctly received) DEXG call.

  Data I/O is only triggered if the slave has (correctly) received data during the last cycle. If the slave did not receive data (e.g., due to a communication error), the Data Outputs are not changed and no Data Strobe is generated ("arm+fire" principle). The inputs, however, are always sampled at the trigger event.
- If **the slave with the lowest address in the network** is operated in the Synchronous Data I/O Mode, it postpones the output event for the received data for a full AS-i cycle. This is to keep all output data of a particular cycle image together.

  Note: To make this feature useful, the master must generate a data output cycle image once before the start of every AS-i cycle. The image is derived from the input data of the previous cycle(s) and other control events. If an AS-i cycle has started, the image must not change. If A and B slaves are installed in parallel at one address, the master must address all A Slaves in one cycle and all B Slaves in the other cycle.

The input data, sampled at the slave with the lowest slave address in the network, is sent back to the master without any delay. Thus, the input data cycle image is fully captured at the end of an AS-i cycle, just as in networks without any Synchronous Data I/O Mode slaves. In other words, the input data sampling point has simply moved to the beginning of the AS-i cycle for all Synchronous Data I/O Mode slaves.

- The **first DEXG call** that is received by a particular slave after the activation of the Data Port (*Data_Exchange_Disable* flag has been cleared by a WPAR call is processed as in regular operation. This is to capture valid input data for the first slave response and to activate the outputs as fast as possible.

  The Data I/O operation is repeated together with the I/O cycle of the other Synchronous Data I/O Mode slaves in the network at the common trigger event. By that, the particular slave has fully reached the Synchronous Data I/O Mode.
- If the ***P2_Sync_Data_IO_Activation* flag is set to '1'** at the slave with the lowest address in the network, one data output value is lost when the Synchronous Data I/O Mode is turned off (L/H transition at P2), while the value that is received in the cycle when the IC detects a signal change at P2 (H/L transition) is repeated. This particular behavior is caused by the fact that in *Synchronous Data I/O Mode* the data output at the slave with the lowest address is postponed for a full AS-i cycle (see description above).
- To avoid a general suppression of Data I/O in the special case that a slave in Synchronous Data I/O mode receives **DEXG calls only to its own address** (i.e. employment of a handheld programming device), the Synchronous Data I/O Mode is turned off once the ASI4U receives <u>three</u> consecutive DEXG calls to its own slave address. The IC resumes to Synchronous Data I/O Mode operation after it has observed a DEXG call to a slave address different from its own. The reactivation of the Synchronous Data I/O mode is handled likewise for the first DEXG call after activation of the Data Port (see description above).

The Data Strobe (DSR) signal is also generated in Synchronous Data I/O Mode. The timings of input sampling and output buffering correspond to the regular operation (refer to Figure 4.4 and Table 4.11).

4.7.5. Support of 4I/4O Processing in Extended Address Mode, Profile 7.A.x.E

In Extended Address Mode, the information bit I3 of the AS-i master telegram is used to distinguish between A and B Slaves that operate in parallel at the same AS-i slave address. For more detailed information, refer to the *AS-Interface Complete Specification.*

In addition to the benefit of an increased address range, the cycle time per slave is increased in Extended Address Mode from 5ms to 10ms and the useable output data is reduced from 4 to 3 bits. Because of the latter, Extended Address Mode slaves can usually control a maximum of only 3 data outputs. The input data transmission is not affected since the slave response still carries 4 data information bits in Extended Address Mode.

Applications that require 4-bit wide output data in Extended Address Mode, but can tolerate further increased cycle times (i.e., push buttons and pilot lights), are directly supported by a new Slave Profile 7.A.x.E that is defined in the *AS-Interface Complete Specification V3.0*.

If the IC is operated in Extended Address Mode <u>and</u> the *Ext_Addr_4I/4O_Mode* flag is set (= 1) in the EEPROM, it treats information bit I2 as the selector for two 2-bit wide data output banks (*Bank_1, Bank_2*).

The Master transmits data alternating between *Bank_1* and *Bank_2*, toggling the information bit I2 in the respective master calls. The ASI4U triggers a data output event (modification of the data output ports and generation of the Data Strobe) <u>only</u> at a *Data_Exchange* call that contains I2 = 0 <u>and</u> if the ASI4U received a *Data_Exchange* call with I2 = 1 in the previous cycle. Thus, new output data is issued at the Data Port synchronously for both banks at a falling edge of I2. The I2 toggle detector starts on state I2 = 0 after reset.

Input data is captured and returned to the master at every cycle, independent of the value of information bit I2. As a consequence, the cycle time is different for input data and output data:

- **Data input values** become refreshed in the master image in **less than 10 ms**.
- **Data output values** become refreshed at the slave in **less than 21 ms**.

The following coding applies:

Table 4.16 Meaning of Master Call Bits I0, I1, I2, and I3 in Ext_Addr_4I/4O_Mode

BIT IN MASTER CALL	OPERATION / MEANING
I0	If I2 = ‘1’ then I0/I1 are directed to temporary data output registers DO0_tmp/DO1_tmp If I2 = ‘0’ then I0/I1 are directed to the data output registers DO2/DO3 and DO0_tmp/DO1_tmp are directed to the data output registers DO0/DO1
I1	
I2	I2: /Select-bit for transmission to *Bank_1* (DO0/DO1) / *Bank_2* (DO2/DO3)
I3	I3: /Select bit for A-Slave/B-Slave addressing

4.7.6. Safety Mode Operation

The enhanced data input features described above require additional registers in the data input path that store the input values for a specific time before the values are sent to the AS-i transmitter. This causes a time delay in the input path and could lead to a delayed “turn off” event in AS-i Safety Applications, which in turn results in an increase in safety reaction time for the application.

To safely exclude an activation of the enhanced data I/O features in Safety Applications, a special Safety Mode of the IC must always be selected if the ASI4U is used for safe AS-Interface communication purposes. The Safety Mode is activated by setting the *Safety_Mode* flag in the firmware area of the EEPROM.

The Safety Mode contains the following properties:

Additional multiplexer: An additional 2:1 multiplexer is added in front of the send multiplexer that is controlled by the *Safety_Mode* flag. For deactivated Safety Mode, the regular data path is active.

Exchange of data inputs: The internal data paths of D3 and D2 are exchanged in Safety Mode and must be exchanged in the external code generator that controls the data inputs of the ASI4U as well. In case the Safety Mode becomes accidentally deactivated by a hardware fault, an exchange of the bits would be recognized after 4 cycles in a running application (see Figure 4.8).

Inverter at the data inputs: In Safety Mode it is still possible to use the “Data Input Invert” functionality (either joint-input inverting or bit-selective input inverting) of the IC. This allows transforming the default signal level of the external application (either HIGH or LOW) to the required default input level for AS-i Safety. For safety considerations, there is no difference if the inverter is integrated in the ASI4U or added externally. An error in the inverter or inverter activation will be recognized by a running application within the next cycle.

The following feature descriptions relate to the logical signals after the (optional) data input inverters.

Important Note: As described above, the pin assignment of DI2 and DI3 is exchanged in Safety Mode. However, the configuration register for selective input inverting is directly associated with the physical IC ports and is not changed. Thus, in Safety Mode bit 3 of the *DI_Invert_Configuration* register defines the inverting of the logical signal DI2 and bit 2 defines the inverting the signal DI3.

Modification of code sequence: The transmitted value for D0 is calculated according to the following equation:

D0 = D0 XOR (D1 AND D2 AND D3)

Thus, the ASI4U will generate ‘1110’ from the input value ‘1111’ and ‘1111’ from the input value ‘1110’. To comply with the coding rules of the safe AS-Interface communication, which prohibit ‘1111’ as a valid state in the data stream, the external code generator must store ‘1111’ instead of ‘1110’.

If the Safety Mode becomes accidentally deactivated by a hardware fault, the IC discontinues performing the D0 combination. The Safety Monitor would detect this as an error by reception of ‘1111’ (see Figure 4.9).

Deactivation of the standard data path: Theoretically, the Safety Mode could become deactivated for a single bit only if a (single) fault occurs at one of the multiplexers. This would lead to code sequences where three bits are routed in the Safety Path and the fourth bit is routed in the Standard Path. Therefore, an additional OR gate is added in the Standard Path that ties the Standard Path to constant ‘1’ if the Safety Mode is activated.

A valid data transfer in Standard Mode or Safety Mode is only possible if all four multiplexers are switched to the same direction. Any other state will be recognized by the Safety Monitor.

Activation of *Data_Exchange_Disable*: The *Data_Exchange_Disable* flag is set by the IC after a reset and will be cleared after the first parameter call. If the flag is set, the IC does not respond to *Data_Exchange* calls. If the Safety Mode is activated <u>and</u> the *Synchronous_Data_IO* flag <u>or</u> any of the *DI_Filter_Configuration* flags are set in the firmware area of the EEPROM, the *Data_Exchange_Disable* flag cannot be cleared. This prevents any data communication in this case. See Figure 4.10.

The flow charts given in Figure 4.8 are valid in the Safety Mode of the ASI4U:

Note: The following symbols are used in Figure 4.8, Figure 4.9, and Figure 4.10.

>=1 represents a logical **OR**
=1 represents a logical **XOR**
& represents a logical **AND**

The IC contains only a single inverter that generates the inverted Safety Mode signal for all requirements. See Figure 4.9.

Figure 4.8 Flowchart – Input DI3, DI2, and DI1 in Safety Mode

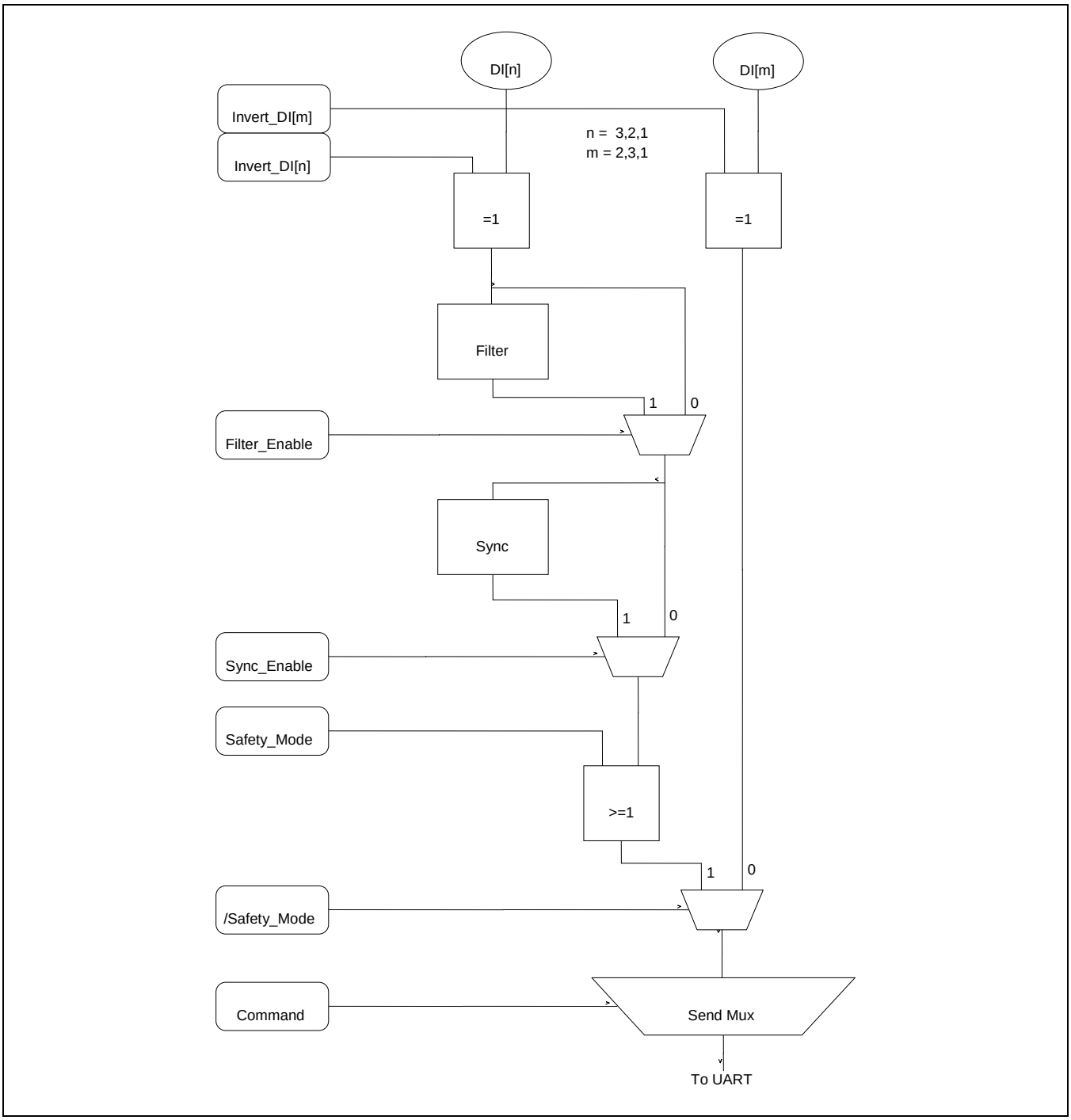


Figure 4.9 Flowchart – Input DI0 in Safety Mode

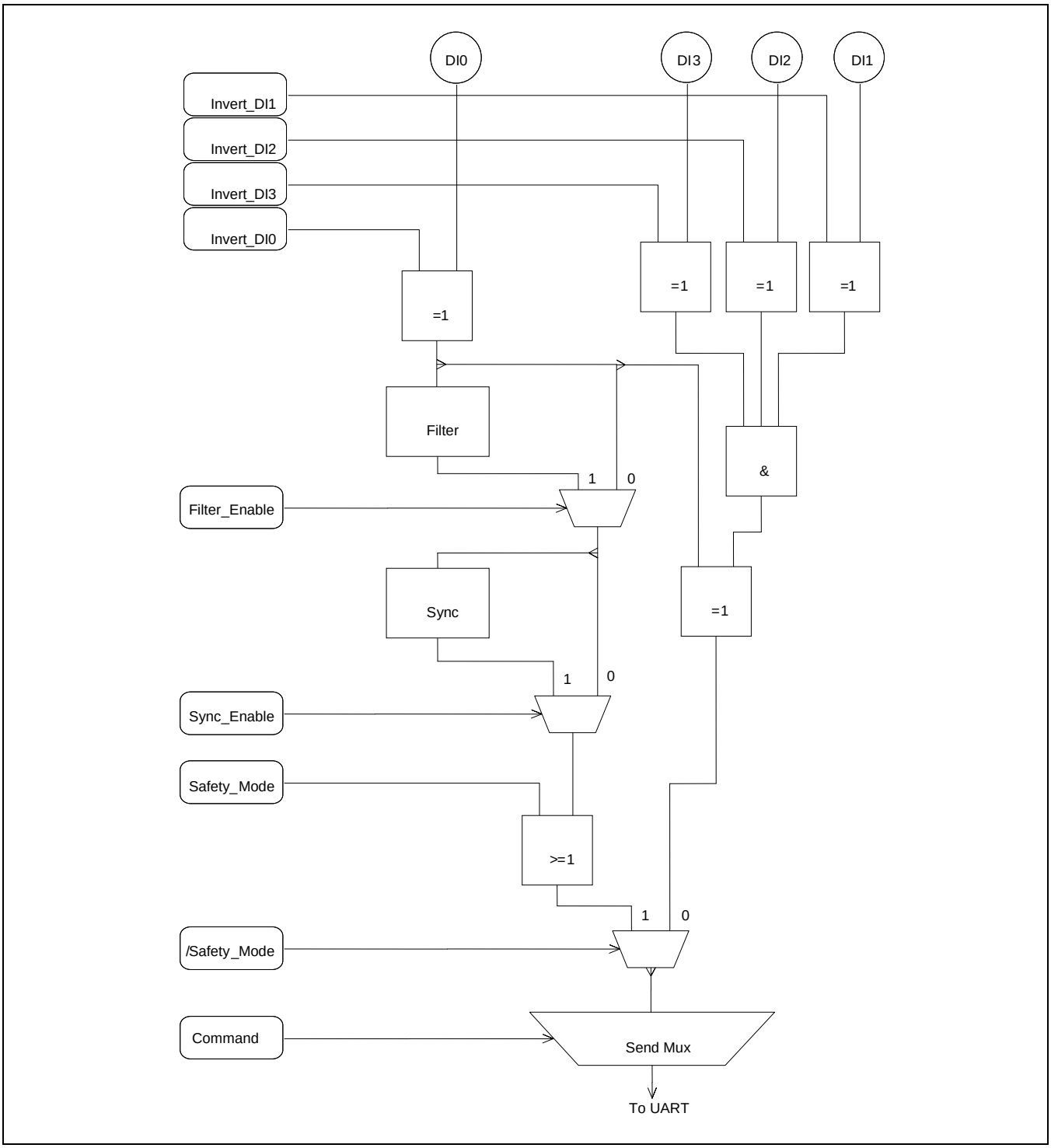
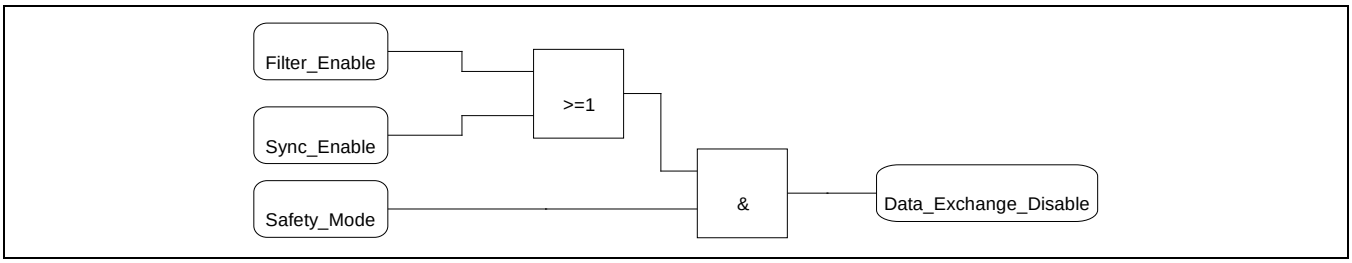


Figure 4.10 Flowchart – Data_Exchange_Disable



4.7.7. Master, Repeater, and Monitor Modes

In the Master, Repeater, and Monitor Modes, the configurations of the data input and data output ports are different than in Slave Mode. The control signals defined in Table 4.17 are provided at the data input port in the Master, Repeater, and Monitor Modes.

Table 4.17 Control Signal Inputs in the Master, Repeater, and Monitor Modes

DATA INPUT PORT	SIGNAL NAME	DESCRIPTION
DI0	*invert_ird_a*	If the signals *invert_ird_a* and *invert_ird_b* are not equal, the IRD input signal is inverted before further processing. See Table 4.6.
DI1	*invert_ird_b*	
DI2	*invert_led1_a*	If the signals *invert_led1_a* and *invert_led1_b* are not equal, the LED1 output signal is inverted after processing. See Table 4.21.
DI3	*invert_led1_b*	

Note: The complemented definition is designed to retain backward compatibility to A²SI-based AS-i Master designs.

The Data Output Port is used exclusively in Monitor Mode to provide additional UART error signals. The signals are defined to be active LOW and will be set immediately after a telegram error was detected. They become reset at the beginning of the next telegram. The signals described in Table 4.18 are available:

Table 4.18 Error Signal Outputs in Monitor Mode

DATA PORT OUTPUT	UART ERROR SIGNAL	DESCRIPTION	
DO0	plscod_err	Pulse Code Error	Indicates faulty AS-i pulses. This is a disjunction of alternation error, start bit error and end bit error. See section 4.12.1.
DO1	no_info_err	No Information Error Length Error	The output signal is a disjunction of *No_Information_Error* and *Length_Error* as defined in the *AS-Interface Complete Spec V3.0*. The Monitor Mode does not distinguish between synchronized and non-synchronized UART Mode. There is always only one bit time supervised after the end of a telegram.
DO2	parb_err	Parity Bit Error	Received parity bit does not match the check sum calculated by the UART.
DO3	ird_man_err	Manchester-II-Code Error at IRD input	Signal at IRD input violates Manchester-II-coding rules.

4.7.8. Special Function of DSR

In addition to its standard output function, the *Data Strobe* (DSR) pin serves as an external reset input for all operational modes of the IC. Pulling the DSR pin LOW for more than a minimum reset time generates an unconditioned reset of the IC, which is immediately followed by a re-initialization of the IC (EEPROM read out).

Further information on the IC reset behavior, especially for the signal timing, can be found in section 4.11.

4.8. Fault Indication Input Pin FID

4.8.1. Slave Mode

The fault indication input FID pin is provided for sensing a peripheral fault-messaging signal in Slave Mode. It has a high-voltage, high-impedance input stage that affects the status bit S1 of an AS-i Slave directly. The DC properties of the pin are specified in Table 4.7.

If the *FID_Invert* flag (Firmware Area of the EEPROM) is not set, a peripheral fault is signaled by a logic HIGH at the FID input. In this case, S1 and FID are logically equivalent, which is the default state.

If instead *FID_Invert* = '1', the FID input value is inverted before any further processing. The *FID_Invert* feature was added to provide special support for certain fault conditions.

Signal transitions at the FID pin become visible in S1 with a slight delay because the signal is first processed by a clock synchronizing circuit.

4.8.2. Master and Monitor Modes

In the Master and Monitor Modes, the FID input provides a voltage sense comparator for power failure detection. Its threshold voltage is set to 2.00V +/-3%.

A power failure event is recognized and displayed at the Parameter Port pin P1 if the input voltage falls below the reference voltage for more than 0.7 to 0.9 ms (see Table 4.10). No "Power Fail" signal is generated while the IC is performing its initialization procedure.

Table 4.19 Power Failure Detection at FID (Master Mode and Monitor Mode)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
FID reference voltage to detect a power failure	V_{FID-PF}	An external voltage divider is required for the measurement of the AS-I-voltage.	1.94.	2.06	V
Input resistance of FID input	R_{IN-FID}		2M		Ω
Power supply break down time to generate a "Power Fail" signal	t_{Loff}		0.7	0.9	ms

4.9. LED Outputs

4.9.1. Slave Mode

The ASI4U provides two LED pins for enhanced status indication: LED1 and LED2. Both pins contain NMOS open drain output drivers. In addition, LED2 contains a high-voltage, high-impedance input stage for purposes of the IC production test.

> Note: For compatibility to A²SI board layouts, where pin number 23 (former U5RD) must be connected to U5R, the **LED2** function is turned **OFF by default**, keeping LED2 always at the high impedance state. This is to protect LED2 against shorting the 5V supply (U5R) to ground. LED2 will be activated if the *Enhanced_Status_Indication* flag **and/or** the *Dual_LED_Mode* flag are set in the EEPROM.

In order to comply with the signaling schemes defined in the *AS-Interface Complete Specification V3.0,* a **red LED** must be connected to **LED1** and a **green LED** must be connected to **LED2.** Direct operation of a **dual LED** is also supported but requires the *Dual_LED_Mode* flag to be set. This is because LED1 and LED2 must be controlled differently for AS-Interface compliant dual LED signaling.

Table 4.20 gives the definitions for the status indications that are supported by the IC.

The flashing frequency of any flashing status indication is approximately **2Hz**.

As shown in Table 4.20, the LED2 pin is deactivated in Standard Status Indication Mode (i.e., when *Extended_Status_Indication* = ‘0’ and *Dual_LED_Mode* = ‘0’) for downward compatibility. In this case, the green LED must be connected directly to the UOUT pin or a different sensor supply.

Table 4.20 LED Status Indication

SYMPTOM	STANDARD STATUS INDICATION		EXTENDED STATUS INDICATION		NOTES
	Normal	Dual LED	Normal	Dual LED	
Power Off					No power supply available
Normal operation	green	green	green	green	Data communication is established
No data exchange	green red	red	green red	red	The *Data_Exchange_Disable* flag is still set, prohibiting Data Port communication. IC is waiting for a *Write_Parameter* request. The Communication Monitor has detected no Data Exchange status or the IC was reset by the Watchdog IC Reset.
No data exchange (Address=0)			green red	yellow red	Slave is waiting for address assignment. Data Port communication is not possible.
Peripheral Fault	green red	red/ green Alternating	green red Alternating	red/ green Alternating	Periphery Fault signal generated at FID input.
Serious Periphery Fault with Reset			green red	red	Data Strobe driven LOW for more than 44µs.

4.9.2. Communication via Addressing Channel

As soon as the Addressing Channel becomes activated for telegram communication (see section 4.3), LED1 is operated as an Addressing Channel output port. This output mode takes precedence over any status indication at LED1. If the *Dual_LED_Mode* flag is set, LED2 is switched to being inactive (high impedance) while the *Addressing Channel* is active. This is to avoid interference to the data communication by mixed optical signals.

4.9.3. Master, Repeater, and Monitor Modes

In the Master, Repeater, and Monitor Modes, LED1 provides the Manchester-II-coded, re-synchronized equivalent of the telegram signal received at the AS-i input channel. The polarity of the Manchester-II-coded bit stream depends on the values of the DI2 and DI3 pins.

Table 4.21 Polarity of Manchester-II Signal at LED1

INPUT VALUES AT DI2 AND DI3	DESCRIPTION
Equal (“11”, “00”)	Manchester-II signal is active HIGH (default logic output value at no communication is ‘0’). This mode is compatible with the A²SI LED output
Unequal (“01”, “10”)	Manchester-II signal is active LOW (default logic output value at no communication is ‘1’).

Note: The complemented definition is designed to retain backward compatibility to A²SI-based AS-i Master designs.

Every received AS-i telegram is checked for consistency with the protocol specifications and timing jitters are removed if they remain within the specified limits. If a telegram error is detected, the output signal becomes disrupted in such a way that subsequent logic can also recognize the Manchester-II-coded output signal as being erroneous.

LED2 is always logic HIGH (high impedance) in the Master, Repeater, and Monitor Modes to reduce internal power dissipation of the IC. In such applications, the green LED must be connected to the UOUT pin or different supply levels.

4.10. Oscillator Pins OSC1, OSC2

Table 4.22 Oscillator Pin Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	V_{OSC_IN}		-0.3		V_{U5R}	V
External parasitic capacitor at oscillator pins OSC1, OSC2	C_{OSC}		0		8	pF
Dedicated load capacity	C_{LOAD}			12		pF
Input ”low” voltage for external clock applied to OSC1	V_{IL}		0		1.5	V
Input ”high” voltage for external clock applied to OSC1	V_{IH}		3.5		V_{U5R}	V

4.11. IC Reset

Any IC reset turns the Data Output and Parameter Output registers to F_{HEX} and forces the corresponding output drivers to high impedance state. Except at power-on reset, Data Strobe and Parameter Strobe signals are simultaneously generated to visualize possibly changed output data to external circuitry.

The *Data_Exchange_Disable* flag becomes set during IC reset, prohibiting any data port activity right after IC initialization and as long as the external circuitry was not pre-conditioned by decent parameter output data. Consequently the AS-i master has to send a *Write_Parameter* call in advance of the first *Data_Exchange* request to an initialized slave. Following IC initialization times apply:

Table 4.23 IC Initialization Times

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Initialization time after software reset (generated by master calls *Reset_Slave* or *Broadcast_Reset*) or external reset via DSR [1)]	t_{INIT}			2	ms
Initialization time after power on [2)]	t_{INIT2}	$C_{UOUT} \leq 10\mu F$ (see Table 4.27)		30	ms
Initialization time after power on with high-capacitive load [1)]	t_{INIT3}	$C_{UOUT} = 470\mu F$		1000	ms

1) Guaranteed by design.
2) Power starts when V_{UIN} = 18V at the latest.

4.11.1. Power-On Reset

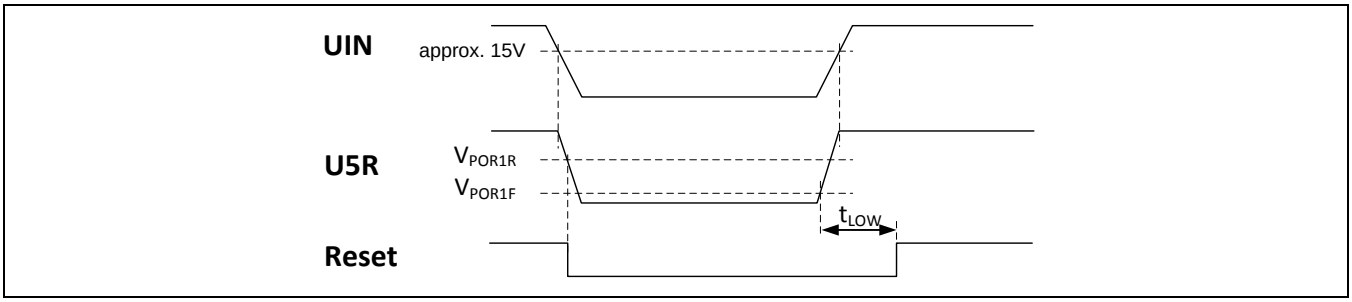
In order to force the IC into a defined state after power up and to avoid uncontrolled switching of the digital logic if the 5V supply (U5R) breaks down below a minimum level, a power-on reset is executed under the conditions listed in Table 4.24.

Table 4.24 Power-On Reset Threshold Voltages

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
V_{U5R} voltage to trigger internal reset procedure, falling voltage [1)]	V_{POR1F}		1.2	1.7	V
V_{U5R} voltage to trigger INIT procedure, rising voltage [1)]	V_{POR1R}		3.5	4.3	V
Power-on reset pulse width	t_{Low}		4	6	µs

1) Guaranteed by design.

Figure 4.11 Power-On Behavior (All Modes)



Note: The power-on reset circuit has a threshold voltage reference. This reference matches the process tolerance of the logic levels and therefore is not accurate. All values depend slightly on the rise and fall time of the supply voltage.

4.11.2. Logic Controlled Reset

The IC is also reset after reception of *Reset_Slave* or *Broadcast_Reset* commands, expiration of the Communication Watchdog (if enabled; see section 4.15), or entering a forbidden state machine state (i.e. due to heavy EMI).

Important Note: If the Addressing Channel is activated *and* the AC Current Input Mode is selected, *Reset_Slave* and *Broadcast_Reset* calls are processed differently than in normal operation. See corresponding explanations in section 4.3.

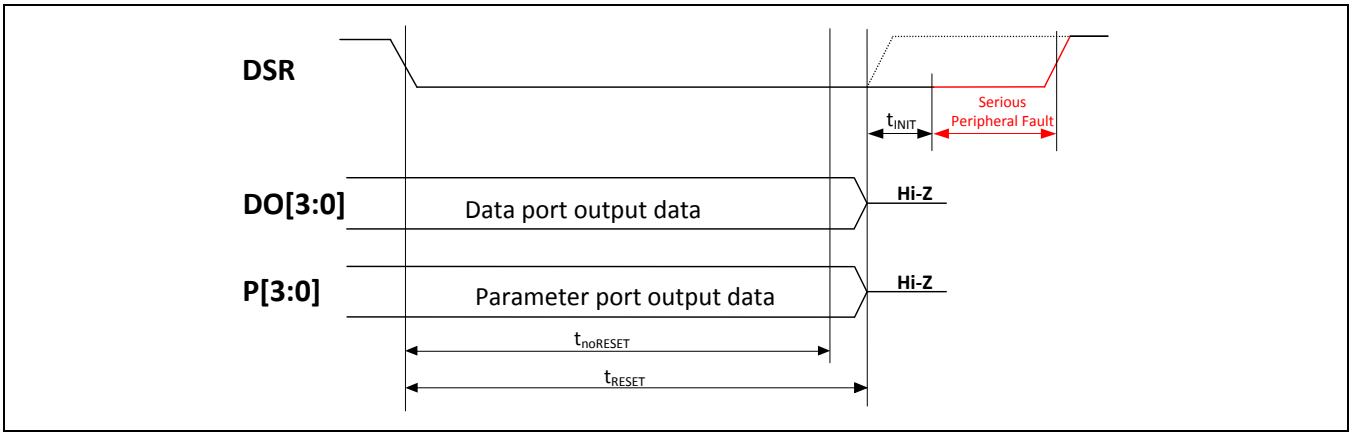
4.11.3. External Reset

The IC can be reset externally by pulling the DSR pin LOW for more than a minimum reset time. The external reset input function is provided in every operational mode of the IC: Slave Mode, Master Mode, Repeater Mode, and Monitor Mode. The signal timings given in Table 4.25 apply to all modes.

Table 4.25 Timing of External Reset

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
DSR LOW time for no reset initiation	$t_{noRESET}$			35	µs
Reset execution time for DSR HIGH/LOW transition to Hi-Z output drives at DO0 to DO3, P0 to P3	t_{RESET}			44	µs
State Machine initialization time after reset (EEPROM read out)	t_{INIT}			2	ms

Figure 4.12 Timing Diagram External Reset via DSR



In contrast to the A²SI, the external reset is generated "edge sensitive" to the expiration of the t_{RESET} timer. The initialization procedure starts immediately after the event, independent of the state of the DSR pin. A Serious Peripheral Fault is recognized in *Slave Mode* if DSR remains LOW after t_{RESET} + t_{INIT}. The corresponding error state display is described in section 4.9.

4.12. UART

The *UART* performs a syntactical and timing analysis of the received telegrams at both telegram input channels (AS-i input, Addressing Channel input), converts the pulse coded AS-i input signal into a Manchester-II-coded bit stream, and provides the Receive Register with decoded telegram bits.

The UART also performs the Manchester-II-coding of a slave answer (Slave Mode only) and controls the telegram data paths at the different operational modes of the IC (Slave Mode, Master Mode, Repeater Mode, and Monitor Mode).

In Slave Mode, data communication takes place on the AS-i input and AS-i output ports (AS-i receiver + AS-i transmitter) by default. The Addressing Channel (IRD input + LED1 output) can be activated by a Magic Sequence sent to the IRD input (see section 4.3). If the Addressing Channel is activated, the AS-i channel is turned inactive. Re-activation of the AS-i channel requires a reset of the IC.

In the Master, Repeater, and Monitor Modes, the output signal of the Manchester-II-coder (AS-i pulse to Manchester-II signal conversion) is resynchronized and forwarded to the LED1 pin. Any pulse timing jitters of the received AS-i signal are removed, if they are within the specified maximum limits. If the received AS-i telegram does not pass one of the error checks (see detailed descriptions in section 4.12.1), the LED1 output is distorted so that it no longer forms an AS-i telegram signal.

In the Master, Repeater, and Monitor Modes, the ASI4U provides a simple interface function between AS-i channel and Addressing Channel. The channel receiving an input signal first while the UART is in idle state (no active communication) is activated and locked until a communication pause is detected on that channel.

4.12.1. AS-i Input Channel

The comparator stages at the AS-i-line receiver generate two pulse-coded output signals (*p_pulse*, *n_pulse*) disjoining the positive and negative telegram pulses for further processing. To reduce UART sensitivity to erroneous spike pulses, pulse filters suppress any *p_pulse*, *n_pulse* activity of less than 750ns width.

After filtering, the *p_pulse* and *n_pulse* signals are checked in accordance with the *AS-Interface Complete Specification V3.0* for the following telegram transmission errors:

Start_bit_error The initial pulse following a pause must have negative polarity. Violation of this rule is detected as a *Start_bit_error*. The first pulse is the reference for bit decoding. The first bit detected must be the value 0.

Alternating_error Two consecutive pulses must have different polarity. Violation of this rule is detected as an *Alternating_error*.

Note: A negative pulse must be followed by a positive pulse and vice versa.

Timing_error Within any master request or slave response, the digital pulses that are generated by the receiver are checked to start in periods of $(n * 3\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 to 26 for a master request and n = 1 to 12 for a slave response. Violation of this rule is detected as a *Timing_error.*

Note: There is a specific pulse timing jitter associated with the receiver output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages.

In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the *AS-Interface Complete Specification V3.0*.

No_information_error As derived from the Manchester-II-Coding rule, either a positive or negative pulse must be detected in periods of $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start of the initial negative pulse, where n = 1 to 13 for a master request and n = 1 to 6 for a slave response. Violation of this rule is detected as a *No_information_error*.

Note: The timing specification relates to the receiver comparator output signals. There is a specific pulse timing jitter in the digital output signals (compared to the analog signal waveform) due to sampling and offset effects at the comparator stages.

In order to take the jitter effects into account, the timing tolerance specifications differ slightly from the definitions of the AS-Interface Complete Specification.

Parity_error The sum of all information bits in master requests or slave responses (excluding start and end bits, including the parity bit) must be even. Violation of this rule is detected as a *Parity_error.*

End_bit_error The pulse to be detected $(n * 6\mu s)^{+1.500\mu s}_{-0.875\mu s}$ after the start pulse must be of positive polarity, where n = 13 (i.e., 78 µs) for a master request and n = 6 (i.e., 36 µs) for a slave response. Violation of this rule is detected as an *End_bit_error.*

Note: This stop pulse must finish a master request or slave response.

Length_error Telegram length supervision is processed as follows. A *Length_error* is detected if a signal different from a pause is detected under any of these three conditions: during the first bit time after the end pulse of a master request (equivalent to the 15th bit time) for synchronized slaves; during the first three bit times for non-synchronized slaves (equivalent to the bit times 15 to 17); or during the first bit time after the end pulse of a slave response (equivalent to the 8th bit time).

If at least one of these errors occurs, the received telegram is treated as invalid. In this case, the UART will not generate a Receive Strobe signal, move to asynchronous state, and wait for a pause at the AS-i line input. After a pause has been detected, the UART is ready to receive the next telegram.

Receive Strobe signals are generally used to validate the correctness of the received data. In the Master and Monitor Modes, the signals are visible at the *Parameter Ports* for further processing by external circuitry. Corresponding Parameter Port configurations can be found in Table 4.10.

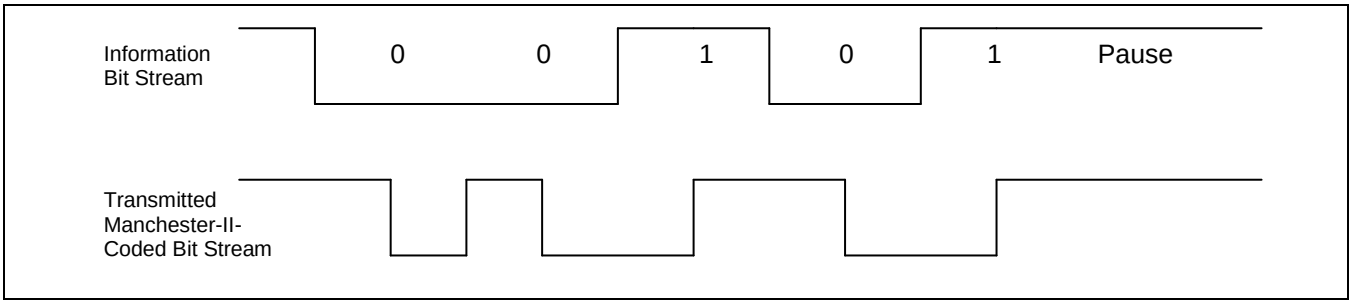
In Slave Mode, a Master Receive Strobe starts the internal processing of a master request. If the UART was in asynchronous state before the signal was generated, it changes to synchronous state thereafter. If the received slave address matches the stored address of the IC, the transmitter is turned on by the Receive Strobe pulse, letting the output driver settle smoothly at the operation point.

4.12.2. Addressing Channel

The signal logic of the Addressing Channel follows the definition of a Manchester-II-coded AS-i signal. The default state (inactive) is defined by a logic HIGH value. Depending on the input mode of the IRD pin (voltage/current) a logic HIGH is either represented by a voltage signal above 2.5V or an input current above $I_{IRD_Offset} + I_{IRD_Amplitude.}$ (see Table 4.3).

A valid communication is started on a falling edge of the input signal (middle of the start bit) and ended on a rising signal edge (middle of the end bit) and followed by the detection of a telegram pause. The information is represented by falling (= ‘0’) or rising (= ‘1’) signal transitions in the middle of every bit time (see Figure 4.13).

Figure 4.13 Manchester-II-Coded Modulation Principle



Equivalent to the AS-i input channel checks, the signals received at the Addressing Channel input (IRD pin) are checked for telegram transmission errors. The checking, however, is only performed in Slave Mode. In the Master, Repeater, and Monitor Modes, the IRD signal is checked only for logical correctness. It is directly forwarded to the AS-i line transmitter avoiding any additional logic delays.

Note: Because the telegram checking is disabled on the Addressing Channel in the Master, Repeater, and Monitor Modes, corresponding Receive Strobe signals are neither displayed at the Parameter Ports nor generated for internal purposes.

The master control logic must care to deliver correctly timed Manchester-II signals, ensuring that the resulting AS-i telegrams fulfill the specified timing limits.

The following telegram transmission errors are detected in Slave Mode:

Start_bit_error The initial signal transition (after a pause) must be of the falling edge. Violation of this rule is detected as a *Start_bit_error*.

No_information_error Within a received telegram, signal transitions (of the rising or falling edge) must occur in periods of $(n * 6\mu s)^{+2.000\mu s}_{-1.000\mu s}$ after the initial falling slope, where n = 1 to 13. Violation of this rule is detected as a *No_information_error*.

Note: The Addressing Channel input (IRD) only accepts master requests in Slave Mode.

Parity_error The sum of all information bits in master requests (excluding start and end bits, including the parity bit) must be even. Violation of this rule is detected as a *Parity_error*.

End_bit_error The signal transition to be detected 13 ∗ 6 µs (i.e., 78 µs) after the initial falling start transition, must be of rising slope. Violation of this rule is detected as an *End_bit_error*.

Note: This stop transition must finish the master request.

Length_error A *Length_error* is detected if a signal different from a pause is detected during the first bit time after the end pulse of a master request (equivalent to the 15th bit time) for synchronized slaves or during the first three bit times for non-synchronized slaves (equivalent to the bit times 15 to 17).

4.13. Main State Machine

The State Machine controls the overall behavior of the IC. Depending on the configuration data stored in the EEPROM, the State Machine activates one of the different IC operational modes and controls the digital I/O ports accordingly. In Slave Mode, it processes the received master telegrams and computes the contents of the slave answer if required. Table 3.2 on page 19 lists all master calls that are decoded by the ASI4U in Slave Mode.

To prevent the critical situation in which the IC gets locked in a prohibited state (e.g., due to exposure to strong electromagnetic radiation) and could thereby jeopardize the entire system, all prohibited states of the State Machine will cause an unconditioned logic reset that is comparable to the AS-i call ”Reset Slave (RES).”

4.14. Status Registers

Table 4.26 shows the ASI4U status register content. The use of status bits S0, S1, and S3 is compliant to the *AS-Interface Complete Specification V3.0*. Status bit S2 is not used. The status register content can be determined by use of a *Read Status* (RDST) master request (refer to Table 3.2).

Table 4.26 Status Register Content

Status Register Bit	Sx = 0	Sx = 1
S0	EEPROM write accessible.	Slave address stored volatile and/or EEPROM access blocked (write in progress). [1]
S1	No peripheral fault detected. EEPROM Firmware Area and Safety Area content consistent	Peripheral fault detected. Parity bit error in EEPROM Firmware Area or Safety Area.
S2	Static zero.	N/A
S3	EEPROM content consistent.	EEPROM contains corrupted data.

1) Status bit S0 is set to '1' if a Delete Address (*DELA)* master request has been received and the slave address was not equal to "0" before. Additionally, it is set for the entire duration of each EEPROM write access.

4.15. Communication Monitor/Watchdog

The IC contains an independent Communication Monitor that observes the processing of *Data_Exchange* and *Write_Parameter* requests. If no such requests have been processed for more than 40.960ms (+5%), the Communication Monitor recognizes a No Data/Parameter Exchange status and turns the red status LED (LED1) on. Any subsequent *Data_Exchange* or *Write_Parameter* request will let the Communication Monitor start over and turn the red status LED off.

The Communication Monitor is only activated at slave addresses unequal to zero (0) and while the IC is processing the first *Write_Parameter* request after initialization. It becomes deactivated at any IC reset or after the reception of a *Delete_Address* Request.

If the *Watchdog_Active* flag (EEPROM Firmware Area) is set *or* the *P0_Watchdog_Activation* flag is set and Parameter Port P0 is logic HIGH, the Communication Monitor is switched to the Watchdog Mode.

If the Communication Monitor detects a No Data/Parameter Exchange status in active Watchdog Mode, it immediately invokes an unconditioned IC reset, switching all Data and Parameter outputs inactive, generating corresponding Data and Parameter Strobe signals, setting the *Data_Exchange_Disable* flag, and starting the IC initialization procedure.

In order to resume normal Data Port communication after *a* Watchdog IC Reset, the master must send a *Write_Parameter* request again before Data Port communication can be reestablished. This ensures new parameter setup of any connected external circuitry.

4.16. Toggle Watchdog for 4I/4O Processing in Extended Address Mode

As described in section 4.7.5, a special 4I/4O data processing is supported in Extended Address Mode. The transmission of a 4-bit wide output word is achieved by alternation of a high and a low nibble in consecutive transactions. To ensure that both output nibbles become refreshed continuously by the master, the alternation of the I2 bit in the *Data_Exchange* call can be supervised by an I2 Toggle Watchdog in the IC.

The Toggle Watchdog is enabled at slave addresses unequal to zero (0) and while the IC is processing the first data output event after initialization. It becomes disabled at any IC reset or after the reception of a *Delete_Address* request.

The Toggle Watchdog function becomes activated only if the IC is operated in 4I/4O Mode (*ID_Code* = A_{HEX}, *Ext_Addr_4I/4O_Mode* = '1') *and* if either the *Watchdog_Active* flag is set in the EEPROM *or* the *P0_Watchdog_Activation* flag (EEPROM) is set and Parameter Port P0 is logic HIGH.

If there is no alternation of bit I2 for **327ms (+16ms)** at any time after the enable event, an activated Toggle Watchdog invokes an unconditioned IC reset, switching all Data and Parameter outputs inactive, generating corresponding Data and Parameter Strobe signals, setting the *Data_Exchange_Disable* flag, and starting the IC initialization procedure. Thus, the reaction of the IC is the same as for an expired Communication Watchdog.

4.17. Write Protection of *ID_Code_Extension_1*

The *ID_Code_Extension_1* register can either be manufacturer configurable or user configurable.

- **Manufacturer configurable**: If the flag *ID_Code1_Protect* is set ('1') in the Firmware Area of the EEPROM, *ID_Code_Extension_1* is manufacturer configurable.
  In this case the slave response to a *Read_ID_Code_1* request is constructed from the data stored in the *Protected_ID_Code_Extension_1* register in the Firmware Area of the EEPROM.

  It does not matter which data is stored in the *ID_Code_Extension_1* register in the User Area. The IC will always respond with the protected manufacturer programmed value.

  There is one exception to this principle. If the IC is operated in Extended Address Mode, bit 3 of the returned slave response is taken from the *ID_Code_Extension_1* register in the *User Area*. This is because bit 3 functions as the A/B Slave selector bit in this case and must remain user configurable.

  To ensure consistency of the *ID_Code_Extension_1* stored in the data image of the master as well as in the EEPROM of the slave, the ASI4U <u>will not process a *Write_ID_Code1* request</u> if the data sent does not match the data that is stored in protected part of the *ID_Code_Extension_1* register. It will neither access the EEPROM nor send a slave response in this case.

  Note: As defined in the *AS-Interface Complete Specification*, a modification of the A/B Slave selector bit must be performed bit selective. This means the AS-i master must read the *ID_Code_Extension_1* first, modify bit 3, and send the new 4-bit word that consists of the modified bit 3 and the unmodified bits 2 to 0 back to the slave.

- **User configurable**: If the *ID_Code1_Protect* flag is *not* set ('0'), *ID_Code_Extension_1* is completely user configurable. The data to construct the slave response to a *Read_ID_Code_1* request is taken completely from the *ID_Code_Extension_1* register in the User Area.
  In this configuration, a *Write_ID_Code1* request will always be answered and initiate an EEPROM write access procedure.

4.18. Power Supply

The power supply block provides a sensor supply, which is inductively decoupled from the AS-i bus voltage, at pin UOUT. The decoupling is realized by an electronic inductor circuit, which basically consists of a current source and a controlling low pass filter. The time constant of the low pass, which affects the input impedance at the UIN pin, can be adjusted by an external capacitor at the CAP pin.

The electronic inductor can be turned off if the CAP pin is connected to 0V. This shuts down the current source between UIN and UOUT requiring an external connection between UIN and UOUT for proper IC operation. The ability to turn off the electronic inductor is helpful for designing high symmetrical extended power applications (e.g., AS-i-connected actuators with large load currents).

Overloading the electronic inductor for more than 2 seconds by drawing too much current shuts down the entire IC in order to avoid a deviation of the input impedance, which would have a negative effect on the communication of the remaining AS-i network clients. The Fail-Safe Shutdown Mode can only be left by power cycling the AS-i supply voltage.

A second function of the power supply block is to generate a regulated 5V supply for operation of the internal logic and some analog circuitry. The voltage is provided at the U5R pin and can be used to supply external circuitry as well, if the current requirements remain within in the specified limits (see Table 4.27). Because the 5V supply is generated out of the decoupled sensor supply at UOUT, the current drawn at U5R must be subtracted from the total available load current at UOUT.

The power supply dissipates the major amount of power (see Table 4.27):

$$P_{tot} = V_{Drop} * I_{UOUT} + (V_{UOUT} - 5V) * I_{5V}$$

In total, the power dissipation must not exceed the specified values of section 2.1.

To cope with fast internal and external load changes (spikes) external capacitors at UOUT and U5R are required. The 0V pin defines the ground reference voltage for both UOUT and U5R.

4.18.1. Voltage Output Pins UOUT and U5R

Table 4.27 Properties of Voltage Output Pins UOUT and U5R

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Positive supply voltage for IC operation [1)]	V_{UIN}		16	33.1	V
Voltage drop from UIN pin to UOUT pin [2)]	V_{DROP}	V_{UIN} > 22V	5.5	6.7	V
UOUT output supply voltage	V_{UOUT}	I_{UOUT} = $I_{UOUTmax}$	V_{UIN}- $V_{DROPmax}$	V_{UIN}- $V_{DROPmin}$	V
UOUT output voltage pulse deviation [2)]	V_{UOUTp}	C_{UOUT} = 10µF		1.5	V
UOUT output voltage pulse deviation width [2)]	t_{UOUTp}	C_{UOUT} = 10µF		2	ms
5V supply voltage	V_{U5R}		4.5	5.5	V
UOUT output supply current [2)]	I_{UOUT}	I_{U5R} = 0	0	55	mA
U5R output supply current	I_{U5R}		0	4	mA
Total output current I_{UOUT} + I_{5V}	I_o			55	mA
Short circuit output current	I_{UOUTS}		50		mA
Blocking capacitance at UOUT	C_{UOUT}		10	470	µF
Blocking capacitance at U5R	C_{U5R}		1		µF

1) Parameter is also given in Table 2.2.

2) C_{UOUT} = 10µF; output current switches from 0 to $I_{UOUTmax}$ and vice versa.

4.18.2. Input Impedance (AS-Interface Bus Load)

The following parameters are determined with a short circuit between the pins ASIP and UIN and the pins ASIN and 0V, respectively.

Table 4.28 AS-Interface Bus Load Properties

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Equivalent resistance of the IC [1), 2)]	R_{IN1}		13.5		kΩ
Equivalent inductance of the IC [1), 2)]	L_{IN1}		13.5		mH
Equivalent capacitance of the IC [1), 2)]	C_{IN1}			30	pF
Equivalent resistance of the IC [1), 2)]	R_{IN2}		13.5		kΩ
Equivalent inductance of the IC [1), 2)]	L_{IN2}		12	13.5	mH
Equivalent capacitance of the IC [1), 2)]	C_{IN2}			15 + (L-12mH)∗10pF/mH	pF
Parasitic capacitance of the external over-voltage protection diode (Zener diode) [1)]	C_{Zener}			20	pF

1) The equivalent circuit of a slave, which is calculated from the impedance of the IC and the paralleled external over-voltage protection diode (Zener diode), must satisfy the requirements of the *AS-Interface Complete Specification* for Extended Address Mode slaves.

2) After the maximum parasitic capacitance of the external over-voltage protection diode (20pF) has been subtracted, the specifications group including R_{IN1}, L_{IN1} and C_{IN1} or the specifications group including R_{IN2}, L_{IN2} and C_{IN2} must be met for compliance with the *AS-Interface Complete Specification V3.0*.

Table 4.29 CAP Pin Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	Typical	MAX	UNIT
Input voltage range	V_{CAP_IN}		-0.3		V_{U5R}	V
External decoupling capacitor	C_{CAP}			47		nF

Note: In some applications, a resistor connected in series with C_{CAP} might improve the impedance behavior of the internal electronic inductor. Depending of the application, this resistor must be dimensioned in the range of 10Ω to 100Ω.

The decoupling capacitor defines an internal low-pass filter time constant; lower values decrease the impedance but improve the turn-on time. Higher values do not improve the impedance but do increase the turn-on time.

The turn-on time also depends on the load capacitor at UOUT. After connecting the slave to the power, the capacitor is charged with the maximum current I_{UOUT}. The impedance will increase when the voltage allows the analog circuitry to fully operate.

4.19. Thermal and Overload Protection

The IC continuously observes its silicon die temperature. If the temperature rises above approximately 140°C for more than 2 seconds, the IC will be put into shutdown and stay there until the next power-on reset occurs.

The circuit is also shut down if UOUT pin is overloaded (e.g., shorted to GND) for more than 2 seconds.

Table 4.30 Shutdown Temperature

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Chip temperature for over-temperature shut down	T_{Shut}		125	160	°C

5 Application Circuits

The following figures show typical application cases for the ASI4U. Note that these schematics show only basic circuit principles. For more detailed application information, see the *ASI4U Application Note – Evaluation Board.* Figure 5.1 outlines a standard slave application circuit. Figure 5.2 shows an extended power application circuit with an externally decoupled sensor supply. A Master/Repeater Mode application is shown in Figure 5.3.

Figure 5.1 Standard Application Circuit with Bi-directional Data I/O

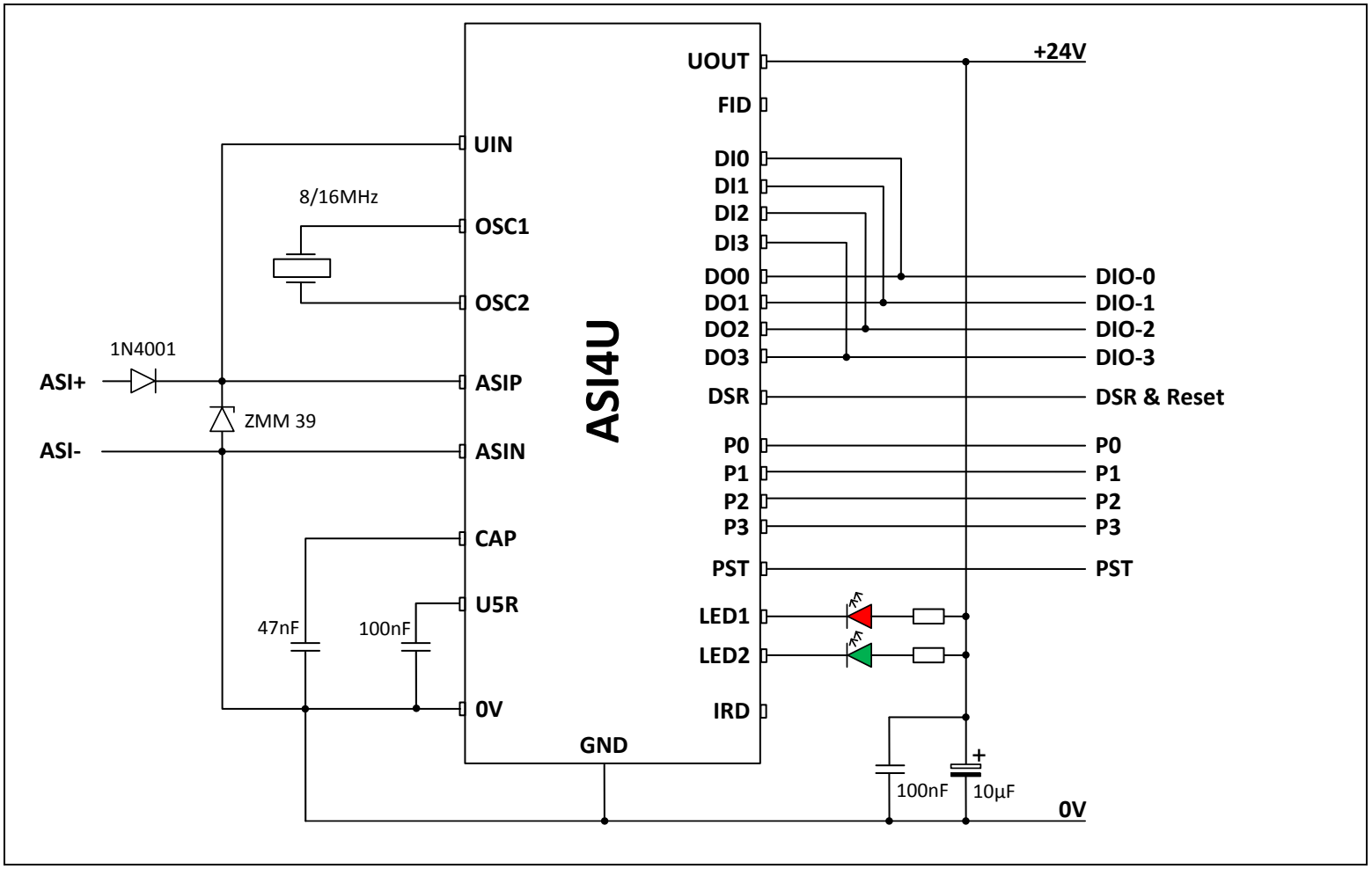


Figure 5.2 Extended Power Application Circuit with IR-Addressing Option

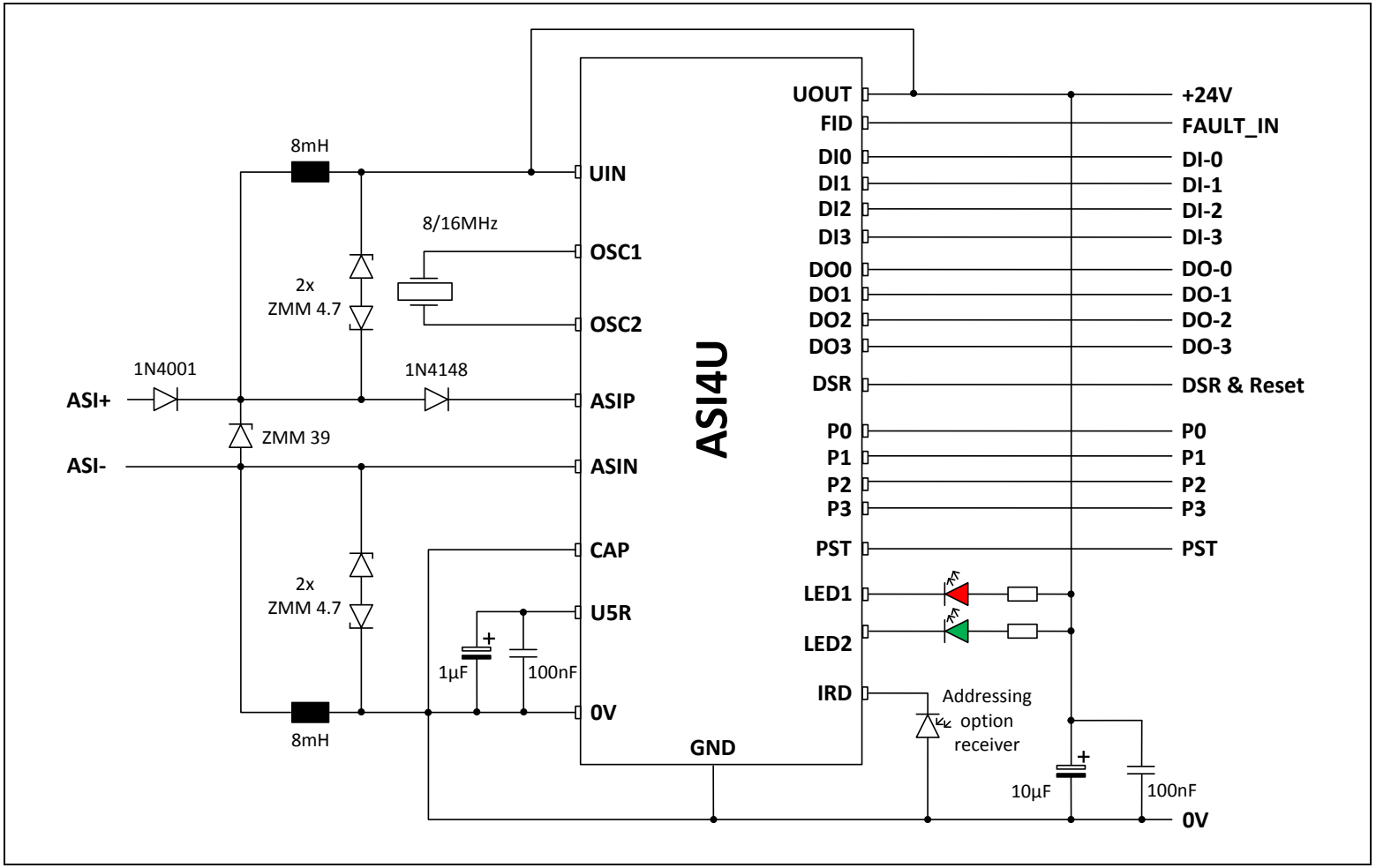
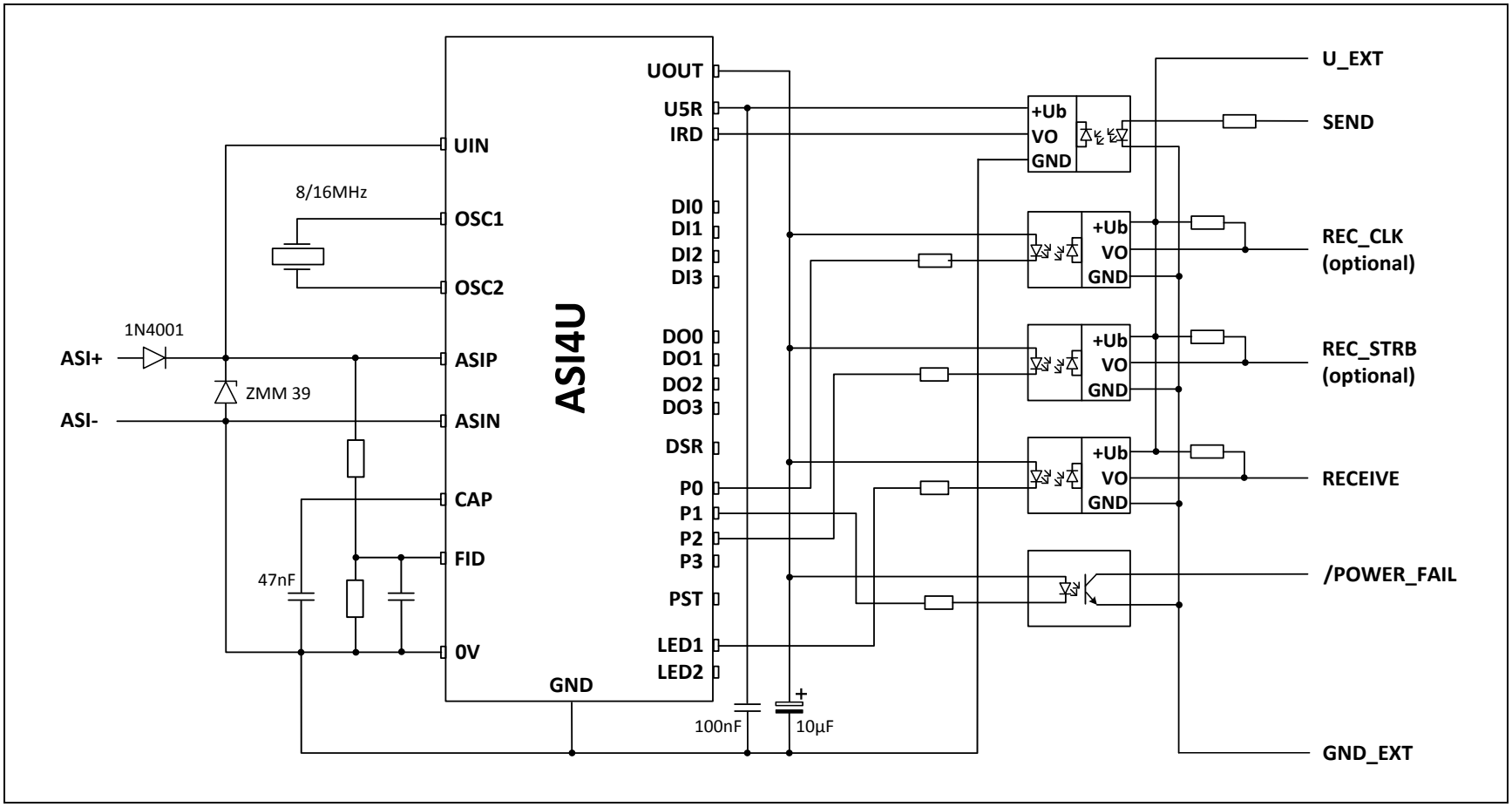


Figure 5.3 ASI4U Master/Repeater Mode Application



6 Package Specifications

6.1. Package Pin Assignment

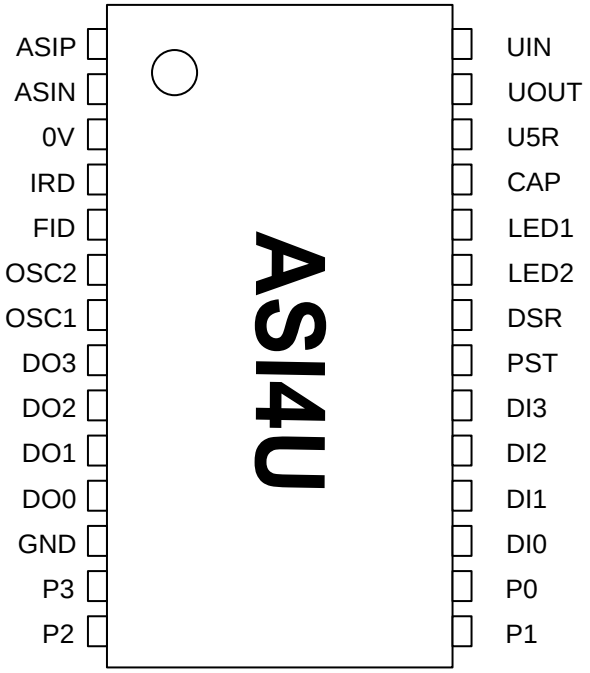
Table 6.1 ASI4U Package Pin List

Note: All open drain outputs are NMOS based. Pull-up properties at input stages are achieved by current sources referenced to U5R.

PIN	NAME	DIRECTION	TYPE	DESCRIPTION
1	ASIP	IN	Analog	AS-i transmitter/receiver input; to be connected to the ASI+ lead of the AS-i cable via a reverse-polarity protection diode
2	ASIN	OUT	Analog	AS-i transmitter/receiver output; to be connected to the ASI- lead of the AS-i cable
3	0V		Supply	IC ground; common ground for all IC ports except ASIP and ASIN; to be connected to ASIN if no external coils are used
4	IRD	IN	Analog / CMOS (5V)	Addressing Channel input
5	FID	IN	Pull-up	Peripheral fault input
6	OSC2	OUT	Analog (5V)	Crystal oscillator
7	OSC1	IN	Analog / CMOS (5V)	Crystal oscillator / external clock input
8	DO3	OUT	Open drain	Data port output D3
9	DO2	OUT	Open drain	Data port output D2
10	DO1	OUT	Open drain	Data port output D1
11	DO0	OUT	Open drain	Data port output D0
12	GND		Supply	Digital I/O ground; to be connected to 0V
13	P3	I/O	Pull-up / open drain	Parameter port P3
14	P2	I/O	Pull-up / open drain	Parameter port P2 / Receive Strobe output in Master Mode
15	P1	I/O	Pull-up / open drain	Parameter port P1 / Power Fail output in Master Mode
16	P0	I/O	Pull-up / open drain	Parameter port P0 / data clock output in Master Mode
17	DI0	IN	Pull-up	Data port input D0
18	DI1	IN	Pull-up	Data port input D1
19	DI2	IN	Pull-up	Data port input D2
20	DI3	IN	Pull-up	Data port input D3
21	PST	I/O	Pull-up / open drain	Parameter strobe output (input function used for IC test purposes only)
22	DSR	I/O	Pull-up / open drain	Data strobe output / reset input
23	LED2	OUT	Open drain	Enhanced diagnosis LED output; to be activated by the *Enhanced_Status_Indication* flag in the Firmware Area of the EEPROM

PIN	NAME	DIRECTION	TYPE	DESCRIPTION
24	LED1	I/O	Pull-up / open drain	AS-i diagnostic LED output / Addressing Channel output (input function used for IC test purposes only)
25	CAP	I/O	Analog	Filter control (electronic inductor)
26	U5R	OUT	Analog	Regulated internal/external 5V supply
27	UOUT	OUT	Analog	Decoupled actuator/sensor supply
28	UIN		Supply	Power supply input

Figure 6.1 ASI4U Package Pin Assignment



6.2. SOP28 Package Outline for ASI4U-E

The ASI4U-E is packaged in a 28-pin SOP-package. Its dimensions are given in Figure 6.2 and Table 6.2.

Figure 6.2 SOP28 Package Outline Dimensions

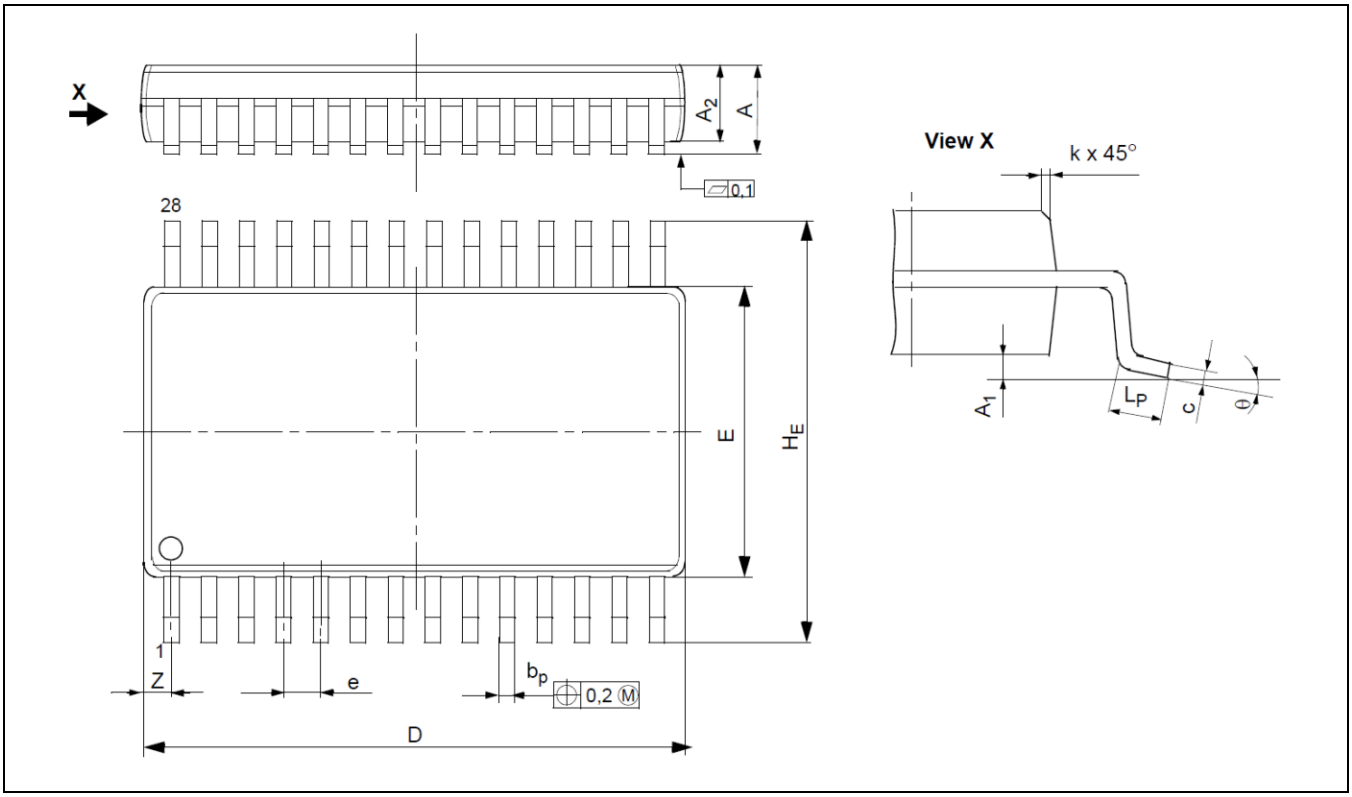


Table 6.2 SOP28 Package Dimensions (mm)

Symbol	A	A_1	A_2	b_P	c	e	D	E	H_E	k	L_P	Z	θ
Nominal						1.27							
Minimum	2.35	0.10	2.25	0.35	0.23		17.70	7.40	10.01	0.25	0.40		0°
Maximum	2.65	0.30	2.45	0.49	0.32		18.10	7.60	10.64			0.81	8°

6.3. SSOP28 Package Outline for ASI4U and ASI4U-F

The ASI4U and ASI4U-F have a 28-pin SSOP-package. The dimensions are given in Figure 6.3 and Table 6.3.

Figure 6.3 SSOP28 Package Outline Dimensions

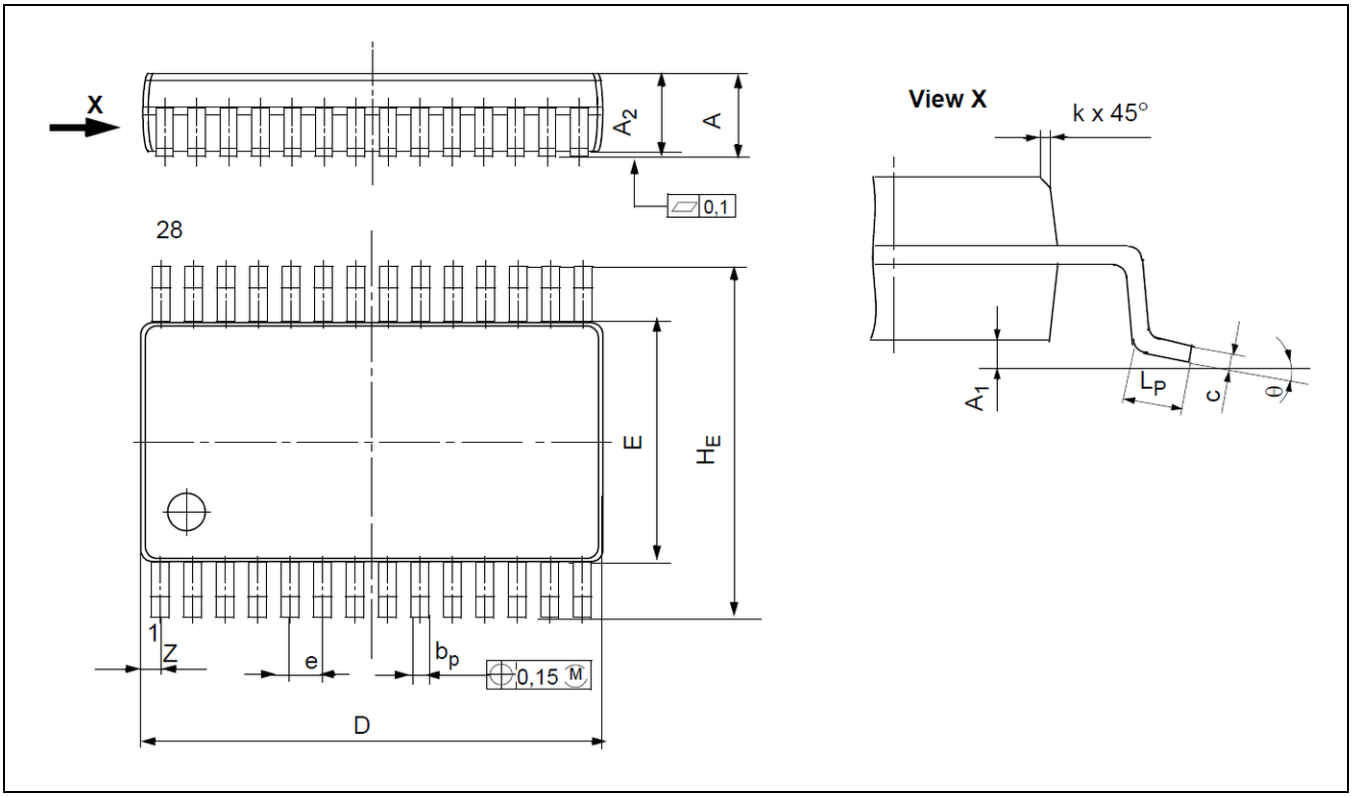
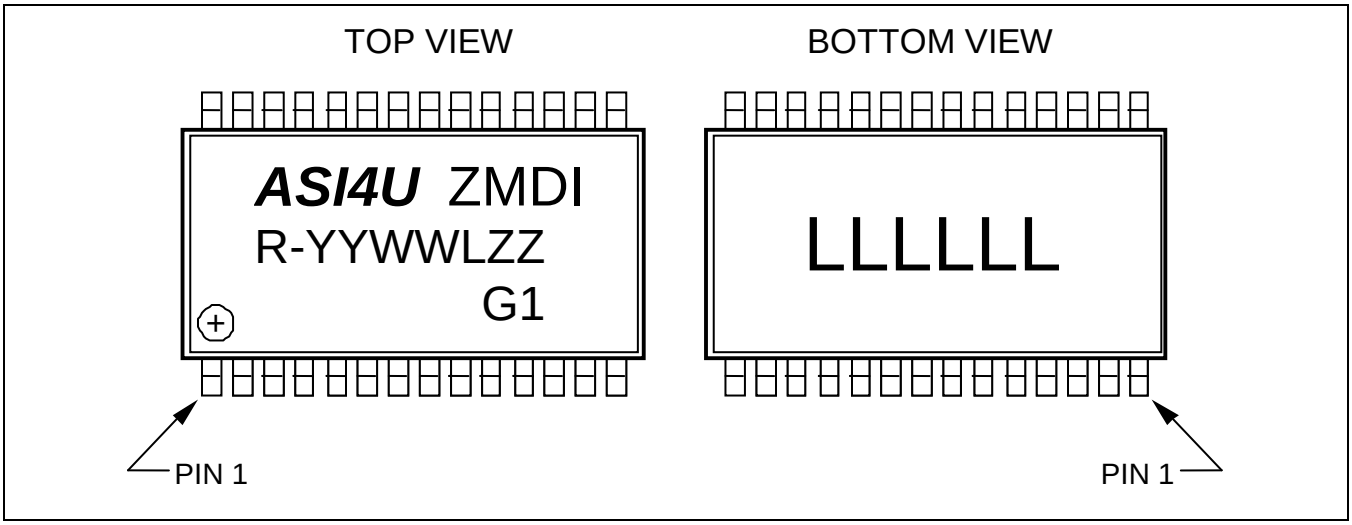


Table 6.3 SSOP28 Package Dimensions (mm)

Symbol	A	A_1	A_2	b_P	c	e	D	E	H_E	k	L_P	Z	θ
Nominal						0.65							
Minimum	1.73	0.05	1.68	0.25	0.09		10.07	5.20	7.65	0.25	0.63		0°
Maximum	1.99	0.21	1.78	0.38	0.20		10.33	5.38	7.90			1.22	10°

6.4. Package Marking

Figure 6.4 Package Marking



Top Marking:

ASI4U or ASI4U-E or ASI4U-F	Product name
IDT	Manufacturer
R	Revision code
YYWW	Date code (year and week)
L	Assembly location
ZZ	Traceability code
G1	“Green” RoHS-compliant package

Bottom Marking:

LLLLLL	IDT Lot Number

For ICs pre-programmed to Master Mode, the string “-M” follows the product name.

For ICs with an operation temperature up to 105°C, the string “-E” follows the product name.

For ICs with an operation temperature up to -40°C, the string “-F” follows the product name.

7 Ordering Information

Ordering Code	Type	Package	T_a [°C]	RoHS Conform	Packaging	Minimum Order Quantity
ASI4UE-G1-ST	Standard	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-SR	Standard	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-G1-SR-7	Standard	SSOP28	-25 to 85	Y	Tape & Reel 7” (500 parts/reel)	500
ASI4UE-G1-MT	Master	SSOP28	-25 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-G1-MR	Master	SSOP28	-25 to 85	Y	Tape & Reel (1500 parts/reel)	1500
ASI4UE-E-G1-ST	Standard	SOP28	-25 to 105	Y	Tube (27 parts/tube)	270
ASI4UE-E-G1-SR	Standard	SOP28	-25 to 105	Y	Tape & Reel (1000 parts/reel)	1000
ASI4UE-F-G1-ST	Standard	SSOP28	-40 to 85	Y	Tube (47 parts/tube)	470
ASI4UE-F-G1-SR	Standard	SSOP28	-40 to 85	Y	Tape & Reel (1500 parts/reel)	1500

8 Related Documents

Document
ASI4U/ASI4U-E/ASI4U-F Feature Sheet
ASI4U/ASI4U-E/ASI4U-F Release Note RevE
ASI4U/ASI4U-E/ASI4U-F Errata Sheet
*Production and Repair of AS-i Safety Slaves **
*ASI4U Application Note – Evaluation Board **

Visit the *ASI4U/ASI4U-E/ASI4U-F* web page at www.IDT.com/products/as-interface/ASI4U or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) require a free customer login account..

9 Glossary

Term	Description
DEXG	Data Exchange
DSR	Data Strobe and Reset
EMI	Electromagnetic Interference
FID	Fault Indication
IRD	Integrated Receiver/Decoder
PST	Parameter Strobe
UART	Universal Asynchronous Receiver/Transmitter
WPAR	Write Parameter

10 Document Revision History

Revision	Date	Description
1.00	August 9, 2005	First release.
1.07	April 10, 2008	ASI4U-E added
2.20	April 2, 2012	ASI4U-F added
2.30	April 13, 2015	Section 4.14 status registers added. Update for contact information and imagery for cover and headers. Formatting revisions.
	January 26, 2016	Changed to IDT branding.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.