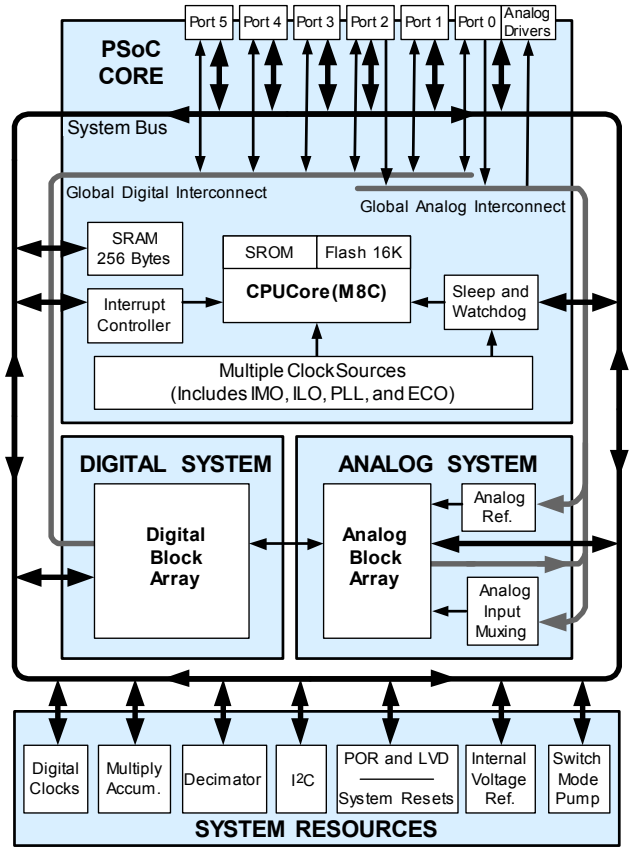
# CY8C27143, CY8C27243
# CY8C27443, CY8C27543, CY8C27643

## PSoC® Programmable System-on-Chip™

## Features

- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3.0 to 5.25V Operating Voltage
  - Operating Voltages Down to 1.0V Using On-Chip Switch Mode Pump (SMP)
  - Industrial Temperature Range: -40°C to +85°C
- Advanced Peripherals (PSoC® Blocks)
  - 12 Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 8 Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Up to 2 Full-Duplex UARTs
    - Multiple SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- Precision, Programmable Clocking
  - Internal 2.5% 24/48 MHz Oscillator
  - 24/48 MHz with Optional 32 kHz Crystal
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep
- Flexible On-Chip Memory
  - 16K Flash Program Storage 50,000 Erase/Write Cycles
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - a. 25 mA Sink on all GPIO
  - b. Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - c. Up to 12 Analog Inputs on GPIO
  - d. Four 30 mA Analog Outputs on GPIO
  - e. Configurable Interrupt on all GPIO
- Additional System Resources
  - I2C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Trace Memory

### Logic Block Diagram



## PSoC Functional Overview

The PSoC® family consists of many *Programmable System-on-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C27x43 family can have up to five IO ports that connect to the global digital and analog interconnects, providing access to 8 digital blocks and 12 analog blocks.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

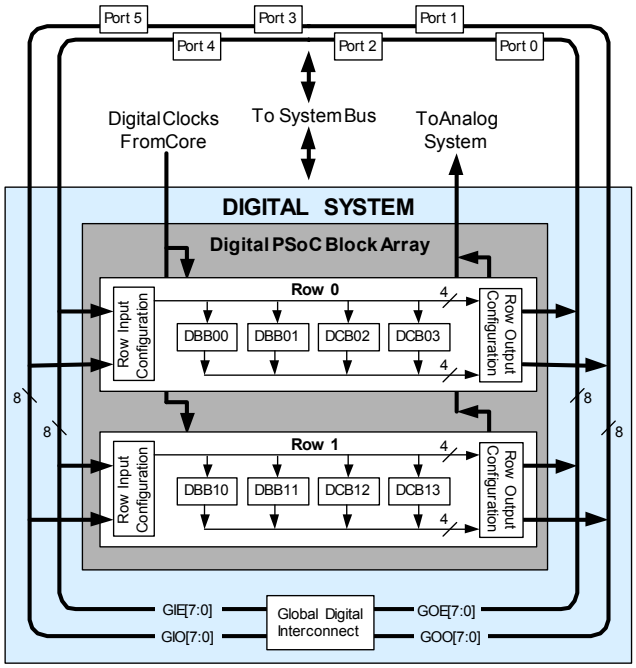
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

### Digital System

The Digital System is composed of 8 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

**Figure 1. Digital System Block Diagram**




Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I2C slave and multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 2)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 4.



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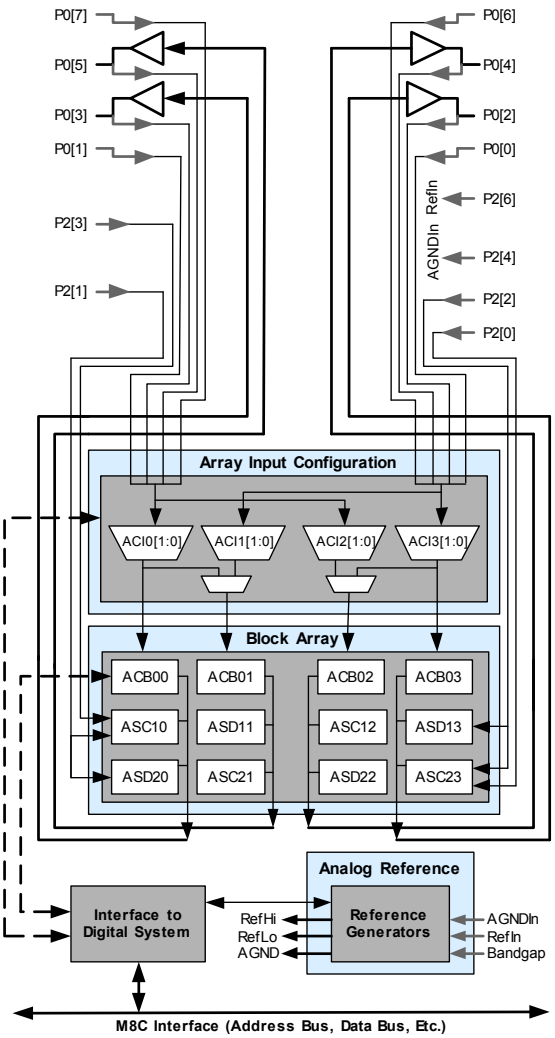
## Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

**Figure 2. Analog System Block Diagram**






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### Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource are below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

### PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups.The PSoC device covered by this data sheet is highlighted below.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---|---|---|---|---|---|---|---|---|---|
| CY8C29x66 | up to 64 | 4 | 16 | 12 | 4 | 4 | 12 | 2K | 32K |
| **CY8C27x43** | **up to 44** | **2** | **8** | **12** | **4** | **4** | **12** | **256 Bytes** | **16K** |
| CY8C24x94 | 49 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K |
| CY8C24x23 | up to 24 | 1 | 4 | 12 | 2 | 2 | 6 | 256 Bytes | 4K |
| CY8C24x23A | up to 24 | 1 | 4 | 12 | 2 | 2 | 6 | 256 Bytes | 4K |
| CY8C21x34 | up to 28 | 1 | 4 | 28 | 0 | 2 | 4[1] | 512 Bytes | 8K |
| CY8C21x23 | 16 | 1 | 4 | 8 | 0 | 2 | 4[2] | 256 Bytes | 4K |
| CY8C20x34 | up to 28 | 0 | 0 | 28 | 0 | 0 | 3[2] | 512 Bytes | 8K |

**Notes**
1. Limited analog functionality.
2. Two analog blocks and one CapSense.

## Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming information, see the PSoC® Programmable System-on-Chip™ Technical Reference Manual for CY8C28xxx PSoC devices.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

### Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

### Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

### Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.



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## Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built in support for third party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

### PSoC Designer Software Subsystems

*System-Level View*

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Programmable System-on-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

*Chip-Level View*

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

*Hybrid Designs*

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

*Code Generation Tools*

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

**Assemblers.** The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

*Debugger*

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

*Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

### In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.



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## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

### Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces ($I^2C$-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

### Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

### Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C `main()` program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.



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# Document Conventions

## Acronyms Used

This table lists the acronyms used in this data sheet.

**Table 2. Acronyms**

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| EEPROM | electrically erasable programmable read-only memory |
| FSR | full scale range |
| GPIO | general purpose IO |
| ICE | in-circuit emulator |
| IDE | integrated development environment |
| IO | input/output |
| ISSP | in-system serial programming |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| PGA | programmable gain amplifier |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC® | Programmable System-on-Chip™ |
| PWM | pulse width modulator |
| ROM | read only memory |
| SC | switched capacitor |
| SMP | switch mode pump |
| SRAM | static random access memory |

## Units of Measure

A units of measure table is located in the section Electrical Specifications on page 19. Table 13 on page 19 lists all the abbreviations used to measure the PSoC devices.

## Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.



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## Pinouts

The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

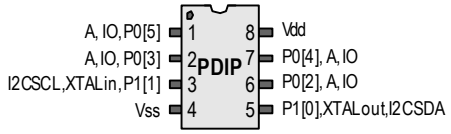
### 8-Pin Part Pinout

**Table 3. Pin Definitions - 8-Pin PDIP**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | IO | P0[5] | Analog column mux input and column output. |
| 2 | IO | IO | P0[3] | Analog column mux input and column output. |
| 3 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 4 | Power | | Vss | Ground connection. |
| 5 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 6 | IO | IO | P0[2] | Analog column mux input and column output. |
| 7 | IO | IO | P0[4] | Analog column mux input and column output. |
| 8 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

**Figure 3. CY8C27143 8-Pin PSoC Device**



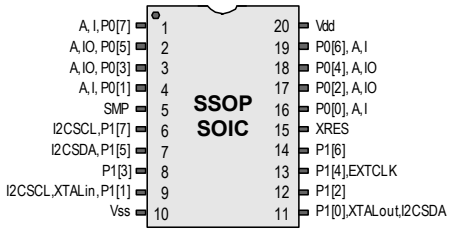

### 20-Pin Part Pinout

**Table 4. Pin Definitions - 20-Pin SSOP, SOIC**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 6 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 7 | IO | | P1[5] | I2C Serial Data (SDA). |
| 8 | IO | | P1[3] | |
| 9 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 10 | Power | | Vss | Ground connection. |
| 11 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 12 | IO | | P1[2] | |
| 13 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 14 | IO | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down. |
| 16 | IO | I | P0[0] | Analog column mux input. |
| 17 | IO | IO | P0[2] | Analog column mux input and column output. |
| 18 | IO | IO | P0[4] | Analog column mux input and column output. |
| 19 | IO | I | P0[6] | Analog column mux input. |
| 20 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

**Figure 4. CY8C27243 20-Pin PSoC Device**






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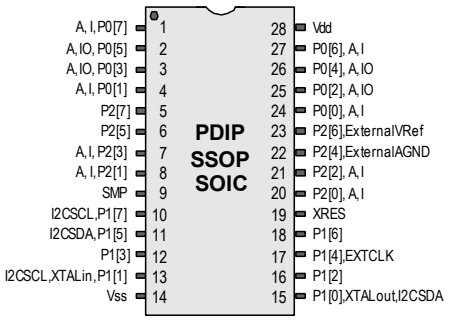
## 28-Pin Part Pinout

**Table 5. Pin Definitions - 28-Pin PDIP, SSOP, SOIC**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 10 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 11 | IO | | P1[5] | I2C Serial Data (SDA). |
| 12 | IO | | P1[3] | |
| 13 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 14 | Power | | Vss | Ground connection. |
| 15 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 16 | IO | | P1[2] | |
| 17 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 18 | IO | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down. |
| 20 | IO | I | P2[0] | Direct switched capacitor block input. |
| 21 | IO | I | P2[2] | Direct switched capacitor block input. |
| 22 | IO | | P2[4] | External Analog Ground (AGND). |
| 23 | IO | | P2[6] | External Voltage Reference (VRef). |
| 24 | IO | I | P0[0] | Analog column mux input. |
| 25 | IO | IO | P0[2] | Analog column mux input and column output. |
| 26 | IO | IO | P0[4] | Analog column mux input and column output. |
| 27 | IO | I | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.

**Figure 5. CY8C27443 28-Pin PSoC Device**





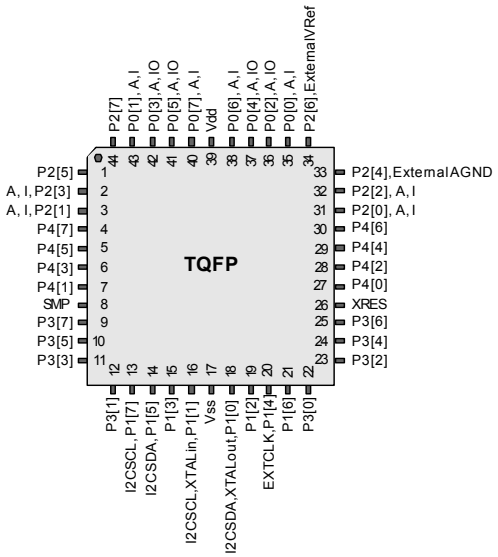

[+] Feedback

## 44-Pin Part Pinout

### Table 6. Pin Definitions - 44-Pin TQFP

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | | P2[5] | |
| 2 | IO | I | P2[3] | Direct switched capacitor block input. |
| 3 | IO | I | P2[1] | Direct switched capacitor block input. |
| 4 | IO | | P4[7] | |
| 5 | IO | | P4[5] | |
| 6 | IO | | P4[3] | |
| 7 | IO | | P4[1] | |
| 8 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 9 | IO | | P3[7] | |
| 10 | IO | | P3[5] | |
| 11 | IO | | P3[3] | |
| 12 | IO | | P3[1] | |
| 13 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 14 | IO | | P1[5] | I2C Serial Data (SDA). |
| 15 | IO | | P1[3] | |
| 16 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 17 | Power | | Vss | Ground connection. |
| 18 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 19 | IO | | P1[2] | |
| 20 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 21 | IO | | P1[6] | |
| 22 | IO | | P3[0] | |
| 23 | IO | | P3[2] | |
| 24 | IO | | P3[4] | |
| 25 | IO | | P3[6] | |
| 26 | Input | | XRES | Active high external reset with internal pull down. |
| 27 | IO | | P4[0] | |
| 28 | IO | | P4[2] | |
| 29 | IO | | P4[4] | |
| 30 | IO | | P4[6] | |
| 31 | IO | I | P2[0] | Direct switched capacitor block input. |
| 32 | IO | I | P2[2] | Direct switched capacitor block input. |
| 33 | IO | | P2[4] | External Analog Ground (AGND). |
| 34 | IO | | P2[6] | External Voltage Reference (VRef). |
| 35 | IO | I | P0[0] | Analog column mux input. |
| 36 | IO | IO | P0[2] | Analog column mux input and column output. |
| 37 | IO | IO | P0[4] | Analog column mux input and column output. |
| 38 | IO | I | P0[6] | Analog column mux input. |
| 39 | Power | | Vdd | Supply voltage. |
| 40 | IO | I | P0[7] | Analog column mux input. |
| 41 | IO | IO | P0[5] | Analog column mux input and column output. |
| 42 | IO | IO | P0[3] | Analog column mux input and column output. |
| 43 | IO | I | P0[1] | Analog column mux input. |
| 44 | IO | | P2[7] | |

**Figure 6. CY8C27543 44-Pin PSoC Device**




**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Programmable System-on-Chip Technical Reference Manual* for details.



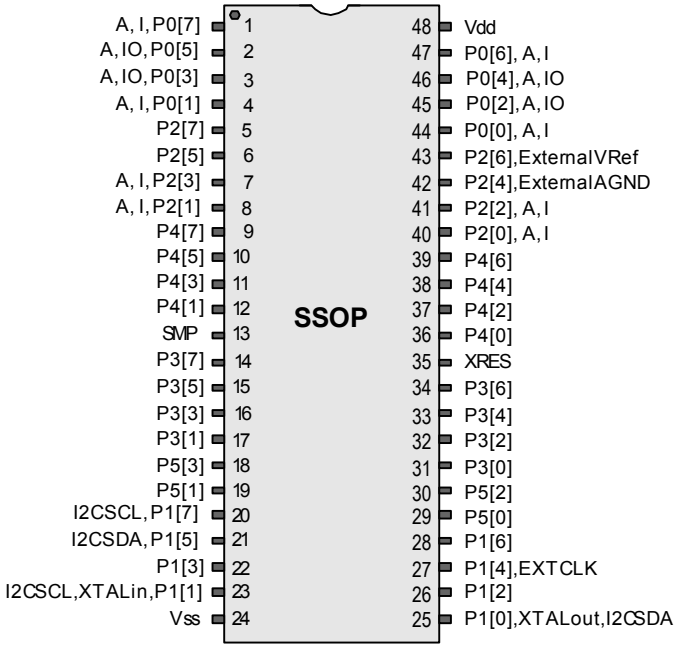
[+] Feedback

## 48-Pin Part Pinout

**Table 7. 48-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Ana-log | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | IO | | P4[7] | |
| 10 | IO | | P4[5] | |
| 11 | IO | | P4[3] | |
| 12 | IO | | P4[1] | |
| 13 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 14 | IO | | P3[7] | |
| 15 | IO | | P3[5] | |
| 16 | IO | | P3[3] | |
| 17 | IO | | P3[1] | |
| 18 | IO | | P5[3] | |
| 19 | IO | | P5[1] | |
| 20 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 21 | IO | | P1[5] | I2C Serial Data (SDA). |
| 22 | IO | | P1[3] | |
| 23 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 24 | Power | | Vss | Ground connection. |
| 25 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA.* |
| 26 | IO | | P1[2] | |
| 27 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 28 | IO | | P1[6] | |
| 29 | IO | | P5[0] | |
| 30 | IO | | P5[2] | |
| 31 | IO | | P3[0] | |
| 32 | IO | | P3[2] | |
| 33 | IO | | P3[4] | |
| 34 | IO | | P3[6] | |
| 35 | Input | | XRES | Active high external reset with internal pull down. |
| 36 | IO | | P4[0] | |
| 37 | IO | | P4[2] | |
| 38 | IO | | P4[4] | |
| 39 | IO | | P4[6] | |
| 40 | IO | I | P2[0] | Direct switched capacitor block input. |
| 41 | IO | I | P2[2] | Direct switched capacitor block input. |
| 42 | IO | | P2[4] | External Analog Ground (AGND). |

**Figure 7. CY8C27643 48-Pin PSoC Device**






[+] Feedback

**Table 7. 48-Pin Part Pinout (SSOP)**

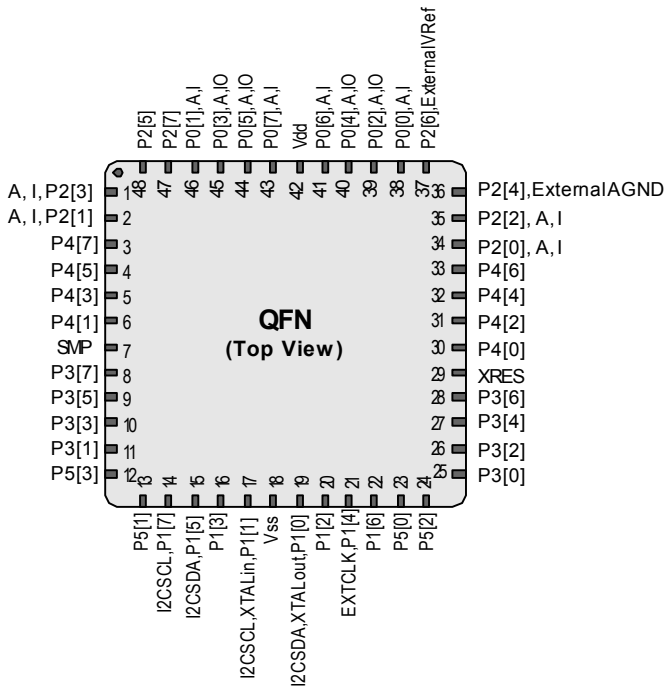
| | | | | |
|---|---|---|---|---|
| 43 | IO | | P2[6] | External Voltage Reference (VRef). |
| 44 | IO | I | P0[0] | Analog column mux input. |
| 45 | IO | IO | P0[2] | Analog column mux input and column output. |
| 46 | IO | IO | P0[4] | Analog column mux input and column output. |
| 47 | IO | I | P0[6] | Analog column mux input. |
| 48 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.

**Table 8. 48-Pin Part Pinout (QFN)***

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P2[3] | Direct switched capacitor block input. |
| 2 | IO | I | P2[1] | Direct switched capacitor block input. |
| 3 | IO | | P4[7] | |
| 4 | IO | | P4[5] | |
| 5 | IO | | P4[3] | |
| 6 | IO | | P4[1] | |
| 7 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 8 | IO | | P3[7] | |
| 9 | IO | | P3[5] | |
| 10 | IO | | P3[3] | |
| 11 | IO | | P3[1] | |
| 12 | IO | | P5[3] | |
| 13 | IO | | P5[1] | |
| 14 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 15 | IO | | P1[5] | I2C Serial Data (SDA). |
| 16 | IO | | P1[3] | |
| 17 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK**. |
| 18 | Power | | Vss | Ground connection. |
| 19 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA**. |
| 20 | IO | | P1[2] | |
| 21 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 22 | IO | | P1[6] | |
| 23 | IO | | P5[0] | |
| 24 | IO | | P5[2] | |
| 25 | IO | | P3[0] | |
| 26 | IO | | P3[2] | |
| 27 | IO | | P3[4] | |
| 28 | IO | | P3[6] | |
| 29 | Input | | XRES | Active high external reset with internal pull down. |
| 30 | IO | | P4[0] | |
| 31 | IO | | P4[2] | |
| 32 | IO | | P4[4] | |
| 33 | IO | | P4[6] | |

**Figure 8. CY8C27643 48-Pin PSoC Device**






[+] Feedback

**Table 8. 48-Pin Part Pinout (QFN)***

| | | | | |
|---|---|---|---|---|
| 34 | IO | I | P2[0] | Direct switched capacitor block input. |
| 35 | IO | I | P2[2] | Direct switched capacitor block input. |
| 36 | IO | | P2[4] | External Analog Ground (AGND). |
| 37 | IO | | P2[6] | External Voltage Reference (VRef). |
| 38 | IO | I | P0[0] | Analog column mux input. |
| 39 | IO | IO | P0[2] | Analog column mux input and column output. |
| 40 | IO | IO | P0[4] | Analog column mux input and column output. |
| 41 | IO | I | P0[6] | Analog column mux input. |
| 42 | Power | | Vdd | Supply voltage. |
| 43 | IO | I | P0[7] | Analog column mux input. |
| 44 | IO | IO | P0[5] | Analog column mux input and column output. |
| 45 | IO | IO | P0[3] | Analog column mux input and column output. |
| 46 | IO | I | P0[1] | Analog column mux input. |
| 47 | IO | | P2[7] | |
| 48 | IO | | P2[5] | |

**LEGEND**: A = Analog, I = Input, and O = Output.
* The QFN package has a center pad that must be connected to ground (Vss).
** These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.



[+] Feedback

## 56-Pin Part Pinout

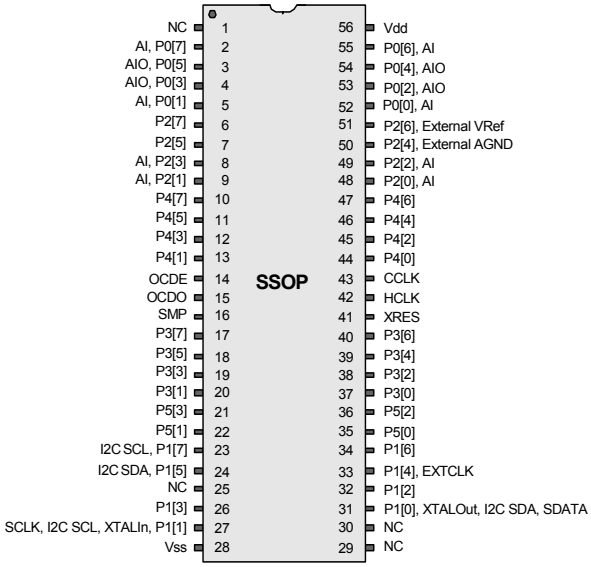
The 56-pin SSOP part is for the CY8C27002 On-Chip Debug (OCD) PSoC device.

**Note** This part is only used for in-circuit debugging. It is NOT available for production.

**Table 9. 56-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Ana-log | | |
| 1 | | | NC | No connection. |
| 2 | IO | I | P0[7] | Analog column mux input. |
| 3 | IO | I | P0[5] | Analog column mux input and column output. |
| 4 | IO | I | P0[3] | Analog column mux input and column output. |
| 5 | IO | I | P0[1] | Analog column mux input. |
| 6 | IO | | P2[7] | |
| 7 | IO | | P2[5] | |
| 8 | IO | I | P2[3] | Direct switched capacitor block input. |
| 9 | IO | I | P2[1] | Direct switched capacitor block input. |
| 10 | IO | | P4[7] | |
| 11 | IO | | P4[5] | |
| 12 | IO | I | P4[3] | |
| 13 | IO | I | P4[1] | |
| 14 | OCD | | OCDE | OCD even data IO. |
| 15 | OCD | | OCDO | OCD odd data output. |
| 16 | Power | | SMP | Switch Mode Pump (SMP) connection to required external components. |
| 17 | IO | | P3[7] | |
| 18 | IO | | P3[5] | |
| 19 | IO | | P3[3] | |
| 20 | IO | | P3[1] | |
| 21 | IO | | P5[3] | |
| 22 | IO | | P5[1] | |
| 23 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 24 | IO | | P1[5] | I2C Serial Data (SDA). |
| 25 | | | NC | No connection. |
| 26 | IO | | P1[3] | |
| 27 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 28 | Power | | Vdd | Supply voltage. |
| 29 | | | NC | No connection. |
| 30 | | | NC | No connection.. |
| 31 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 32 | IO | | P1[2] | |
| 33 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 34 | IO | | P1[6] | |
| 35 | IO | | P5[0] | |
| 36 | IO | | P5[2] | |
| 37 | IO | | P3[0] | |
| 38 | IO | | P3[2] | |
| 39 | IO | | P3[4] | |
| 40 | IO | | P3[6] | |

**Figure 9. CY8C27002 56-Pin PSoC Device**




**Not for Production**



[+] Feedback

**Table 9. 56-Pin Part Pinout (SSOP)**

| | | | | |
|---|---|---|---|---|
| 41 | Input | | XRES | Active high external reset with internal pull down. |
| 42 | OCD | | HCLK | OCD high-speed clock output. |
| 43 | OCD | | CCLK | OCD CPU clock output. |
| 44 | IO | | P4[0] | |
| 45 | IO | | P4[2] | |
| 46 | IO | | P4[4] | |
| 47 | IO | | P4[6] | |
| 48 | IO | I | P2[0] | Direct switched capacitor block input. |
| 49 | IO | I | P2[2] | Direct switched capacitor block input. |
| 50 | IO | | P2[4] | External Analog Ground (AGND). |
| 51 | IO | | P2[6] | External Voltage Reference (VRef). |
| 52 | IO | I | P0[0] | Analog column mux input. |
| 53 | IO | I | P0[2] | Analog column mux input and column output. |
| 54 | IO | I | P0[4] | Analog column mux input and column output. |
| 55 | IO | I | P0[6] | Analog column mux input. |
| 56 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.



[+] Feedback

## Register Reference

This chapter lists the registers of the CY8C27x43 PSoC device. For detailed register information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*.

### Register Conventions

The register conventions specific to this section are listed in the following table.

**Table 10. Register Conventions**

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

**Table 11. Register Map Bank 0 Table: User Space**

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | | 48 | | ASC12CR0 | 88 | RW | | C8 | |
| PRT2IE | 09 | RW | | 49 | | ASC12CR1 | 89 | RW | | C9 | |
| PRT2GS | 0A | RW | | 4A | | ASC12CR2 | 8A | RW | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | | CB | |
| PRT3DR | 0C | RW | | 4C | | ASD13CR0 | 8C | RW | | CC | |
| PRT3IE | 0D | RW | | 4D | | ASD13CR1 | 8D | RW | | CD | |
| PRT3GS | 0E | RW | | 4E | | ASD13CR2 | 8E | RW | | CE | |
| PRT3DM2 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DR | 10 | RW | | 50 | | ASD20CR0 | 90 | RW | | D0 | |
| PRT4IE | 11 | RW | | 51 | | ASD20CR1 | 91 | RW | | D1 | |
| PRT4GS | 12 | RW | | 52 | | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | | D3 | |
| PRT5DR | 14 | RW | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| PRT5IE | 15 | RW | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| PRT5GS | 16 | RW | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | ASD22CR0 | 98 | RW | I2C_DR | D8 | RW |
| | 19 | | | 59 | | ASD22CR1 | 99 | RW | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | ASD22CR2 | 9A | RW | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | ASD22CR3 | 9B | RW | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | ASC23CR0 | 9C | RW | | DC | |
| | 1D | | | 5D | | ASC23CR1 | 9D | RW | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | ASC23CR2 | 9E | RW | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | ASC23CR3 | 9F | RW | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |

**Blank fields are Reserved and must not be accessed.** # Access is bit specific.



[+] Feedback

**Table 11. Register Map Bank 0 Table: User Space** (continued)

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | MUL_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | MUL_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | MUL_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | | AB | | MUL_DL | EB | R |
| DCB03DR0 | 2C | # | | 6C | | | AC | | ACC_DR1 | EC | RW |
| DCB03DR1 | 2D | W | | 6D | | | AD | | ACC_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | | 6E | | | AE | | ACC_DR3 | EE | RW |
| DCB03CR0 | 2F | # | | 6F | | | AF | | ACC_DR2 | EF | RW |
| DBB10DR0 | 30 | # | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10DR1 | 31 | W | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10DR2 | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBB10CR0 | 33 | # | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11DR0 | 34 | # | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11DR1 | 35 | W | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11DR2 | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBB11CR0 | 37 | # | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12DR0 | 38 | # | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12DR1 | 39 | W | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12DR2 | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | | FA | |
| DCB12CR0 | 3B | # | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13DR0 | 3C | # | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13DR1 | 3D | W | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13DR2 | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCB13CR0 | 3F | # | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** # Access is bit specific.

**Table 12. Register Map Bank 1 Table: Configuration Space**

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | ASC12CR0 | 88 | RW | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | ASC12CR1 | 89 | RW | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | ASC12CR2 | 8A | RW | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | ASD13CR0 | 8C | RW | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | ASD13CR1 | 8D | RW | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | ASD13CR2 | 8E | RW | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DM0 | 10 | RW | | 50 | | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | | 51 | | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | | 52 | | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | | 56 | | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | ASD22CR0 | 98 | RW | | D8 | |
| | 19 | | | 59 | | ASD22CR1 | 99 | RW | | D9 | |
| | 1A | | | 5A | | ASD22CR2 | 9A | RW | | DA | |
| | 1B | | | 5B | | ASD22CR3 | 9B | RW | | DB | |

**Blank fields are Reserved and must not be accessed.** # Access is bit specific.



[+] Feedback

**Table 12. Register Map Bank 1 Table: Configuration Space** (continued)

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1C | | | 5C | | ASC23CR0 | 9C | RW | | DC | |
| | 1D | | | 5D | | ASC23CR1 | 9D | RW | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | ASC23CR2 | 9E | RW | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | ASC23CR3 | 9F | RW | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | ALT_CR1 | 68 | RW | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | CLK_CR2 | 69 | RW | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | | 6C | | | AC | | | EC | |
| DCB03IN | 2D | RW | | 6D | | | AD | | | ED | |
| DCB03OU | 2E | RW | | 6E | | | AE | | | EE | |
| | 2F | | | 6F | | | AF | | | EF | |
| DBB10FN | 30 | RW | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10IN | 31 | RW | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10OU | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11FN | 34 | RW | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11IN | 35 | RW | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11OU | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12FN | 38 | RW | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12IN | 39 | RW | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12OU | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | | FA | |
| | 3B | | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13FN | 3C | RW | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13IN | 3D | RW | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13OU | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| | 3F | | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and must not be accessed.** # Access is bit specific.



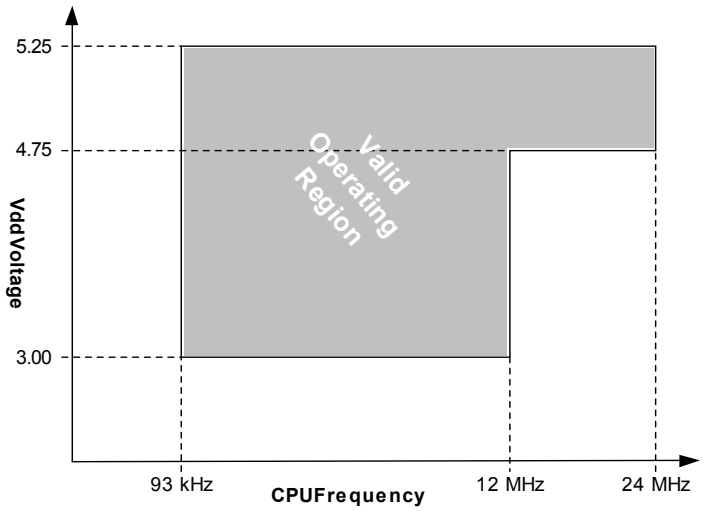
[+] Feedback

## Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C27x43 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ $T_A$ ≤ 85°C and $T_J$ ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ $T_A$ ≤ 70°C and $T_J$ ≤ 82°C.

**Figure 10. Voltage versus CPU Frequency**




The following table lists the units of measure that are used in this chapter.

**Table 13. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µW | microwatts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | W | ohm |
| MHz | megahertz | pA | picoampere |
| MΩ | megaohm | pF | picofarad |
| µA | microampere | pp | peak-to-peak |
| µF | microfarad | ppm | parts per million |
| µH | microhenry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | microvolts | s | sigma: one standard deviation |
| µVrms | microvolts root-mean-square | V | volts |



[+] Feedback

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 14. Absolute Maximum Ratings**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | 25 | +100 | °C | Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability. |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +85 | °C | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss- 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| $I_{MAIO}$ | Maximum Current into any Port Pin Configured as Analog Driver | -50 | – | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch up Current | – | – | 200 | mA | |

## Operating Temperature

**Table 15. Operating Temperature**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +85 | °C | |
| $T_J$ | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 46. The user must limit the power consumption to comply with this requirement. |



[+] Feedback

# DC Electrical Characteristics

## DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 16. DC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 3.00 | – | 5.25 | V | |
| $I_{DD}$ | Supply Current | – | 5 | 8 | mA | Conditions are Vdd = 5.0V, $T_A$ = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{DD3}$ | Supply Current | – | 3.3 | 6.0 | mA | Conditions are Vdd = 3.3V, $T_A$ = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[3] | – | 3 | 6.5 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ $T_A$ ≤ 55 °C. |
| $I_{SBH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[3] | – | 4 | 25 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < $T_A$ ≤ 85 °C. |
| $I_{SBXTL}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[3] | – | 4 | 7.5 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C ≤ $T_A$ ≤ 55 °C. |
| $I_{SBXTLH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[3] | – | 5 | 26 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, 55 °C < $T_A$ ≤ 85 °C. |
| $V_{REF}$ | Reference Voltage (Bandgap) for Silicon A [4] | 1.275 | 1.300 | 1.325 | V | Trimmed for appropriate Vdd. |
| $V_{REF}$ | Reference Voltage (Bandgap) for Silicon B [4] | 1.280 | 1.300 | 1.320 | V | Trimmed for appropriate Vdd. |

**Notes**
3. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This must be compared with devices that have similar functions enabled.
4. Refer to the "Ordering Information" on page 50.



[+] Feedback

## DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 17. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 1.0 | – | – | V | IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | Vdd = 3.0 to 5.25 |
| $V_{IH}$ | Input High Level | 2.1 | – | | V | Vdd = 3.0 to 5.25 |
| $V_H$ | Input Hysterisis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |

## DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 18. 5V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value)<br>Power = Low, Opamp Bias = High<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br>–<br>–<br>– | <br>1.6<br>1.3<br>1.2 | <br>10<br>8<br>7.5 | <br>mV<br>mV<br>mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | μV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 μA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range<br>Common Mode Voltage Range (high power or high opamp bias) | 0.0<br>0.5 | –<br>– | Vdd<br>Vdd - 0.5 | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |



[+] Feedback

**Table 18. 5V DC Operational Amplifier Specifications** (continued)

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $CMRR_{OA}$ | Common Mode Rejection Ratio<br>Power = Low<br>Power = Medium<br>Power = High | <br>60<br>60<br>60 | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| $G_{OLOA}$ | Open Loop Gain<br>Power = Low<br>Power = Medium<br>Power = High | <br>60<br>60<br>80 | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| $V_{OHIGHOA}$ | High Output Voltage Swing (internal signals)<br>Power = Low<br>Power = Medium<br>Power = High | <br>Vdd - 0.2<br>Vdd - 0.2<br>Vdd - 0.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V<br>V<br>V | |
| $V_{OLOWOA}$ | Low Output Voltage Swing (internal signals)<br>Power = Low<br>Power = Medium<br>Power = High | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.2<br>0.2<br>0.5 | <br>V<br>V<br>V | |
| $I_{SOA}$ | Supply Current (including associated AGND buffer)<br>Power = Low, Opamp Bias = Low<br>Power = Low, Opamp Bias = High<br>Power = Medium, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = Low<br>Power = High, Opamp Bias = High | <br>–<br>–<br>–<br>–<br>–<br>– | <br>150<br>300<br>600<br>1200<br>2400<br>4600 | <br>200<br>400<br>800<br>1600<br>3200<br>6400 | <br>µA<br>µA<br>µA<br>µA<br>µA<br>µA | |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | 60 | – | – | dB | Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd. |

**Table 19. 3.3V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value)<br>Power = Low, Opamp Bias = High<br>Power = Medium, Opamp Bias = High<br>High Power is 5 Volts Only | <br>–<br>– | <br>1.65<br>1.32 | <br>10<br>8 | <br>mV<br>mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | µV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.2 | – | Vdd - 0.2 | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| $CMRR_{OA}$ | Common Mode Rejection Ratio<br>Power = Low<br>Power = Medium<br>Power = High | <br>50<br>50<br>50 | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |



[+] Feedback

**Table 19. 3.3V DC Operational Amplifier Specifications** (continued)

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $G_{OLOA}$ | Open Loop Gain<br>Power = Low<br>Power = Medium<br>Power = High | <br>60<br>60<br>80 | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| $V_{OHIGHOA}$ | High Output Voltage Swing (internal signals)<br>Power = Low<br>Power = Medium<br>Power = High is 5V only | <br>Vdd - 0.2<br>Vdd - 0.2<br>Vdd - 0.2 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V<br>V<br>V | |
| $V_{OLOWOA}$ | Low Output Voltage Swing (internal signals)<br>Power = Low<br>Power = Medium<br>Power = High | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.2<br>0.2<br>0.2 | <br>V<br>V<br>V | |
| $I_{SOA}$ | Supply Current (including associated AGND buffer)<br>Power = Low, Opamp Bias = Low<br>Power = Low, Opamp Bias = High<br>Power = Medium, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = Low<br>Power = High, Opamp Bias = High | <br>–<br>–<br>–<br>–<br>–<br>– | <br>150<br>300<br>600<br>1200<br>2400<br>4600 | <br>200<br>400<br>800<br>1600<br>3200<br>6400 | <br>µA<br>µA<br>µA<br>µA<br>µA<br>µA | |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | 50 | 80 | – | dB | Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd. |

## DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 20. DC Low Power Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{REFLPC}$ | Low power comparator (LPC) reference voltage range | 0.2 | – | Vdd - 1 | V |
| $I_{SLPC}$ | LPC supply current | – | 10 | 40 | µA |
| $V_{OSLPC}$ | LPC voltage offset | – | 2.5 | 30 | mV |



[+] Feedback

## DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 21. 5V DC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV |
| $TCV_{OSOB}$ | Average Input Offset Voltage Drift | – | +6 | – | µV/°C |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | – | Vdd - 1.0 | V |
| $R_{OUTOB}$ | Output Resistance<br>Power = Low<br>Power = High | <br>–<br>– | <br>1<br>1 | <br>–<br>– | <br>W<br>W |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 32 ohms to Vdd/2)<br>Power = Low<br>Power = High | <br>0.5 x Vdd + 1.3<br>0.5 x Vdd + 1.3 | <br>–<br>– | <br>–<br>– | <br>V<br>V |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 32 ohms to Vdd/2)<br>Power = Low<br>Power = High | <br>–<br>– | <br>–<br>– | <br>0.5 x Vdd - 1.3<br>0.5 x Vdd - 1.3 | <br>V<br>V |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load)<br>Power = Low<br>Power = High | <br>–<br>– | <br>1.1<br>2.6 | <br>5.1<br>8.8 | <br>mA<br>mA |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 60 | 64 | – | dB |

**Table 22. 3.3V DC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV |
| $TCV_{OSOB}$ | Average Input Offset Voltage Drift | – | +6 | – | µV/°C |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | - | Vdd - 1.0 | V |
| $R_{OUTOB}$ | Output Resistance<br>Power = Low<br>Power = High | <br>–<br>– | <br>1<br>1 | <br>–<br>– | <br>W<br>W |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 1k ohms to Vdd/2)<br>Power = Low<br>Power = High | <br>0.5 x Vdd + 1.0<br>0.5 x Vdd + 1.0 | <br>–<br>– | <br>–<br>– | <br>V<br>V |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 1k ohms to Vdd/2)<br>Power = Low<br>Power = High | <br>–<br>– | <br>–<br>– | <br>0.5 x Vdd - 1.0<br>0.5 x Vdd - 1.0 | <br>V<br>V |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load)<br>Power = Low<br>Power = High | <br><br>– | <br>0.8<br>2.0 | <br>2.0<br>4.3 | <br>mA<br>mA |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 60 | 64 | – | dB |



[+] Feedback

## DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 23. DC Switch Mode Pump (SMP) Specifications**

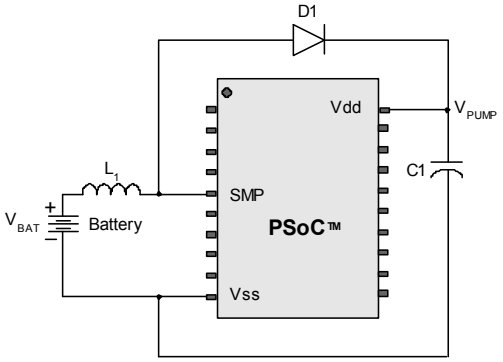
| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{PUMP}$ 5V | 5V Output Voltage | 4.75 | 5.0 | 5.25 | V | Configuration of footnote.[5] Average, neglecting ripple. SMP trip voltage is set to 5.0V. |
| $V_{PUMP}$ 3V | 3V Output Voltage | 3.00 | 3.25 | 3.60 | V | Configuration of footnote.[5] Average, neglecting ripple. SMP trip voltage is set to 3.25V. |
| $I_{PUMP}$ | Available Output Current<br>$V_{BAT}$ = 1.5V, $V_{PUMP}$ = 3.25V<br>$V_{BAT}$ = 1.8V, $V_{PUMP}$ = 5.0V | <br>8<br>5 | <br>–<br>– | <br>–<br>– | <br>mA<br>mA | Configuration of footnote.[5]<br>SMP trip voltage is set to 3.25V.<br>SMP trip voltage is set to 5.0V. |
| $V_{BAT}$5V | Input Voltage Range from Battery | 1.8 | – | 5.0 | V | Configuration of footnote.[5] SMP trip voltage is set to 5.0V. |
| $V_{BAT}$3V | Input Voltage Range from Battery | 1.0 | – | 3.3 | V | Configuration of footnote.[5] SMP trip voltage is set to 3.25V. |
| $V_{BATSTART}$ | Minimum Input Voltage from Battery to Start Pump | 1.1 | – | – | V | Configuration of footnote.[5] |
| $\Delta V_{PUMP_Line}$ | Line Regulation (over $V_{BAT}$ range) | – | 5 | – | $\%V_O$ | Configuration of footnote.[5] $V_O$ is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 29 on page 30. |
| $\Delta V_{PUMP_Load}$ | Load Regulation | – | 5 | – | $\%V_O$ | Configuration of footnote.[5] $V_O$ is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 29 on page 30. |
| $\Delta V_{PUMP_Ripple}$ | Output Voltage Ripple (depends on capacitor/load) | – | 100 | – | mVpp | Configuration of footnote.[5] Load is 5 mA. |
| $E_3$ | Efficiency | 35 | 50 | – | % | Configuration of footnote.[5] Load is 5 mA. SMP trip voltage is set to 3.25V. |
| $F_{PUMP}$ | Switching Frequency | – | 1.3 | – | MHz | |
| $DC_{PUMP}$ | Switching Duty Cycle | – | 50 | – | % | |

**Note**
5. $L_1$ = 2 mH inductor, $C_1$ = 10 mF capacitor, $D_1$ = Schottky diode. See Figure 11.



[+] Feedback

**Figure 11. Basic Switch Mode Pump Circuit**




## DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

**Note** Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

**Table 24. Silicon Revision A – 5V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BG | Bandgap Voltage Reference | 1.274 | 1.30 | 1.326 | V |
| – | AGND = Vdd/2[6] | Vdd/2 - 0.030 | Vdd/2 - 0.004 | Vdd/2 + 0.003 | V |
| – | AGND = 2 x BandGap[6] | 2 x BG - 0.043 | 2 x BG - 0.010 | 2 x BG + 0.024 | V |
| – | AGND = P2[4] (P2[4] = Vdd/2)[6] | P2[4] - 0.013 | P2[4] | P2[4] + 0.014 | V |
| – | AGND = BandGap[6] | BG - 0.009 | BG | BG + 0.009 | V |
| – | AGND = 1.6 x BandGap[6] | 1.6 x BG - 0.018 | 1.6 x BG | 1.6 x BG + 0.018 | V |
| – | AGND Block to Block Variation (AGND = Vdd/2)[6] | -0.034 | 0.000 | 0.034 | V |
| – | RefHi = Vdd/2 + BandGap | Vdd/2 + BG - 0.140 | Vdd/2 + BG - 0.018 | Vdd/2 + BG + 0.103 | V |
| – | RefHi = 3 x BandGap | 3 x BG - 0.112 | 3 x BG - 0.018 | 3 x BG + 0.076 | V |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V) | 2 x BG + P2[6] - 0.113 | 2 x BG + P2[6] - 0.018 | 2 x BG + P2[6] + 0.077 | V |
| – | RefHi = P2[4] + BandGap (P2[4] = Vdd/2) | P2[4] + BG - 0.130 | P2[4] + BG - 0.016 | P2[4] + BG + 0.098 | V |
| – | RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) | P2[4] + P2[6] - 0.133 | P2[4] + P2[6] - 0.016 | P2[4] + P2[6] + 0.100 | V |
| – | RefHi = 3.2 x BandGap | 3.2 x BG - 0.112 | 3.2 x BG | 3.2 x BG + 0.076 | V |
| – | RefLo = Vdd/2 – BandGap | Vdd/2 - BG - 0.051 | Vdd/2 - BG + 0.024 | Vdd/2 - BG + 0.098 | V |
| – | RefLo = BandGap | BG - 0.082 | BG + 0.023 | BG + 0.129 | V |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V) | 2 x BG - P2[6] - 0.084 | 2 x BG - P2[6] + 0.025 | 2 x BG - P2[6] + 0.134 | V |
| – | RefLo = P2[4] – BandGap (P2[4] = Vdd/2) | P2[4] - BG - 0.056 | P2[4] - BG + 0.026 | P2[4] - BG + 0.107 | V |
| – | RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) | P2[4] - P2[6] - 0.057 | P2[4] - P2[6] + 0.026 | P2[4] - P2[6] + 0.110 | V |

**Note**
6. AGND tolerance includes the offsets of the local buffer in the PSoC block.



[+] Feedback

**Table 25. Silicon Revision B – 5V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BG | Bandgap Voltage Reference | 1.28 | 1.30 | 1.32 | V |
| – | AGND = Vdd/2[7] | Vdd/2 - 0.030 | Vdd/2 | Vdd/2 + 0.007 | V |
| – | AGND = 2 x BandGap[7] | 2 x BG - 0.043 | 2 x BG | 2 x BG + 0.024 | V |
| – | AGND = P2[4] (P2[4] = Vdd/2)[7] | P2[4] - 0.011 | P2[4] | P2[4] + 0.011 | V |
| – | AGND = BandGap[7] | BG - 0.009 | BG | BG + 0.009 | V |
| – | AGND = 1.6 x BandGap[7] | 1.6 x BG - 0.018 | 1.6 x BG | 1.6 x BG + 0.018 | V |
| – | AGND Block to Block Variation (AGND = Vdd/2)[7] | -0.034 | 0.000 | 0.034 | V |
| – | RefHi = Vdd/2 + BandGap | Vdd/2 + BG - 0.1 | Vdd/2 + BG - 0.01 | Vdd/2 + BG + 0.1 | V |
| – | RefHi = 3 x BandGap | 3 x BG - 0.06 | 3 x BG - 0.01 | 3 x BG + 0.06 | V |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V) | 2 x BG + P2[6] - 0.06 | 2 x BG + P2[6] - 0.01 | 2 x BG + P2[6] + 0.06 | V |
| – | RefHi = P2[4] + BandGap (P2[4] = Vdd/2) | P2[4] + BG - 0.06 | P2[4] + BG - 0.01 | P2[4] + BG + 0.06 | V |
| – | RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) | P2[4] + P2[6] - 0.06 | P2[4] + P2[6] - 0.01 | P2[4] + P2[6] + 0.06 | V |
| – | RefHi = 3.2 x BandGap | 3.2 x BG - 0.06 | 3.2 x BG - 0.01 | 3.2 x BG + 0.06 | V |
| – | RefLo = Vdd/2 – BandGap | Vdd/2 - BG - 0.051 | Vdd/2 - BG + 0.01 | Vdd/2 - BG + 0.06 | V |
| – | RefLo = BandGap | BG - 0.06 | BG + 0.01 | BG + 0.06 | V |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V) | 2 x BG - P2[6] - 0.04 | 2 x BG - P2[6] + 0.01 | 2 x BG - P2[6] + 0.04 | V |
| – | RefLo = P2[4] – BandGap (P2[4] = Vdd/2) | P2[4] - BG - 0.056 | P2[4] - BG + 0.01 | P2[4] - BG + 0.056 | V |
| – | RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V) | P2[4] - P2[6] - 0.056 | P2[4] - P2[6] + 0.01 | P2[4] - P2[6] + 0.056 | V |

**Table 26. Silicon Revision A – 3.3V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BG | Bandgap Voltage Reference | 1.274 | 1.30 | 1.326 | V |
| – | AGND = Vdd/2[8] | Vdd/2 - 0.027 | Vdd/2 - 0.003 | Vdd/2 + 0.002 | V |
| – | AGND = 2 x BandGap[8] | Not Allowed | | | |
| – | AGND = P2[4] (P2[4] = Vdd/2) | P2[4] - 0.008 | P2[4] + 0.001 | P2[4] + 0.009 | V |
| – | AGND = BandGap[8] | BG - 0.009 | BG | BG + 0.009 | V |
| – | AGND = 1.6 x BandGap[8] | 1.6 x BG - 0.018 | 1.6 x BG | 1.6 x BG + 0.018 | V |
| – | AGND Block to Block Variation (AGND = Vdd/2)[8] | -0.034 | 0.000 | 0.034 | V |
| – | RefHi = Vdd/2 + BandGap | Not Allowed | | | |
| – | RefHi = 3 x BandGap | Not Allowed | | | |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefHi = P2[4] + BandGap (P2[4] = Vdd/2) | Not Allowed | | | |
| – | RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) | P2[4] + P2[6] - 0.075 | P2[4] + P2[6] - 0.009 | P2[4] + P2[6] + 0.057 | V |
| – | RefHi = 3.2 x BandGap | Not Allowed | | | |
| – | RefLo = Vdd/2 - BandGap | Not Allowed | | | |

**Note**
7. AGND tolerance includes the offsets of the local buffer in the PSoC block.



[+] Feedback

**Table 26. Silicon Revision A – 3.3V DC Analog Reference Specifications** (continued)

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| – | RefLo = BandGap | Not Allowed | | | |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefLo = P2[4] – BandGap (P2[4] = Vdd/2) | Not Allowed | | | |
| – | RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) | P2[4] - P2[6] - 0.048 | P2[4] - P2[6] + 0.022 | P2[4] - P2[6] + 0.092 | V |

**Table 27. Silicon Revision B – 3.3V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BG | Bandgap Voltage Reference | 1.28 | 1.30 | 1.32 | V |
| – | AGND = Vdd/2[8] | Vdd/2 - 0.027 | Vdd/2 | Vdd/2 + 0.005 | V |
| – | AGND = 2 x BandGap[8] | Not Allowed | | | |
| – | AGND = P2[4] (P2[4] = Vdd/2) | P2[4] - 0.008 | P2[4] | P2[4] + 0.009 | V |
| – | AGND = BandGap[8] | BG - 0.009 | BG | BG + 0.009 | V |
| – | AGND = 1.6 x BandGap[8] | 1.6 x BG - 0.018 | 1.6 x BG | 1.6 x BG + 0.018 | V |
| – | AGND Block to Block Variation (AGND = Vdd/2)[8] | -0.034 | 0.000 | 0.034 | mV |
| – | RefHi = Vdd/2 + BandGap | Not Allowed | | | |
| – | RefHi = 3 x BandGap | Not Allowed | | | |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefHi = P2[4] + BandGap (P2[4] = Vdd/2) | Not Allowed | | | |
| – | RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) | P2[4] + P2[6] - 0.06 | P2[4] + P2[6] - 0.01 | P2[4] + P2[6] + 0.057 | V |
| – | RefHi = 3.2 x BandGap | Not Allowed | | | |
| – | RefLo = Vdd/2 - BandGap | Not Allowed | | | |
| – | RefLo = BandGap | Not Allowed | | | |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefLo = P2[4] – BandGap (P2[4] = Vdd/2) | Not Allowed | | | |
| – | RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V) | P2[4] - P2[6] - 0.048 | P2[4] - P2[6] + 0.01 | P2[4] - P2[6] + 0.048 | V |

## DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 28. DC Analog PSoC Block Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $R_{CT}$ | Resistor Unit Value (Continuous Time) | – | 12.2 | – | kΩ |
| $C_{SC}$ | Capacitor Unit Value (Switch Cap) | – | 80 | – | fF |

**Note**
8. AGND tolerance includes the offsets of the local buffer in the PSoC block. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.



[+] Feedback

## DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Note** The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Programmable System-on-Chip Technical Reference Manual* for more information on the VLT_CR register.

**Table 29. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| | Vdd Value for PPOR Trip (positive ramp) | | | | | Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog. |
| $V_{PPOR0R}$ | PORLEV[1:0] = 00b | | 2.91 | | V | |
| $V_{PPOR1R}$ | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| $V_{PPOR2R}$ | PORLEV[1:0] = 10b | | 4.55 | | V | |
| | Vdd Value for PPOR Trip (negative ramp) | | | | | |
| $V_{PPOR0}$ | PORLEV[1:0] = 00b | | 2.82 | | V | |
| $V_{PPOR1}$ | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| $V_{PPOR2}$ | PORLEV[1:0] = 10b | | 4.55 | | V | |
| | PPOR Hysteresis | | | | | |
| $V_{PH0}$ | PORLEV[1:0] = 00b | – | 92 | – | mV | |
| $V_{PH1}$ | PORLEV[1:0] = 01b | – | 0 | – | mV | |
| $V_{PH2}$ | PORLEV[1:0] = 10b | – | 0 | – | mV | |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD0}$ | VM[2:0] = 000b | 2.86 | 2.92 | 2.98[9] | V | |
| $V_{LVD1}$ | VM[2:0] = 001b | 2.96 | 3.02 | 3.08 | V | |
| $V_{LVD2}$ | VM[2:0] = 010b | 3.07 | 3.13 | 3.20 | V | |
| $V_{LVD3}$ | VM[2:0] = 011b | 3.92 | 4.00 | 4.08 | V | |
| $V_{LVD4}$ | VM[2:0] = 100b | 4.39 | 4.48 | 4.57 | V | |
| $V_{LVD5}$ | VM[2:0] = 101b | 4.55 | 4.64 | 4.74[10] | V | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.63 | 4.73 | 4.82 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.72 | 4.81 | 4.91 | V | |
| | | | | | V | |
| | Vdd Value for PUMP Trip | | | | | |
| $V_{PUMP0}$ | VM[2:0] = 000b | 2.96 | 3.02 | 3.08 | V | |
| $V_{PUMP1}$ | VM[2:0] = 001b | 3.03 | 3.10 | 3.16 | V | |
| $V_{PUMP2}$ | VM[2:0] = 010b | 3.18 | 3.25 | 3.32 | V | |
| $V_{PUMP3}$ | VM[2:0] = 011b | 4.11 | 4.19 | 4.28 | V | |
| $V_{PUMP4}$ | VM[2:0] = 100b | 4.55 | 4.64 | 4.74 | V | |
| $V_{PUMP5}$ | VM[2:0] = 101b | 4.63 | 4.73 | 4.82 | V | |
| $V_{PUMP6}$ | VM[2:0] = 110b | 4.72 | 4.82 | 4.91 | V | |
| $V_{PUMP7}$ | VM[2:0] = 111b | 4.90 | 5.00 | 5.10 | V | |
| | | | | | V | |

**Notes**
9. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
10. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.



[+] Feedback

## DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 30. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDP}$ | Supply Current During Programming or Verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| $I_{IHP}$ | Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| $V_{OLV}$ | Output Low Voltage During Programming or Verify | – | – | Vss + 0.75 | V | |
| $V_{OHV}$ | Output High Voltage During Programming or Verify | Vdd - 1.0 | – | Vdd | V | |
| $Flash_{ENPB}$ | Flash Endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash Endurance (total)[11] | 1,800,000 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash Data Retention | 10 | – | – | Years | |

**Note**

11. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information



[+] Feedback

# AC Electrical Characteristics

## AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 31. AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO}$ | Internal Main Oscillator Frequency | 23.4 | 24 | 24.6[12] | MHz | Trimmed. Utilizing factory trim values. |
| $F_{CPU1}$ | CPU Frequency (5V Nominal) | 0.93 | 24 | 24.6[12,13] | MHz | Trimmed. Utilizing factory trim values. |
| $F_{CPU2}$ | CPU Frequency (3.3V Nominal) | 0.93 | 12 | 12.3[13,14] | MHz | Trimmed. Utilizing factory trim values. |
| $F_{48M}$ | Digital PSoC Block Frequency | 0 | 48 | 49.2[12,13, 15] | MHz | Refer to the AC Digital Block Specifications below. |
| $F_{24M}$ | Digital PSoC Block Frequency | 0 | 24 | 24.6[13, 15] | MHz | |
| $F_{32K1}$ | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | |
| $F_{32K2}$ | External Crystal Oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| $F_{PLL}$ | PLL Frequency | – | 23.986 | – | MHz | Multiple (x732) of crystal frequency. |
| Jitter24M2 | 24 MHz Period Jitter (PLL) | – | – | 600 | ps | |
| $T_{PLLSLEW}$ | PLL Lock Time | 0.5 | – | 10 | ms | |
| $T_{PLLSLEWSLOW}$ | PLL Lock Time for Low Gain Setting | 0.5 | – | 50 | ms | |
| $T_{OS}$ | External Crystal Oscillator Startup to 1% | – | 1700 | 2620 | ms | |
| $T_{OSACC}$ | External Crystal Oscillator Startup to 100 ppm | – | 2800 | 3800 | ms | The crystal oscillator frequency is within 100 ppm of its final value by the end of the $T_{osacc}$ period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40°C ≤ $T_A$ ≤ 85°C. |
| Jitter32k | 32 kHz Period Jitter | – | 100 | | ns | |
| $T_{XRST}$ | External Reset Pulse Width | 10 | – | – | µs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| Fout48M | 48 MHz Output Frequency | 46.8 | 48.0 | 49.2[12,14] | MHz | Trimmed. Utilizing factory trim values. |
| Jitter24M1 | 24 MHz Period Jitter (IMO) | – | 600 | | ps | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $T_{RAMP}$ | Supply Ramp Time | 0 | – | – | µs | |

**Notes**
12. 4.75V < Vdd < 5.25V.
13. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
14. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
15. See the individual user module data sheets for information on maximum frequencies for user modules.



[+] Feedback

**Figure 12. PLL Lock Timing Diagram**

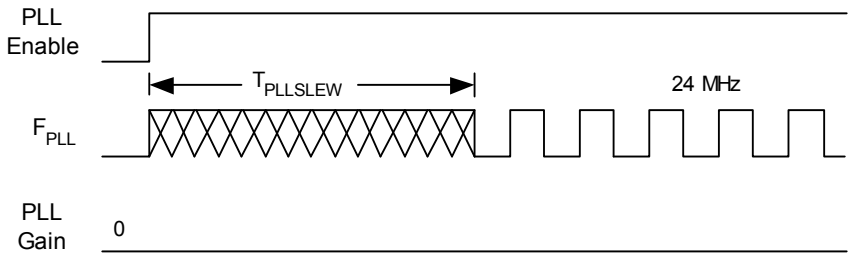



**Figure 13. PLL Lock for Low Gain Setting Timing Diagram**

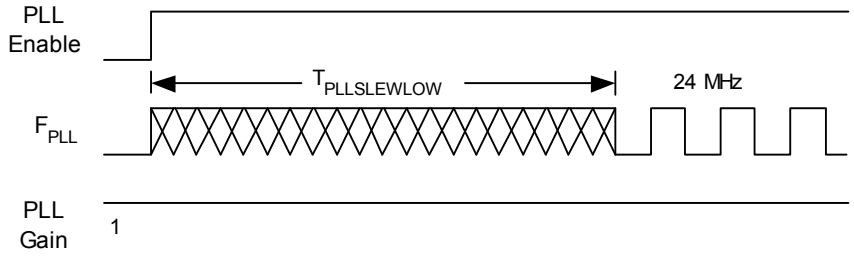



**Figure 14. External Crystal Oscillator Startup Timing Diagram**

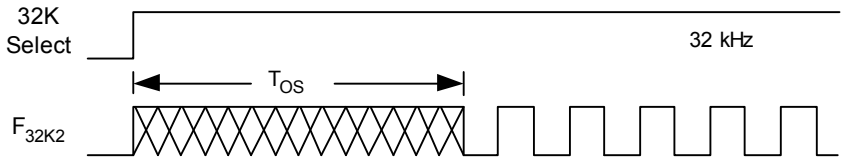



**Figure 15. 24 MHz Period Jitter (IMO) Timing Diagram**

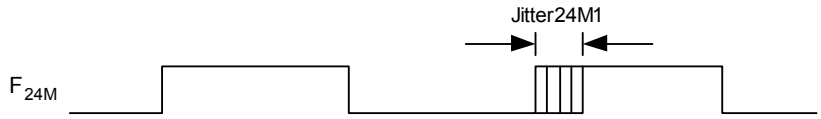
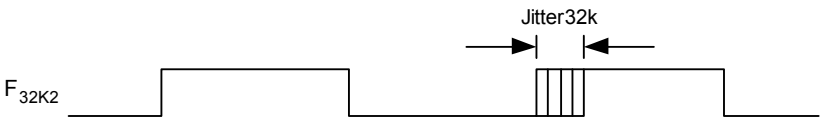



**Figure 16. 32 kHz Period Jitter (ECO) Timing Diagram**






[+] Feedback

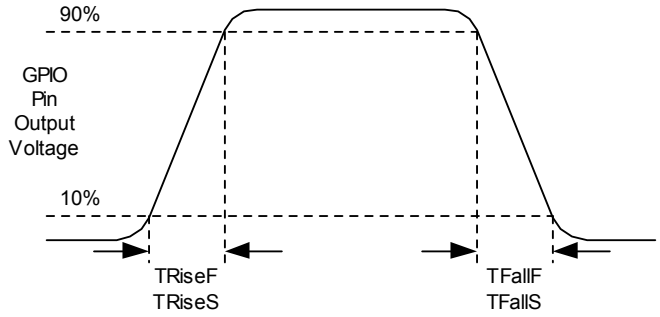
## AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 32. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO Operating Frequency | 0 | – | 12 | MHz | Normal Strong Mode |
| TRiseF | Rise Time, Normal Strong Mode, Cload = 50 pF | 3 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TFallF | Fall Time, Normal Strong Mode, Cload = 50 pF | 2 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TRiseS | Rise Time, Slow Strong Mode, Cload = 50 pF | 10 | 27 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |
| TFallS | Fall Time, Slow Strong Mode, Cload = 50 pF | 10 | 22 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |

**Figure 17. GPIO Timing Diagram**




## AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

**Table 33. 5V AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br><br>–<br>– | <br><br>–<br>– | <br><br>3.9<br>0.72 | <br><br>µs<br>µs |
| | | – | – | 0.62 | µs |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br><br>–<br>– | <br><br>–<br>– | <br><br>5.9<br>0.92 | <br><br>µs<br>µs |
| | | – | – | 0.72 | µs |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br>0.15<br>1.7<br>6.5 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V/µs<br>V/µs<br>V/µs |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br>0.01<br>0.5<br>4.0 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>V/µs<br>V/µs<br>V/µs |



[+] Feedback

**Table 33. 5V AC Operational Amplifier Specifications** (continued)

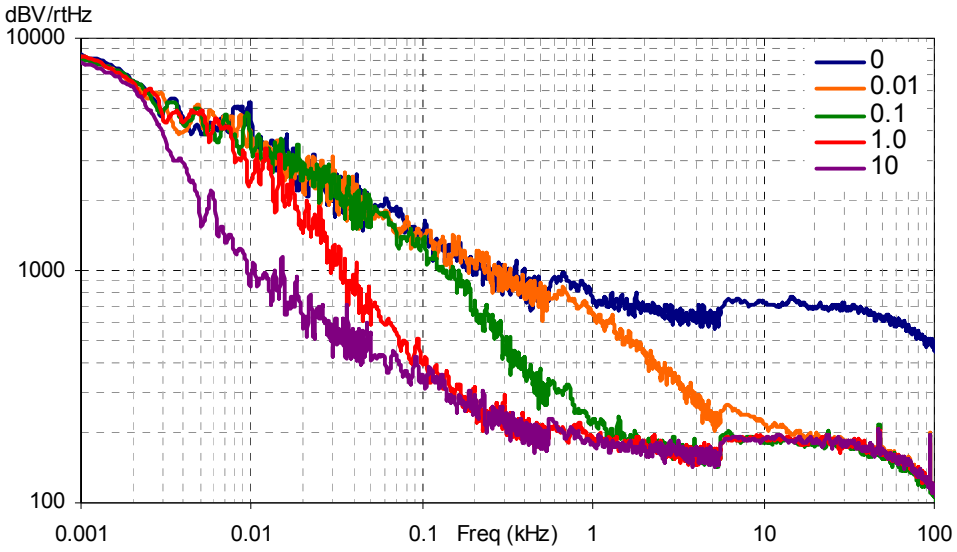
| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $BW_{OA}$ | Gain Bandwidth Product<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High<br>Power = High, Opamp Bias = High | <br>0.75<br>3.1<br>5.4 | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>MHz<br>MHz<br>MHz |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz |

**Table 34. 3.3V AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Low, Opamp Bias = High | <br><br>– | <br><br>– | <br>3.92<br>0.72 | <br>µs<br>µs |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High | <br><br>– | <br><br>– | <br>5.41<br>0.72 | <br>µs<br>µs |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High | <br>0.31<br>2.7 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High | <br>0.24<br>1.8 | <br>–<br>– | <br>–<br>– | <br>V/µs<br>V/µs |
| $BW_{OA}$ | Gain Bandwidth Product<br>Power = Low, Opamp Bias = Low<br>Power = Medium, Opamp Bias = High | <br>0.67<br>2.8 | <br>–<br>– | <br>–<br>– | <br>MHz<br>MHz |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz |

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

**Figure 18. Typical AGND Noise with P2[4] Bypass**

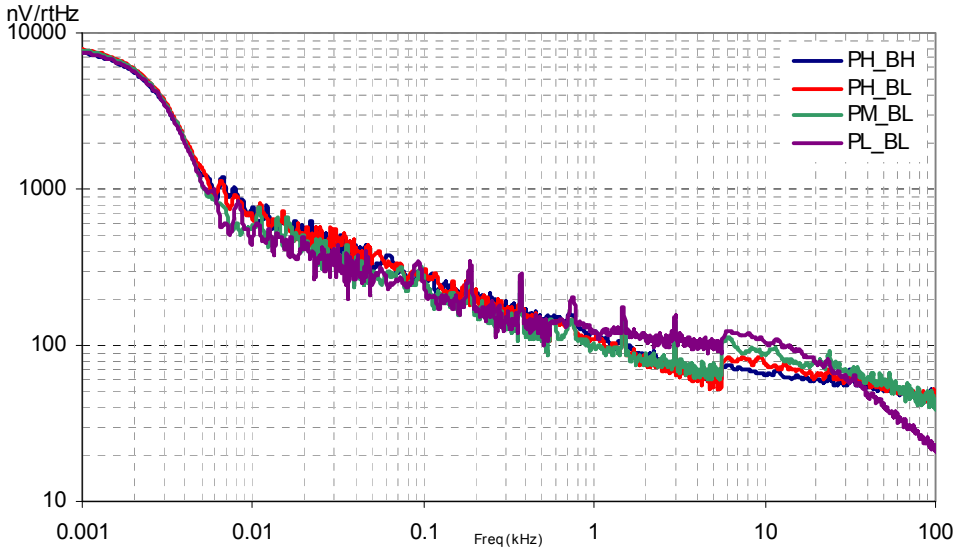



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.



[+] Feedback

**Figure 19. Typical Opamp Noise**




## AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 35. AC Low Power Comparator Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{RLPC}$ | LPC response time | – | – | 50 | µs | ≥ 50 mV overdrive comparator reference set within $V_{REFLPC}$. |

## AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 36. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| All Functions | Maximum Block Clocking Frequency (> 4.75V) | | | 49.2 | | 4.75V < Vdd < 5.25V |
| | Maximum Block Clocking Frequency (< 4.75V) | | | 24.6 | | 3.0V < Vdd < 4.75V |
| Timer | Capture Pulse Width | 50[16] | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| | Maximum Frequency, With Capture | – | – | 24.6 | MHz | |
| Counter | Enable Pulse Width | 50[16] | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| | Maximum Frequency, Enable Input | – | – | 24.6 | MHz | |

**Notes**
16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
17. Refer to Table 47 on page 50



[+] Feedback

**Table 36. AC Digital Block Specifications** (continued)

| Function | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50[16] | – | – | ns | |
| | Disable Mode | 50[16] | – | – | ns | |
| | Maximum Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.6 | MHz | |
| SPIM | Maximum Input Clock Frequency | – | – | 8.2 | MHz | Maximum data rate at 4.1 MHz due to 2 x over clocking. |
| SPIS | Maximum Input Clock Frequency | – | – | 4.1 | MHz | |
| | Width of SS_ Negated Between Transmissions | 50[16] | – | – | MHz | |
| Trans-mitter | Maximum Input Clock Frequency [16]<br>Silicon A | – | – | 16.4 | MHz | Maximum data rate at 2.05 MHz due to 8 x over clocking. |
| | Silicon B | – | – | 24.6 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| | Silicon B Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits | – | – | 49.2 | MHz | Maximum data rate at 6.15 MHz due to 8 x over clocking. |
| Receiver | Maximum Input Clock Frequency [17]<br>Silicon A | – | – | 16.4 | MHz | Maximum data rate at 2.05 MHz due to 8 x over clocking. |
| | Silicon B | – | – | 24.6 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| | Silicon B Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits | – | – | 49.2 | MHz | Maximum data rate at 6.15 MHz due to 8 x over clocking. |



[+] Feedback

## AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 37. 5V AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{ROB}$ | Rising Settling Time to 0.1%, 1V Step, 100 pF Load | | | | |
| | Power = Low | – | – | 2.5 | µs |
| | Power = High | – | – | 2.5 | µs |
| $T_{SOB}$ | Falling Settling Time to 0.1%, 1V Step, 100 pF Load | | | | |
| | Power = Low | – | – | 2.2 | µs |
| | Power = High | – | – | 2.2 | µs |
| $SR_{ROB}$ | Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load | | | | |
| | Power = Low | 0.65 | – | – | V/µs |
| | Power = High | 0.65 | – | – | V/µs |
| $SR_{FOB}$ | Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load | | | | |
| | Power = Low | 0.65 | – | – | V/µs |
| | Power = High | 0.65 | – | – | V/µs |
| $BW_{OB}$ | Small Signal Bandwidth, 20m$V_{pp}$, 3dB BW, 100 pF Load | | | | |
| | Power = Low | 0.8 | – | – | MHz |
| | Power = High | 0.8 | – | – | MHz |
| $BW_{OB}$ | Large Signal Bandwidth, 1$V_{pp}$, 3dB BW, 100 pF Load | | | | |
| | Power = Low | 300 | – | – | kHz |
| | Power = High | 300 | – | – | kHz |

**Table 38. 3.3V AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{ROB}$ | Rising Settling Time to 0.1%, 1V Step, 100 pF Load | | | | |
| | Power = Low | – | – | 3.8 | µs |
| | Power = High | – | – | 3.8 | µs |
| $T_{SOB}$ | Falling Settling Time to 0.1%, 1V Step, 100 pF Load | | | | |
| | Power = Low | – | – | 2.6 | µs |
| | Power = High | – | – | 2.6 | µs |
| $SR_{ROB}$ | Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load | | | | |
| | Power = Low | 0.5 | – | – | V/µs |
| | Power = High | 0.5 | – | – | V/µs |
| $SR_{FOB}$ | Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load | | | | |
| | Power = Low | 0.5 | – | – | V/µs |
| | Power = High | 0.5 | – | – | V/µs |
| $BW_{OB}$ | Small Signal Bandwidth, 20m$V_{pp}$, 3dB BW, 100 pF Load | | | | |
| | Power = Low | 0.7 | – | – | MHz |
| | Power = High | 0.7 | – | – | MHz |
| $BW_{OB}$ | Large Signal Bandwidth, 1$V_{pp}$, 3dB BW, 100 pF Load | | | | |
| | Power = Low | 200 | – | – | kHz |
| | Power = High | 200 | – | – | kHz |



[+] Feedback

## AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 39. 5V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.6 | MHz |
| – | High Period | 20.6 | – | 5300 | ns |
| – | Low Period | 20.6 | – | – | ns |
| – | Power Up IMO to Switch | 150 | – | – | µs |

**Table 40. 3.3V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 1[18] | 0.093 | – | 12.3 | MHz |
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 2 or greater[19] | 0.186 | – | 24.6 | MHz |
| – | High Period with CPU Clock divide by 1 | 41.7 | – | 5300 | ns |
| – | Low Period with CPU Clock divide by 1 | 41.7 | – | – | ns |
| – | Power Up IMO to Switch | 150 | – | – | µs |

## AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 41. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall Time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash Erase Time (Block) | – | 10 | – | ms | |
| $T_{WRITE}$ | Flash Block Write Time | – | 10 | – | ms | |
| $T_{DSCLK}$ | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns | Vdd > 3.6 |
| $T_{DSCLK3}$ | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | 3.0 ≤ Vdd ≤ 3.6 |

**Notes**
18. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
19. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.

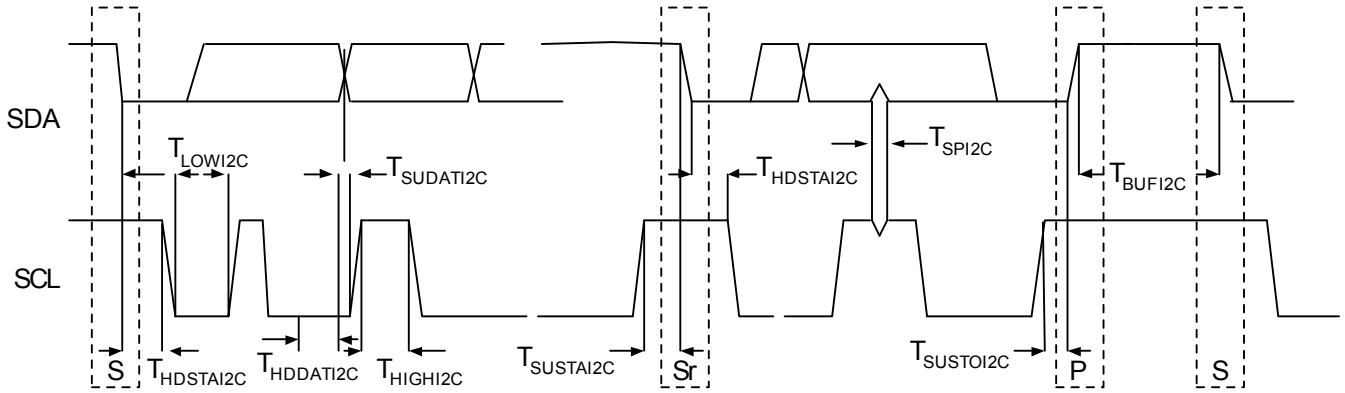
## AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

**Table 42. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs |
| $T_{SUSTAI2C}$ | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs |
| $T_{SUDATI2C}$ | Data Set-up Time | 250 | – | 100[20] | – | ns |
| $T_{SUSTOI2C}$ | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | µs |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns |

**Figure 20. Definition for Timing for Fast/Standard Mode on the I2C Bus**




**Note**

20. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.



[+] Feedback

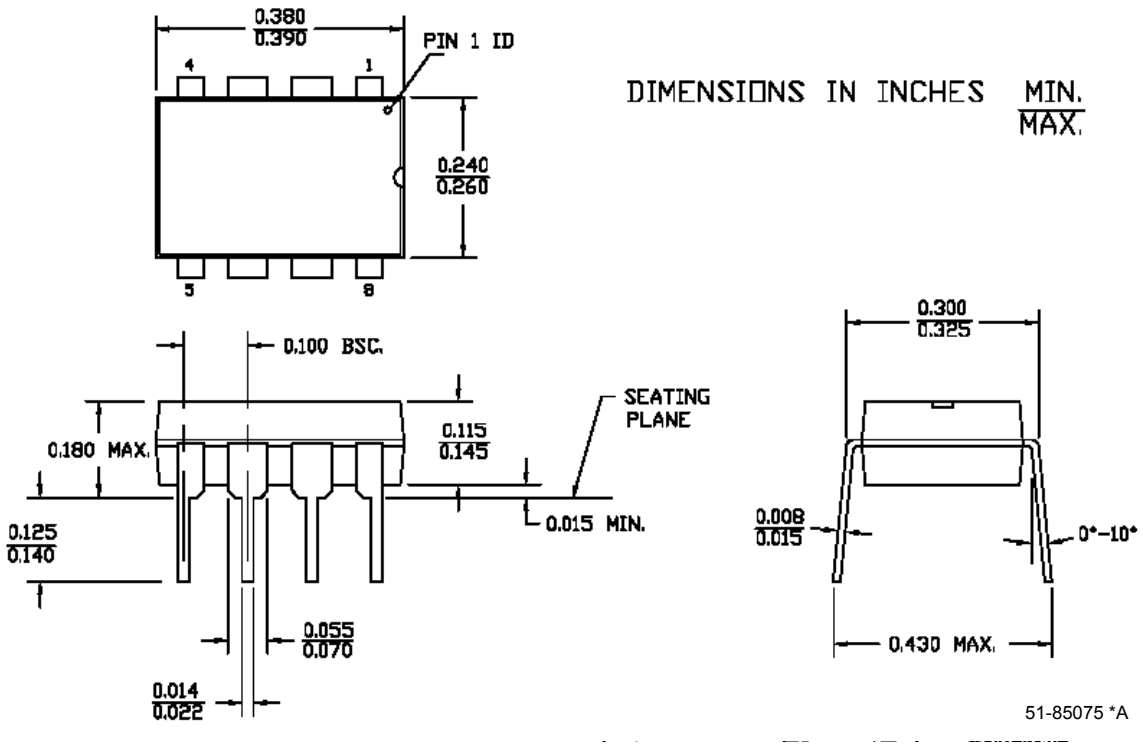
## Packaging Information

This section illustrates the packaging specifications for the CY8C27x43 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

### Packaging Dimensions

**Figure 21. 8-Pin (300-Mil) PDIP**






[+] Feedback

**Figure 22. 20-Pin (210-Mil) SSOP**

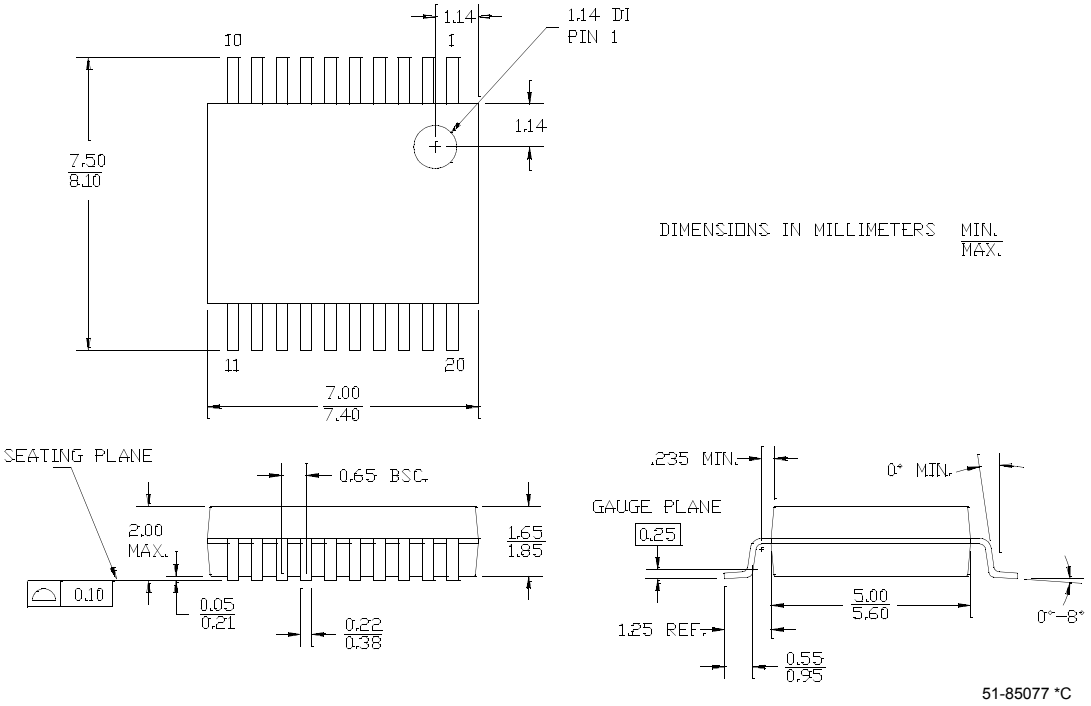
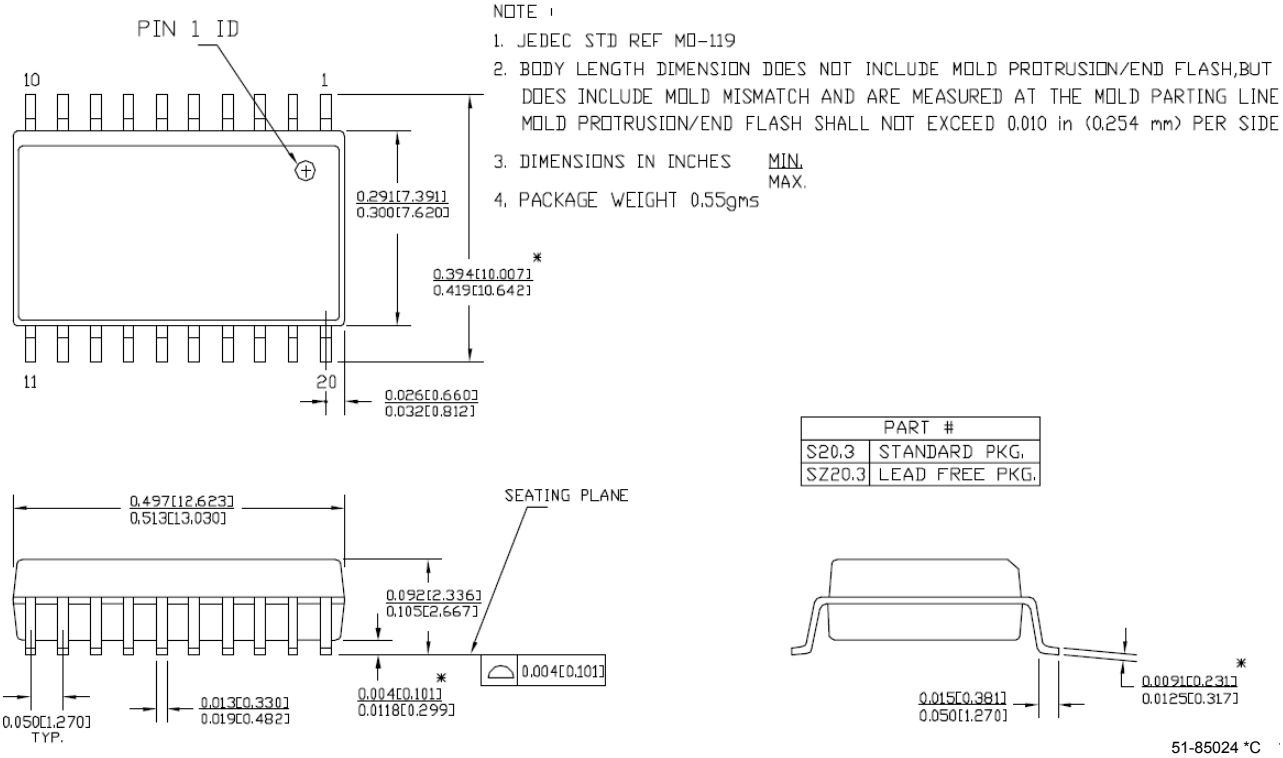



**Figure 23. 20-Pin (300-Mil) Molded SOIC**






[+] Feedback

**Figure 24. 28-Pin (300-Mil) Molded DIP**

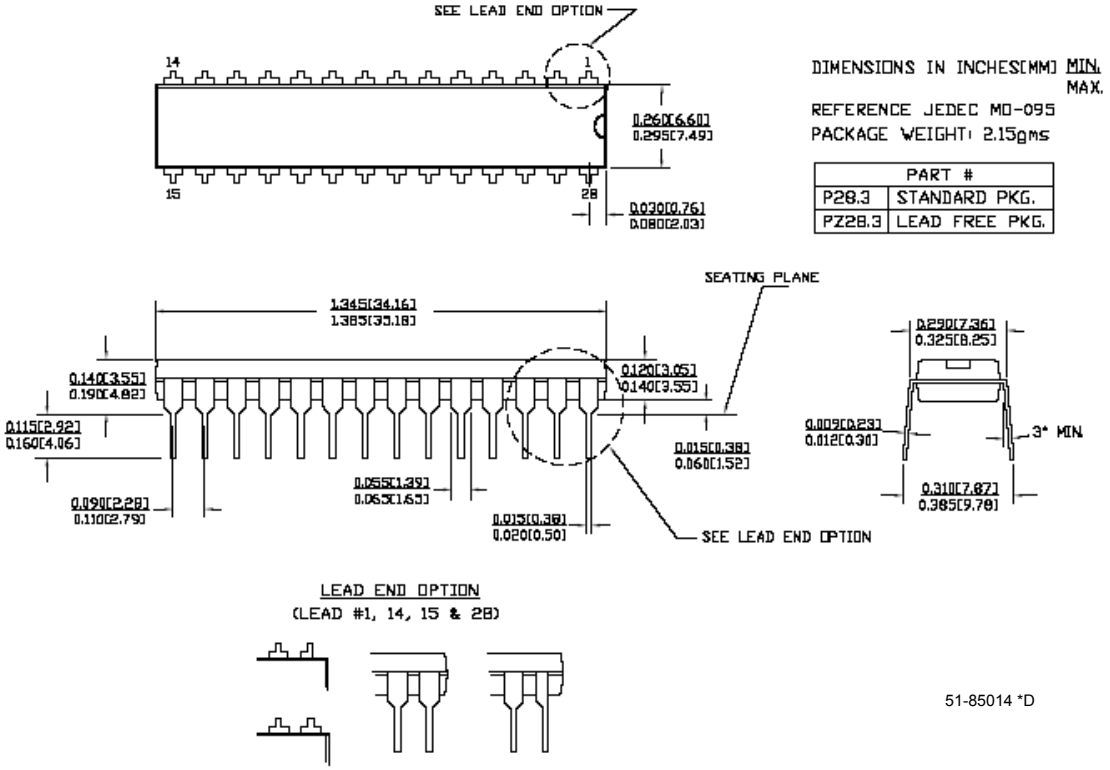
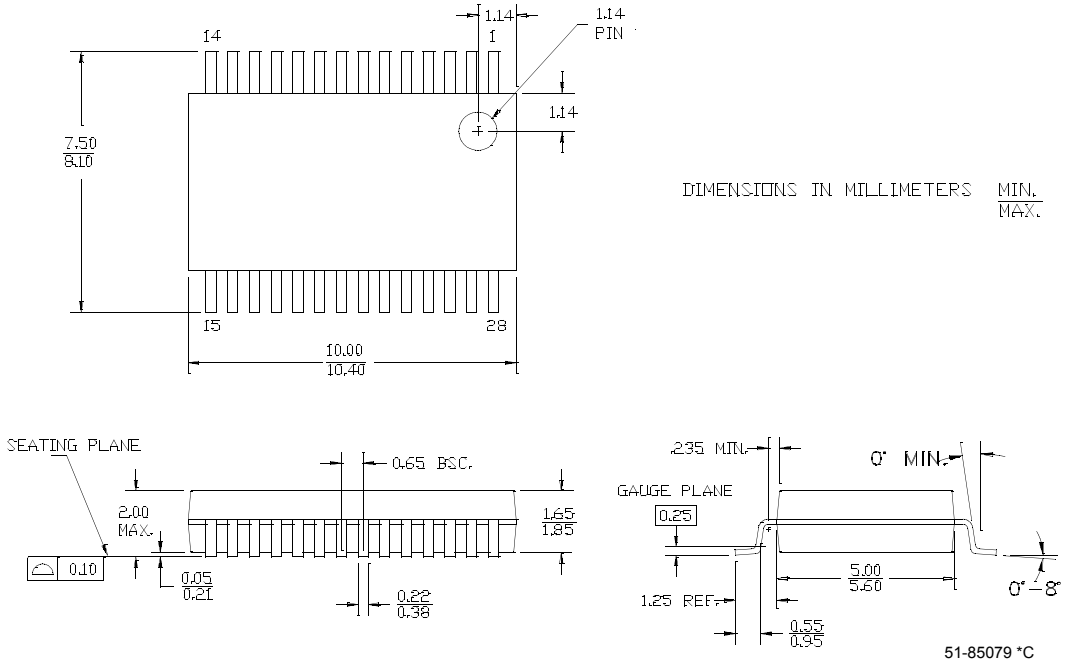



**Figure 25. 28-Pin (210-Mil) SSOP**






[+] Feedback

**Figure 26. 28-Pin (300-Mil) Molded SOIC**

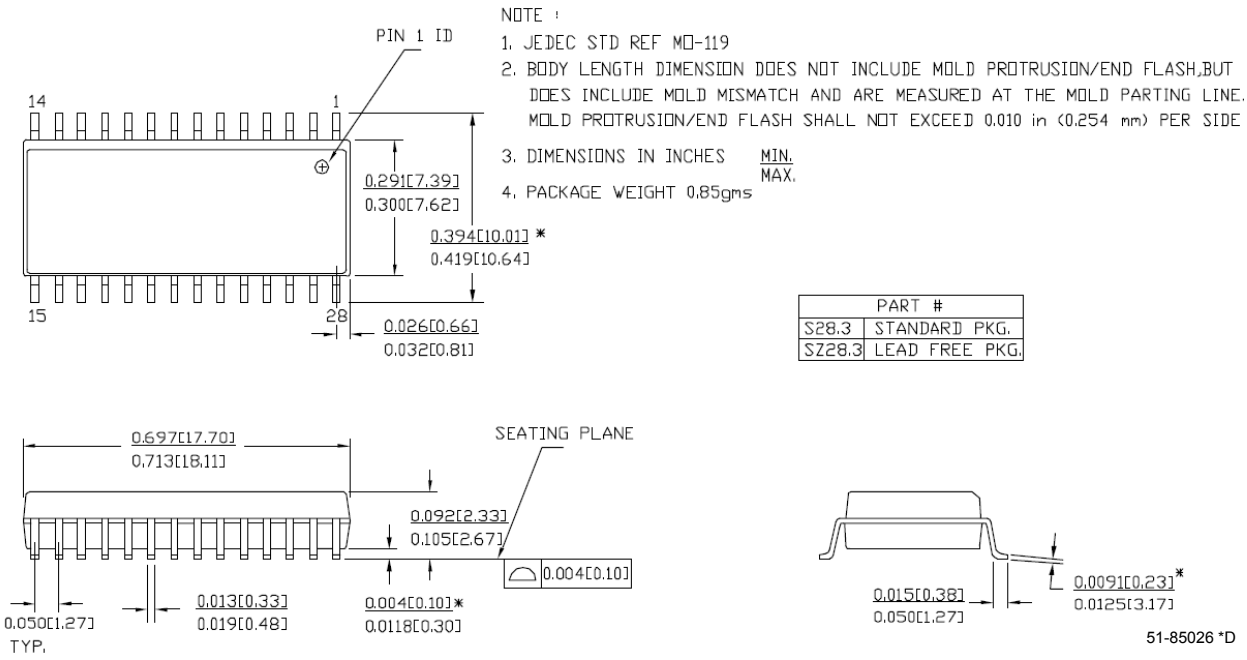
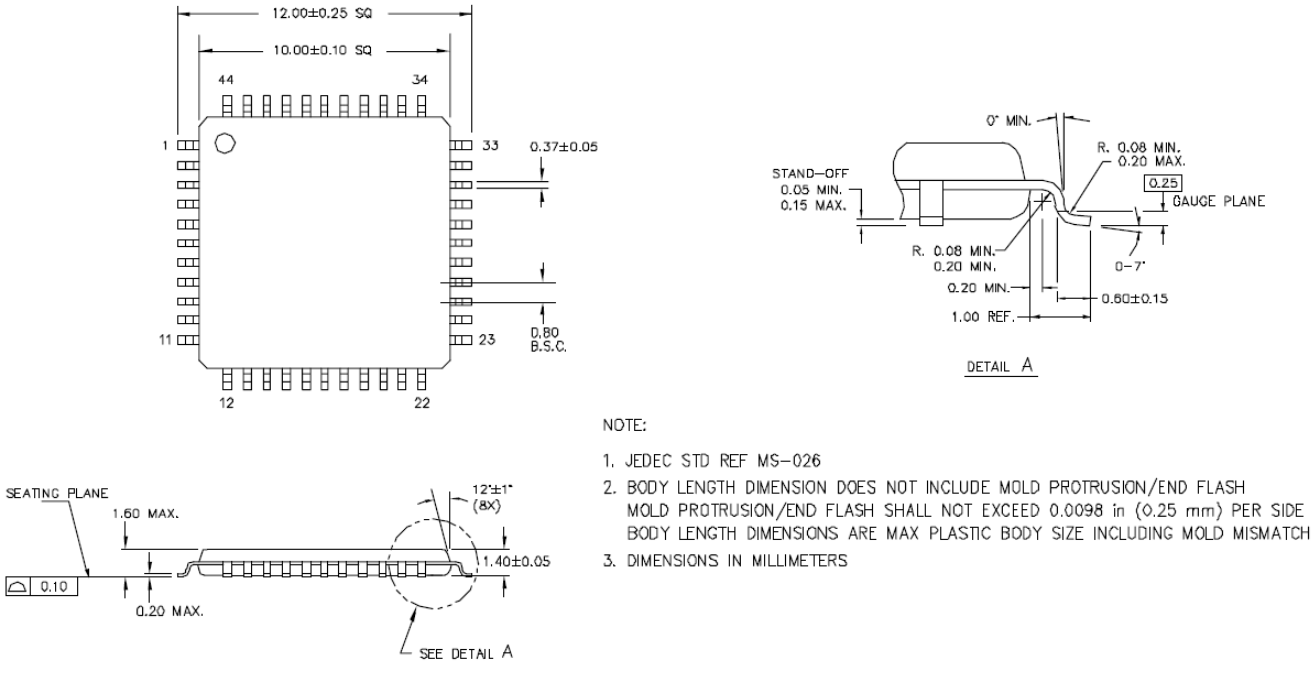



**Figure 27. 44-Pin TQFP**






[+] Feedback

**Figure 28. 48-Pin (300-Mil) SSOP**

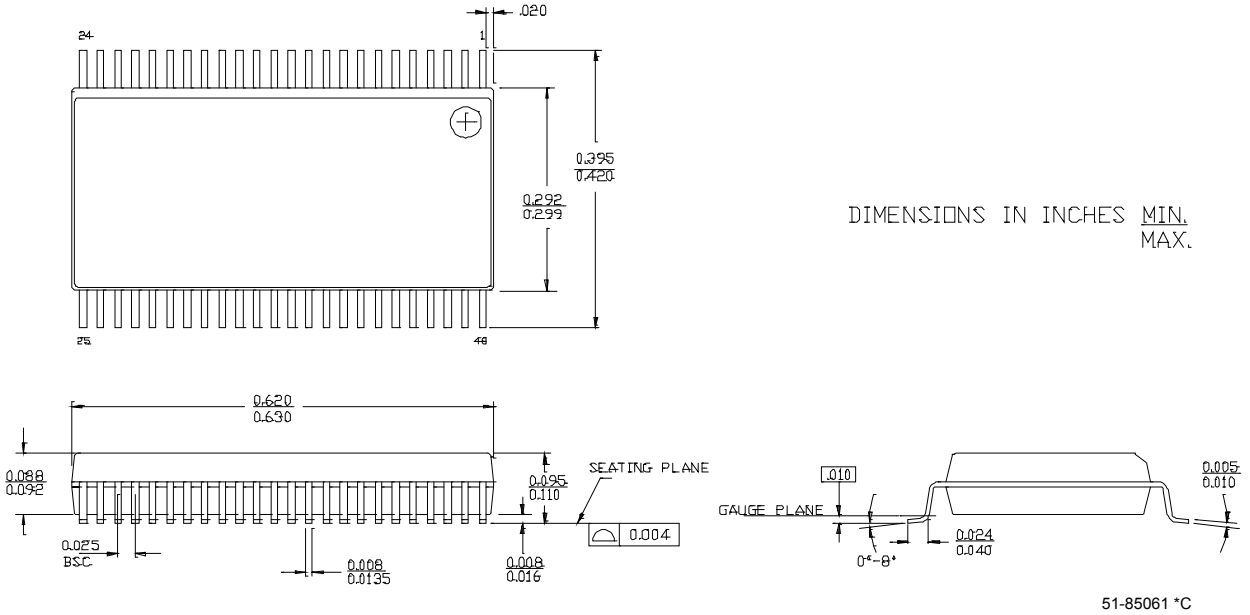
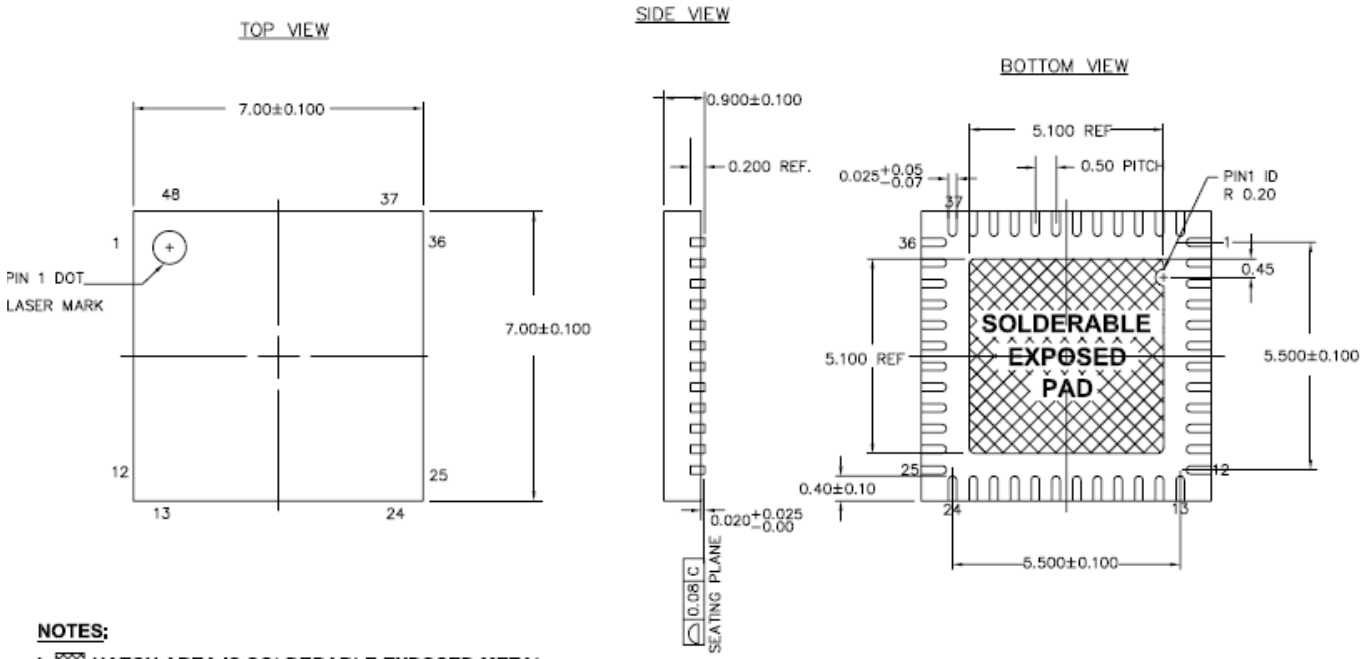


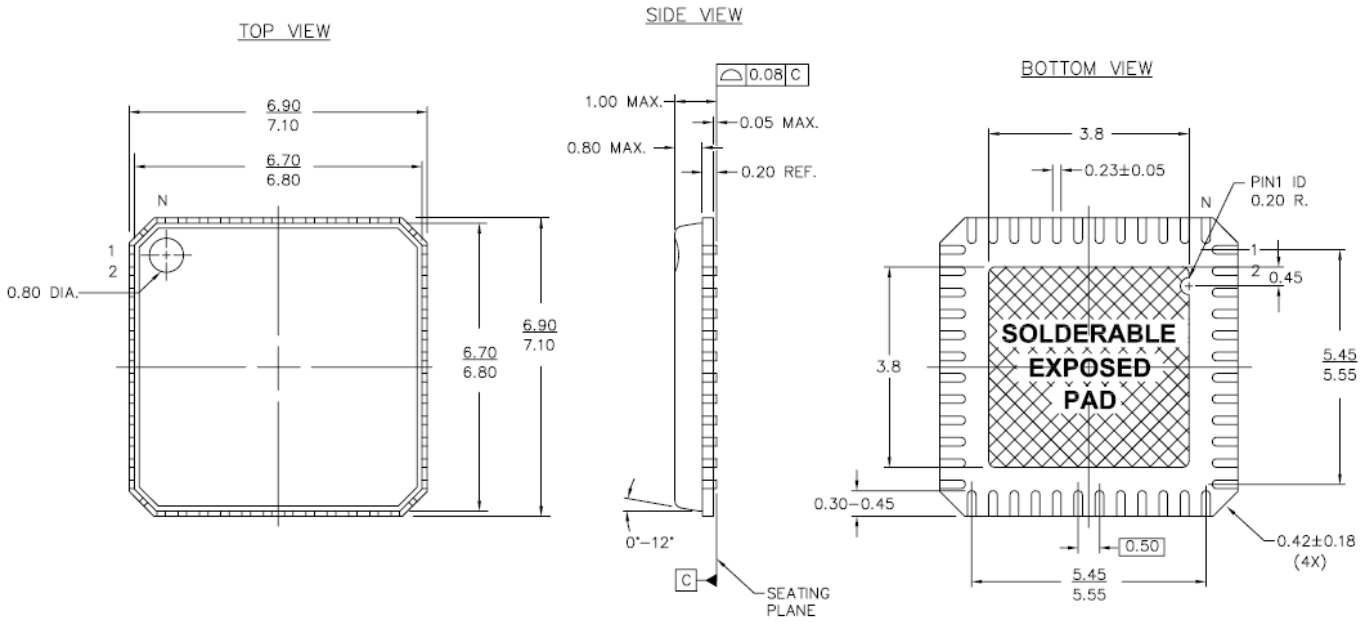

**Figure 29. 48-Pin QFN 7X7X 0.90 MM (Sawn Type)**






[+] Feedback

**Figure 30. 48-Pin (7x7 mm) QFN**




51-85152 *C

**Important Note** For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

## Thermal Impedances

**Table 43. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ * |
|---|---|
| 8 PDIP | 120 °C/W |
| 20 SSOP | 116 °C/W |
| 20 SOIC | 79 °C/W |
| 28 PDIP | 67 °C/W |
| 28 SSOP | 95 °C/W |
| 28 SOIC | 68 °C/W |
| 44 TQFP | 61 °C/W |
| 48 SSOP | 69 °C/W |
| 48 QFN | 18 °C/W |

* $T_J = T_A + POWER \times \theta_{JA}$

## Capacitance on Crystal Pins

**Table 44. Typical Package Capacitance on Crystal Pins**

| Package | Package Capacitance |
|---|---|
| 8 PDIP | 2.8 pF |
| 20 SSOP | 2.6 pF |
| 20 SOIC | 2.5 pF |
| 28 PDIP | 3.5 pF |
| 28 SSOP | 2.8 pF |
| 28 SOIC | 2.7 pF |
| 44 TQFP | 2.6 pF |
| 48 SSOP | 3.3 pF |
| 48 QFN | 2.3 pF |



[+] Feedback

### Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

**Table 45. Solder Reflow Peak Temperature**

| Package | Silicon A* | | Silicon B* | |
|---|---|---|---|---|
| | Minimum Peak Temperature** | Maximum Peak Temperature | Minimum Peak Temperature* | Maximum Peak Temperature |
| 8 PDIP | 220°C | 240°C | 240°C | 260°C |
| 20 SSOP | 220°C | 240°C | 240°C | 260°C |
| 20 SOIC | 220°C | 240°C | 220°C | 260°C |
| 28 PDIP | 220°C | 240°C | 240°C | 260°C |
| 28 SSOP | 220°C | 240°C | 240°C | 260°C |
| 28 SOIC | 220°C | 240°C | 220°C | 260°C |
| 44 TQFP | 220°C | 240°C | 220°C | 260°C |
| 48 SSOP | 220°C | 240°C | 220°C | 260°C |
| 48 QFN | 220°C | 240°C | 240°C | 260°C |

*Refer to Table 47 on page 50.

**Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.



[+] Feedback

## Development Tool Selection

This chapter presents the development tools available for all current PSoC device families including the CY8C27x43 family.

### Software

*PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under DESIGN RESOURCES >> Software and Drivers.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

*CY3202-C iMAGEcraft C Compiler*

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

### Development Kits

All development kits can be purchased from the Cypress Online Store.

*CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

*CY3210-ExpressDK PSoC Express Development Kit*

The CY3210-ExpressDK is for advanced prototyping and development with PSoC Express (may be used with ICE-Cube In-Circuit Emulator). It provides access to $I^2C$ buses, voltage reference, switches, upgradeable modules and more. The kit includes:

- PSoC Express Software CD
- Express Development Board
- 4 Fan Modules
- 2 Proto Modules
- MiniProg In-System Serial Programmer
- MiniEval PCB Evaluation Board
- Jumper Wire Kit
- USB 2.0 Cable
- Serial Cable (DB9)
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- 2 CY8C24423A-24PXI 28-PDIP Chip Samples
- 2 CY8C27443-24PXI 28-PDIP Chip Samples
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

### Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable



[+] Feedback

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3214-PSoCEvalUSB*

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

### Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3216 Modular Programmer*

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
**Note**: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 46. Emulation and Programming Accessories**

| Part # | Pin Package | Flex-Pod Kit[21] | Foot Kit[22] | Adapter[23] |
|---|---|---|---|---|
| CY8C27143-24PXI | 8 PDIP | CY3250-27XXX | CY3250-8PDIP-FK | Adapters can be found at http://www.emulation.com. |
| CY8C27243-24PVXI | 20 SSOP | CY3250-27XXX | CY3250-20SSOP-FK | |
| CY8C27243-24SXI | 20 SOIC | CY3250-27XXX | CY3250-20SOIC-FK | |
| CY8C27443-24PXI | 28 PDIP | CY3250-27XXX | CY3250-28PDIP-FK | |
| CY8C27443-24PVXI | 28 SSOP | CY3250-27XXX | CY3250-28SSOP-FK | |
| CY8C27443-24SXI | 28 SOIC | CY3250-27XXX | CY3250-28SOIC-FK | |
| CY8C27543-24AXI | 44 TQFP | CY3250-27XXX | CY3250-44TQFP-FK | |
| CY8C27643-24PVXI | 48 SSOP | CY3250-27XXX | CY3250-48SSOP-FK | |
| CY8C27643-24LFXI | 48 QFN | CY3250-27XXXQFN | CY3250-48QFN-FK | |

**Notes**
21. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
22. Foot kit includes surface mount feet that can be soldered to the target PCB.
23. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.



[+] Feedback

### 3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under DESIGN RESOURCES >> Evaluation Boards.

### Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/an2323.

## Ordering Information

The following table lists the CY8C27x43 PSoC device’s key package features and ordering codes.

**Table 47. CY8C27x43 PSoC Device Key Features and Ordering Information**

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks (Rows of 4) | Analog Blocks (Columns of 3) | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CY8C27x43 Silicon B – These parts are lead free and offer the following improvements. The DEC_CR1 register selections are enhanced to allow any digital block to be the decimator clock source, the ECO EX and ECO EXW bits in the CPU_SCR1 register are readable, and the accuracy of the analog reference is enhanced (see the Electrical Specifications chapter). All silicon A errata are fixed in silicon B. | | | | | | | | | | | |
| 8 Pin (300 Mil) DIP | CY8C27143-24PXI | 16K | 256 | No | -40C to +85C | 8 | 12 | 6 | 4 | 4 | No |
| 20 Pin (210 Mil) SSOP | CY8C27243-24PVXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin (210 Mil) SSOP (Tape and Reel) | CY8C27243-24PVXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin (300 Mil) SOIC | CY8C27243-24SXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin 300 Mil) SOIC (Tape and Reel) | CY8C27243-24SXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 28 Pin (300 Mil) DIP | CY8C27443-24PXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (210 Mil) SSOP | CY8C27443-24PVXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8C27443-24PVXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (300 Mil) SOIC | CY8C27443-24SXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (300 Mil) SOIC (Tape and Reel) | CY8C27443-24SXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 44 Pin TQFP | CY8C27543-24AXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 40 | 12 | 4 | Yes |
| 44 Pin TQFP (Tape and Reel) | CY8C27543-24AXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 40 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP | CY8C27643-24PVXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP (Tape and Reel) | CY8C27643-24PVXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7x7) QFN | CY8C27643-24LFXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7x7) QFN (Tape and Reel) | CY8C27643-24LFXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 56 Pin OCD SSOP | CY8C27002-24PVXI[24] | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 14 | 4 | Yes |
| **CY8C27x43 Silicon A** – Silicon A is not recommended for new designs. | | | | | | | | | | | |
| 8 Pin (300 Mil) DIP | CY8C27143-24PI | 16K | 256 | No | -40C to +85C | 8 | 12 | 6 | 4 | 4 | No |
| 20 Pin (210 Mil) SSOP | CY8C27243-24PVI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin (210 Mil) SSOP (Tape and Reel) | CY8C27243-24PVIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin (300 Mil) SOIC | CY8C27243-24SI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 20 Pin 300 Mil) SOIC (Tape and Reel) | CY8C27243-24SIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 16 | 8 | 4 | Yes |
| 28 Pin (300 Mil) DIP | CY8C27443-24PI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (210 Mil) SSOP | CY8C27443-24PVI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8C27443-24PVIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |

**Note**
24. This part may be used for in-circuit debugging. It is NOT available for production.



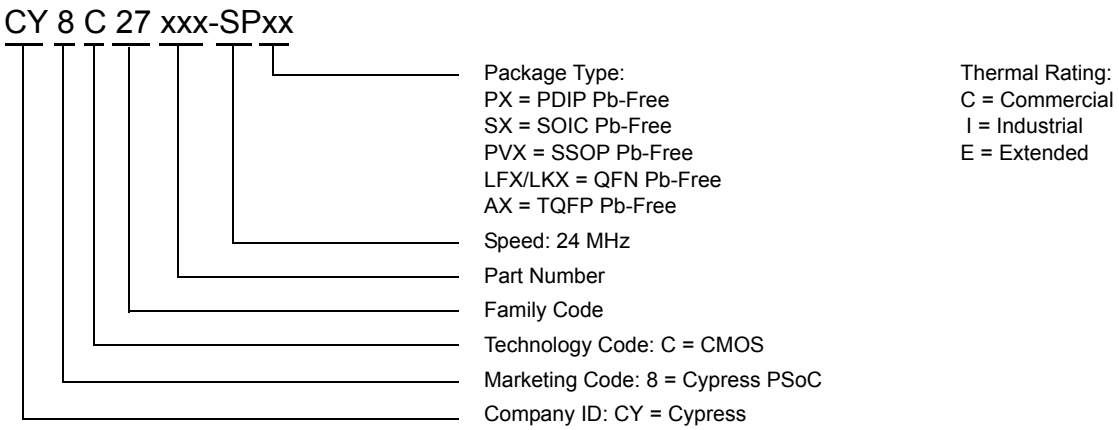
[+] Feedback

**Table 47. CY8C27x43 PSoC Device Key Features and Ordering Information** (continued)

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks (Rows of 4) | Analog Blocks (Columns of 3) | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 28 Pin (300 Mil) SOIC | CY8C27443-24SI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (300 Mil) SOIC (Tape and Reel) | CY8C27443-24SIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 24 | 12 | 4 | Yes |
| 44 Pin TQFP | CY8C27543-24AI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 40 | 12 | 4 | Yes |
| 44 Pin TQFP (Tape and Reel) | CY8C27543-24AIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 40 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP | CY8C27643-24PVI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP (Tape and Reel) | CY8C27643-24PVIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7x7) MLF | CY8C27643-24LFI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7x7) MLF (Tape and Reel) | CY8C27643-24LFIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7X7X 0.90 MM) QFN (Sawn) | CY8C27643-24LTXI | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (7X7X 0.90 MM) QFN (Sawn) | CY8C27643-24LTXIT | 16K | 256 | Yes | -40C to +85C | 8 | 12 | 44 | 12 | 4 | Yes |

**Note** For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

### Ordering Code Definitions






[+] Feedback

## Document History Page

| Document Title: CY8C27143, CY8C27243, CY8C27443, CY8C27543, CY8C27643 PSoC® Programmable System-on-Chip™<br>Document Number: 38-12012 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN No.** | **Submission Date** | **Origin of Change** | **Description of Change** |
| ** | 127087 | 7/01/2003 | New Silicon. | New document (Revision **). |
| *A | 128780 | 7/29/2003 | Engineering and NWJ. | New electrical spec additions, fix of Core Architecture links, corrections to some text, tables, drawings, and format. |
| *B | 128992 | 8/14/2003 | NWJ | Interrupt controller table fixed, refinements to Electrical Spec section and Register chapter. |
| *C | 129283 | 8/28/2003 | NWJ | Significant changes to the Electrical Specifications section. |
| *D | 129442 | 9/09/2003 | NWJ | Changes made to Electrical Spec section. Added 20/28-Lead SOIC packages and pinouts. |
| *E | 130129 | 10/13/2003 | NWJ | Revised document for Silicon Revision A. |
| *F | 130651 | 10/28/2003 | NWJ | Refinements to Electrical Specification section and I2C chapter. |
| *G | 131298 | 11/18/2003 | NWJ | Revisions to GDI, RDI, and Digital Block chapters. Revisions to AC Digital Block Spec and miscellaneous register changes. |
| *H | 229416 | See ECN | SFV | New data sheet format and organization. Reference the *PSoC Programmable System-on-Chip Technical Reference Manual* for additional information. Title change. |
| *I | 247529 | See ECN | SFV | Added Silicon B information to this data sheet. |
| *J | 355555 | See ECN | HMT | Add DS standards, update device table, swap 48-pin SSOP 45 and 46, add Reflow Peak Temp. table. Add new color and logo. Re-add pinout ISSP notation. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications. |
| *K | 523233 | See ECN | HMT | Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add new Dev. Tool section. Add CY8C20x34 to PSoC Device Characteristics table. Add OCD pinout and package diagram. Add ISSP note to pinout tables. Update package diagram revisions. Update typical and recommended Storage Temperature per industrial specs. Update CY branding and QFN convention. Update copyright and trademarks. |
| *L | 2545030 | 07/29/08 | YARA | Added note to DC Analog Reference Specification table and Ordering Information. |
| *M | 2696188 | 04/22/2009 | DPT/PYRS | Changed title from " CY8C27143, CY8C27243, CY8C27443, CY8C27543, and CY8C27643 PSoC Mixed Signal Array Final Data Sheet" to "CY8C27143, CY8C27243, CY8C27443, CY8C27543, CY8C27643 PSoC® Programmable System-on-Chip™". Updated data sheet template. Added 48-Pin QFN (Sawn) package outline diagram and Ordering information details for CY8C27643-24LTXI and CY8C27643-24LTXIT parts |



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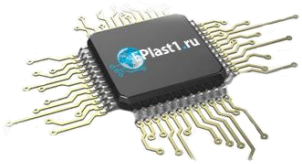
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- Техническая поддержка проекта;
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**Как с нами связаться**

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