TDF8590TH

2 × 80 W SE (4 Ω) or 1 × 160 W BTL (8 Ω) class-D amplifier

Rev. 02 — 23 April 2007 Product data sheet

1. General description

The TDF8590TH is a high-efficiency class-D audio power amplifier with low power dissipation for application in car audio systems. The typical output power is 2 × 80 W into 4 Ω.

The TDF8590TH is available in an HSOP24 power package with a small internal heat sink. Depending on the supply voltage and load conditions, a small or even no external heat sink is required. The amplifier operates over a wide supply voltage range from ±14 V to ±29 V and consumes a low quiescent current.

2. Features

- Zero dead time switching
- Advanced output current protection
- No DC offset induced pop noise at mode transitions
- High efficiency
- Supply voltage from ±14 V to ±29 V
- Low quiescent current
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Fixed gain of 26 dB in SE and 32 dB in BTL
- High BTL output power: 160 W into 8 Ω, 120 W into 4 Ω
- Suitable for speakers in the range of 2 Ω to 8 Ω
- High supply voltage ripple rejection
- Internal oscillator or synchronized to an external clock
- Full short-circuit proof outputs across load and to supply lines
- Thermal foldback and thermal protection

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDF8590TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

founded by Philips

4. Block diagram

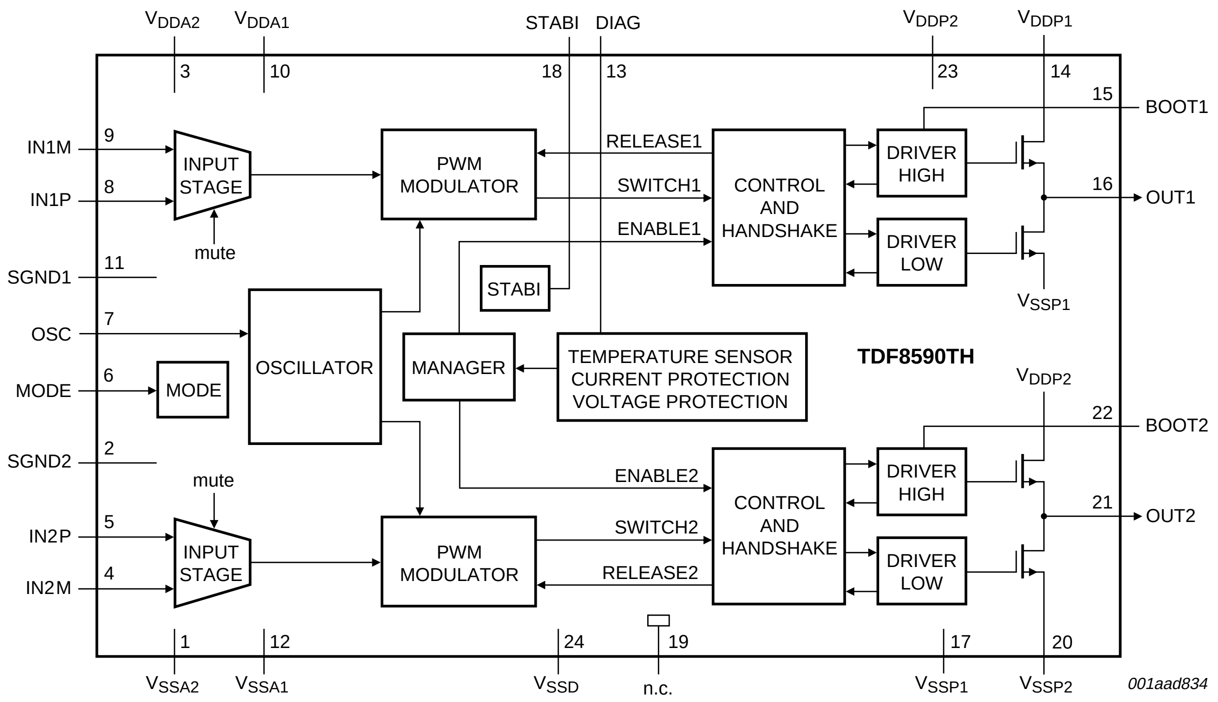


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

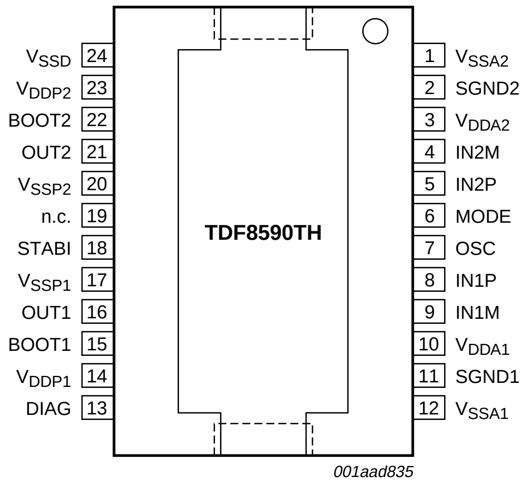


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SSA2}	1	negative analog supply voltage for channel 2
SGND2	2	signal ground for channel 2
V_{DDA2}	3	positive analog supply voltage for channel 2
IN2M	4	negative audio input for channel 2
IN2P	5	positive audio input for channel 2
MODE	6	mode selection input: standby, mute or operating
OSC	7	oscillator frequency adjustment or tracking input
IN1P	8	positive audio input for channel 1
IN1M	9	negative audio input for channel 1
V_{DDA1}	10	positive analog supply voltage for channel 1
SGND1	11	signal ground for channel 1
V_{SSA1}	12	negative analog supply voltage for channel 1
DIAG	13	diagnostic for activated current protection
V_{DDP1}	14	positive power supply voltage for channel 1
BOOT1	15	bootstrap capacitor for channel 1
OUT1	16	PWM output from channel 1
V_{SSP1}	17	negative power supply voltage for channel 1
STABI	18	decoupling of internal stabilizer for logic supply
n.c.	19	not connected
V_{SSP2}	20	negative power supply voltage for channel 2
OUT2	21	PWM output from channel 2
BOOT2	22	bootstrap capacitor for channel 2
V_{DDP2}	23	positive power supply voltage for channel 2
V_{SSD}	24	negative digital supply voltage[1]

[1] The heatsink is internally connected to pin V_{SSD}.

6. Functional description

6.1 Introduction

The TDF8590TH is a dual channel audio power amplifier using class-D technology. The audio input signal is converted into a Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high-side and low-side. An external 2nd-order low-pass filter converts the PWM output signal to an analog audio signal across the loudspeakers.

The TDF8590TH contains two independent amplifier channels with a differential input stage, high output power, high efficiency (90 %), low distortion and a low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Dual Single-Ended (SE) amplifiers

The TDF8590TH also contains circuits common to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager. For protection a thermal foldback, temperature, current and voltage protection are built in.

6.2 Mode selection

The TDF8590TH can be switched in three operating modes via pin MODE:

- Standby mode; the amplifiers are switched off to achieve a very low supply current
- Mute mode; the amplifiers are switching idle (50 % duty cycle), but the audio signal at the output is suppressed by disabling the VI-converter input stages
- Operating mode; the amplifiers are fully operational with output signal

The input stage (see Figure 1) contributes to the DC offset measured at the amplifier output. To avoid pop noise the DC output offset voltage should be increased gradually at a mode transition from mute to operating, or vice versa, by limiting the dV_{MODE}/dt on pin MODE, resulting in a small $dV_{O(offset)}/dt$ for the DC output offset voltage. The required time constant for a gradually increase of the DC output offset voltage between mute and operating is generated via an RC network on pin MODE. An example of a switching circuit for driving pin MODE is illustrated in Figure 3 and explained in Table 3.

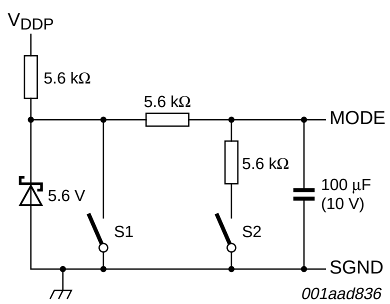


Fig 3. Example of mode selection circuit

Table 3. Mode selection

S1	S2	Mode selection
closed	closed	Standby mode
closed	open	Standby mode
open	closed	Mute mode
open	open	Operating mode

The value of the RC time constant should be dimensioned for 500 ms. If the 100 μF capacitor is left out of the application the voltage on pin MODE will be applied with a much smaller time constant, which might result in audible pop noises during start-up (depending on DC output offset voltage and used loudspeaker).

In order to fully charge the coupling capacitors at the inputs, the amplifier will remain automatically in Mute mode for approximately 150 ms before switching to Operating mode. A complete overview of the start-up timing is given in Figure 4.

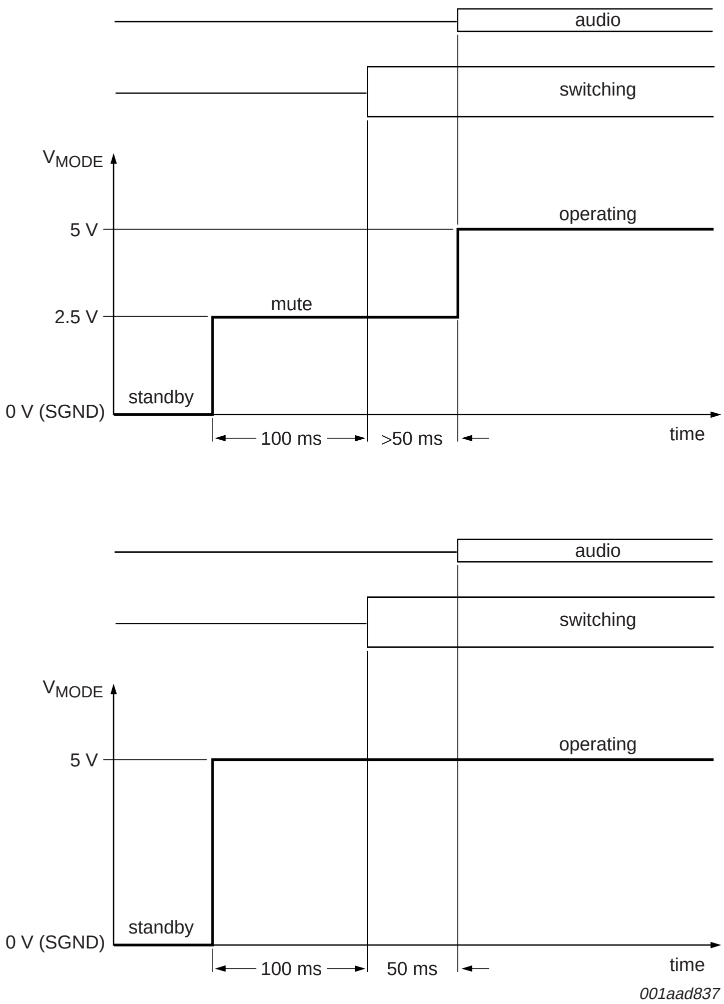


Fig 4. Timing on mode selection input

6.3 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a switching frequency that is set by an external resistor $R_{ext(OSC)}$ connected between pins OSC and V_{SSA}. An optimum setting for the carrier frequency is between 300 kHz and 350 kHz. An external resistor $R_{ext(OSC)}$ of 30 kΩ sets the frequency to 310 kHz.

If two or more class-D amplifiers are used in the same audio application, it is recommended to synchronize the switching frequency of all devices to an external clock (see Section 12.3).

6.4 Protections

The following protections are included in TDF8590TH:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protections
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - Unbalance Protection (UBP)

The reaction of the device on the different fault conditions differs per protection and is described in Section 6.4.1 to Section 6.4.5.

6.4.1 Thermal foldback

If the junction temperature $T_j > 145$ °C, then the TF gradually reduced the gain, resulting in a smaller output signal and less dissipation. At $T_j = 155$ °C the outputs are fully muted.

6.4.2 Overtemperature protection

If $T_j > 160$ °C, then the OTP will shut down the power stage immediately.

6.4.3 Overcurrent protection

The OCP will detect a short-circuit between the loudspeaker terminals or if one of the loudspeaker terminals is short-circuited to one of the supply lines.

If the output current tends to exceed the maximum output current of 8 A, the output voltage of the TDF8590TH will be regulated to a level where the maximum output current is limited to 8 A while the amplifier outputs remain switching, the amplifier does not shut down. When this active current limiting continues longer than a time τ (see Figure 5) the capacitor on pin DIAG is discharged below a threshold value and the TDF8590TH shuts down. Activation of current limiting and the triggering of the OCP is observed at pin DIAG (see Figure 5).

A maximum value for the capacitor on pin DIAG is 47 pF. The reference voltage on pin DIAG is V_{SSA}. Pin DIAG should not be connected to an external pull-up.

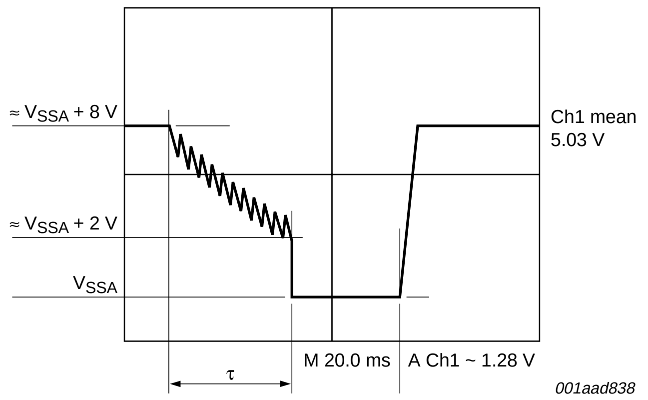


Fig 5. Pin DIAG with activated current limiting

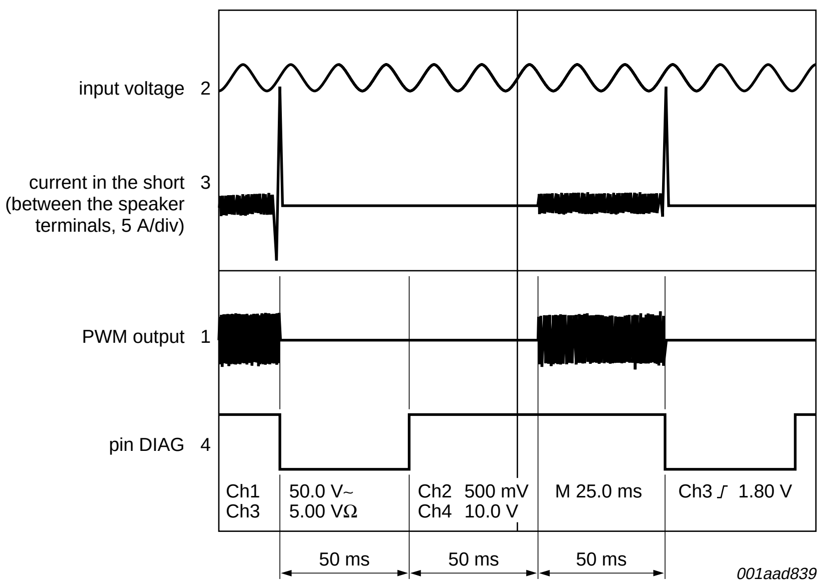


Fig 6. Restart of the TDF8590TH

When the loudspeaker terminals are short-circuited and the OCP is triggered the TDF8590TH is switched off completely and will try to restart every 100 ms (see Figure 6):

- 50 ms after switch off pin DIAG will be released
- 100 ms after switch off the amplifier will return to mute
- 150 ms after switch off the amplifier will return to operation. If the short-circuit condition is still present after this time this cycle will be repeated. The average dissipation will be low because of the small duty cycle

A short of the loudspeaker terminals to one of the supply lines will also trigger the activation of the OCP and the amplifier will shut down. During restart the window protection will be activated. As a result the amplifier will not start up after 100 ms and pin DIAG will remain LOW until the short to the supply lines is removed.

6.4.4 Window protection

The WP checks the conditions at the output terminals of the power stage and is activated:

- During the start-up sequence, when pin MODE is switched from standby to mute. In the event of a short-circuit at one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the TDF8590TH waits until the short to the supply lines has been removed. Because the test is done before enabling the power stages, no large currents will flow in the event of a short-circuit.
- When the amplifier is completely shut down due to activation of the OCP because a short to one of the supply lines is made, then during restart (after 100 ms) the window protection will be activated. As a result the amplifier will not start up until the short to the supply lines is removed.

6.4.5 Supply voltage protections

If the supply voltage drops below ±12.5 V, the UVP circuit is activated and the TDF8590TH switch-off will be silent and without pop noise. When the supply voltage rises above ±12.5 V, the TDF8590TH is restarted again after 100 ms.

If the supply voltage exceeds ±33 V the OVP circuit is activated and the power stages will shut down. It is re-enabled as soon as the supply voltage drops below ±33 V. So in this case no timer of 100 ms is started. The maximum operating supply voltage is ±29 V and if the supply voltage is above the maximal allowable voltage of ±34 V (see Section 7), the TDF8590TH can be damaged, irrespective of an activated OVP. See Section 12.6 "Pumping effects" for more information about the use of the OVP.

An additional UBP circuit compares the positive analog (V_{DDA}) and the negative analog (V_{SSA}) supply voltages and is triggered if the voltage difference between them exceeds the unbalance threshold level, which is expressed as follows:

$$V_{th(unb)} \approx 0.15 \times (V_{DDA} - V_{SSA})\ \mathrm{V}$$

When the supply voltage difference $V_{DDA} - V_{SSA}$ exceeds $V_{th(unb)}$, the TDF8590TH switches off and is restarted again after 100 ms.

Example: With a symmetrical supply of V_{DDA} = 20 V and V_{SSA} = −20 V, the unbalance protection circuit will be triggered if the unbalance exceeds approximately 6 V.

In Table 4 an overview is given of all protections and the effect on the output signal.

Table 4. Overview protections TDF8590TH

Protection name	Complete shut down	Restart directly	Restart every 100 ms	DIAG
TF	N	Y[1]	N	N
OTP	Y	Y[2]	N[2]	N
OCP	N[3]	Y[3]	N[3]	Y
WP	Y[4]	Y	N	Y
UVP	Y	N	Y	N
OVP	Y	Y	N	N
UBP	Y	N	Y	N

[1] Amplifier gain will depend on junction temperature and heat sink size.

[2] Thermal foldback will influence restart timing depending on heat sink size.

[3] Only complete shut down of amplifier in case of a short-circuit. In all other cases current limiting resulting in clipping output signal.

[4] Fault condition detected during (every) transition between standby-to-mute and during restart after activation of OCP (short to one of the supply lines).

6.5 Diagnostic output

Pin DIAG is pulled LOW when the OCP is triggered. With a continuous shorted load a switching pattern in the voltage on pin DIAG is observed (see Figure 6). A permanent LOW on pin DIAG indicates a short to the supply lines whereas a shorted load causes a switching DIAG pin (see Section 6.4.3).

The pin DIAG reference voltage is V_{SSA}. Pin DIAG should not be connected to an external pull-up. An example of a circuit to read out and level shift the diagnostic data is given in Figure 7. V5V represents a logic supply that is used in the application by the microprocessor that reads out the DIAG data.

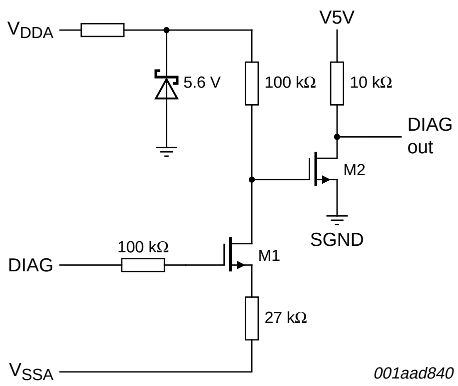


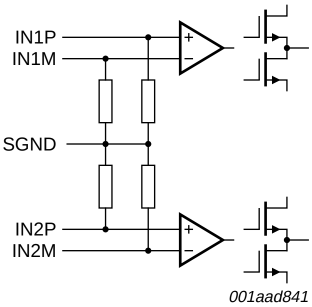
Fig 7. DIAG readout circuit with level shift

6.6 Differential inputs

For a high Common Mode Rejection Ratio (CMRR) and a maximum of flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels can be inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier.

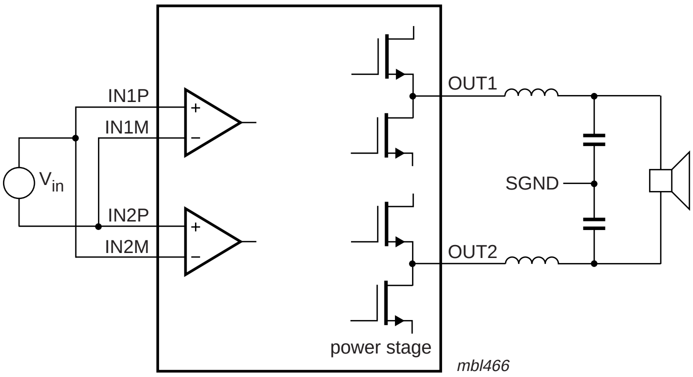
The input configuration for a mono BTL application is illustrated in Figure 8.

In the stereo SE configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies (supply pumping).



Input resistors are referred to SGND.

a. Internal circuitry



b. External connections

Fig 8. Input configuration for mono BTL application

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	V_{DDP1} and V_{DDA1} referred to SGND1; V_{DDP2} and V_{DDA2} referred to SGND2		–0.3	+34	V
V_{SS}	negative supply voltage	V_{SSP1} and V_{SSA1} referred to SGND1; V_{SSP2} and V_{SSA2} referred to SGND2		–34	+0.3	V
V_P	supply voltage			–0.3	+66	V
I_{OSM}	non-repetitive peak output current			-	12	A
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			–40	+150	°C
V_{BOOT1}	voltage on pin BOOT1	referred to OUT1	[1]	0	14	V
V_{BOOT2}	voltage on pin BOOT2	referred to OUT2	[1]	0	14	V
V_{STABI}	voltage on pin STABI	referred to V_{SSD}	[2]	-	14	V

Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{MODE}	voltage on pin MODE	referred to SGND2		0	8	V
V_{OSC}	voltage on pin OSC	referred to V_{SSD}		0	40	V
V_{IN1M}	voltage on pin IN1M	referred to SGND1		–5	+5	V
V_{IN1P}	voltage on pin IN1P	referred to SGND1		–5	+5	V
V_{IN2M}	voltage on pin IN2M	referred to SGND2		–5	+5	V
V_{IN2P}	voltage on pin IN2P	referred to SGND2		–5	+5	V
V_{DIAG}	voltage on pin DIAG	referred to V_{SSD}	[3]	0	9	V
V_O	output voltage			$V_{SSP} - 0.3$	$V_{DDP} + 0.3$	V

[1] Pin BOOT should not be loaded by any other means than the boot capacitor. Shorting pin BOOT to V_{SS} will damage the device.

[2] Pin STABI should not be loaded by an external circuit. Shorting pin STABI to a voltage source or V_{SS} will damage the device.

[3] Pin DIAG should not be connected to a voltage source or to a pull-up resistor. An example of a circuit that can be used to read out diagnostic data is given in Figure 7.

8. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case		1.1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	35	K/W

9. Static characteristics

Table 7. Static characteristics

$V_P = \pm27$ V; f_{osc} = 310 kHz; T_{amb} = –40 °C to +85 °C; T_j = –40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage		[1]	±14	±27	±29	V
$I_{q(tot)}$	total quiescent current	no load, no filter, no snubber network connected		-	50	65	mA
I_{stb}	standby current	T_j = –40 °C to +85 °C		-	150	500	μA
Mode select input; pin MODE (reference to SGND2)							
I_{MODE}	current on pin MODE	V_{MODE} = 5.5 V		-	100	300	μA
V_{MODE}	voltage on pin mode	Standby mode	[2][3]	0	-	0.8	V
		Mute mode	[2][3]	2.2	-	2.8	V
		Operating mode	[2][3]	4.2	-	6	V
Diagnostic output; pin DIAG (reference to V_{SSD})							
V_{OL}	LOW-level output voltage	activated OCP or WP	[4]	-	-	0.8	V
V_{OH}	HIGH-level output voltage	no activated OCP or WP	[4]	-	8.4	9	V
Audio inputs; pins IN1M, IN1P (reference to SGND1), IN2P and IN2M (reference to SGND2)							
V_I	input voltage		[2]	-	0	-	V

Table 7. Static characteristics *...continued*

$V_P = \pm 27$ V; $f_{osc} = 310$ kHz; $T_{amb} = -40$ °C to +85 °C; $T_j = -40$ °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier outputs; pins OUT1 and OUT2							
$V_{O(offset)}$	output offset voltage	SE; mute		-	-	20	mV
		SE; operating	[5]	-	-	170	mV
		BTL; mute		-	-	30	mV
		BTL; operating	[5]	-	-	240	mV
Stabilizer output; pin STABI (reference to V_{SSP1})							
V_O	output voltage	mute and operating; with respect to V_{SSD}		11	12.5	14	V
Temperature protection							
T_{prot}	protection temperature			-	160	180	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature	closed loop SE voltage gain reduced with 6 dB	[6]	145	150	-	°C

[1] The circuit is DC adjusted at $V_P = \pm 12.5$ V to ±30 V.

[2] Refers to usage in a symmetrical supply application (see Section 12.7). In an asymmetrical supply application the SGND voltage should be defined by an external circuit.

[3] The transition between Standby and Mute mode contains hysteresis, while the slope of the transition between Mute and Operating mode is determined by the time constant on pin MODE (see Figure 9).

[4] Pin DIAG should not be connected to an external pull-up.

[5] DC output offset voltage is applied to the output during the transition between Mute and Operating mode in a gradual way. The $dV_{O(offset)}/dt$ caused by any DC output offset is determined by the time constant on pin MODE.

[6] At a junction temperature of approximately $T_{act(th\_fold)} - 5$ °C the gain reduction will commence and at a junction temperature of approximately $T_{act(th\_fold)} + 5$ °C the amplifier mutes.

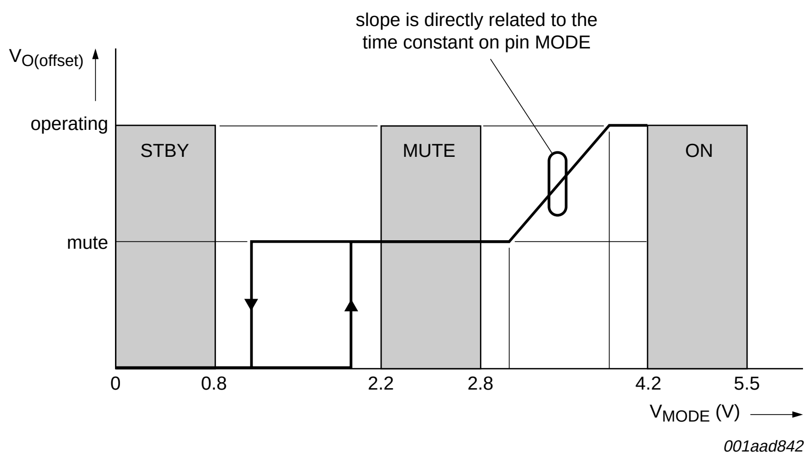


Fig 9. Behavior of pin MODE

10. Dynamic characteristics

10.1 Dynamic characteristics (SE)

Table 8. Dynamic characteristics (SE)

$V_P = \pm 27$ V; $R_L = 4\ \Omega$; $f_i = 1$ kHz; $f_{osc} = 310$ kHz; $R_{s(L)} < 0.1\ \Omega$ [1]; $T_{amb} = -40\ °C$ to $+85\ °C$; $T_j = -40\ °C$ to $+150\ °C$; unless otherwise specified. See Section 12.7 for the SE application schematics. The 2nd-order demodulation filter coil is referred to as L and the capacitor as C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 10 μH; C = 1 μF; T_j = 85 °C; R_L = 2 Ω; V_P = ±18 V; THD = 0.5 %	[2]	-	48	-	W
		L = 10 μH; C = 1 μF; T_j = 85 °C; R_L = 2 Ω; V_P = ±18 V; THD = 10 %	[2]	-	60	-	W
		L = 22 μH; C = 680 nF; T_j = 85 °C; R_L = 4 Ω; V_P = ±27 V; THD = 0.5 %	[2]	-	65	-	W
		L = 22 μH; C = 680 nF; T_j = 85 °C; R_L = 4 Ω; V_P = ±27 V; THD = 10 %	[2]	-	80	-	W
I_{OM}	peak output current	current limiting, see Section 6.4.3		8	-	-	A
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.02	0.2	%
		P_o = 1 W; f_i = 10 kHz	[3]	-	0.10	-	%
$G_{v(cl)}$	closed-loop voltage gain			25	26	27	dB
SVRR	supply voltage rejection ratio	operating; f_{ripple} = 100 Hz	[4]	-	55	-	dB
		operating; f_{ripple} = 1 kHz	[4]	40	50	-	dB
		mute; f_{ripple} = 1 kHz	[4]	-	55	-	dB
		standby; f_{ripple} = 100 Hz	[4]	-	80	-	dB
$\lvert Z_{i(dif)} \rvert$	differential input impedance	between the input pins INP and INM		45	68	-	kΩ
$V_{n(o)}$	noise output voltage	operating; V_P = ±27 V; R_S = 0 Ω	[5]	-	170	-	μV
		operating; V_P = ±18 V; R_S = 0 Ω	[5]	-	145	-	μV
		mute; V_P = ±27 V	[6]	-	125	-	μV
		mute; V_P = ±18 V	[6]	-	85	-	μV
α_{cs}	channel separation	P_o = 1 W; R_S = 0 Ω; f_i = 1 kHz		-	70	-	dB
$\lvert \Delta G_v \rvert$	voltage gain difference			-	-	1	dB
α_{mute}	mute attenuation	f_i = 1 kHz; V_{in} = 1 V (RMS value)		-	73	-	dB
CMRR	common mode rejection ratio	$f_{i(CM)}$ = 1 kHz; $V_{i(CM)}$ = 1 V (RMS value)	[7]	-	75	-	dB

[1] $R_{s(L)}$ is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement (see Section 12.3).

[3] THD is measured in a bandwidth of 22 Hz to 20 kHz, AES brick wall. Maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)}$ = 2 V (peak-to-peak value); source resistance R_S = 0 Ω.

[5] Frequency bandwidth B = 22 Hz to 20 kHz, AES brick wall (see Section 12.4).

[6] B = 22 Hz to 20 kHz, AES brick wall, independent of R_S (see Section 12.4).

[7] $V_{i(CM)}$ is the input common mode voltage.

10.2 Dynamic characteristics (BTL)

Table 9. Dynamic characteristics (BTL)

$V_P = \pm 27$ V; $R_L = 8\ \Omega$; $f_i = 1$ kHz; $f_{osc} = 310$ kHz; $R_{s(L)} < 0.1\ \Omega$ [1]; $T_{amb} = -40$ °C to +85 °C; $T_j = -40$ °C to +150 °C; unless otherwise specified. See Section 12.7 for the BTL application schematics. The 2nd order demodulation filter coil is referred to as L and the capacitor as C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 10 µH, C = 1 µF; T_j = 85 °C; $R_L = 4\ \Omega$; $V_P = \pm 18$ V; THD = 0.5 %	[2]	-	97	-	W
		L = 10 µH; C = 1 µF; T_j = 85 °C; $R_L = 4\ \Omega$; $V_P = \pm 18$ V; THD = 10 %	[2]	-	120	-	W
		L = 22 µH; C = 680 nF; T_j = 85 °C; $R_L = 8\ \Omega$; $V_P = \pm 27$ V; THD = 0.5 %	[2]	-	130	-	W
		L = 22 µH; C = 680 nF; T_j = 85 °C; $R_L = 8\ \Omega$; $V_P = \pm 27$ V; THD = 10 %	[2]	-	160	-	W
I_{OM}	peak output current	current limiting, see Section 6.4.3		8	-	-	A
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.02	0.2	%
		P_o = 1 W; f_i = 10 kHz	[3]	-	0.15	-	%
$G_{v(cl)}$	closed-loop voltage gain			31	32	33	dB
SVRR	supply voltage rejection ratio	operating; f_{ripple} = 100 Hz	[4]	-	68	-	dB
		operating; f_{ripple} = 1 kHz	[4]	50	68	-	dB
		mute; f_{ripple} = 1 kHz	[4]	-	68	-	dB
		standby; f_{ripple} = 100 Hz	[4]	-	80	-	dB
$\|Z_{i(dif)}\|$	differential input impedance	measured between the input pins INP and INM		22	34	-	kΩ
$V_{n(o)}$	noise output voltage	operating; $V_P = \pm 27$ V; $R_S = 0\ \Omega$	[5]	-	240	-	µV
		operating; $V_P = \pm 18$ V; $R_S = 0\ \Omega$	[5]	-	200	-	µV
		mute; $V_P = \pm 27$ V	[6]	-	180	-	µV
		mute; $V_P = \pm 18$ V	[6]	-	125	-	µV
α_{mute}	mute attenuation	f_i = 1 kHz; V_{in} = 1 V (RMS value)		-	70	-	dB
CMRR	common mode rejection ratio	$f_{i(CM)}$ = 1 kHz; $V_{i(CM)}$ = 1 V (RMS value)		-	75	-	dB

[1] $R_{s(L)}$ is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement (see Section 12.3).

[3] THD is measured in a bandwidth of 22 Hz to 20 kHz, AES brick wall. Maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)}$ = 2 V (peak-to-peak value); $R_S = 0\ \Omega$.

[5] B = 22 Hz to 20 kHz, AES brick wall (see Section 12.4).

[6] B = 22 Hz to 20 kHz, AES brick wall, independent on R_S (see Section 12.4).

11. Switching characteristics

Table 10. Switching characteristics

V_{DD} = 27 V; T_{amb} = –40 °C to +85 °C; T_j = –40 °C to +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	typical; $R_{ext(OSC)}$ = 30.0 kΩ	290	310	344	kHz
		maximum; $R_{ext(OSC)}$ = 15.4 kΩ	-	560	-	kHz
		minimum; $R_{ext(OSC)}$ = 48.9 kΩ	-	200	-	kHz
External oscillator or frequency tracking						
$V_{H(OSC)min}$	minimum HIGH-level voltage on pin OSC	referred to SGND	4	-	6	V
$V_{L(OSC)max}$	maximum LOW-level voltage on pin OSC	referred to SGND	0	-	1	V
Δf_{track}	tracking frequency range		210	-	600	kHz
Drain source on-state resistance of the output transistors						
$R_{DSon(ls)}$	low-side drain-source on-state resistance	T_j = 85 °C; I_{DS} = 6 A	-	250	275	mΩ
		T_j = 25 °C; I_{DS} = 6 A	-	190	210	mΩ
$R_{DSon(hs)}$	high-side drain-source on-state resistance	T_j = 85 °C; I_{DS} = 6 A	-	300	330	mΩ
		T_j = 25 °C; I_{DS} = 6 A	-	220	240	mΩ

12. Application information

12.1 BTL application

When using the power amplifier in a mono BTL application the inputs of both channels must be connected in parallel and the phase of one of the inputs must be inverted (see Figure 7). The loudspeaker is connected between the outputs of the two single-ended demodulation filters.

12.2 Output power estimation

The achievable output powers in SE and BTL applications can be estimated using the following expressions:

$$\text{SE: } P_{o(0.5\%)} = \frac{\left(\dfrac{R_L}{R_L + R_{DSon(hs)} + R_{s(L)}} \times V_P \times (1 - t_{w(min)} \times f_{osc})\right)^2}{2 \times R_L} \text{ W}$$

$$\text{BTL: } P_{o(0.5\%)} = \frac{\left(\dfrac{R_L}{R_L + (R_{DSon(hs)} + R_{DSon(ls)}) + 2R_{s(L)}} \times 2V_P \times (1 - t_{w(min)} \times f_{osc})\right)^2}{2 \times R_L} \text{ W}$$

Peak output current, internally limited to 8 A:

SE: $$I_{OM} = \frac{V_P \times (1 - t_{w(min)} \times f_{osc})}{R_L + R_{DSon(hs)} + R_{s(L)}} \text{ A}$$

BTL: $$I_{OM} = \frac{2V_P - (1 - t_{w(min)} \times f_{osc})}{R_L + (R_{DSon(hs)} + R_{DSon(ls)}) + 2R_{s(L)}} \text{ A}$$

Variables:

R_L = load resistance

$R_{s(L)}$ = series resistance of the filter coil

$R_{DSon(hs)}$ = high side drain source on-state resistance (temperature dependent)

$R_{DSon(ls)}$ = low side drain source on-state resistance (temperature dependent)

f_{osc} = oscillator frequency

$t_{w(min)}$ = minimum pulse width (typical 150 ns, temperature dependent)

V_P = supply voltage [or 0.5 (V_{DD} + V_{SS})]

$P_{o(0.5\%)}$ = output power at the onset of clipping

I_{OM} should be below 8 A (see Section 7). I_{OM} is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

12.3 External clock

If two or more class-D amplifiers are used it is recommended that all devices run at the same switching frequency. This can be realized by connecting all OSC pins together and feed them from an external oscillator.

The internal oscillator requires an external $R_{ext(OSC)}$ and $C_{ext(OSC)}$ between pins OSC and V_{SSA}. For application of an external oscillator it is necessary to force OSC to a DC level above SGND. The internal oscillator is disabled and the PWM modulator will switch with the external frequency. The duty cycle of the external clock should be between 47.5 % and 52.5 %.

The noise contribution of the internal oscillator is supply voltage dependent. In low noise applications running at high supply voltage an external low noise oscillator is recommended.

12.4 Noise

Noise should be measured using a high-order low-pass filter with a cut-off frequency of 20 kHz. The standard audio band pass filters used in audio analyzers do not suppress the residue of the carrier frequency sufficiently to ensure a reliable measurement of the audible noise. Noise measurements should preferably be carried out using AES 17 (Brick Wall) filters or the Audio Precision AUX 0025 filter, which was designed especially for measuring switching (class-D) amplifiers.

12.5 Heat sink requirements

In some applications it may be necessary to connect an external heat sink to the TDF8590TH. The thermal foldback activates on T_j = 140 °C. The expression below shows the relationship between the maximum power dissipation before activation of the thermal foldback and the total thermal resistance from junction to ambient:

$$R_{th(j-a)} = \frac{T_j - T_{amb}}{P}\ \Omega$$

The power dissipation is determined by the efficiency η of the TDF8590TH. The efficiency measured as a function of output power is given in Figure 23. The power dissipation can be derived as function of output power (see Figure 24).

Example of a heatsink calculation for the 8 Ω BTL application with ±27 V supply:

- An audio signal with a crest factor of 10 (the ratio between peak power and average power is 10 dB), this means that the average output power is 1/10th of the peak power
- The peak RMS output power level is 130 W (0.5 % THD level)
- The average power is 0.1 × 130 W = 13 W
- The dissipated power at an output power of 13 W is approximately 5 W
- The total $R_{th(j-a)}$ = (140 – 85) / 5 = 11 K/W, if the maximum expected T_{amb} = 85 °C
- The total thermal resistance $R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$
- $R_{th(j-c)}$ = 1.1 K/W, $R_{th(c-h)}$ = 0.5 K/W to 1 K/W (dependent on mounting), so $R_{th(h-a)}$ would then be: 11 – (1.1 + 1) = 8.9 K/W

12.6 Pumping effects

When the TDF8590TH is used in a SE configuration, a so-called pumping effect can occur. During one switching interval, energy is taken from one supply (e.g. V_{DDA1}), while a part of that energy is delivered back to the other supply line (e.g. V_{SSA1}) and visa versa. When the voltage supply source cannot sink energy, the voltage across the output capacitors of that voltage supply source will increase: the supply voltage is pumped to higher levels. The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels

The pumping effect should not cause a malfunction of either the audio amplifier and/or the voltage supply source. For instance, this malfunction can be caused by triggering of the UVP, OVP or UBP of the amplifier. Best remedy for pumping effects is to use the TDF8590TH in a mono full-bridge application. In case of dual half-bridge application adapt the power supply (e.g. increase supply decoupling capacitors).

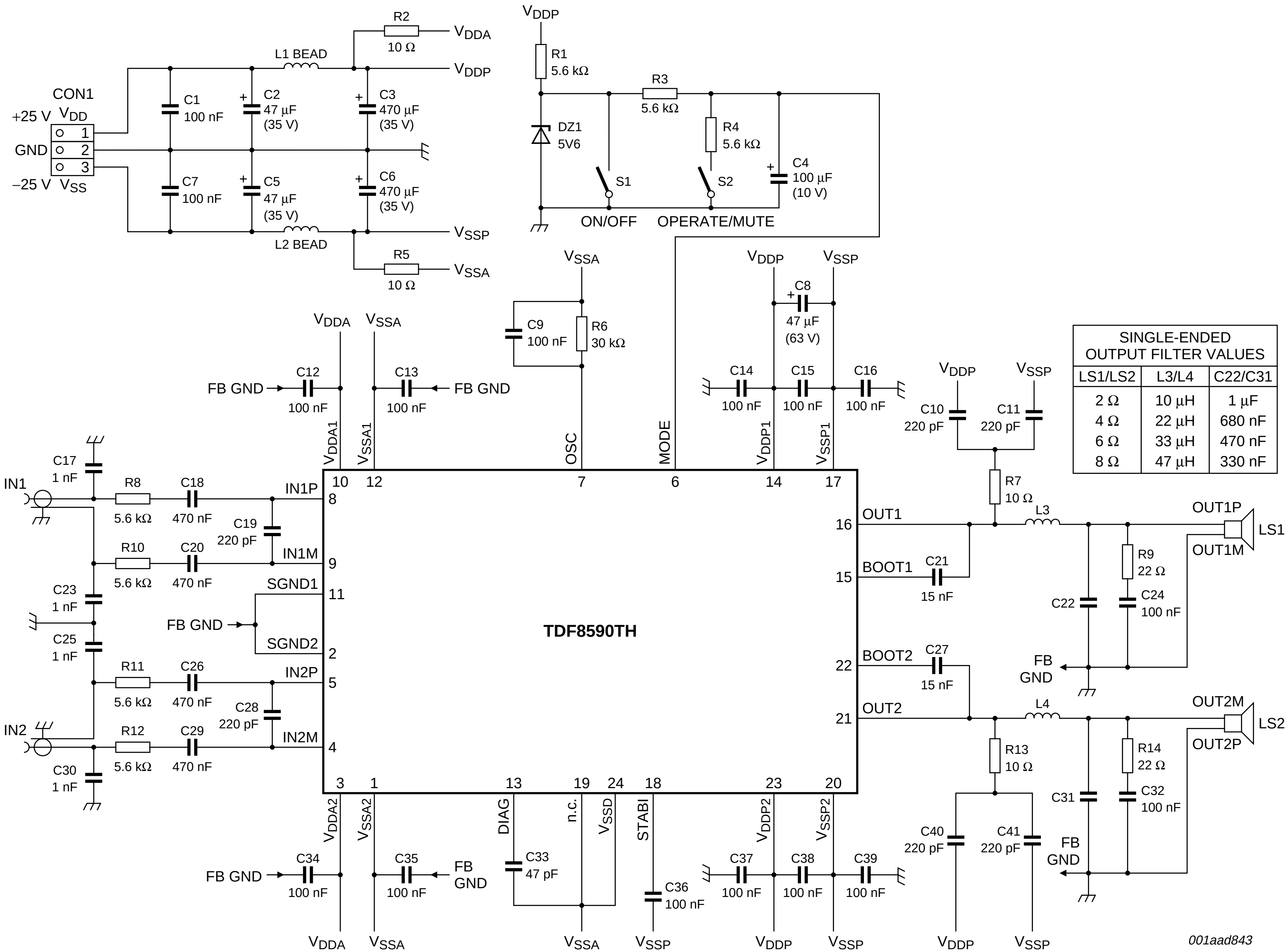
12.7 Application schematics

For SE application (see Figure 10):

- A solid ground plane around the TDF8590TH is necessary to prevent emission
- 100 nF SMD capacitors must be placed as close as possible to the power supply pins of the TDF8590TH
- The heatsink of the HSOP24 package of the TDF8590TH is connected to pin V_{SSD}
- The external heatsink must be connected to the ground plane
- Use a thermal conductive, electrically isolating Sil-Pad between the backside of the TDF8590TH and the external heatsink

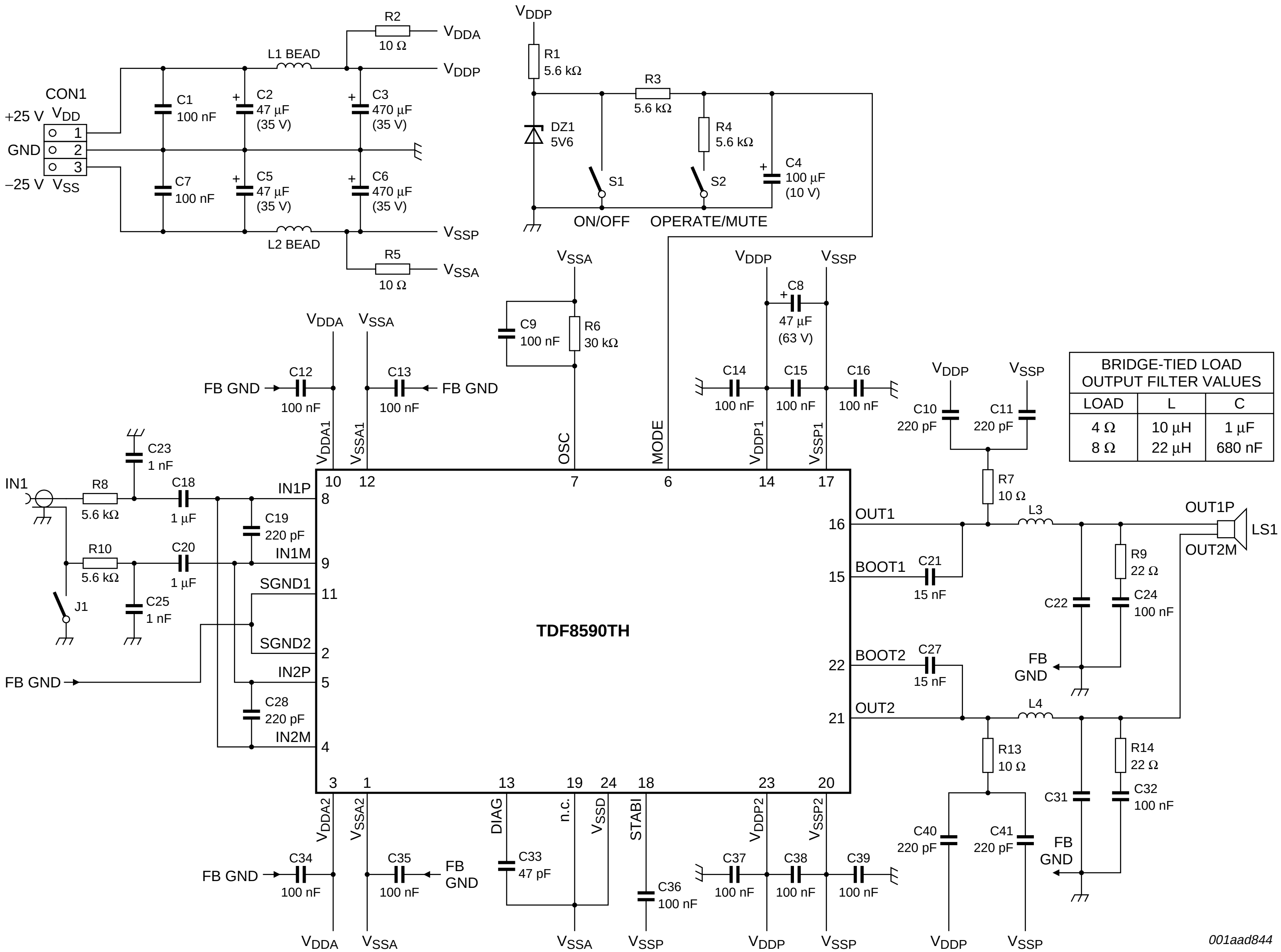
For BTL application (see Figure 11):

- A solid ground plane around the TDF8590TH is necessary to prevent emission
- 100 nF SMD capacitors must be placed as close as possible to the power supply pins of the TDF8590TH
- The heatsink of the HSOP24 package of the TDF8590TH is connected to pin V_{SSD}
- The external heatsink must be connected to the ground plane
- Use a thermal conductive, electrically isolating Sil-Pad between the backside of the TDF8590TH and the external heatsink
- The differential inputs enable the best system level audio performance with unbalanced signal sources. In case of hum due to floating inputs connect the shielding or source ground to the amplifier ground. The jumper J1 is open on set level and is closed on the stand-alone demo board
- Minimum total required capacity per power supply line is 3300 μF



SINGLE-ENDED OUTPUT FILTER VALUES		
LS1/LS2	L3/L4	C22/C31
2 Ω	10 µH	1 µF
4 Ω	22 µH	680 nF
6 Ω	33 µH	470 nF
8 Ω	47 µH	330 nF

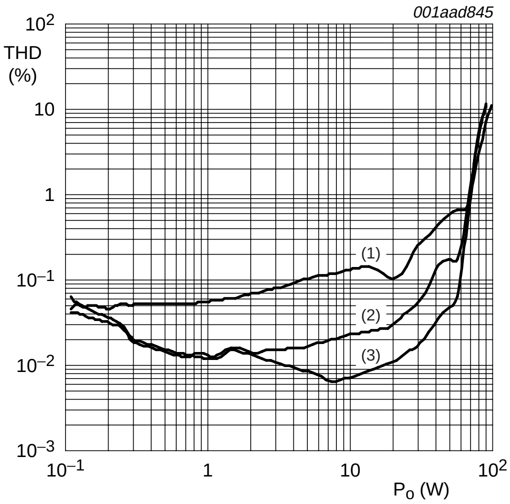
Fig 10. SE application schematic



BRIDGE-TIED LOAD OUTPUT FILTER VALUES		
LOAD	L	C
4 Ω	10 µH	1 µF
8 Ω	22 µH	680 nF

Fig 11. BTL application schematic

12.8 Curves measured in reference design

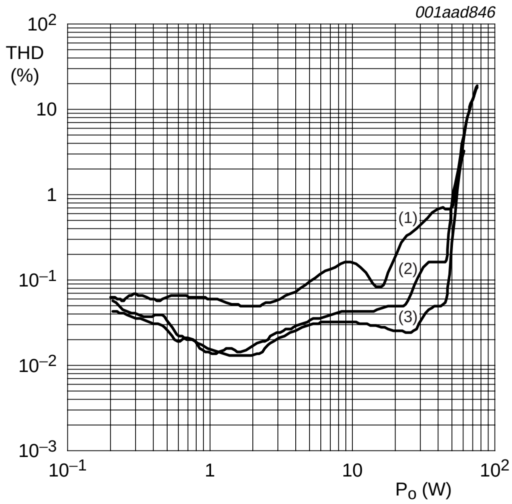


(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

a. $V_P = \pm27$ V; $R_L = 4\ \Omega$.



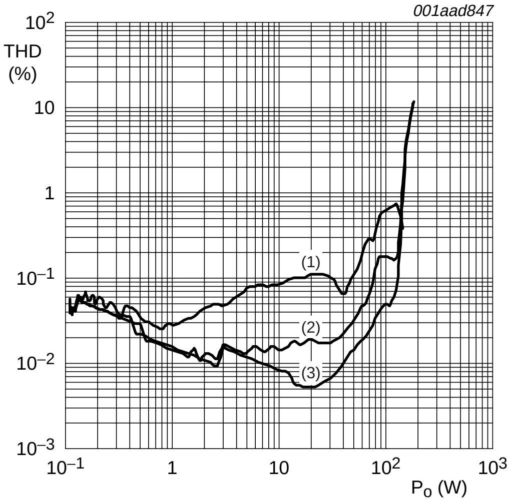
(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

b. $V_P = \pm18$ V; $R_L = 2\ \Omega$.

Fig 12. Total harmonic distortion as a function of output power, SE application

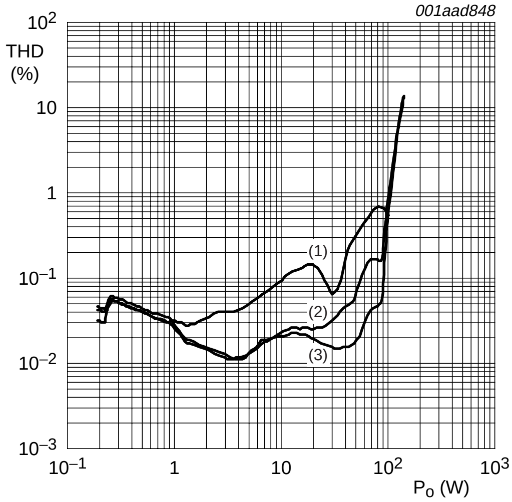


(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

a. $V_P = \pm27$ V; $R_L = 8\ \Omega$



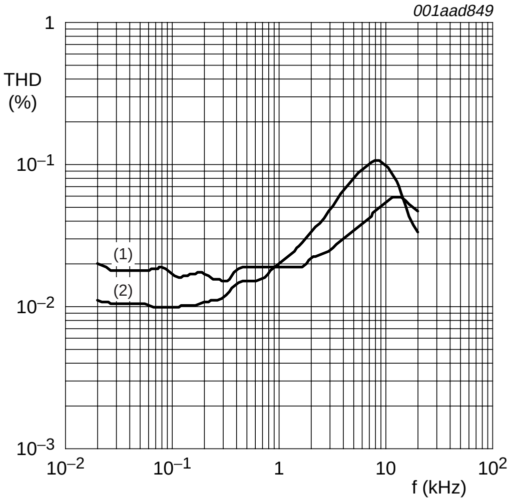
(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

b. $V_P = \pm18$ V; $R_L = 4\ \Omega$

Fig 13. Total harmonic distortion as a function of output power, BTL application

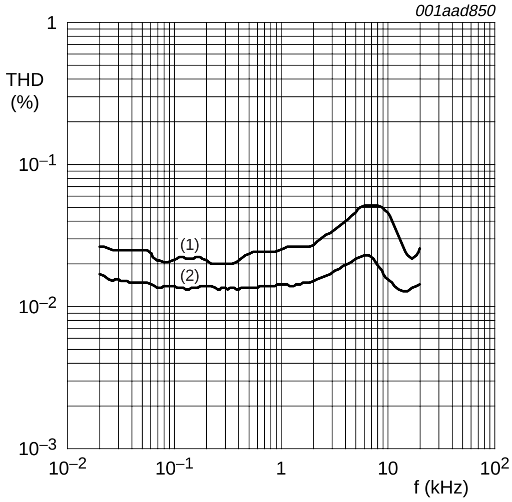


P_o = 1 W.

(1) V_P = ±27 V; R_L = 4 Ω.

(2) V_P = ±18 V; R_L = 2 Ω.

a. SE application



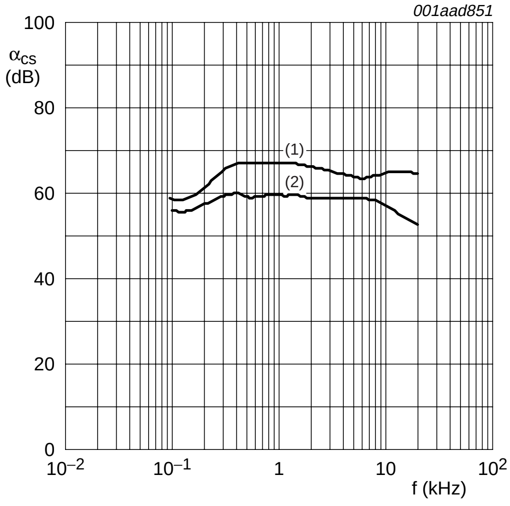
P_o = 1 W.

(1) V_P = ±18 V; R_L = 4 Ω.

(2) V_P = ±27 V; R_L = 8 Ω.

b. BTL application

Fig 14. Total harmonic distortion as a function of frequency

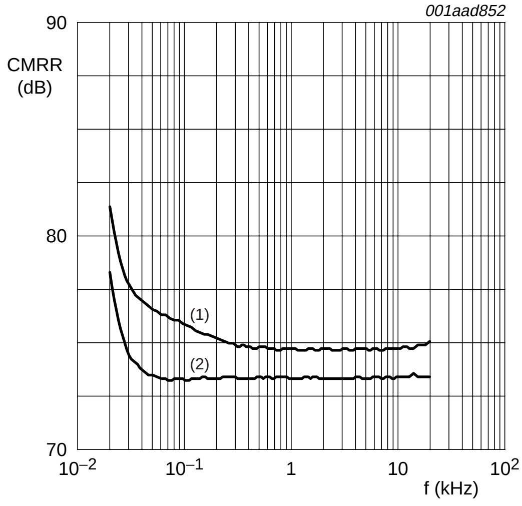


P_o = 1 W; R_S = 0 Ω.

(1) V_P = ±27 V; R_L = 4 Ω.

(2) V_P = ±18 V; R_L = 2 Ω.

Fig 15. Channel separation as a function of frequency

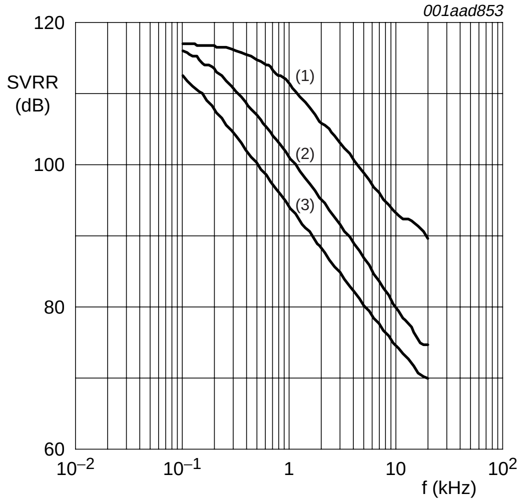


$V_{i(CM)}$ = 1 V (RMS); R_L = 4 Ω; plus and minus input DC shorted.

(1) SE application.

(2) BTL application.

Fig 16. Common mode rejection ratio as a function of frequency



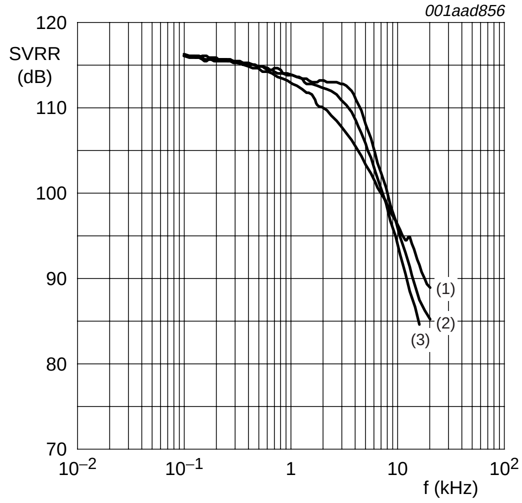
$V_P = \pm 27$ V; $R_L = 4\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

(1) ripple on both supply lines, ripple in phase.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on one supply line.

a. SE application



$V_P = \pm 27$ V; $R_L = 8\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

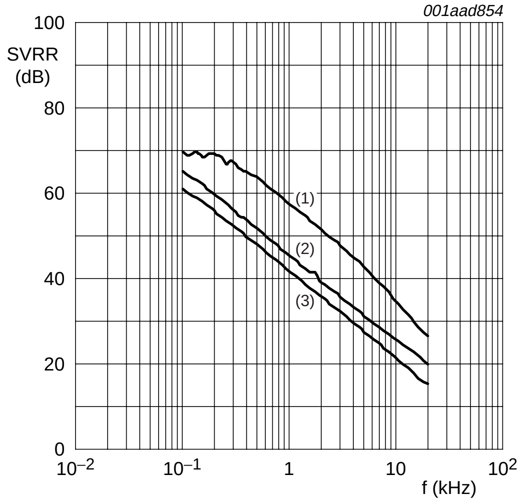
(1) ripple on one supply line.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on both supply lines, ripple in phase.

b. BTL application

Fig 17. Supply voltage ripple rejection as a function of frequency; Standby mode



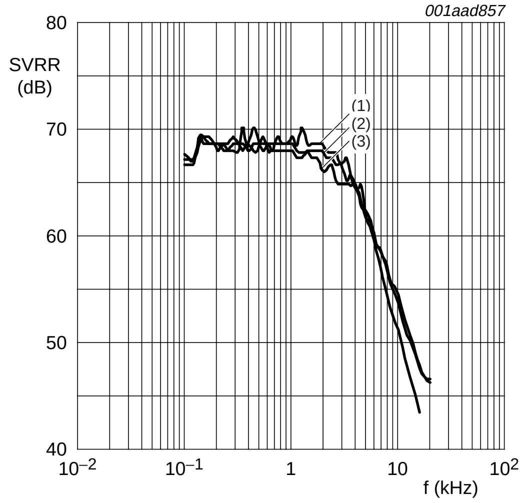
$V_P = \pm 27$ V; $R_L = 4\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

(1) ripple on both supply lines, ripple in phase.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on one supply line.

a. SE application



$V_P = \pm 27$ V; $R_L = 8\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

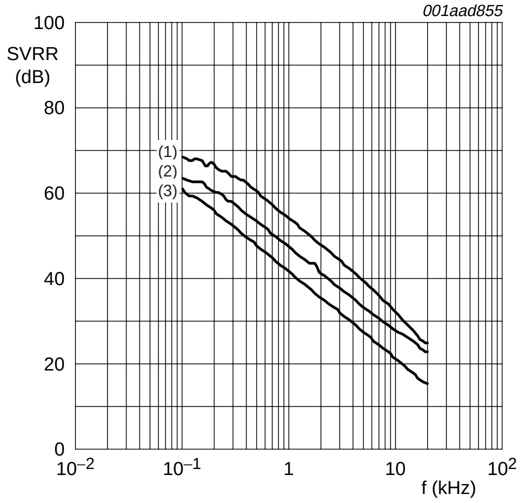
(1) ripple on both supply lines, ripple in phase.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on one supply line.

b. BTL application

Fig 18. Supply voltage ripple rejection as a function of frequency; Mute mode



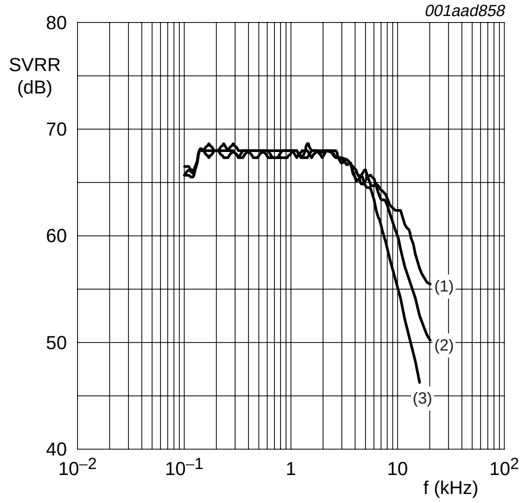
$V_P = \pm 27$ V; $R_L = 4\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

(1) ripple on both supply lines, ripple in phase.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on one supply line.

a. SE application



$V_P = \pm 27$ V; $R_L = 8\ \Omega$; $R_S = 0\ \Omega$; $V_{ripple} = 2$ V (p-p).

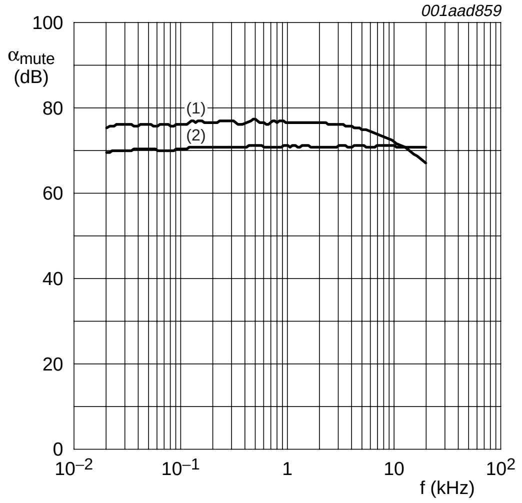
(1) ripple on one supply line.

(2) ripple on both supply lines, ripple in antiphase.

(3) ripple on both supply lines, ripple in phase.

b. BTL application

Fig 19. Supply voltage ripple rejection as a function of frequency; Operating mode

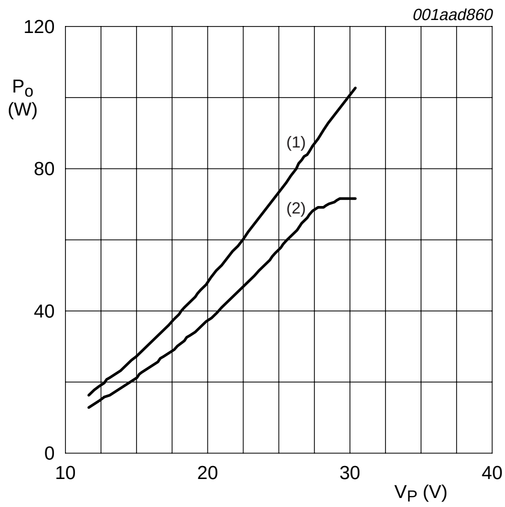


$V_I = 1$ V (RMS).

(1) SE application; $V_P = \pm 27$ V; $R_L = 4\ \Omega$.

(2) BTL application; $V_P = \pm 18$ V; $R_L = 4\ \Omega$.

Fig 20. Mute attenuation as a function of frequency

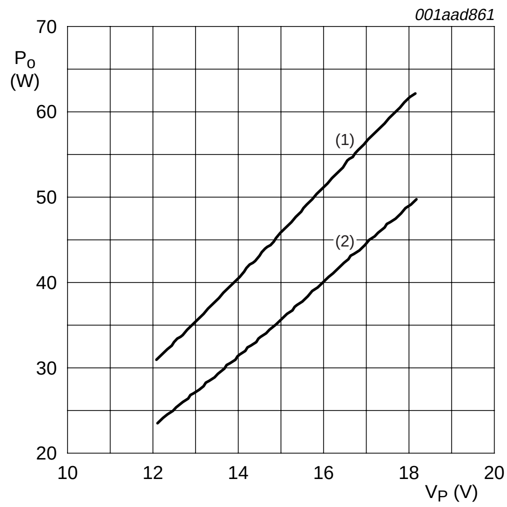


f = 1 kHz.

(1) THD = 10 %.

(2) THD = 0.5 %.

a. $R_L = 4\ \Omega$



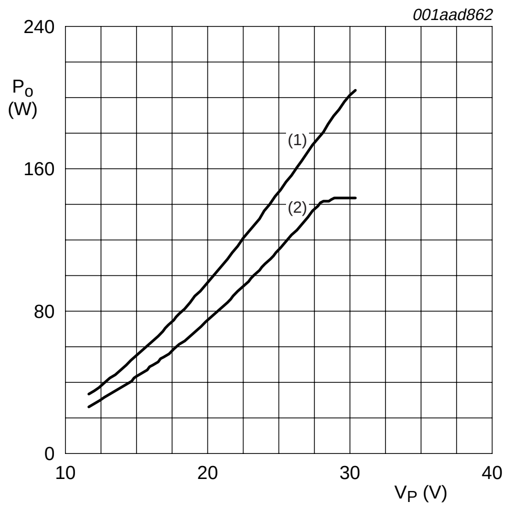
f = 1 kHz.

(1) THD = 10 %.

(2) THD = 0.5 %.

b. $R_L = 2\ \Omega$

Fig 21. Output power as a function of supply voltage, SE application

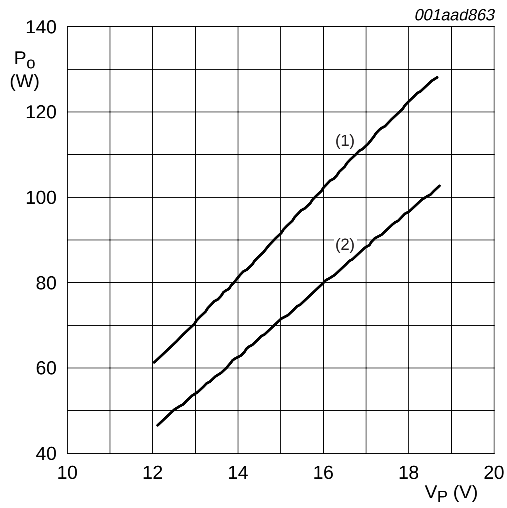


f = 1 kHz.

(1) THD = 10 %.

(2) THD = 0.5 %.

a. $R_L = 8\ \Omega$



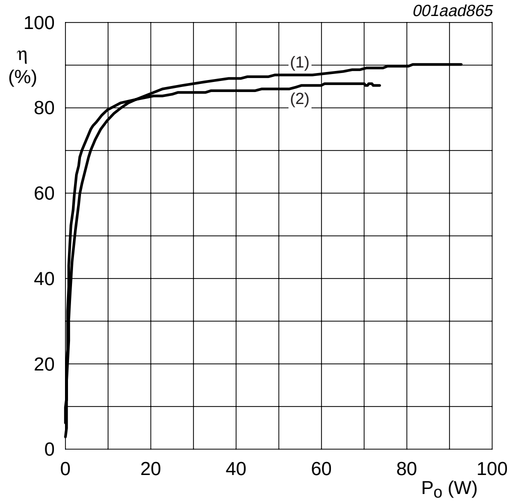
f = 1 kHz.

(1) THD = 10 %.

(2) THD = 0.5 %.

b. $R_L = 4\ \Omega$

Fig 22. Output power as a function of supply voltage, BTL application

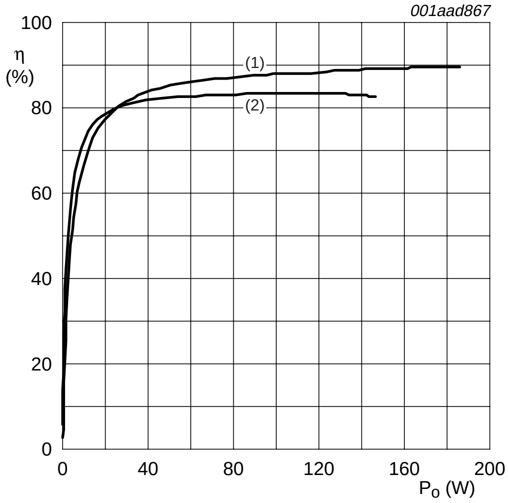


f = 1 kHz.

(1) $V_P = \pm 27$ V; $R_L = 4\ \Omega$.

(2) $V_P = \pm 18$ V; $R_L = 2\ \Omega$.

a. SE application



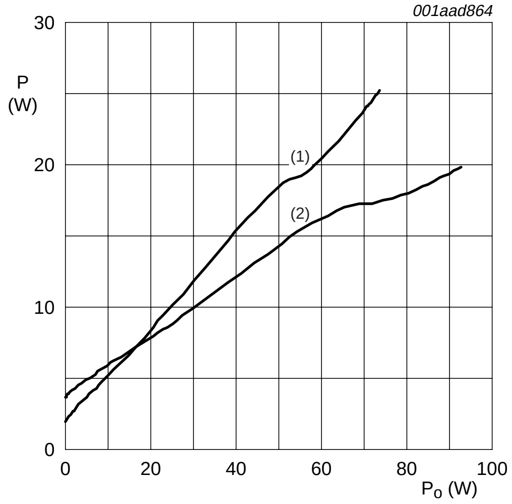
f = 1 kHz.

(1) $V_P = \pm 27$ V; $R_L = 8\ \Omega$.

(2) $V_P = \pm 18$ V; $R_L = 4\ \Omega$.

b. BTL application

Fig 23. Efficiency as a function of output power

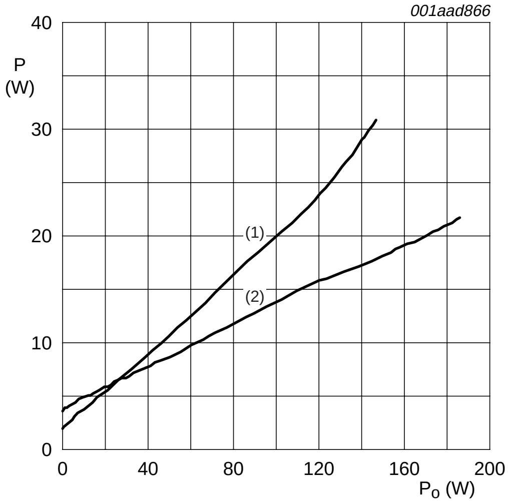


f = 1 kHz.

(1) $V_P = \pm 18$ V; $R_L = 2\ \Omega$.

(2) $V_P = \pm 27$ V; $R_L = 4\ \Omega$.

a. SE application



f = 1 kHz.

(1) $V_P = \pm 18$ V; $R_L = 4\ \Omega$.

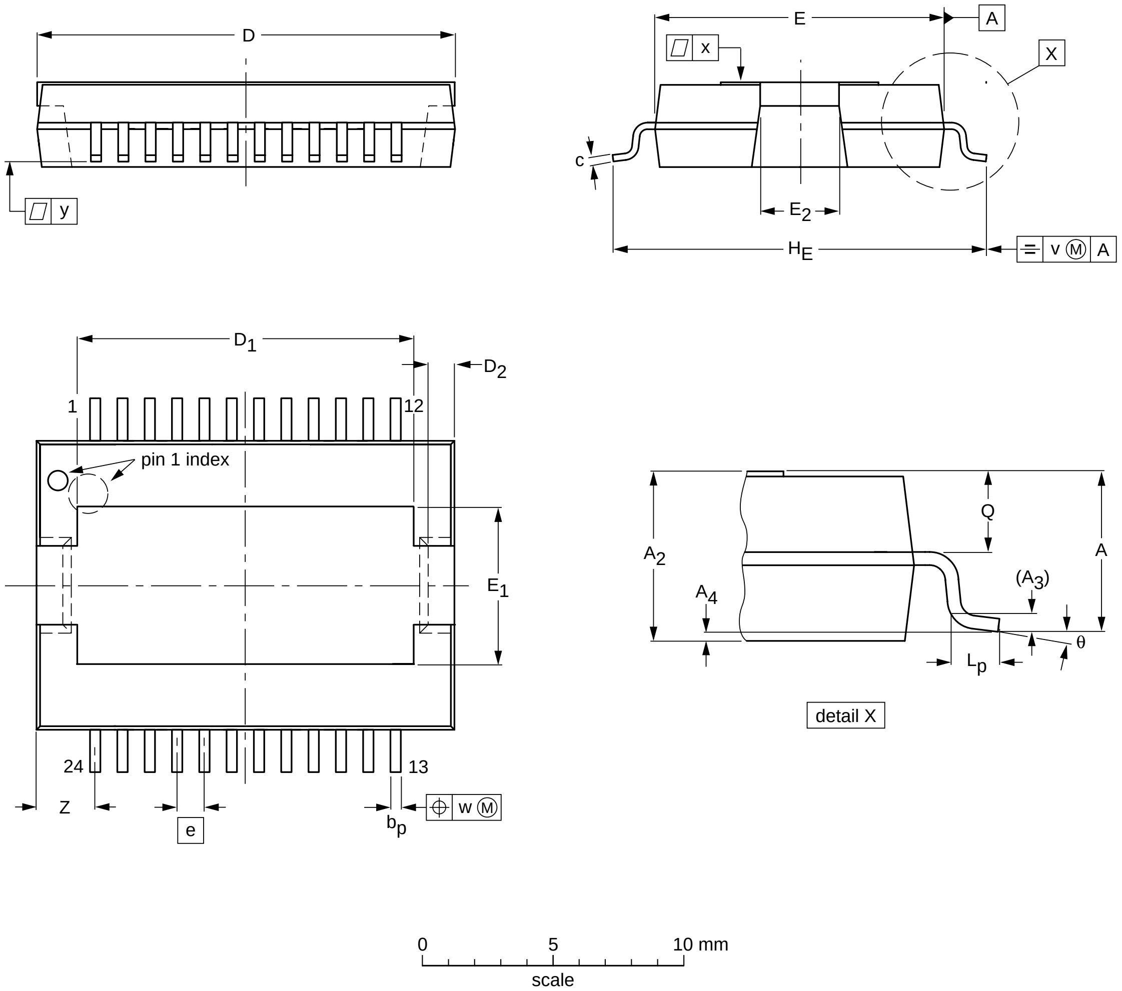
(2) $V_P = \pm 27$ V; $R_L = 8\ \Omega$.

b. BTL application

Fig 24. Power dissipation as a function of output power

13. Package outline

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 25. Package outline SOT566-3 (HSOP24)

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDF8590TH_2	20070423	Product data sheet	-	TDF8590TH_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • All I^2C-related items were removed. • Figure 7 was modified. • In Section 2 “Features” 80 W BTL was changed into 120 W.			
TDF8590TH_1	20060613	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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