Request Security User Guide ›

EVALUATION KIT AVAILABLE

Click here for production status of specific part numbers.

DS2477

DeepCover Secure SHA-3 Coprocessor with ChipDNA PUF Protection

General Description

The DS2477 secure I²C coprocessor with built-in 1-Wire® master combines FIPS202-compliant secure hash algorithm (SHA-3) challenge and response authentication with Maxim's patented ChipDNA™ feature, a physically unclonable technology (PUF) to provide a cost-effective solution with the ultimate protection against security attacks. The ChipDNA implementation utilizes the random variation of semiconductor device characteristics that naturally occur during wafer fabrication. The ChipDNA circuit generates a unique output value that is repeatable over time, temperature, and operating voltage. Attempts to probe or observe ChipDNA operation modifies the underlying circuit characteristics thus preventing discovery of the unique value used by the chip cryptographic functions. The DS2477 utilizes the ChipDNA output as key content to cryptographically secure all device-stored data. With ChipDNA capability, the device provides a core set of cryptographic tools derived from integrated blocks including a SHA-3 engine, a FIPS/NIST compliant true random number generator (TRNG), 2Kb of secured EEPROM, and a unique 64-bit ROM identification number (ROM ID). The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. The DS2477 provides the SHA-3 and memory functionality required by a host system to communicate with and operate a 1-Wire SHA-3 slave. In addition, it performs protocol conversion between the I²C master and any attached 1-Wire SHA-3 slaves. For 1-Wire line driving, internal user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. The 1-Wire line can be powered down under software control. Strong pullup features support 1-Wire power delivery for commands that require higher current consumption.

Applications

- Authentication of Medical Sensors and Tools
- Secure Management of Limited Use Consumables
- IoT Node Authentication
- Peripheral Authentication
- Reference Design License Management
- Printer Cartridge Identification and Authentication

Benefits and Features

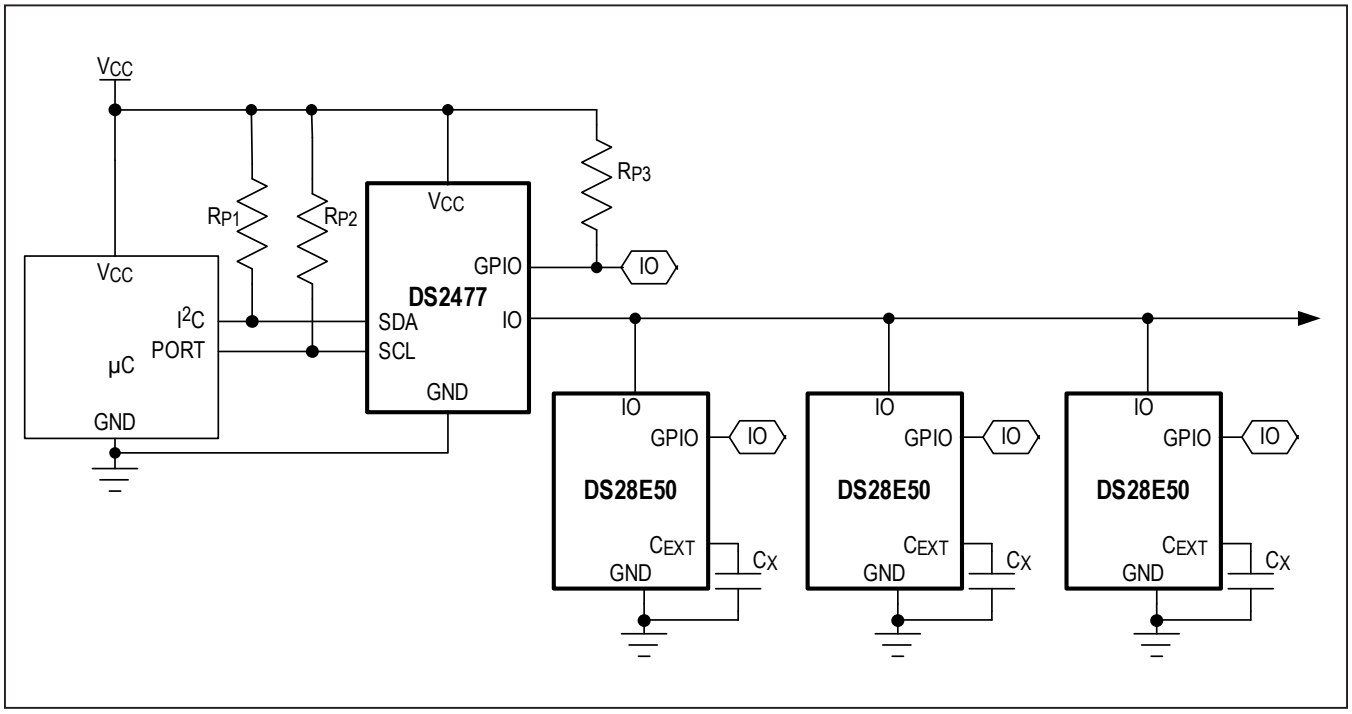
- Robust Countermeasures Protect Against Security Attacks
  - Patented Physically Unclonable Function Secures Device Data
  - Actively Monitored Die Shield Detects and Reacts to Intrusion Attempts
  - All Stored Data Cryptographically Protected from Discovery
- Efficient Secure Hash Algorithm Authenticates and Manages Peripherals
  - FIPS 202-Compliant SHA-3 Algorithm for Bidirectional Authentication
  - FIPS 198-Compliant Keyed-Hash Message Authentication Code (HMAC)
  - TRNG with NIST SP 800-90B Compliant Entropy Source
- Supplemental Features Enable Easy Integration into End Applications
  - 2Kb of EEPROM for User Data, Key, and Control Registers
  - One Open-Drain GPIO Pin
  - Unique and Unalterable Factory Programmed 64-Bit Identification Number (ROM ID)
  - Large 1-Wire Block Buffer (126 bytes) for Efficient Data Transfer
  - 1-Wire Standard and Overdrive Timing Communication Speeds
  - I²C Communication, Up to 1MHz
  - Operating Range: 3.3V ±10%, -40°C to +85°C
  - 6-Pin TDFN-EP Package (3mm x 3mm)

***Ordering Information* appears at end of data sheet.**

19-100402; Rev 1; 3/19

maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND .....-0.5V to 4.0V
Maximum Current into Any Pin..... -20mA to 20mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +125°C
Lead temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 TDFN-EP

Package Code	T633+2
Outline Number	**21-0137**
Land Pattern Number	**90-0058**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	55ºC/W
Junction to Case (θ_{JC})	9ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42ºC/W
Junction to Case (θ_{JC})	9ºC/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	2.97	3.3	3.63	V
Supply Current	I_{CC}	Standby			400	µA
		Communicating/active (Note 2)			10	mA
1-Wire Input High	V_{IH1}	Low configuration	0.6 x V_{CC}			V
		Medium configuration	0.6 x V_{CC}			
		High configuration	0.85 x V_{CC}			

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-to-High Switching Threshold	V_{TH}	Low configuration (Notes 3, 4)		0.25 x V_{CC}		V
		Medium configuration (Notes 3, 4)		0.4V x V_{CC}		
		High configuration (Notes 3, 4)		0.75 x V_{CC}		
1-Wire Input Low	V_{IL1}	Low configuration			0.15 x V_{CC}	V
		Medium configuration			0.3 x V_{CC}	
		High configuration			0.3 x V_{CC}	
High-to-Low Switching Threshold	V_{TL}	(Notes 3, 5)		0.65 x V_{CC}		V
Switching Hysteresis	V_{HY}	(Notes 3, 6)		0.3		V
1-Wire Weak Pullup Resistor (Notes 3, 7)	R_{WPU}	Ultra-low range	250	333	675	Ω
		Low range	375	500	750	
		High range	750	1000	1400	
		External high impedance		10Meg		
1-Wire Output Low	V_{OL1}	V_{CC} = 2.97V, 4mA sink current			0.28	V
Active Pullup on Threshold	V_{IAPO}	Low configuration (Note 3)		0.25 x V_{CC}		V
		Medium configuration (Note 3)		0.4 x V_{CC}		
		High configuration (Note 3)		0.75 x V_{CC}		
Active Pullup on Time (Notes 3, 8)	t_{APU}	1-Wire standard speed (default value)		2.5		µs
		1-Wire overdrive speed (default value)		0.5		
Active Pullup Impedance	R_{APU}	V_{CC} = 2.97V, 10mA load (Note 3)			50	Ω
Operation Time	t_{OP}	(Note 3)			5	ms
IO PIN: 1-Wire TIMING (Note 9)						
1-Wire Output Fall Time (Note 3)	t_F	Standard and overdrive		Settable		µs
Reset Low Time	t_{RSTL}	Standard and overdrive	-5%	Settable	+5%	µs
Reset High Time	t_{RSTH}	Standard and overdrive (Note 10)	-5%	Settable	+5%	µs
Presence-Detect Sample Time	t_{MSP}	Standard and overdrive	-5%	Settable	+5%	µs
Sampling for Short and Interrupt	t_{MSI}	Standard and overdrive	-5%	Settable	+5%	µs
Write-1/Read Low Time	t_{W1L}	Standard and overdrive	-5%	Settable	+5%	µs
Read Sample Time	t_{MSR}	Standard and overdrive	-5%	Settable	+5%	µs

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write-0 Low Time	t_{W0L}	Standard and overdrive	-5%	Settable	+5%	µs
Recovery Time	t_{REC}	Standard and overdrive (Note 10)	-5%	Settable	+5%	µs
1-Wire Time Slot	t_{SLOT}	Standard and overdrive		Equal to t_{W0L} + t_{REC}		µs
CRYPTO FUNCTIONS						
Computation Current	I_{CMP}	(Notes 3, 11)			10	mA
Computation Time	t_{CMP}	(Note 3)			5	ms
TRNG Generation	t_{RNG}				25	ms
TRNG On-Demand Check	t_{ODC}				50	ms
EEPROM						
Read Memory	t_{RM}				50	ms
Write Memory	t_{WM}				100	ms
Write State	t_{WS}				15	ms
Write/Erase Cycles (Endurance)	N_{CY}	T_A = +85°C (Note 12)	100K			
Data Retention	t_{DR}	T_A = +85ºC (Notes 13, 14)	10			years
GPIO PIN						
Output Low	GPIO V_{OL}	GPIOI_{OL} = 4mA (Note 15)			0.4	V
Input Low	GPIO V_{IL}		-0.3		0.2 x V_{CC}	V
Input High	GPIO V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Leakage Current	GPIO I_L		-1		+1	µA
I²C SCL AND SDA PINS (Note 16)						
Low-Level Input Voltage	V_{IL}		-0.3		0.2 × V_{CC}	V
High-Level Input Voltage	V_{IH}		0.7 × V_{CC}		V_{CC} + 0.3V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	(Note 3)		0.05 × V_{CC}		V
Low-Level Output Voltage at 4mA Sink Current	V_{OL}	(Note 15)			0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(Note 3)		30		ns
Pulse Width of Spikes that are Suppressed by the Input Filter	t_{SP}	(Note 3)			50	ns
Input Current with an Input Voltage Between 0.1V_{CCmax} and 0.9V_{CCmax}	I_I	(Notes 3, 17)	-1		+1	µA

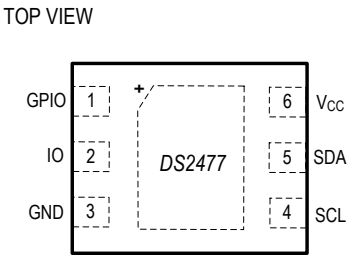
Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_I	(Note 3)		10		pF
SCL Clock Frequency	f_{SCL}	(Note 1)	0		1	MHz
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.45			µs
Low Period of the SCL Clock	t_{LOW}	(Note 18)	0.65			µs
High Period of the SCL Clock	t_{HIGH}	(Note 3)	0.35			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(Note 3)	0.35			µs
Data Hold Time	$tH_{D:DAT}$	(Notes 3, 18, 19)			0.35	µs
Data Setup Time	$t_{SU:DAT}$	(Notes 3, 18, 20)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 3)	0.35			µs
Bus Free Time Between a STOP andSTART Condition	t_{BUF}	(Note 3)	0.6			µs
Capacitive Load for Each Bus Line	C_B	(Notes 1, 21)			400	pF
Warm-Up Time	t_{OSCWUP}	(Note 1, 22)			1	ms

Note 1: System requirement.
Note 2: Operating current with 1-Wire write byte sequence followed by continuous write/read of 1-Wire Block command at 1MHz in overdrive.
Note 3: Guaranteed by design and/or characterization only. Not production tested.
Note 4: Voltage above which, during a rising edge on IO, a logic-one is detected.
Note 5: Voltage below which, during a t_F on IO, a logic-zero is detected.
Note 6: After V_{TH} is crossed during a rising edge on IO for high configuration only, the voltage on IO must drop by at least V_{HY} to be detected as logic-zero.
Note 7: Active pullup or resistive pullup and range are configurable.
Note 8: The active pullup does not apply to the rising edge of a presence pulse outside of a 1-Wire reset cycle or during the recovery after a short on the 1-Wire line.
Note 9: All 1-Wire timing specifications are derived from the same timing circuit.
Note 10: Up to an additional 10us of idle high time may occur between a 1-Wire Reset Cycle and the first time slot or between each 1-Wire byte during a command sequence.
Note 11: Current drawn from V_{CC} during the EEPROM programming interval or SHA-3 computation.
Note 12: Write-cycle endurance is tested in compliance with JESD47G.
Note 13: Not 100% production tested; guaranteed by reliability monitor sampling.
Note 14: Data retention is tested in compliance with JESD47G.
Note 15: The I-V characteristic is linear for voltages less than 1V.
Note 16: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.
Note 17: I/O pins of the DS2477 do not obstruct the SDA and SCL lines if V_{CC} is switched off.
Note 18: t_{LOW} min = $t_{HD:DAT}$ max + 200ns for rise or fall time + $t_{SU:DAT}$ min. Values greater than these can be accommodated by extending t_{LOW} accordingly.
Note 19: The DS2477 provides a hold time of at least 100ns for the SDA signal (referenced to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 20: The DS2477 can be used in a standard-mode I^2C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. Also the acknowledge timing must meet this setup time (I^2C bus specification Rev. 03, 19 June 2007).
Note 21: C_B = Total capacitance of one bus line in pF. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application (I^2C bus specification Rev. 03, 19 June 2007).
Note 22: I^2C communication should not take place for the max t_{OSCWUP} time following a power-on reset.

Pin Configuration



TDFN-EP
3mm x 3mm

Pin Description

PIN	NAME	FUNCTION
1	GPIO	Open-Drain, General-Purpose Input/Output. Requires external pullup resistor to V_{CC} when used as an output.
2	IO	1-Wire Input/Output Driver. The 1-Wire line can be pulled up by an internal weak pullup (R_{WPU}), an external pullup, or have both an external pullup and internal weak pullup.
3	GND	Ground
4	SCL	I^2C Serial Clock Input. Must be connected to V_{CC} through a pullup resistor.
5	SDA	Open-Drain, I^2C Serial Data Input/Output. Must be connected to V_{CC} through a pullup resistor.
6	V_{CC}	Power Supply Input
–	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Detailed Description

The DS2477 integrates the Maxim ChipDNA capability to protect all device stored data from invasive discovery. In addition to the PUF, the device integrates a FIPS/NIST compliant TRNG, 2Kb EEPROM for user memory, secret storage, and control registers. The self-timed 1-Wire master function supports advanced 1-Wire waveform features including standard and overdrive speeds, active pullup, and strong pullup for power delivery. The active pullup affects rising edges on the 1-Wire side. The strong pullup function uses the same pullup transistor as the active pullup, but with a different control algorithm. Once supplied with command and data, the input/output controller of the DS2477 performs time-critical 1-Wire communication functions such as reset/presence-detect cycle, read-byte, write-byte, read-block, write-block, single-bit R/W, triplets for ROM Search, and full command sequences for 1-Wire authenticators, without requiring interaction with the host processor. The GPIO pin can be independently operated under command control. All secrets, GPIO control, ROM memory, and user memory are located in a linear address space. The DS2477 communicates with a host processor through its I^2C bus interface in standard mode or in fast mode.

Design Resource Overview

Operation of the DS2477 involves use of device EEPROM and execution of specified device commands. Refer to the ***DS2477 Security User Guide*** for details.

Memory

A 2Kb secured EEPROM array provides SHA-3 secret storage and/or general-purpose, user-programmable memory. Depending on the memory area, there are either default or user-programmable options to set protection modes.

Open-Drain GPIO

A dedicated volatile memory region is used to control and/or read the open-drain GPIO pin. Upon power-up, the GPIO pin is high impedance. Refer to the ***DS2477 Security User Guide*** for details.

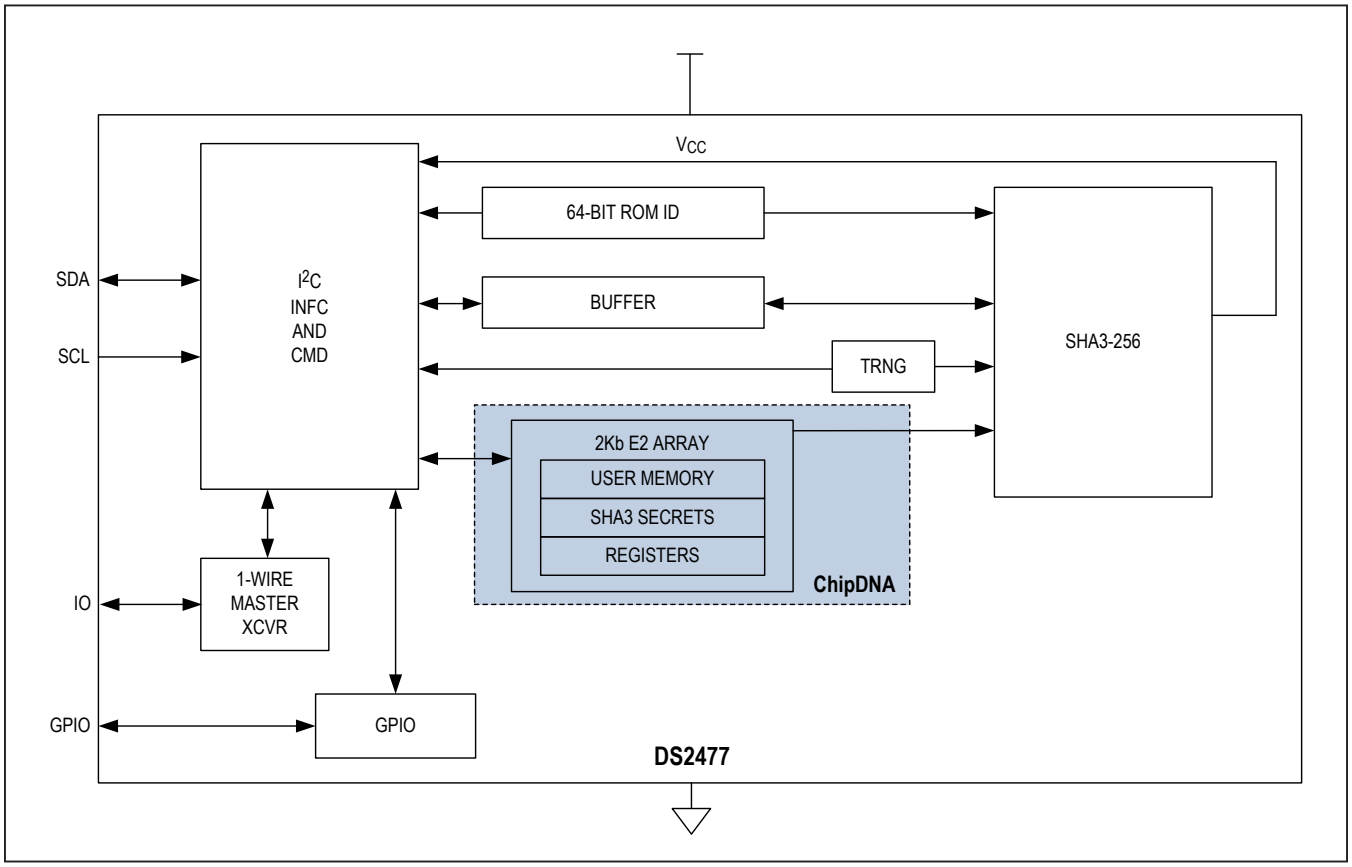


Figure 1. Block Diagram

1-Wire Master

The 1-Wire master reports data and status from the 1-Wire side to the host processor. Refer to the ***DS2477 Security User Guide*** for details.

Transaction Sequence

The protocol for accessing a connected slave device through the 1-Wire master is as follows:

- Initialization
- ROM Function command
- Device Function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the 1-Wire master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the slave is on the bus and is ready to operate. For more details, see the *1-Wire Signaling and Timing* section.

1-Wire Signaling and Timing

The 1-Wire protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the 1-Wire master initiates all falling edges. The 1-Wire master can communicate at two speeds: standard and overdrive. While in overdrive mode, the fast timing applies to all waveforms.

Figure 2 shows the initialization sequence required to begin any communication. A reset pulse followed by a presence pulse indicates that a slave is ready to receive data, given the correct ROM and device function command.

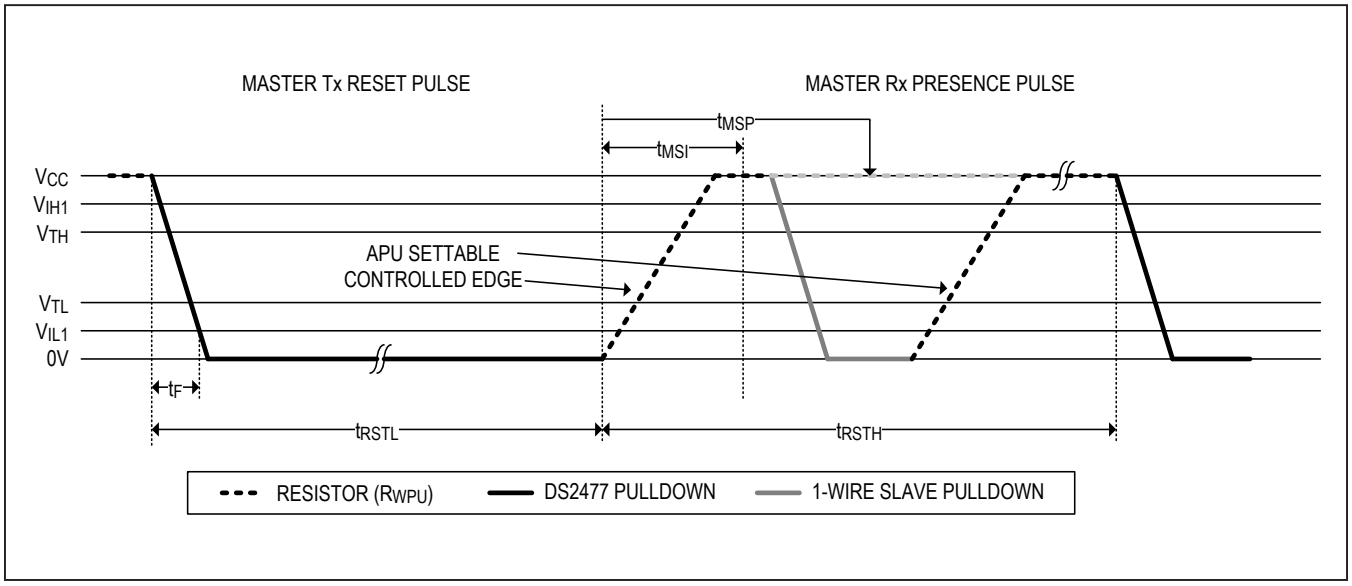


Figure 2. 1-Wire Reset/Presence-Detect Cycle

Read/Write Time Slots

Data communication on the 1-Wire bus takes place in time slots that carry a single bit each. Write time slots transport data from 1-Wire master to a connected slave. Read time slots transfer data from slave to the 1-Wire master. Figure 3 illustrates the definitions of the write and read time slots.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the slave starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window required by the slave. After the V_{TH} threshold has been crossed, the DS2477 needs a recovery time t_{REC} before it is ready for the next time slot.

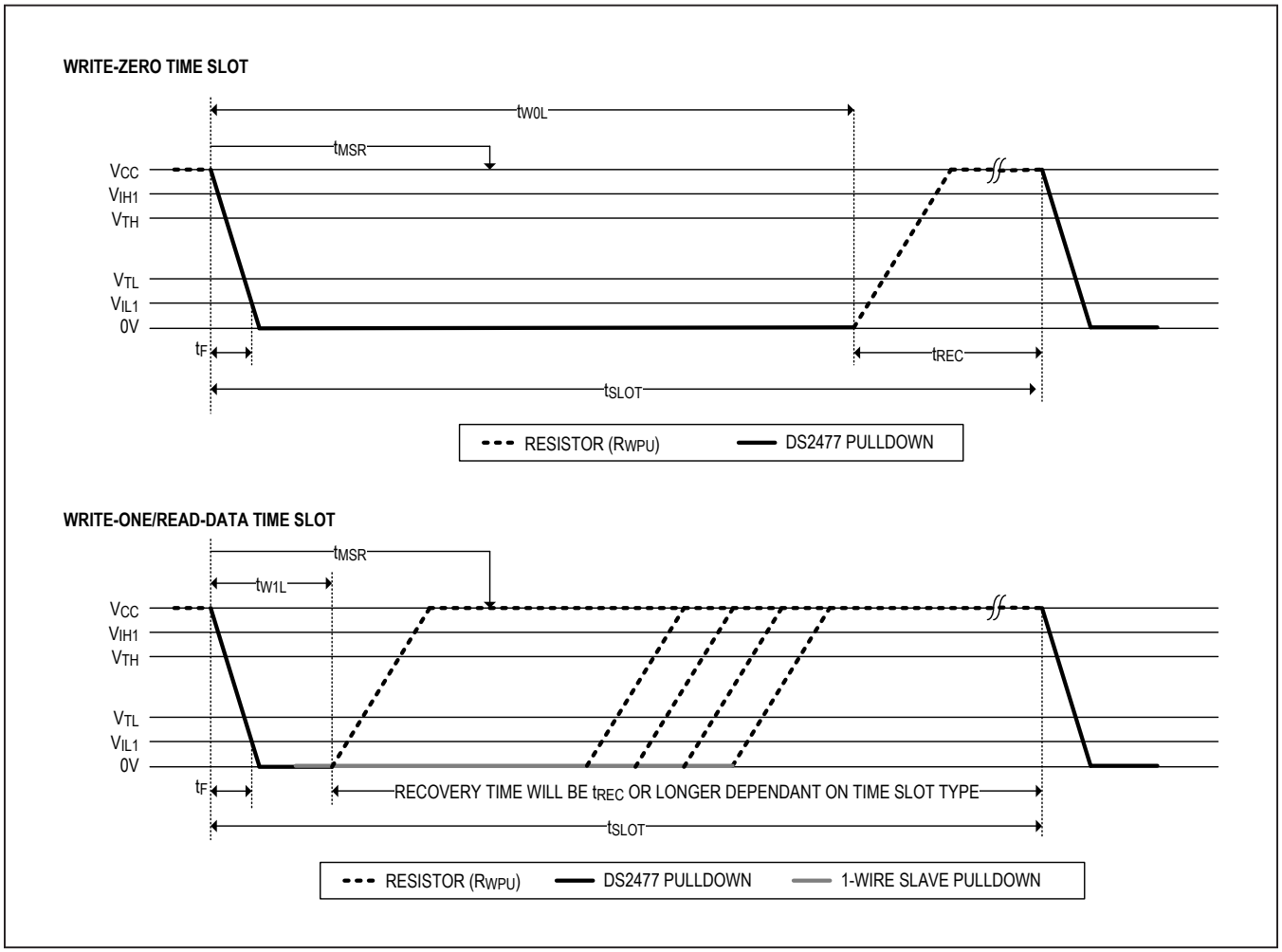


Figure 3. Read/Write Timing Diagrams

Slave-to-Master

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL}(read low time) is expired. During the t_{RL} window, when responding with a 0, the slave starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the slave does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over. Note that the slave t_{RL} during a logic 1 is adequately an approximation of the 1-Wire master t_{W1L} setting.

The slave t_{RL} plus the bus rise time on the near end and the internal timing generator of the slave on the far end define the 1-Wire master sampling window, in which the 1-Wire master performs a read from the data line. After reading from the data line, the 1-Wire master waits until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the slave to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single slave attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance.

Strong Pullup

The strong pullup function can be activated prior to a 1-Wire Write Byte, 1-Wire Read Byte, 1-Wire Single Bit, 1-Wire Block or 1-Wire Write Block command. Strong pullup is commonly used with 1-Wire EEPROM devices when copying buffer data to the main memory or when performing a SHA computation. The respective device data sheets specify the location in the communications protocol after which the strong pullup should be applied. The strong pullup can be enabled immediately prior to issuing the command that puts the 1-Wire device into the state where it needs the extra power for primitive 1-Wire commands or as an integral part of advanced commands. The strong pullup uses the same internal pullup transistor as the active pullup feature. See the R_{APU} parameter in the *Electrical Characteristics* table to determine whether the voltage drop is low enough to maintain the required 1-Wire voltage at a given load current and supply voltage. If the strong pullup is enabled, the DS2477 treats the rising edge of the time slot in which the strong pullup starts as if the active pullup was activated. However, in contrast to the active pullup, the strong pullup, i.e., the internal pullup transistor, remains conducting, as shown in Figure 4, until the DS2477 receives a command that generates 1-Wire communication (the typical case), or until the strong pullup is disabled or the 1-Wire master is reset. When the strong pullup ends, it is automatically disabled. Using the strong pullup feature does not change the active pullup settings.

Active Pullup (APU)

The APU is a function that accelerates the rise-time during a 1-Wire reset cycle, write time slot, or read time slot. The 1-wire master triggering mechanism is always ready after the initial low time of a 1-Wire reset cycle or time slot completes. This rise-time acceleration is accomplished by an active pullup impedance (R_{APU}) that begins driving once the active pullup on threshold (V_{IAPO}) is crossed from low to high. APU does not apply to the rising-edge of a recovery from a short on the line, a power-up presence pulse of a slave, or any other event outside of a 1-Wire reset cycle or a time slot. Enabling APU is generally recommended for best 1-Wire performance.

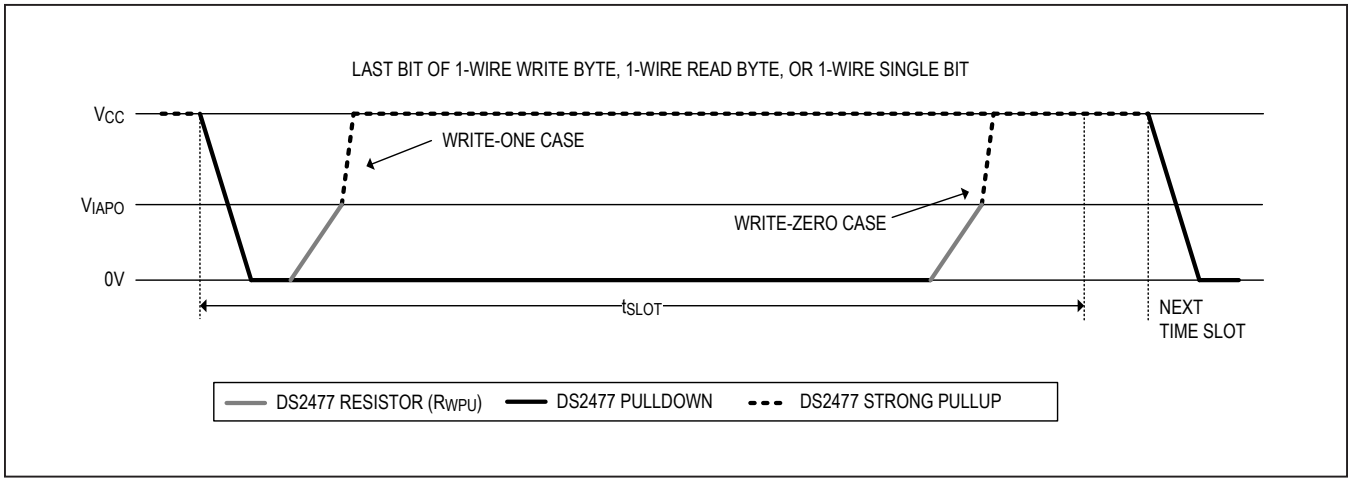


Figure 4. Strong Pullup Timing

Active Pullup for 1-Wire Reset Cycle

Figure 5 illustrates an active pullup for a 1-Wire reset cycle. A 1-Wire reset cycle begins by driving the line low for a t_{RSTL} period. When the t_{RSTL} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. APU then remains on for a duration of t_{APU}. After the completion of t_{APU}, the APU trigger mechanism is reset to be on again and triggers when the V_{IAPO} level is crossed from low to high upon a presence pulse completing. APU then remains on until the duration of t_{RSTH} expires.

Active Pullup for Read/Write Time Slots

Figure 6 illustrates an active pullup for a 1-Wire write zero or one time slot. A write zero time slot begins by the 1-Wire master driving the line low for a t_{W0L} period. When the t_{W0L} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. APU then remains on until t_{REC} expires. A write one-time slot begins by the 1-Wire master driving the line low for a t_{W1L} period. When the t_{W1L} expires, the APU triggering mechanism is on and triggers when the V_{IAPO} level is crossed from low to high. Unlike the the write zero time slot, the write one-time slot has APU for a much longer recovery duration defined by (t_{W0L} - t_{W1L}) + t_{REC}.

Figure 7 illustrates an active pullup for 1-Wire read time slots. On a 1-Wire read zero time slot, the master pulls the line low. The slave detects the low, and takes over driving the line. At that point, both the master and slave are driving the line low until t_{W1L} expires. After t_{W1L}, the master turns on the normal pullup (R_{WPU}), and enables the APU triggering mechanism. The master samples the read data at t_{MSR}. After the slave response time (t_{SPD}) expires, the slave releases the line. The APU triggers when the V_{IAPO} level is crossed from low to high. The APU remains on until the end of the slot as defined in Figure 7. On a 1-Wire read one-time slot, the master pulls the line low for t_{W1L}. The slave detects the low, but does not drive the line. When the t_{W1L} expires, the master turns on the normal pullup, and enables the APU triggering mechanism. The APU triggers when the V_{IAPO} level is crossed from low to high. The APU remains on until the end of the slot as defined by (t_{W0L} - t_{W1L}) + t_{REC}. The read one recovery time is longer than the read zero case.

I²C

General Characteristics

The I²C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates of up to 100kbps in standard mode and up to 400kbps in fast mode. The DS2477 works in both modes or up to a clock rate of 1MHz. A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus. Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP Figure 8. Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

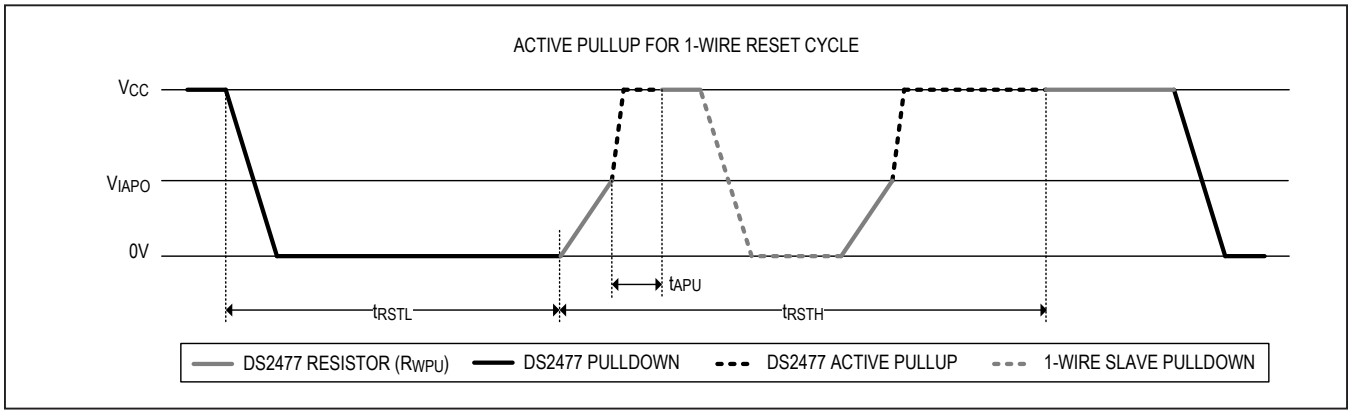


Figure 5. Active Pullup for a 1-Wire Reset Cycle

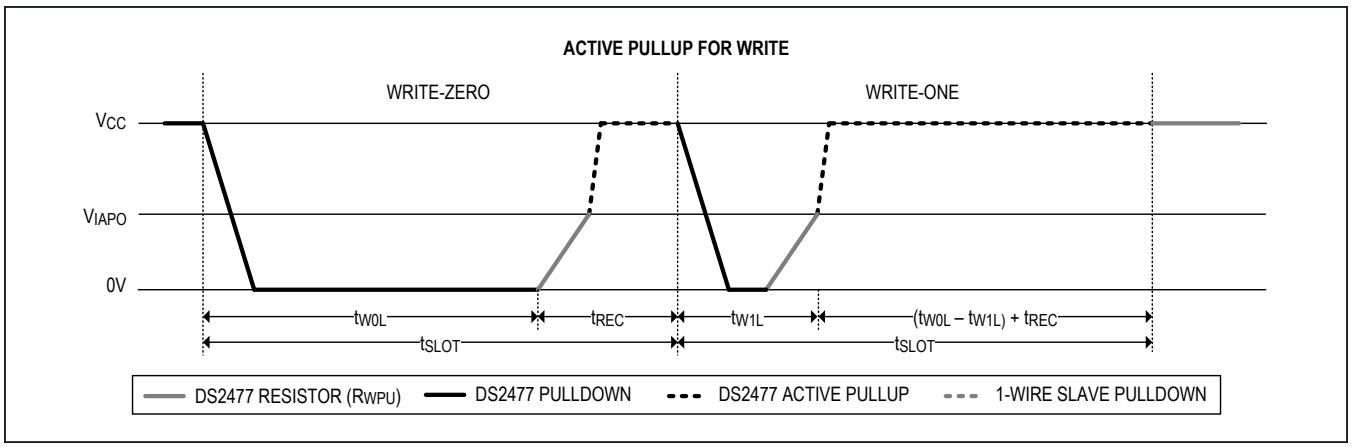


Figure 6. Active Pullup for 1-Wire Write Time Slot

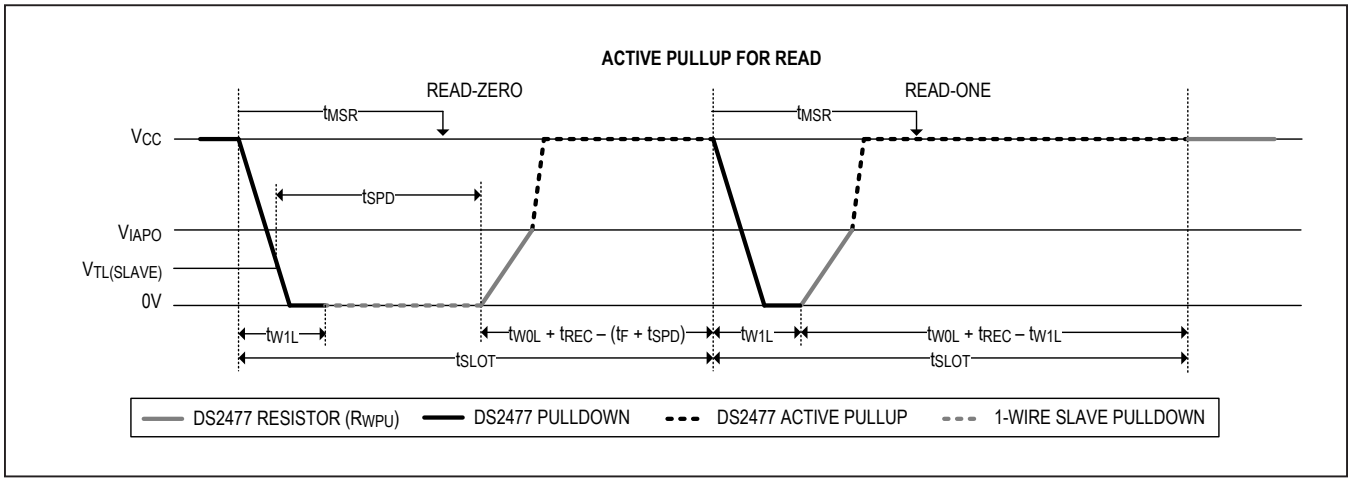


Figure 7. Active Pullup for 1-Wire Read Time Slot

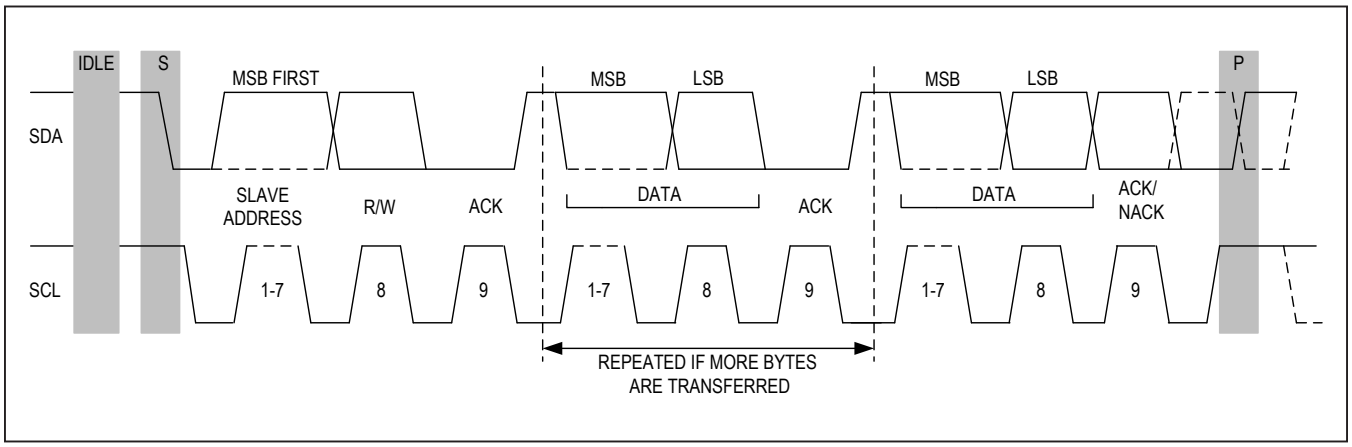


Figure 8. I²C Protocol Overview

Slave Address

The slave address to which the DS2477 responds is shown in Figure 9. The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/W) defines the data direction. When set to 0, subsequent data flows from master to slave (write access); when set to 1, data flows from slave to master (read access).

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. The timing references are defined in Figure 10.

Bus Idle or Not Busy

Both SDA and SCL are inactive and in their logic-high states.

START Condition

To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

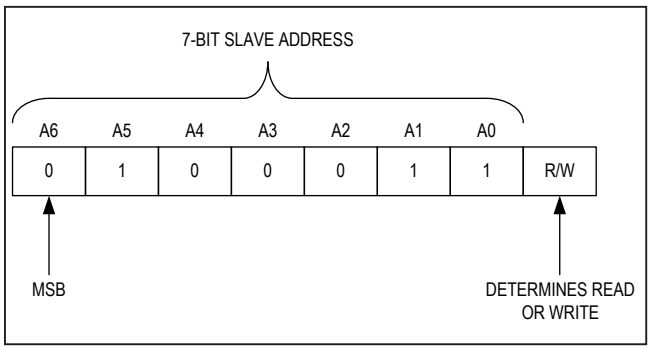


Figure 9. DS2477 I²C Slave Address

STOP Condition

To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition

Repeated STARTs are commonly used for read accesses after having specified a memory address to read from in a preceding write access. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid

With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 10). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT,}$ + t_R in Figure 10) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

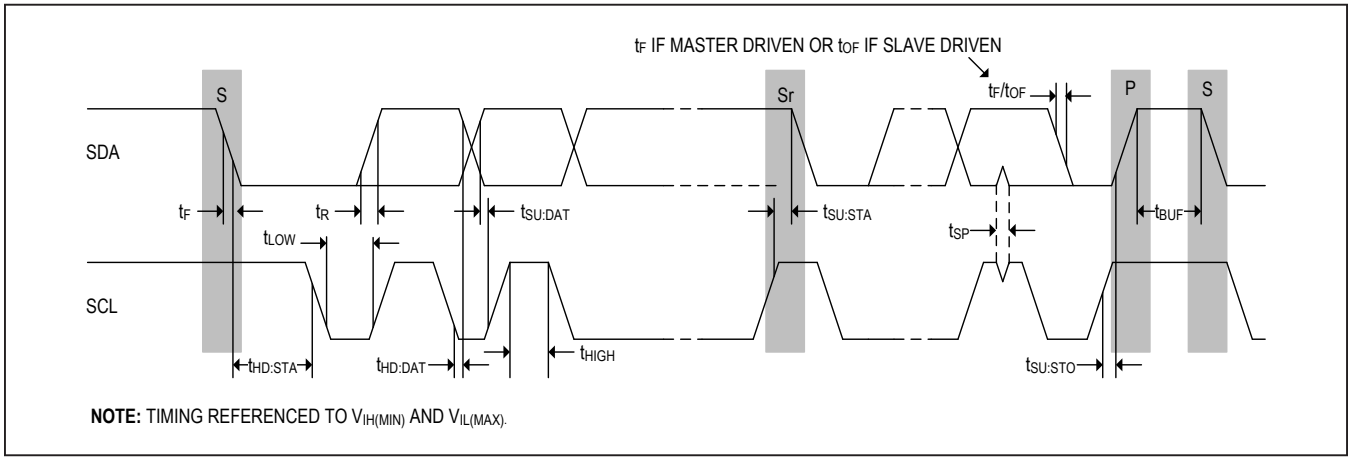


Figure 10. I²C Timing Diagram

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2477Q+T	-40°C to +85°C	6 TDFN (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/18	Initial release	—
0.1		Added Security User Guide and Developer Software hyperlink	1
1	3/19	Updated *Benefits and Features* section	1

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

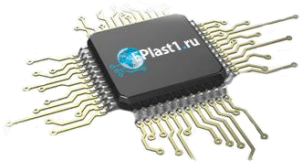
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.