

SINGLE CHIP PC AUDIO SYSTEM

CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO+I2S

92HD92

Description

The 92HD92 single-chip audio system is a low power optimized, high fidelity, 4-channel audio codec with integrated speaker amplifier, capless headphone amplifier, and low drop out voltage regulator.

Dual High Definition Audio and I2S Interfaces allow for docking and secondary audio support with a single codec.

The integrated combo jack allows for dual-function headphone and headset detection.

The integrated high-pass and band-pass filters allow for Hardware EQ and speaker protection.

The high integration of the 92HD92 enables the smallest PCB footprint with the lowest system audio BOM count and cost.

The 92HD92 provides high quality HD Audio capability to notebook and business desktop PC applications.

Features

- **4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
 - Supports full-duplex stereo audio and simultaneous VoIP
 - Provides a mono output
 - 2.1 audio crossover support
- **2W/channel Class-D stereo BTL speaker amplifier @ 4 ohms and 5V**
 - 10 band hardware parametric equalizer
 - Hardware compressor limiter
- **Capless headphone amplifier with charge pump/LDO**
- **I2S support (2 input, 1 output)**
- **Aux Audio Mode with I2C**
- **Combo Jack Support allowing for dual-function headphone and headset detection**
- **Speaker Protection**
 - Dedicated BTL high pass filter
 - Mono bandpass filter
- **Full HDA015-B low power support**
- **Internal digital core LDO voltage regulator**
- **Microsoft WLP desktop premium logo compliant**
- **Dual SPDIF for WLP compliant support of simultaneous HDMI and SPDIF output**
- **Support for 1.5V and 3.3V HDA signaling**
- **Two digital microphone inputs (mono, stereo, or quad microphones)**
- **High performance analog mixer**
- **2 adjustable VREF Out pins for analog microphone bias**
- **3 analog ports with port presence detect (2 single ended, 1 BTL)**
- **Digital PC Beep support**
- **48-pad QFN RoHS packages in Commercial and Industrial Temperature Ranges**

Full HDA015-B low power support

- Audio inactivity transitions codec from D0 to D3 low power mode
- Resume from D3 to D0 with audio activity in < 10 msec
- D3 to D0 transition with < -65dB pop/click
- Port presence detect in D3 with or without bit clock
- PC beep wake up in D3
- Additional vendor specific modes for even lower power

Software Support

- Intuitive IDT HD Sound graphical user interface that allows configurability and preference settings
- 12 band fully parametric equalizer
 - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
 - System-level effects automatically disabled when external audio connections made
- Dynamics Processing
 - Enables improved voice articulation
 - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- IDT Vista APO wrapper
 - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
 - Improved multi-streaming user experience with less support calls
- Broad 3rd party branded software including Creative, Dolby, DTS, and SRS

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92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

1. DESCRIPTION

1.1. Overview

The 92HD92 audio CODEC provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. SPDIF outputs support sample rates of 192kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

An integrated BTL stereo amplifier is ideal for driving 4ohm or 8ohm integrated speakers in mobile and ultra-mobile computers. For desktop computers or mobile computers using only one speaker, the BTL output stage may be configured to support a single mono speaker.

The 92HD92 audio CODEC supports a wide range of desktop and laptop configurations. The 2 independent SPDIF output interfaces provide connectivity to consumer electronic equipment or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible. All inputs can be programmed with 0-30 dB gain in 10 dB steps allowing for line or microphone use of any input.

Port presence detect capabilities allow the CODEC to detect when audio devices are connected to the CODEC. The fully parametric Internal EQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD92 audio CODEC operates with a 3.3V digital supply and a 5V (4.75V allowed when using external voltage regulator) analog supply. It allows for 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

The 92HD92 audio CODEC is offered in a 48-pin QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

| | |
|-------------------|------------------------------|
| 92HD92B1X5NLGXyyX | Aux mode |
| 92HD92B2X5NLGXyyX | No Aux mode |
| 92HD92B1X5NLGIyyX | Aux mode. Industrial Temp |
| 92HD92B2X5NLGIyyX | No Aux mode. Industrial Temp |

yy = silicon stepping/revision, contact sales for current data.
Add an "8" to the end for tape and reel delivery.

Please note that Industrial Temp is only available on revision WC and forward.

2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input/Output) ports allow for the highest possible flexibility and supporting a wide variety of consumer desktop and mobile system use models.

- Port A supports
 - Headphone Out
 - Line Out
 - Line Input
 - Mic with 0/10/20/30 dB Boost
- Port B supports
 - Capless Headphone Out
 - Capless Line Out
- Port D supports
 - BTL stereo output
 - BTL (L+/L-) mono out
- Port E supports
 - Headpone Out
 - Line Out (I2S)
- Port F supports
 - Line In (I2S)
 - Mic with 0/10/20/30 dB boost and Vref_Out
- Mono Out supports
 - Line Out

| Pins 48-QFN | Port | Input | Output | Headphone | BTL | Mic Bias (Vref pin) | Input boost amp |
|-------------|----------------------------|---------|---------|-----------|-----|---------------------|-----------------|
| 28/29 | A | Yes | Yes | Yes | | Yes | Yes |
| 31/32 | B | | Yes | Yes | | | |
| 40/41/43/44 | D | | Yes | | Yes | | |
| 17 | E | | Yes I2S | Yes | | | Yes |
| 24 | F | Yes I2S | | | | | Yes |
| 25 | Mono Out | | Yes | | | | |
| 48 | SPDIF_OUT0 | | Yes | | | | |
| 46 | DMIC1/SPDIFOUT1/ Aux_In | Yes | Yes | | | | Yes |
| 4 (CLK=2) | DMIC0 | Yes | | | | | Yes |

Table 1. Port Functionality

Note: Pins 15/16/18 are shared for I2S clocking. Port C is vendor reserved for this device

2.1.1. Port Characteristics

Universal (Bi-directional) jacks are supported on ports A, E, and F for all family members. Ports A and B are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 50K (nominal) at the pin.

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

DAC full scale outputs and intended full scale input levels are 1V rms at 5V. Line output ports and Headphone output ports on the 92HD92 codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in power state D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use the codec, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

| AFG Power State | Input Enable | Output Enable | Used as output for DAC/Mixer | Used as output for analog PC_Beep | Used as input for ADC, mixer | Port Behavior |
|-----------------|--------------|---------------|--|-----------------------------------|------------------------------|---|
| D0-D2 | 1 | 1 | Don't care | Don't care | Yes | Not allowed. Port is active as input. |
| | | | | | No | Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 1 | 0 | NA | NA | Yes | Active - Port enabled as input |
| | 1 | 0 | NA | NA | No | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 0 | 1 | currently used by DAC, mixer, beep, or is traditional line or headphone output | | NA | Active - Port enabled as output |
| | | | not currently used by DAC, mixer, beep and is capless HP/BTL port | | | Inactive (Power Down) |
| | 0 | 0 | NA | NA | NA | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D3 | 1 | 1 | NA | NA | Don't care | Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 1 | 0 | NA | NA | Don't care | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 0 | 1 | currently used by DAC, mixer, beep, or is traditional line or headphone output | | Don't care | Low power state. If enabled, Beep will output from the port |
| | 0 | 1 | not currently used by DAC, mixer, beep and is capless HP/BTL port | | Don't care | Inactive (Power Down) |
| | 0 | 0 | NA | NA | Don't care | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D3cold | - | - | | | | Inactive (lower power) - Port keeps output coupling caps charged if port uses caps. |
| D4 | - | - | | | | Inactive (lower power) - Port keeps output coupling caps charged if port uses caps. |
| D5 | - | - | | | | Off - Charge on coupling caps (if used) will not be maintained. |

Table 2. Analog Output Port Behavior

2.1.2. *Vref_Out*

Port A supports Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

2.1.3. *Jack Detect*

Plugs inserted to a jack on Ports A, B & SPDIFOUT0 are detected using SENSE_A. Plugs inserted to a jack on Ports E, F, DMIC0, & SPDIFOUT1 are detected using SENSE_B. Per HDA015-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per HDA015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages..

| AVdd Nominal Voltage (+/- 5%) | Resistor Tolerance Pull-Up | Resistor Tolerance SENSE_A/B |
|-------------------------------|----------------------------|------------------------------|
| 4.75V | 1% | 1% |

| Resistor | SENSE_A | SENSE_B |
|----------|-----------------|-------------------|
| 39.2K | PORT A (HP0) | Port E |
| 20.0K | PORT B (HP1) | Port F |
| 10.0K | NA | DMIC0 |
| 5.11K | SPDIFOUT0 | SPDIFOUT1 (DMIC1) |
| 2.49K | Pull-up to AVDD | Pull-up to AVDD |

Table 3. 48pin Jack Detect

See reference design for more information on Jack Detect implementation.

2.1.4. *SPDIF Output*

Both SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

Per the HDA015-B, the SPDIF outputs support the ability to provide clocking information even when no stream is selected for the converter, or when in a low power state. Also, the SPDIF output ports support port presence detect.

SPDIF Outputs are outlined in tables below.

| AFG Power State | RESET# | Output Enable | Converter Dig Enable | Stream ID | Keep Alive Enable | Pin Behavior |
|-----------------|--------------------|---------------|----------------------|-----------|-------------------|---|
| D0-D3 | Asserted (Low) | - | - | - | - | Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained. |
| D0 | De-Asserted (High) | Disabled | - | - | - | Hi-Z (internal pull-down enabled) |
| | De-Asserted (High) | Enabled | Disabled | - | - | Active - Pin drives 0 (internal pull-down NA) |
| | De-Asserted (High) | Enabled | Enabled | 0 | - | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| | De-Asserted (High) | Enabled | Enabled | 1-15 | - | Active - Pin drives SPDIFOut0 data (internal pull-down NA) |
| D1-D2 | De-Asserted (High) | Disabled | - | - | - | Hi-Z (internal pull-down enabled) |
| | De-Asserted (High) | Enabled | - | - | 0 | Active - Pin drives 0 (internal pull-down NA) |
| D3 | De-Asserted (High) | Enabled | Enabled | - | 1 | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| | | Disabled | - | - | 1 | Hi-Z (internal pull-down enabled) |
| | | Enabled | Enabled | - | 1 | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| D3cold | - | - | - | - | - | Hi-Z (internal pull-down enabled) |
| D4 | - | - | - | - | - | Hi-Z (port off) |
| D5 | - | - | - | - | - | Hi-Z (port off) |

Table 4. SPDIF OUT 0 Behavior

| AFG Power State | RESET# | GPIO0 Enable | Input Enable | Output Enable | Converter Dig En | Stream ID | Keep Alive En | Pin Behavior |
|-----------------|--------------------|--------------|--------------|---------------|------------------|-----------|---------------|---|
| D0-D3 | Asserted (Low) | - | - | - | - | - | - | Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained. |
| D0-D3 | De-Asserted (High) | Enabled | - | - | - | - | - | Active - Pin reflects GPIO0 configuration (internal pull-down enabled) |
| D0-D3 | De-Asserted (High) | Disabled | Enabled | Disabled | - | - | - | Pin functions as digital mic input (internal pull-down enabled) |

Table 5. SPDIF OUT 1 Behavior

| AFG Power State | RESET# | GPIO0 Enable | Input Enable | Output Enable | Converter Dig En | Stream ID | Keep Alive En | Pin Behavior |
|-----------------|--------------------|--------------|--------------|---------------|------------------|-----------|---------------|--|
| D0 | De-Asserted (High) | Disabled | - | Disabled | - | - | - | Hi-Z (internal pull-down enabled) |
| | | | | Enabled | Disabled | - | - | Active - Pin drives 0 (internal pull-down NA) |
| | | | | | Enabled | 0 | - | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| | | | | | | 1-15 | - | Active - Pin drives SPDIFOut1 data (internal pull-down NA) |
| D1-D2 | De-Asserted (High) | Disabled | Disabled | Disabled | - | - | - | Hi-Z (internal pull-down enabled) |
| | | | | Enabled | Disabled | - | - | Active - Pin drives 0 (internal pull-down NA) |
| | | | | | Enabled | - | 0 | Active - Pin drives 0 (internal pull-down NA) |
| | | | | | | - | 1 | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| D3 | De-Asserted (High) | Disabled | Disabled | Disabled | - | - | - | Hi-Z (internal pull-down enabled) |
| | | | | Enabled | Disabled | - | - | Hi-Z (internal pull-down enabled) |
| | | | | | Enabled | - | 0 | Hi-Z (internal pull-down enabled) |
| | | | | | | - | 1 | Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA) |
| D3cold | - | Disabled | Disabled | - | - | - | - | Hi-Z (internal pull-down enabled) |
| D4 | - | - | - | - | - | - | - | Hi-Z (port off) |
| D5 | - | - | - | - | - | - | - | Hi-Z (port off) |

Table 5. SPDIF OUT 1 Behavior

2.2. Mono Output

The Mono Out port source selection, power state, and mute characteristics are all independently controlled by the mono output port controls. EQ does not apply to this path. An internal 2nd order band-pass filter is provided to restrict the output frequencies when using mono out to drive an external amplified sub-woofer.

The following sources are available for the Mono Out pin:

- DAC0 Output: When selected (by using the port connection list), the DAC0 left and right outputs are summed together.
- DAC1 Output: When selected (by using the port connection list), the DAC1 left and right outputs are summed together.
- Mixer Output: When selected (by using the port connection list), the mixer left and right outputs are summed together.

The stereo inputs are scaled by -6dB and then summed to provide an output that is the average of the two inputs. The full scale output at mono out is designed to be about 0dBV. It is not possible to adjust to a +3dBV output level.

2.3. Mono output Band-Pass Filter

For many applications, the primary speakers are incapable of reproducing low frequency audio. Therefore it is desirable to implement a woofer or sub-woofer speaker. The mono output is ideal for this task.

However, the frequency response should be restricted to prevent interference with the primary speakers. Typically an external filter, known as a cross-over filter, is used. The mono processing path includes a band-pass filter with programmable high and low cut-off frequencies to eliminate the need for an external filter.

2.3.1. Filter Description

The band-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off. The filter may be programmed for a -3dB lower band edge of: 63Hz, 80Hz, 100Hz, 120Hz, 150Hz, 200Hz, 315Hz, or 400Hz. The filter may be programmed for a -3dB upper band edge of: 150Hz, 200Hz, 250Hz, 315Hz, 400Hz, 500Hz, 630Hz, or 800Hz.

The band-pass filter is enabled by default with a cut-off frequencies at 120Hz and 250Hz. The filter may be bypassed using the associated verb (processing state verb).

The Analog PC_Beep input is not affected by the band-pass filter.

2.4. Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available:

- Port A
- Port F
- DAC 0
- DAC 1

2.5. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function :(-16 to +30dB gain in 1dB steps) as an output amp and allow a preselection of one of below possible inputs:

- Port A
- Port F
- Mixer Output
- DMIC 0
- DMIC 1

2.6. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

| Function | D0 | D1 ¹ | D2 | D3 | D3cold | Vendor Specific D4 | Vendor Specific D5 |
|---------------------------|----|-----------------|-----------|------------------------|------------------------|------------------------|--------------------|
| SPDIF Outputs | On | On | On (idle) | On (idle) ⁵ | Off | Off | Off |
| Digital Microphone inputs | On | Off | Off | Off | Off | Off | Off |
| DAC | On | Off | Off | Off | Off | Off | Off |
| D2S | On | Off | Off | Off | Off | Off | Off |
| ADC | On | Off | Off | Off | Off | Off | Off |
| ADC Volume Control | On | Off | Off | Off | Off | Off | Off |
| Ref ADC | On | Off | Off | Off | Off | Off | Off |
| Analog Clocks | On | Off | Off | Off | Off | Off | Off |
| GPIO pins | On | On | On | On ⁵ | On | On | Off |
| VrefOut Pins | On | On | Off | Off | Off | Off | Off |
| Input Boost | On | On | Off | Off | Off | Off | Off |
| Analog mixer | On | On | Off | Off | Off | Off | Off |
| Mixer Volumes | On | On | Off | Off | Off | Off | Off |
| Digital PC_Beep | On | On | On | On ⁵ | Off | Off | Off |
| Lo/HP Amps | On | On | On | Low Drive ² | Low Drive ² | Low Drive ² | Off |
| Capless HP Amps | On | On | On | Low Drive ² | Low Drive ² | Low Drive ² | Off |
| BTL Amp | On | On | On | Low Drive ² | Off | Off | Off |
| VAG amp | On | On | On | Low Drive ³ | Low Drive | Low Drive | Off |
| Port Sense | On | On | On | On ⁴ | Off | Off | Off |
| Reference Bias generator | On | On | On | On | On | On | Off |
| Reference Bandgap core | On | On | On | On | On | On | Off |
| HD Audio-Link | On | On | On | On ⁵ | Limited | Off | Off |

Table 6. Power Management

1. No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2. VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance. The codec will shut down the capless headphone amplifiers and BTL amplifier in D3 and below. In D3, the codec will turn on the BTL and Capless amplifiers if activity is detected on the PC_BEEP input and analog PC_Beep is enabled.
3. VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. Both AVDD and DVDD must be available for Port Sense to operate.
5. Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under IDT Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.7. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.8. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from the D1 to the D0 state within 1 mS.

2.9. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.10. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the HDA015-B section for more information):

| Function | HDA Bus active | HDA Bus stopped |
|-----------------------------------|----------------------|--|
| Port Presence Detect state change | Unsolicited Response | Wake Event followed by an unsolicited response |
| GPIO state change | Unsolicited Response | Wake Event followed by an unsolicited response |

2.10.1. AFG D3cold

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus HDA015-B, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.

2.11. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and HDA015-B. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired. This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.12. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48-QFN package the voltage selection is done dynamically based on the input voltage of DVDD_IO.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.13. Multi-channel capture

The capability to assign multiple ADC Converters to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

| | | |
|--------------|--------------|--------|
| ADC1 CnvtrID | (NID = 0x08) | |
| | [3:0] | Ch = 2 |
| ADC0 CnvtrID | (NID = 0x07) | |
| | [3:0] | Ch=0 |

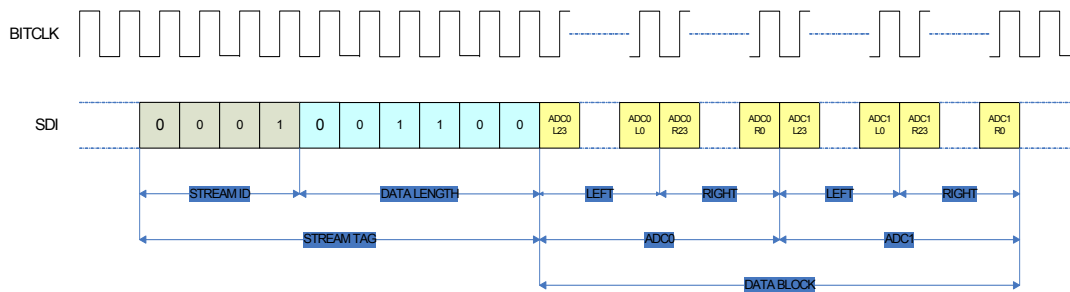
Table 7. Example channel mapping

Figure 1. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 2. Multi-channel timing diagram



| ADC[1:0] Cnvr | Bit Number | Sub Field Name | Description |
|---------------|------------|----------------|--|
| | [15] | StrmType | Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported) |
| | [14] | FrmtSmpIRate | Sample Base Rate 0= 48kHz 1=44.1kHz |
| | [13:11] | SmpIRateMultp | Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 192kHz only, 176.4 not supported 100-111= Reserved |
| | [10:8] | SmpIRateDiv | Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported) |

Table 8: Mult-channel

| | | | |
|--|-------|-------------|---|
| | [6:4] | BitsPerSmpl | Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved |
| | [3:0] | NmbrChan | Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels ... 1111= 16 channels. |
| | [7:4] | Strm | Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused. |
| | [3:0] | Ch | Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2. |

Table 8: Mult-channel

2.14. EAPD

The EAPD pin (pin 47) is a dedicated, bi-directional control pin. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The default state of this pin is 0 (driving low.) The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and HDA015-B, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low. A port will request External Amp Power Up when its power state is active (FG and pin widget power state is D1 or D0) or (Analog PC_Beep is enabled and port is enabled as an output) and the port's EAPD bit is set to 1. The state of the EAPD pin (unless configured as an input or held low by an external circuit when configured as an open drain output) will be the logical OR of the external amp power up requests from all ports.

By default, the EAPD pin also functions as the Mute#/ShutDown# input for the internal BTL amplifier. In this mode, a low value at the pin (either due to internal EAPD being 0, or to an external entity forcing the pin low) will cause the internal BTL amplifier to mute or enter a low power state depending on the amplifier configuration. (See below)

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by a power on reset:

| MODE1 | MODE0 | EAPD Pin Function | Description |
|-------|-------|-------------------|--|
| 0 | 0 | Open Drain I/O | Value at pin is wired-AND of EAPD bit and external signal.(default) |
| 0 | 1 | CMOS Output | Value of EAPD bit in pin widget is forced at pin |
| 1 | 0 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |
| 1 | 1 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |

Table 9. EAPD Pin Mode Select

| Control Flag | Description |
|-------------------|---|
| EAPD PIN MODE 1:0 | Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain) |
| BTL/HP SD | 0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only |
| BTL/HP SD MODE | 0 = Amp will mute when disabled./ 1 = Amp will shut down (enter a low power state) when disabled (default for YA forward) |
| BTL/HP SD INV | 0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high. |

Table 10. Control bit descriptions for BTL amplifier and Headphone amplifier enable configurations

| BTL SD | BTL SD MODE | BTL SD INV | EAPD Pin State | BTL Amp State |
|--------|-------------|------------|----------------|---|
| 0 | 0 | 0 | 0 | Amplifier is mute (default ¹) |
| 0 | 0 | 0 | 1 | Amplifier is active |
| 0 | 0 | 1 | 0 | Amplifier is active |
| 0 | 0 | 1 | 1 | Amplifier is mute |
| 0 | 1 | 0 | 0 | Amplifier is in a low power state |
| 0 | 1 | 0 | 1 | Amplifier is active |
| 0 | 1 | 1 | 0 | Amplifier is active |
| 0 | 1 | 1 | 1 | Amplifier is in a low power state |
| 1 | 0 | NA | NA | Amplifier follows pin/function group power state and will mute when disabled |
| 1 | 1 | NA | NA | Amplifier follows pin/function group power state and will enter a low power state when disabled |

Table 11. BTL Amp Enable Configuration

- EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

| HP SD | HP SD MODE | HP SD INV | EAPD Pin State | Headphone Amp State |
|-------|------------|-----------|----------------|---|
| 0 | 0 | 0 | 0 | Amplifier is mute (default ¹) |
| 0 | 0 | 0 | 1 | Amplifier is active |
| 0 | 0 | 1 | 0 | Amplifier is active |
| 0 | 0 | 1 | 1 | Amplifier is mute |
| 0 | 1 | 0 | 0 | Amplifier is in a low power state |
| 0 | 1 | 0 | 1 | Amplifier is active |

Table 12. Headphone Amp Enable Configuration

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| HP SD | HP SD MODE | HP SD INV | EAPD Pin State | Headphone Amp State |
|-------|------------|-----------|----------------|---|
| 0 | 1 | 1 | 0 | Amplifier is active |
| 0 | 1 | 1 | 1 | Amplifier is in a low power state |
| 1 | 0 | NA | NA | Amplifier follows pin/function group power state and will mute when disabled |
| 1 | 1 | NA | NA | Amplifier follows pin/function group power state and will enter a low power state when disabled |

Table 12. Headphone Amp Enable Configuration

- EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

| Port E Headphone Amp Enable Configuration Bits | Normal Mode | Aux Mode |
|--|-------------|----------------------------|
| SD (EAPD Pin or power setting) | supported | Not supported ¹ |
| SD INV | supported | |
| SD MODE (power down or mute) | supported | |

Table 13. Port E Headphone Amp Enable Configuration support by part and mode

- SD is ignored in Aux mode since the widget power state is "D3" or "D3cold".

| Analog BEEP enabled | EAPD Pin value ¹ | Description |
|---------------------|---|--|
| 0 | Forced to low when in D2 or D3 | Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit. |
| 1 | Forced low in D2 or D3 unless port is enabled as output | Power state is ignored if port is enabled as output and port EAPD=1 to allow PC_Beep support in D2 and D3 |

Table 14. EAPD Analog PC_Beep behavior

- When pin is enabled as Open Drain or CMOS output.

| AFG Power State | RESET# | Analog PC_BEEP | Port Power State | Pin Behavior |
|-----------------|--------------------|----------------|------------------|---|
| D0-D3 | Asserted (Low) | - | - | Active low immediately after power on, otherwise the previous state is retained across FG and link reset events |
| D0 | De-Asserted (High) | - | - | Active - Pin reflects EAPD bit unless held low by external source. |
| D1 | De-Asserted (High) | - | D0-D1 | Active - Pin reflects EAPD bit unless held low by external source. |
| D2 | De-Asserted (High) | Disabled | D0-D2 | Pin forced low to disable external amp |
| D2 | De-Asserted (High) | Enabled | D0-D2 | Active - EAPD Pin high if any port EAPD bit =1 and that port also enabled as output. |
| D3 | De-Asserted (High) | Disabled | D0-D3 | Pin forced low to disable external amp |
| D3 | De-Asserted (High) | Enabled | D0-D3 | Active - EAPD Pin high if any port EAPD bit=1 and that port also enabled as output. |
| D3cold | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D4 | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D5 | De-Asserted (High) | - | - | Pin Hi-Z (off) |

Table 15. EAPD Behavior

Figure 3. HP EAPD Example to be replaced by single pin for internal amp

HP AUDIO CONTROL BLOCK DIAGRAM

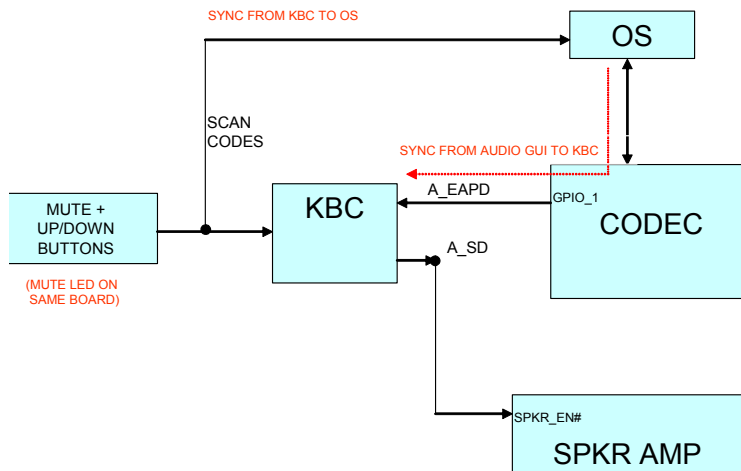
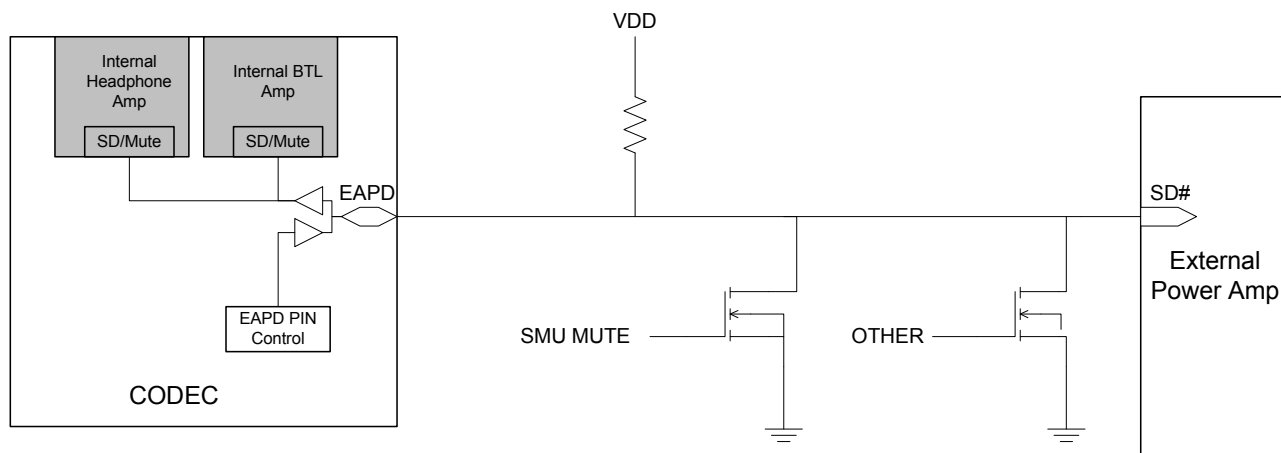


Figure 4. EAPD implementation



2.15. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the

analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-B input.

The codec supports the following digital microphone configurations:

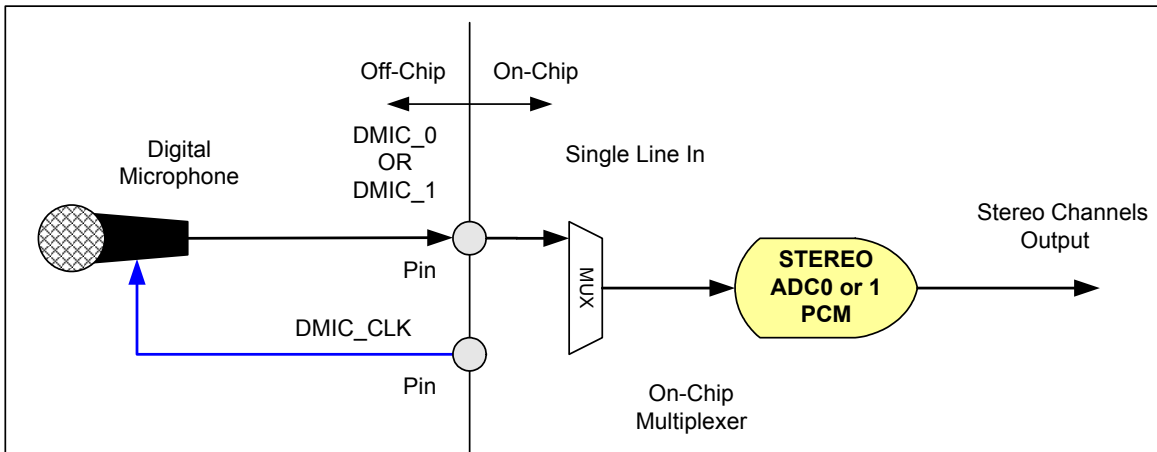
| Digital Mics | Data Sample | ADC Conn. | Notes |
|--------------|---|-----------|--|
| 0 | N/A | N/A | No Digital Microphones |
| 1 | Single Edge | 0, or 1 | Available on either DMIC_0 or DMIC_1 When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for "Left" and select mono operation using the vendor specific verb. "Left" D-mic data is used for ADC left and right channels. |
| 2 | Double Edge on either DMIC_0 or 1 | 0, or 1 | Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge (multiplexed output) capability. |
| 3 | Double Edge on one DMIC pin and Single Edge on the second DMIC pin. | 0, or 1 | Requires both DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge (multiplexed output) capability. Two ADC units are required to support this configuration |
| 4 | Double Edge | 0, or 1 | Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration |

Table 16. Valid Digital Mic Configurations

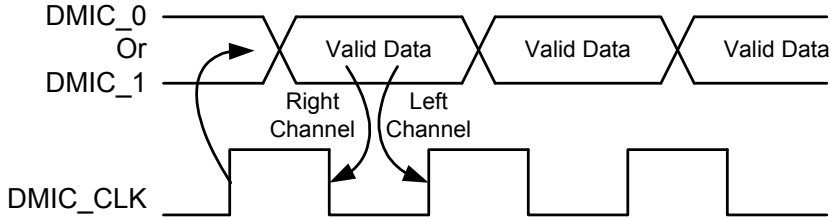
| Power State | DMIC Widget Enabled? | DMIC_CLK Output | DMIC_0,1 | Notes |
|-------------|----------------------|-----------------|----------------|--|
| D0 | Yes | Clock Capable | Input Capable | DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low |
| D1-D3 | Yes | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D0-D3 | No | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D4 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D5 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |

Table 17. DMIC_CLK and DMIC_0,1 Operation During Power States

Figure 5. Single Digital Microphone (data is ported to both left and right channels)



Single Microphone not supporting multiplexed output.



Single "Left" Microphone, DMIC input set to mono input mode.

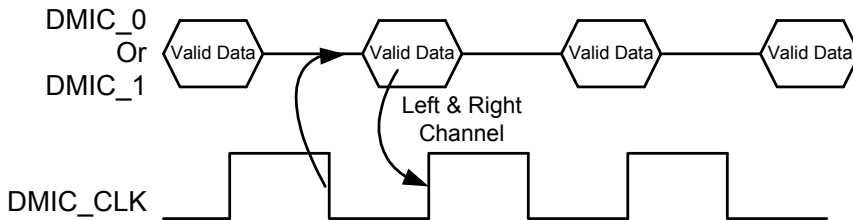
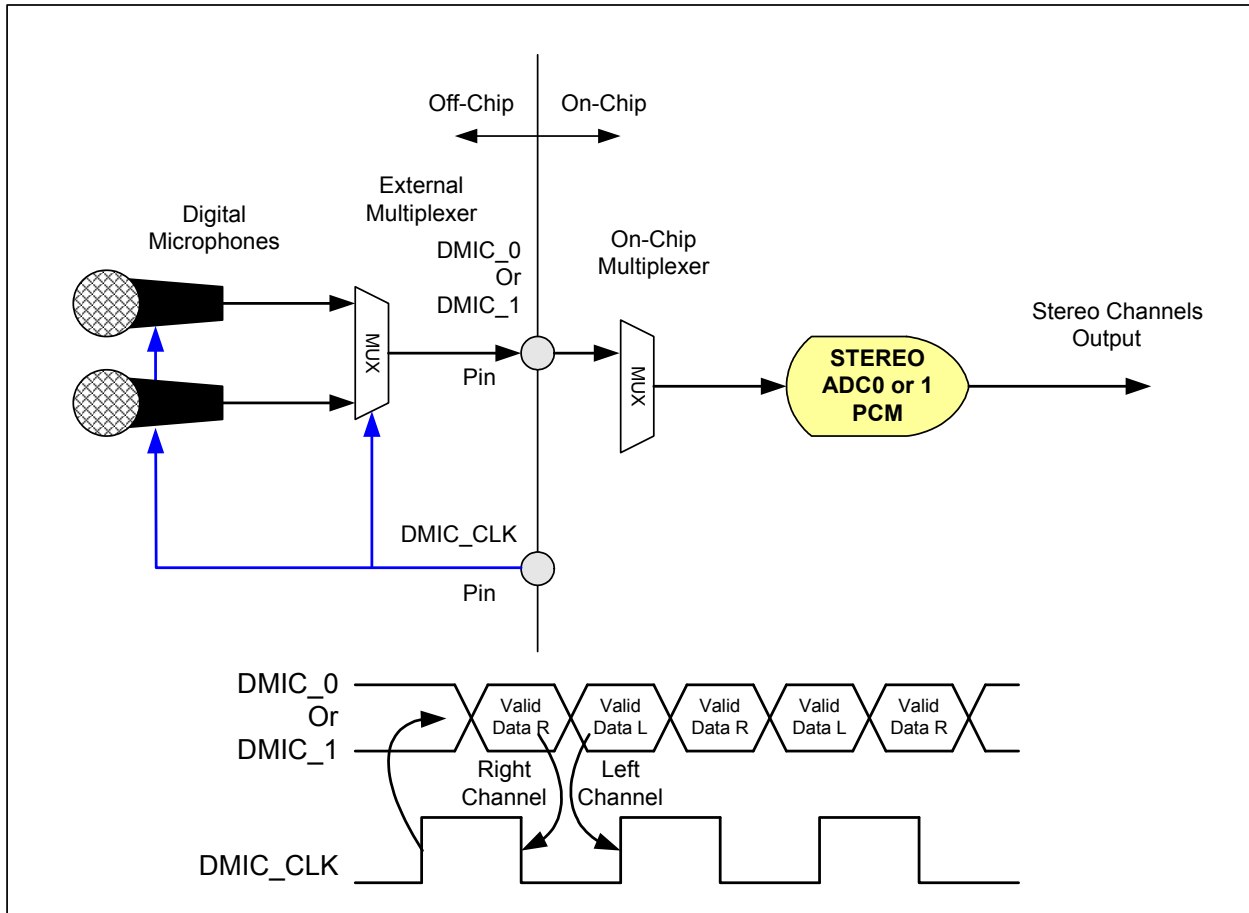


Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

Figure 7. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, in this case the external multiplexer is not required.

2.16. Analog PC-BEEP

The codec supports automatic routing of the PC_BEEP pin to Port A, Port B, and Port D outputs when the HD-Link is in reset.

When the link is active (not held in reset) Analog PC-BEEP may be enabled manually. Analog PC_BEEP is mixed at the port and only ports enabled as outputs will pass PC_BEEP.

Beep activity monitoring is provided when the analog beep path is enabled and the CODEC or amplifier is in a low power state (D3).

The Analog PC Beep input is sampled for 500us every 1ms. If the beep input is high or low (>200mVpp) for at least 37% of that time, it is considered active. If it is active for less than 7.5% of that time, it is possibly inactive. If no activity is detected for 64ms (128ms, 256ms and 512ms also selectable for the idle threshold), then beep is considered inactive.

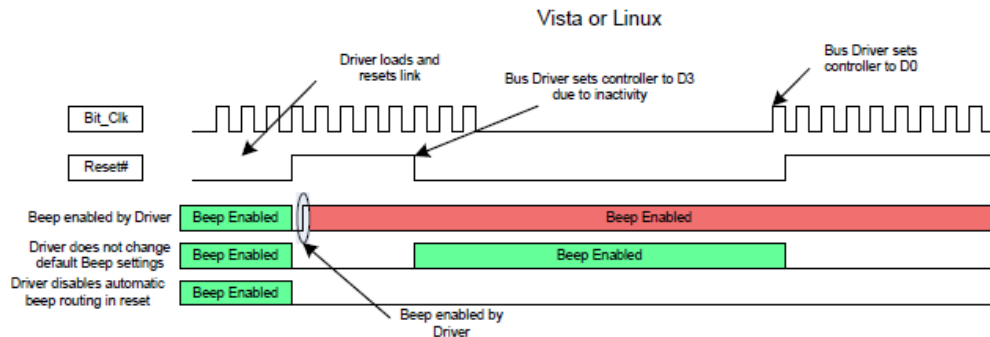


Figure 8. Analog PC Beep Active

Phase 1: analog beep auto-routing phase in the period after application of DVDD, before the first rising edge of link reset.

Once Analog PCbeep is detected(BEEP_PRESENCE=1) after 64ms delays (after POR (power on reset)), the Amplifier will be turned on(port_pwd=0, port_output_en=1, there is a timing between these two signals) and analog_beep_en=1. If BEEP_PRESENCE=0 for longer than the threshold time, the amplifiers will be turned off to save power and prevent unwanted system noise from being heard.

Phase 2: When not in phase 1

A. If analog beep function is disabled by driver.

Analog beep auto-detect will also be disabled.

B. If analog beep function is enabled by driver.

Once analog PCbeep is detected(BEEP_PRESENCE=1), analog pc_beep will be enabled

If in D0-D2, enabled simply means muting or un-muting beep to avoid hearing system noise on the beep input pin but it is acceptable to turn off port amplifiers if not currently used by DACs, mixer, or beep to save power.

If in D3, enabled means that the necessary amplifiers are turned on so that the beep signal may be heard on all ports configured as outputs (see analog pc-beep description section above)

All needed amplifiers are enabled until BEEP_PRESENCE=0 for longer than the idle threshold

A flow chart of Analog PC Beep is below.

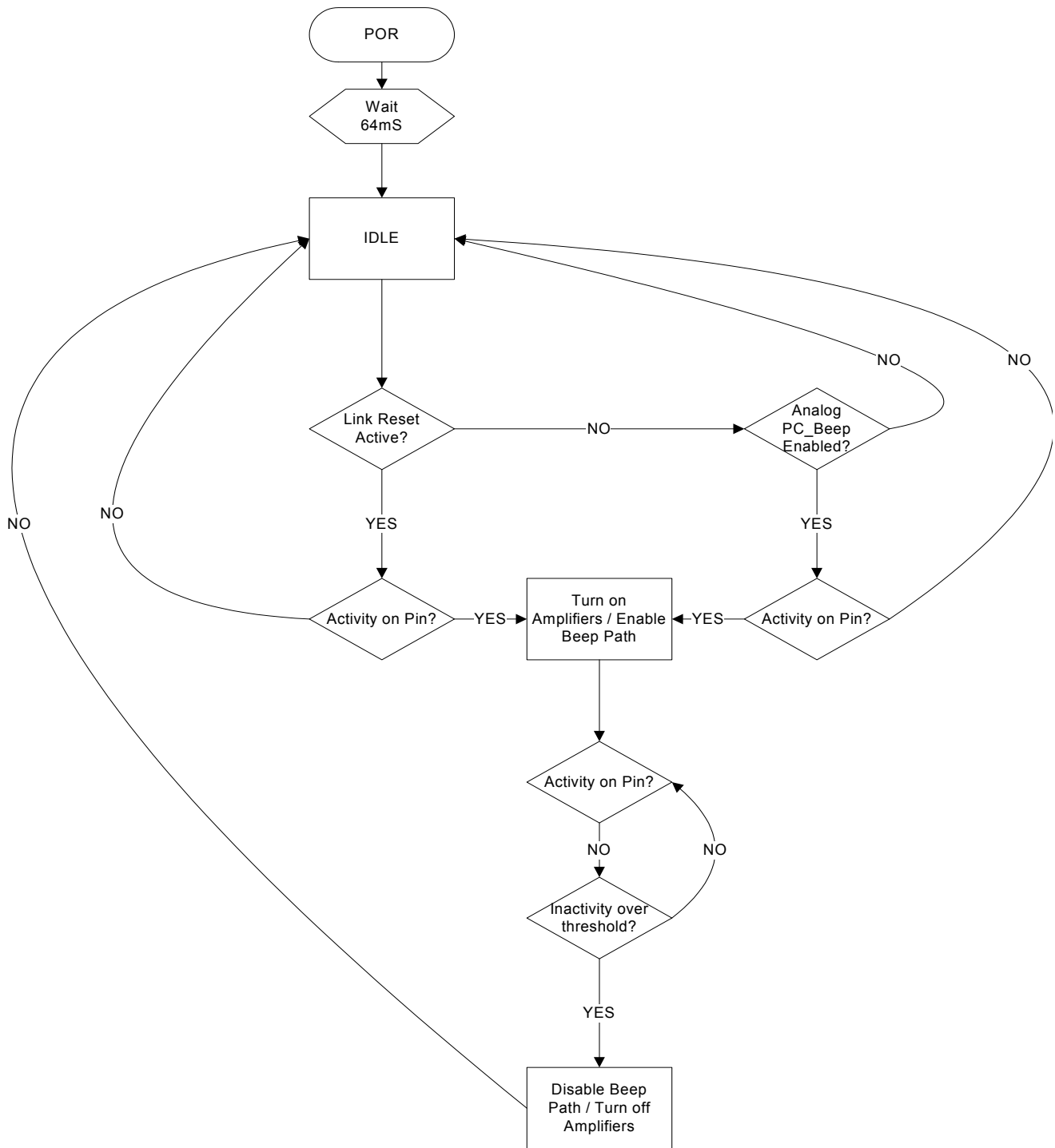


Figure 9. Analog PC Beep Flow chart

2.17. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz HD Audio Sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio

SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced. Digital PC_Beep requires a clock to operate and the CODEC will prevent the system from stopping the bus clock while in D3 by setting the Clock_Stop_OK bit to 0 to indicate that the part requires a clock.

2.18. Headphone Drivers

The codec implements both traditional and capless headphone outputs. The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) The codec does not support power limiting.

Headphone performance will degrade if more than one port is driving a 32 ohm load.

2.19. BTL Amplifier

An integrated class-D stereo BTL amplifier is provided to directly drive 4 ohm speakers (2W @ 4.75V) or 8 ohm speakers (1W @ 4.75V). No external filter is needed for cable runs of 18" or less. An internal DC blocking filter prevents distortion when the audio source has DC content, and prevents unintentional power consumption when pausing audio playback. The amplifier may be controlled using the EAPD pin (see EAPD section.)

Using a vendor specific verb, the BTL amplifier may be configured to support a mono speaker connected to the L +/- pins. In this mode, the Left and Right audio is mixed and sent to the left output only. The right channel is turned off to conserve power.

Maximum gain for the BTL amplifier is programmable. The following 4 gain settings relative to a nominal line output are desired: +6.5dB, +9.5dB, +14.5dB, +16.5dB. Absolute gain may vary and the suggested accuracy is +/-1.5dB.

This gain is exposed in a vendor specific widget and is intended to mimic the pin programmable gain implemented in discrete BTL amplifiers commonly used in notebook computers.

The BTL amplifier includes thermal management circuitry. When the CODEC reaches a temperature of about 140 degrees, the output amplitude of the BTL amp is gradually lowered until the temperature falls below 140. All other functions will remain active if the BTL amplifier is shut down due to die temperature.

2.20. BTL Amplifier High-Pass Filter

For mobile applications, speakers are often incapable of reproducing low frequency audio and unable to handle the maximum output power of the BTL amplifier. A high-pass filter is implemented in the BTL output path to reduce the amount of low frequency energy reaching speakers attached to the BTL amplifier. This can prevent speaker failure.

2.20.1. Filter Description

The high-pass filter is derived from the common biquadratic filter and provides a 12dB/octave roll-off. The filter may be programmed for a -3dB response at: 100Hz, 200Hz, 300Hz, 400Hz, 500Hz, 750Hz, 1KHz, or 2KHz. The high pass filter is enabled by default with a cut-off frequency of 300Hz. The filter may be bypassed using the associated verb (processing state verb).

The analog PC_Beep input is not affected by the digital high-pass filter. To ensure that the speakers attached to the BTL amplifier are not harmed by low frequency audio entering the PC_Beep input, an external filter must be implemented. Fortunately, it is common practice to implement an attenuation circuit and DC blocking capacitor at the PC_Beep input. This attenuator/filter is easily adjusted to restrict low frequency audio. The easiest approach is to reduce the value of the DC blocking capacitor but other approaches are equally effective.

2.21. EQ

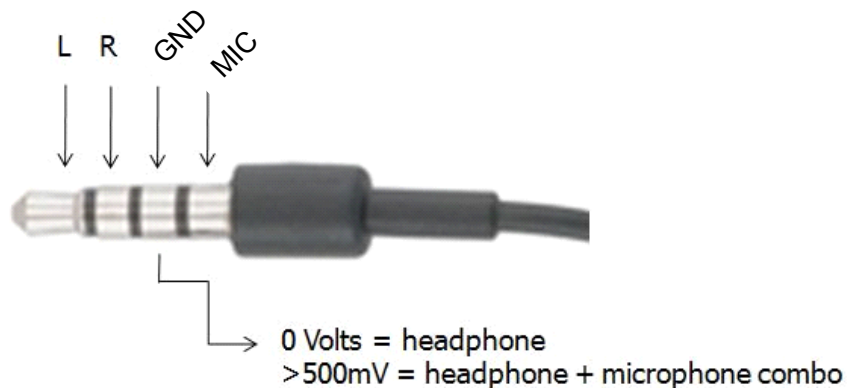
There are 5 bands of parametric EQ (bi-quad) per channel. Due to the flexibility of the bi-quad implementation, each filter band may be configured as a high-pass, low-pass, band-pass, high shelving, low shelving, or other function.

Each band has an independent set of coefficients. A bi-quad filter has 6 coefficients. One coefficient is normalized to 1 and 5 are programmed into the core. Each band supports up to +15dB boost or up to -36dB cut.

2.22. Combo Jack Detection

4 conductor (combo) jacks are becoming popular. In the most common implementation the 4 conductor plug has the same mechanical dimensions as a 3 conductor 3.5mm plug but the sleeve portion has been split into two segments: S1 and S2. When a 4-conductor plug (headset) is inserted into the jack T (Tip) = Left headphone audio, R (Ring) = Right headphone audio, S1 (First half of sleeve) = microphone input, and S2 (Second half of sleeve) = return (GND). When a 3-conductor plug (headphones) is inserted into the jack; T=Left audio, R=Right audio, S1=GND, S2=GND. By monitoring the S1 connection to see if it is shorted to ground, we can distinguish between headsets and headphones. Please note that analog microphone plugs (3-conductor-Lmic/Rmic/GND) and optical SPDIF plugs can not be supported using this implementation.

Figure 10. Combo Jack



Plug insertion is reported on the headphone port using the switch integrated into the jack.

The internal circuit monitors the voltage at the jack to determine if a low impedance load is present.

Detection of a microphone is not reported unless plug insertion is also detected.

2.23. GPIO

2.23.1. GPIO Pin mapping and shared functions

| GPIO # | Pin | Supply | SPDIF In | SPDIF Out | GPIO | GPI | GPO | VrefOut | DMIC | VOL | Pull Up | Pull Down |
|--------|-----|--------|----------|-----------|------|-----|-----|---------|------|-----|---------|-----------|
| 0 | 46 | DVDD | | YES | YES | | | | IN | | | 50K |
| 1 | 2 | DVDD | | | YES | | | | CLK | | | 50K |
| 2 | 4 | DVDD | | | YES | | | | IN | | | 50K |
| 3 | 48 | DVDD | | YES | YES | | | | | | | 50K |
| 4 | 24 | AVDD | | | YES | | | YES | | | | 50K |

2.23.2. SPDIF/Digital Microphone/GPIO Selection

3 functions are available on the DMIC_1/GPIO0/SPDIFOUT1 pin (pin 46). To determine which function is enabled, the order of precedence is followed:

1. If the GPIOs are enabled, they override both SPDIF_OUT and Digital Mics
2. If the GPIOs are not enabled through the AFG, then at reset, the pin is pulled low by an internal pull-down resistor.
3. If the port is enabled as an input, the digital microphones will be used.
4. If the port is enabled as an output, the SPDIF output will be used.
5. In the event that the port is enabled as an input and an output, the port will be an output and the Digital Mic path will be mute.

2.23.3. Digital Microphone/GPIO Selection

2 functions are available on the DMIC_CLK/GPIO1 (pin 2) and the DMIC_0/GPIO2 (pin 4) pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIOs are not enabled through the AFG, then at reset, pins 2 and 4 are pulled low by an internal pull-down resistor.
2. If the GPIO 1 is enabled, the 2 DMIC pins become mute (unless programmed for GPIO or SPDIF use) and pin 2 becomes GPIO with an internal pull-down.
3. If GPIO2 is enabled through the AFG, pin 4 becomes a GPIO and is pulled low by an internal pull-down resistor.
4. If the port is enabled as an input, the digital microphones will be used.
5. If the port is not enabled as an input or if the pin is configured as a GPIO, the digital microphone path will be mute.

2.24. HD Audio HDA015-B support

The codec provides complete support for the HDA015-B specification (now DCN) building on the support already present in previous products. HDA015-B features supported are:

1. Persistence of many configuration options through bus and function group reset.
2. The ability to support port presence detect in D3 even when the HD Audio bus is in a low power state (no clock.)

3. Fast resume times from low power states: 1ms D1 to D0, 2ms D2 to D0, 10mS D3 to D0.
4. Notification if persistent register settings have been unexpectedly reset.
5. SPDIF active in D3 (required)

2.25. Digital Core Voltage Regulator

The digital core operates from a 1.8V (10%) supply voltage. Many systems require that the CODEC use a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 9, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

The digital core voltage regulator is only dependent on DVDD. DVDDIO may be either 3.3 or 1.5V and may precede or follow DVDD in sequence. The CODEC digital logic and I/O (unless referenced to AVDD) will operate in the absence of AVDD. DVDD and AVDD supply sequencing for the application of power and the removal of power is neither defined nor guaranteed. It is common for desktop systems to supply AVDD from the system standby supply and the CODEC will tolerate, indefinitely, the condition where AVDD is active but DVDD and DVDDIO are inactive.

2.26. Digital Audio Port (I2S)

Digital Input and Output capability is provided on Port F and Port E..

2.26.1. Characteristics

I2S output is represented as an output port with a headphone output amplifier. I2S input is represented as an input port. To ensure compatibility with the Microsoft class driver, the port is described as an analog port and provides the same connectivity as a traditional analog port.

The I2S ports share common clocks. Therefore only one set of configuration controls are required. 2 stereo analog ports are replaced by the Data Input(I2S_DIN), Data output(I2S_DOUT), data clock(I2S_SCLK), and frame clock (I2S_LRCLK) signals.

Due to the requirement that input and output converters provide independent sample rates, sample rate conversion support is provided.

Multiple data formats are supported: Left justified, I2S native (Left justified with 1 clock delay), and Right justified modes. Data lengths of 16, 20 and 24 bits are supported. When there is a mismatch between the I2S configuration and the HD Audio link programming (converter widget word length) the word lengths will be aligned using zero padding or truncation as appropriate.

The CODEC may be the clock master or a slave to an external master for the shift clock (SCLK) and frame clock (LRCLK) signals.

Data shift clock is programmable with a default providing 64 Fs for 44.1KHz based rates and 84Fs for 48KHz based rates. A 64Fs shift clock is also available for 48KHz rates but the jitter performance will be much worse than 84Fs. By default, the shift clock will automatically adjust for sample rate. However, the shift clock may also be programmed to provide a constant output independent of the selected sample rate.

| SCLK[3:0] | Frequency (MHz) | PLL clock divisor | suggested sample rate ¹ | clocks/frame | Notes |
|-----------|-----------------|-------------------|------------------------------------|--------------|---|
| 0000 | Auto | Auto | All | 64 | SCLK is always 64Fs (48KHz based rates have jitter) |
| 0001 | 12.288 | 147/16 | 192KHz | 64 | High jitter (<5nS) |
| 0010 | 6.144 | 147/8 | 96KHz | 64 | High jitter (<5nS) |
| 0011 | 3.072 | 147/4 | 48KHz | 64 | High jitter (<5nS) |
| 0100 | 11.2896 | 10 | 88.2KHz | 128 | |
| 0101 | 5.6448 | 20 | 88.2KHz | 64 | |
| 0110 | 2.8224 | 40 | 44.1KHz | 64 | |
| 0111 | | | | | reserved |
| 1000 | Auto | Auto | All | 64/84 | SCLK adjusts for sample rate. 44.1KHz based rates are 64Fs and 48KHz based rates are 84Fs |
| 1001 | 16.128 | 7 | 192KHz | 84 | |
| 1010 | 8.064 | 14 | 96KHz | 84 | |
| 1011 | 4.032 | 28 | 48KHz | 84 | |

Table 18. SCLK Frequency Selection

| SCLK[3:0] | Frequency (MHz) | PLL clock divisor | suggested sample rate ¹ | clocks/frame | Notes |
|-----------|-----------------|-------------------|------------------------------------|--------------|----------|
| 1100 | 7.056 | 16 | 88.2KHz | 80 | |
| 1101 | 3.528 | 32 | 44.1KHz | 80 | |
| 1110 | 1.764 | 64 | 44.1KHz | 40 | |
| 1111 | | | | | reserved |

Table 18. SCLK Frequency Selection

1. In 'Auto' mode SCLK is referenced to the sample rate (SR[2:0] register bits) but in all other settings the SCLK rate is independent of the selected sample rate. Programming a sample rate that uses a different base rate from the suggested sample rate may cause corruption of the audio stream.

It is possible to invert all clocks (shift, master, and LR clocks) as well as the Port F data input and Port E data output.

The 92HD93 inverts the clocks and data by default.

Ports are enabled/disabled using the input / output enables defined in the pin widgets.

Aux Audio Mode will be supported and the CODEC will use the MCLK pin as an input in this mode. A 12MHz input will be accepted. (See the Aux Audio section for more information.)

In normal operation, the MCLK pin is an output by default but may be configured as an input. 8 clock frequencies are available: 22.5792MHz (512x 44.1K), 11.2896MHz (256x 44.1KHz), 5.6448MHz (128x 44.1KHz), 28.224MHz (640x 44.1KHz), 14.112MHz (320x 44.1KHz), 7.056MHz (160x 44.1KHz), 24MHz (500x 48KHz), and 12MHz (250x 48KHz - default)

| MCLK[2:0] | Frequency (MHz) | PLL clock divisor | suggested sample rate | Notes |
|-----------|-----------------|-------------------|-----------------------|-------------------|
| 000 | 24 | NA | 96KHz | HD Audio BitClk |
| 001 | 12 | NA | 48KHz | HD Audio BitClk/2 |
| 010 | 22.5792 | 5 | 88.2KHz | |
| 011 | 11.2896 | 10 | 44.1KHz | |
| 100 | 5.6448 | 20 | 44.1KHz | |
| 101 | 28.224 | 4 | 88.2/96KHz | |
| 110 | 14.112 | 8 | 88.2/48KHz | |
| 111 | 7.056 | 16 | 44.1KHz | |

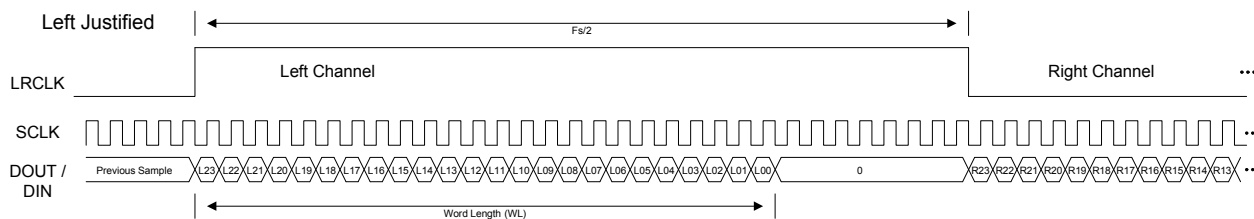
Table 19. MCLK Frequency Selection

A "bit exact mode" is provided. In this mode, the output path will not alter the data from the DAC converter widget (HD Audio stream data) sent to the I2S output port (Port E.) This means that there is no sample rate conversion, rounding, filtering or other processing that will change the sample value. Word length and sample rate are determined by the converter widget connected to the output port and not by the I2S rate and word length configuration bits. The input port (if used) will have its rate and word length converted to the requested rate of the ADC converter widget attached to the input port. The input path may be bit exact if the DAC and ADC converter widgets are programmed to the same rates and word lengths.

2.26.2. Left Justified Audio Interface

In Left Justified mode, the MSB is available on the first rising edge of SCLK following a LRCLK transition. The other bits are then transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present.

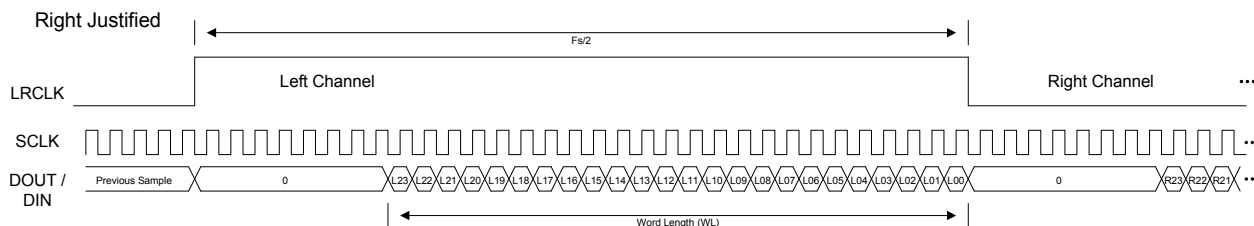
Figure 11. Left Justified Audio Interface (assuming 24-bit word length)



2.26.3. Right Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of SCLK before a LRCLK transition. All other bits are transmitted in order. The LRCLK signal is high when left channel data is present and low when right channel data is present.

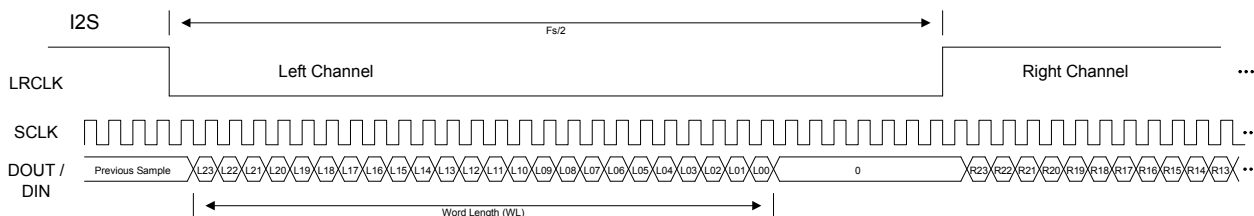
Figure 12. Right Justified Audio Interface (assuming 24-bit word length)



2.26.4. I²S Format Audio Interface

In I²S mode, the MSB is available on the second rising edge of SCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order.

Figure 13. I²S Justified Audio Interface (assuming 24-bit word length)



2.27. Microphone Mute Input

The 92HD93 supports a microphone mute input. An external switch or other circuit may directly mute the CODEC without relying on software control. This is a most helpful feature for allowing the

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end user to conveniently enforce privacy since it bypasses the record gain/mute functions typically controlled by software. While recording is muted, any active stream will receive digital silence.

2.28. Aux Audio Support

The CODEC supports an auxiliary audio mode where audio routing is supported by default after power is supplied with the HD Audio bus disabled. In this mode, an I2S input is routed to one of several output ports depending on jack presence detection, likewise several audio sources (analog, digital mic, I2S) are routed and converted to an I2S output.

In addition to shutting of the CODEC BTL and headphone amplifiers when the dock output jack is used, the BTL amplifier will be disabled when the headphone jacks are used, and the headphone amplifiers will be disabled when not in use.

2.28.1. General conditions in Aux Audio Mode:

HD Audio Link is off (RST# is 0, active, and BitClk is 0, inactive. CODEC does not need to monitor BitClk to enter/exit this mode but must not depend on BitClk to operate.) (Part will enter Aux Audio Mode immediately on application of power if Aux Audio Mode is enabled as default.)

OR

HD Audio CODEC function group power state is set to D3cold and Aux Audio Mode is enabled. (Device enters immediately on transition to D3cold and remains in Aux mode until a double AFG reset event is received or until the next rising edge of RST#)

- HD Audio CODEC analog and digital supplies are active.
- Port A connects to the system microphone jack.
- Port B connects to the system headphone jack.
- Port C is not used
- Port D connects to the internal speakers.
- Port E is connected to the dock Line Out jack/AUX Audio out (it is an output port)
- Port F is connected to the dock Mic Input jack/AUX Audio In (it is an input port)
- The digital microphone clock is generated by the CODEC. The DMIC data is converted to PCM and sent to the Aux Audio Module through the Aux Out port.
- The System microphone jack (Port A) is available to the auxiliary audio subsystem. Vref_Out will be enabled when the system Mic is plugged in.
- EAPD is used to control the power state of the mixer, BTL amplifier, and headphone amplifiers. The amplifiers are off if EAPD is held low.
- Internal circuitry will delay enabling (change power state, un-mute, etc.) the output amplifiers a sufficient amount of time after the application of power or EAPD=1 to prevent pops.
- Internal circuitry will orchestrate power down (EAPD = 0) to prevent pops.
- EAPD must be forced low before removing power.
- No special Dock signal present for the CODEC. Only port presence detect for the dock Line Out (port E) and MinIN (Port F) are used.
- ECR15b operation does not presents a problem. The CODEC will not enter Aux Audio mode unless the function group power state is set to D3cold prior to putting the HD Audio interface into reset (controller D3.)To prevent undesirable behavior (pops, etc.) the bus must not be placed into reset with the clock stopped unless EAPD is forced low or D3cold has been set. The Enable bit in the Aux Audio vendor specific verb is provided so firmware or other software can disable Aux Audio support. The default value of this bit is determined by a bond option and may be determined by reading the device ID. This bit only returns to its default value when a power on reset event is generated or when programmed to that value by software.

2.28.2. Entering Aux Audio Mode

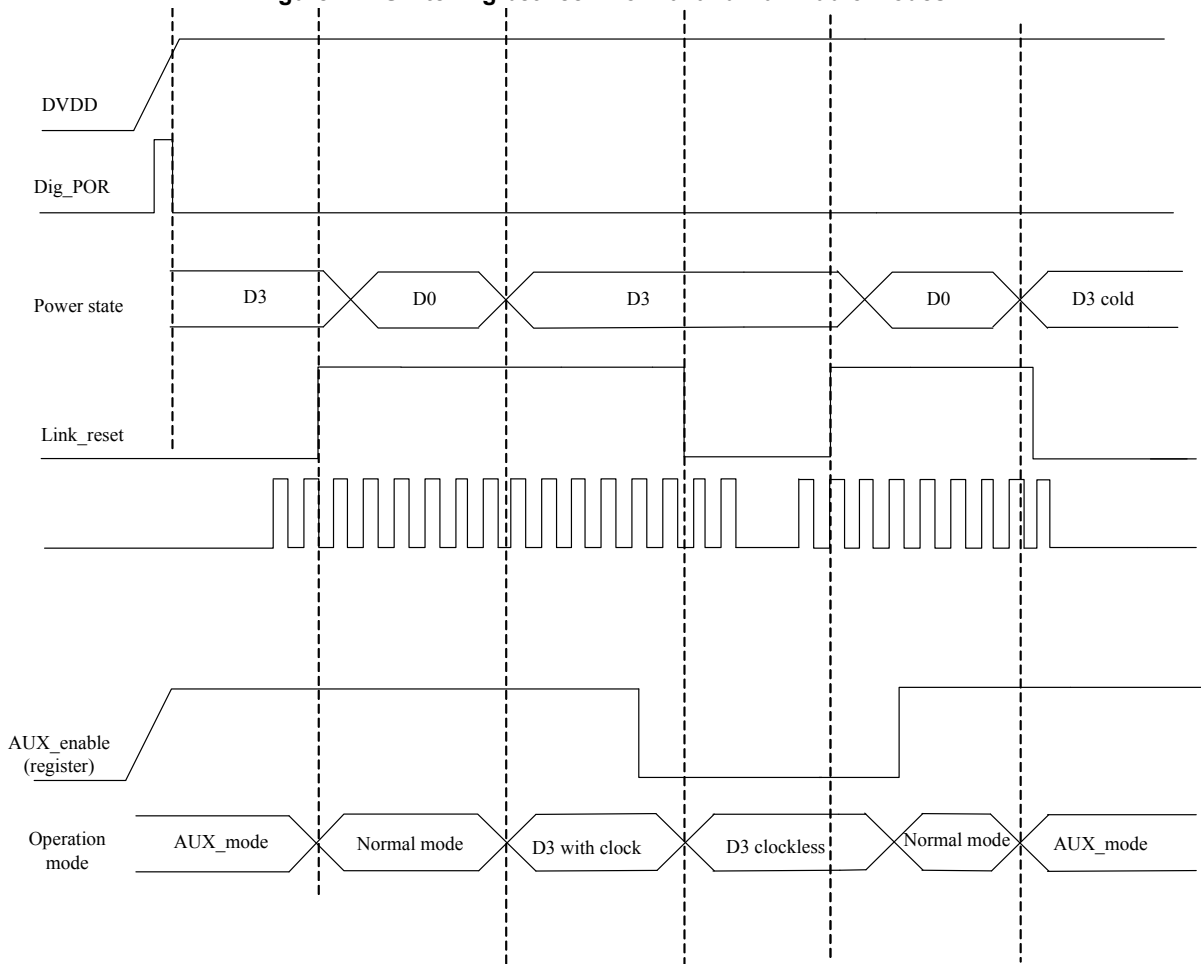
Enter AUX mode under two conditions, refer to figure below:

- When DVDD is powered-up, the value of AUX_enable register is “enabled” (one), and before link reset is de-asserted (pull high).
- If AUX_enable is “enabled” (one) and the Power state is D3cold then chip will also enter AUX mode but the Clock_Stop_OK flag is not required (set to 1 if convenient.). (Note that the part will enter Aux mode immediately upon transition to D3cold. It is possible to return to normal operation by issuing a double AFG reset if the link is still active.)

Note: At that time, Force Portsense and BTL Amp on when we enter link reset if the AuxAudio bit is set. If the AuxAudio bit is not set (by bond option or software) then we will not enter Aux Audio Mode-Portsense and BTL Amp will remain off.

Port F (“dock microphone”) input is routed to Port D (“internal speakers”), Ports B (system head-phone port), and Port E (“dock Line Out”) directly. The analog mixer is disabled to reduce power consumption.

Figure 14. Switching between Normal and Aux Audio Modes



2.28.3. Firmware/Software Requirements:

The reconfiguration outlined in this chapter will be enabled by default (without the help of firmware or OS driver.)

If it is desirable to stop the HD Audio bus while the CODEC is in D3 under OS control per ECR-15b, no action is required. The CODEC will not enter Aux Audio Mode unless placed in D3cold.

2.28.4. *Part Options Supporting I²S I/O*

Ports E and F are implemented using an I²S digital interface. The SPDIF pins (pins 46 and 48) are used to connect to an external Aux Audio Module. The CODEC is a LR_CLK and S_CLK clock slave to the external module, if present, and is the timing master in normal mode. The CODEC is an MCLK slave by default in both Aux Audio and Normal modes.

The internal routing of the playback and record paths are functionally similar to an analog implementation but must be processed differently because the audio data is now digital. In addition, the PC_Beep pin is replaced by a secondary I2S data input that is used in both Aux Audio and normal modes of operation. The following diagrams illustrate.

2.28.5. *“Playback Path” Port Behavior (Digital I/O)*

Input from the Aux Audio Module (Aux_In) is routed to Port D (“internal speakers”), Port B (system headphone port), and Port E (“dock Line Out”) directly. The Secondary Audio input is mixed with the Aux_In input.

2.28.6. *When Port E presence detect = 0*

- Presence detect for Port E = 0 (nothing plugged in)
- Aux_In, the “Aux Audio Playback”, input is mixed with the Secondary Audio input and routed to Port B, or Port D when that port is active.
- If Port B is in use (port presence detect = 1), Port D, internal speakers, will be inactive (off) and Port E, the dock headphone, will be mute.
- The power supply (charge pump) for B will be inactive if B is not in use.
- If Port B is not in use (port presence detect = 0), Port D, internal speakers, will be active and port B will be inactive.
- EAPD must not be forced low due to the dock being absent or high when a dock is present. EAPD is used to indicate if AUX Audio Mode is in use.

2.28.7. *When Port E presence detect = 1*

- Presence detect for Port E = 1 (something plugged in)
- Port D is disabled
- If Port B is in use (port presence detect = 1), that port will be enabled and output the audio entering Aux_In mixed with the audio on the Secondary Audio input.
- The power supply for port B will be active if port B is in use.
- If Port B is not in use (port presence detect = 0), port B will be inactive and the audio on Aux_In will be mixed with the audio from the Secondary Audio input and routed to Port E, the dock headphone jack.
- EAPD must not be forced low due to the dock being absent or high when a dock is present. EAPD is used to indicate if AUX Audio Mode is in use.

| EAPD (pin) | Aux Support Enable ¹ | Port E detect | Port B detect | Port A, C, F, DMIC detect | Port D behavior | Port B behavior | Port E behavior |
|------------|---------------------------------|---------------|---------------|---------------------------|--------------------------|--------------------------|--------------------------|
| 0 | NA | NA | NA | NA | disabled | disabled | disabled (mute) |
| 1 | 0 | NA | NA | NA | Widget controlled | Widget controlled | Widget controlled |
| 1 | 1 | 0 | 0 | NA | enabled Aux+Secondary | disabled | disabled (mute) |
| 1 | 1 | 0 | 1 | NA | disabled | enabled Aux+Secondary | disabled (mute) |
| 1 | 1 | 1 | 0 | NA | disabled | disabled | enabled Aux+Secondary |
| 1 | 1 | 1 | 1 | NA | disabled | enabled Aux+Secondary | disabled (mute) |

1.default value for Aux Audio Enable is determined by bond option.

2.28.8. "Record Path" Port Behavior (Digital I/O)

Digital Microphone input DMIC0 is used as an internal microphone port in normal mode. The Digital Microphone clock pin is enabled in Aux Audio Mode and the digital microphone clock is provided by an internal oscillator. The data on the DMIC0 pin is converted to PCM data and sent to the Auxiliary Audio Module.

If Port F and Port A presence detect = 0, this indicates that nothing is plugged into the dock or system and the digital microphone input is sent to the Auxiliary Audio Module. If Port A presence detect = 1, this indicates that an external microphone is plugged into the system jack and port A is converted to PCM data and sent to the Auxiliary Audio Module through the Aux_Out pin. If Port F presence detect = 1 (and Port A presence detect = 0), this indicates that an external microphone is plugged into the dock. The PCM data from Port F will be routed to the Auxiliary Audio Module through the Aux_Out pin.

As in normal mode, the boost and record gain functions are available in Aux Audio Mode for Port A and DMIC0.

| EAPD (pin) | Aux Support Enable ¹ | D Mic0 detect | Port A detect | Port F detect | Ports B, C, E detect | Port E behavior |
|------------|---------------------------------|---------------|---------------|---------------|----------------------|--|
| 0 | X | X | X | X | NA | disabled |
| 1 | 0 | X | X | X | NA | Widget controlled |
| 1 | 1 | 0 | 0 | 0 | NA | Mute |
| 1 | 1 | 1 | 0 | 0 | NA | DMIC converted to analog and routed to module through port E. DMIC Clock provided by CODEC |
| 1 | 1 | X | 0 | 1 | NA | Dock Mic routed to module (not through CODEC) CODEC DMIC interface and Port A disabled |

1.default value for Aux Audio Enable is determined by bond option.

2.28.9. *EAPD*

Since the Aux Audio mode overrides the default behavior but not the actual port settings when in reset, the logical state of the EAPD pin must be overridden as well. When Aux Audio mode is enabled and the part is in reset as described above, the logical state of EAPD will be 1 (External Amplifier Powered Up) unless held low by an external circuit. This ensures that audio pass-thru and analog PC_Beep will be supported.

2.28.10. *Class-D BTL Issues*

While in Aux Audio mode the HD Audio bus clock (BitClk) is not available. The Class-D controller requires a very high speed clock to operate and an internal clock must be provided. In Aux Audio mode, the actual frequency used by the Class-D controller and its associated ADC will not be exact since an external reference will not be available. The performance characteristics in Aux Audio Mode will be degraded compared to the normal operating mode characteristics specified elsewhere in this document.

2.28.11. *Firmware/Software Requirements:*

The reconfiguration outlined in this chapter is autonomous (without the help of firmware or OS driver.)

This autonomous mode does not interfere with normal operation.

If it is desirable to stop the HD Audio bus while the CODEC is in D3 under OS control per DCN HDA015-B, no action is required. The CODEC will not enter Aux Audio Mode unless placed in D3cold.

2.28.12. SYSTEM DIAGRAMS

Figure 15. Playback Path on Parts Supporting Digital I/O

Aux Audio Mode

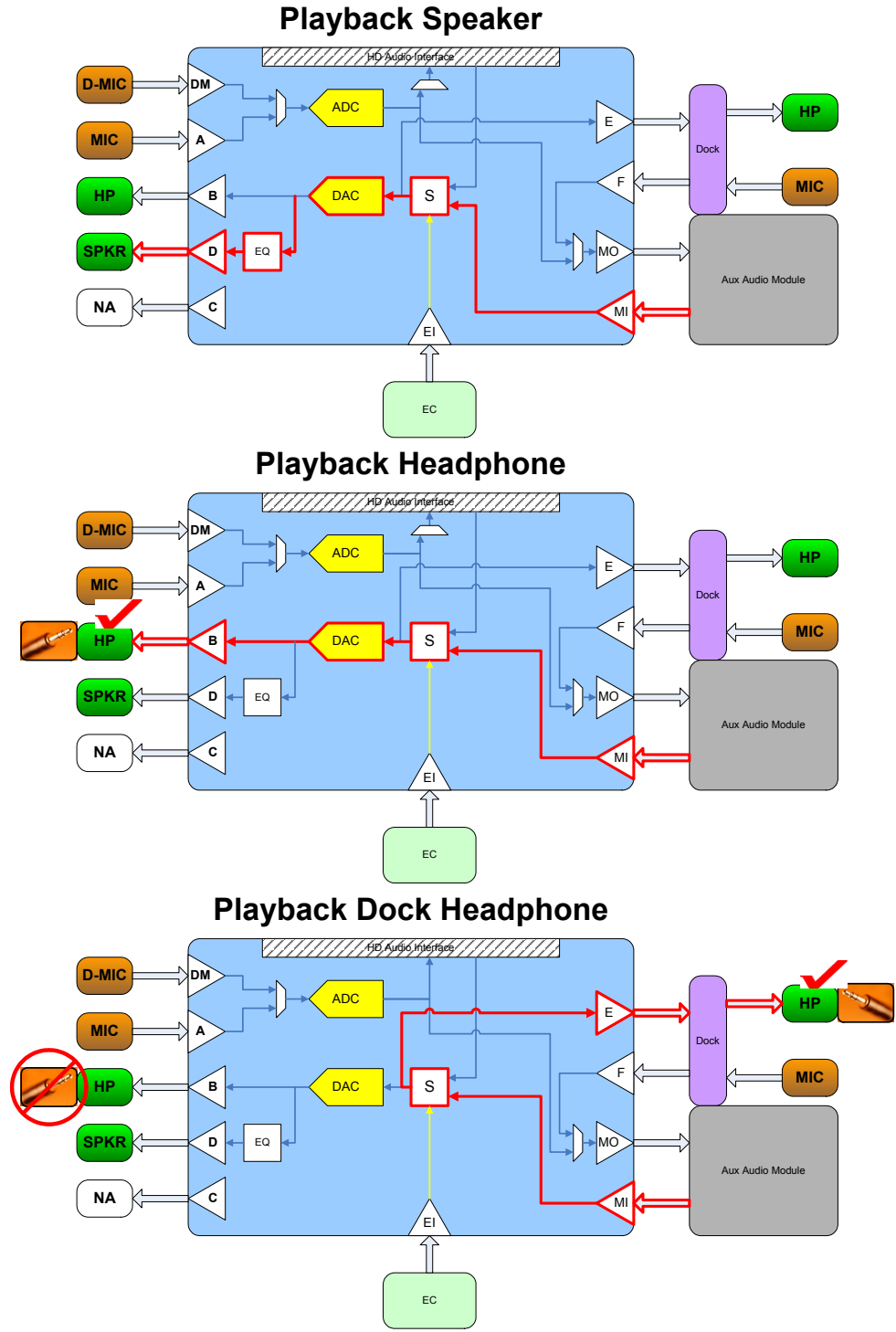
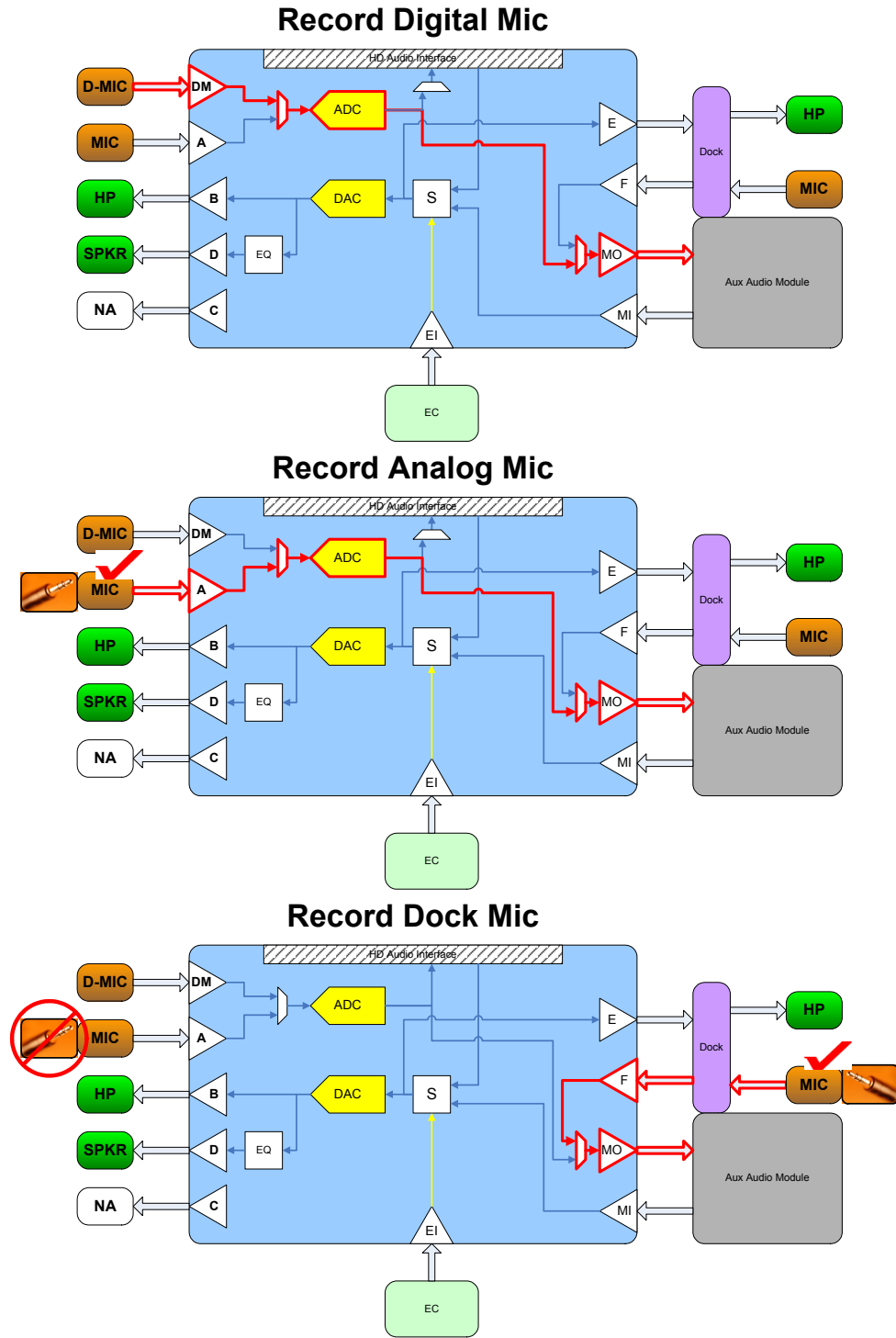


Figure 16. Record Path on Parts Supporting Digital I/O

Aux Audio Mode



2.28.13. I2C control interface

The CODEC supports I2S I/O also supports a 2-wire (I2C and SMBUS compatible) 8-bit slave interface for control while in Aux Audio Mode. The interface supports up to 400KHz operation.

The following must be controlled while in Aux Audio Mode:

6. EQ programming
7. BTL amplifier high-pass filter programming
8. Mono Out path band-pass filter programming
9. BTL amplifier gain
10. Port A mic boost and ADC record gain
11. Dmic0 boost and ADC record gain

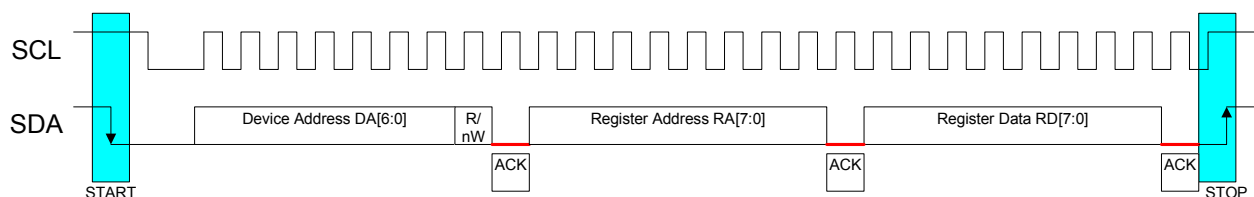
2.28.14. Register Write Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDA (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the codec and the R/W bit is '0', indicating a write, then the codec responds by pulling SDA low on the next clock pulse (ACK); otherwise, the codec returns to the idle condition to wait for a new start condition and valid address.

Once the CODEC has acknowledged a correct address, the controller sends the register address. the codec acknowledges the register address by pulling SDA low for one clock pulse. The controller then sends the 8 bits of register data and the codec acknowledges again by pulling SDA low.

When there is a low to high transition on SDA while SCL is high, the transfer is complete. After receiving a complete address and data sequence the CODEC returns to the idle state. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

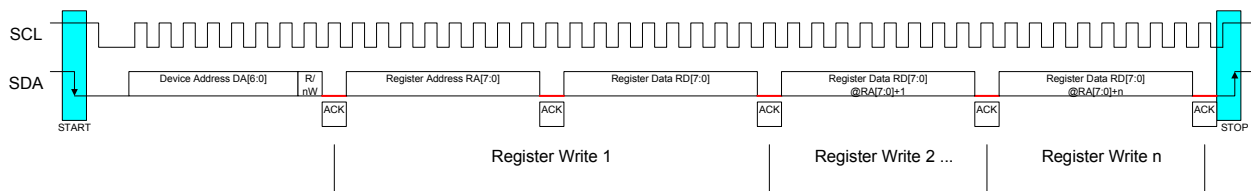
Figure 17. 2-Wire Serial Control Interface



2.28.15. Multiple Write Cycle

The controller may write more than one register within a single write cycle. To write additional registers, the controller will not generate a stop or start (repeated start) command after receiving the acknowledge for the data payload. Instead the controller will repeat sending 8-bit data payloads. The register address will increment automatically after receiving each 8-bit payload.

Figure 18. Multiple Write Cycle



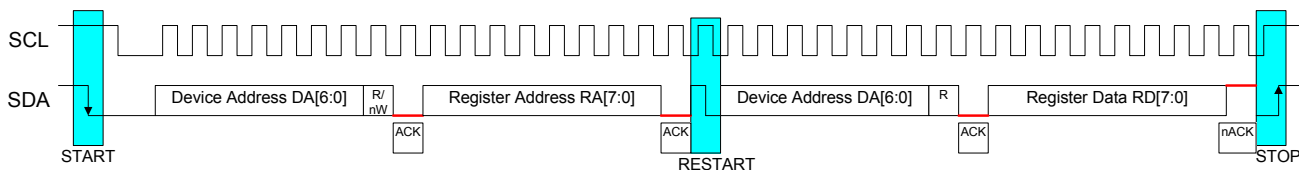
2.29. Register Read Cycle

The controller indicates the start of data transfer with a high to low transition on SDA while SCL remains high, signalling that a device address and data will follow. If the device address received matches the address of the codec and the R/W bit is '0', indicating a write, then the codec responds by pulling SDA low on the next clock pulse (ACK); otherwise, the codec returns to the idle condition to wait for a new start condition and valid address.

Once the codec has acknowledged a correct address, the controller sends a restart command (high to low transition on SDA while SCL remains high). The controller then re-sends the devices address with the R/W bit set to '1' to indicate a read cycle. The codec acknowledges by pulling SDA low for one clock pulse. The controller then receives a byte of register data and the controller acknowledges by pulling SDA low.

When there is a not acknowledge from the controller and a low to high transition on SDA while SCL is high, the transfer is complete. If a start or stop condition is detected out of sequence, the device returns to the idle condition.

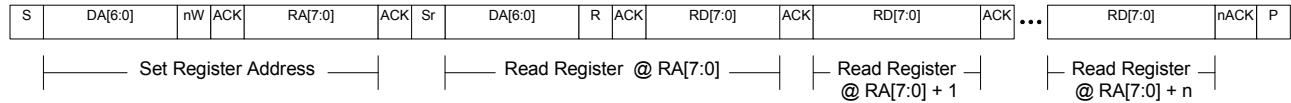
Figure 19. Read Cycle



2.29.1. Multiple Read Cycle

The controller may read more than one register within a single read cycle. To read additional registers, the controller will not generate a stop or start (repeated start) command after sending the acknowledge for the second byte of data. Instead the controller will continue to provide clocks and acknowledge after each byte of transmitted data. The codec will automatically increment the internal register address after each register has had its data successfully read (ACK from host) but will not increment the register address if the data is not received correctly by the host (nACK from host) or if the bus cycle is terminated unexpectedly (however the EQ/Filter address will be incremented even if the register address is not incremented when performing EQ/Filter RAM reads).

Figure 20. Multiple Read Cycle



2.29.2. I2C Registers

The CODEC that supports I2S I/O also supports a 2-wire (I2C and SMBUS compatible) interface for control while in Aux Audio Mode. The interface supports up to 400KHz operation. All registers (except for the reset register) are available when in normal mode through the HD Audio interface. Most are implemented using vendor defined verbs but some (volume controls specifically) are supported through standard verbs at the pin widgets.

| Register | Name | Remarks | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | Default |
|----------|---------|-------------------|--|-------------|--------|--------|-----------------|--------------------|--------------------|--------------|---------------|
| R0(00h) | RSVD | Reserved | | | | | | | | | |
| R1(01h) | SPKVOLL | SPKR Left volume | SPKVOL_L[7:0] | | | | | | | | 30h |
| R2(02h) | SPKVOLR | SPKR Right volume | SPKVOL_R[7:0] | | | | | | | | 30h |
| R3(03h) | RSVD | Reserved | | | | | | | | | |
| R4(04h) | RSVD | Reserved | | | | | | | | | |
| R5(05h) | RSVD | Reserved | | | | | | | | | |
| R6(06h) | AIC1 | Audio Interface 1 | SCLKIN V | MS | LRSWAP | LRP | WL[1:0] | | FORMAT[1:0] | | 4Ah |
| R7(07h) | AIC2 | Audio Interface 2 | TRI | SCLK[3:0] | | | | SR[2:0] | | | 04h |
| R8(08h) | AIC3 | Audio Interface 3 | | | | | MCLKMS | MCLK[2:0] | | | 09h |
| R9(09h) | PWRM | Pwr Mgmt | | | | HPPWD | SPKRPWD | DMICPWD | MCLKout | AUXEn | 03h |
| R10(0Ah) | | | | | | | | | | | |
| R11(0Bh) | | | | | | | | | | | |
| R12(0Ch) | | | | | | | | | | | |
| R13(0Dh) | | | | | | | | | | | |
| R14(0Eh) | | | | | | | | | | | |
| R15(0Fh) | RESET | Reset | writing to this register resets all registers to their default state | | | | | | | | 00h not reset |
| R16(10h) | STATUS | BTL status | limit1latch | limit0latch | | | | limit1 | limit0 | zerodet_flag | 00h |
| R17(11h) | INIT | | | | | | anabee_p_dc_byp | anabee_p_dc_coeff1 | anabee_p_dc_coeff0 | initialize | 04h |
| R18(12h) | CONFIG1 | CONFIG1 | BPF BYP | PRE BYP | EQBYP | | | | | HPF BYP | 60h |

Table 20. I2C Registers

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| Register | Name | Remarks | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | Default |
|----------|------|--------------------------|-----------------------|----------------------|---------------|-----------------------|----------------------|---------------|---------------|---------------|---------|
| R19(13h) | PWM4 | | sc_status_clear_right | sc_status_clear_left | RSVD | sc_Fault_status_right | sc_Fault_status_left | scdly_sel1 | scdly_sel0 | evenbit | 00h |
| R20(14h) | PWM3 | | outctrl1 | outctrl0 | cvalue5 | cvalue4 | cvalue3 | cvalue2 | cvalue1 | cvalue0 | 02h |
| R21(15h) | PWM2 | | dvalue5 | dvalue4 | dvalue3 | dvalue2 | dvalue1 | dvalue0 | pwm_outflip | pwm_outmode | 41h |
| R22(16h) | PWM1 | | | ditherpos4 | ditherpos3 | ditherpos2 | ditherpos1 | ditherpos0 | dither_range | dithclr | 00h |
| R23(17h) | PWM0 | | ph_offset1 | ph_offset0 | clk320mode | roundup | bfclr | fourthorder | add3_sel | Btl_test_mode | 70h |
| R24(18h) | | LMTCTRL | | | | | LZCEN | Limitstep1 | Limitstep0 | Limiter_en | 00h |
| R25(19h) | | LMTATKTIME | ATK10m | LMTAT6 | LMTAT5 | LMTAT4 | LMTAT3 | LMTAT2 | LMTAT1 | LMTAT0 | 00h |
| R26(1Ah) | | LMTHOLDTIME | HOLD10m | LMTHT6 | LMTHT5 | LMTHT4 | LMTHT3 | LMTHT2 | LMTHT1 | LMTHT0 | 00h |
| R27(1Bh) | | LMTRELTIME | REL10m | LMTRT6 | LMTRT5 | LMTRT4 | LMTRT3 | LMTRT2 | LMTRT1 | LMTRT0 | 00h |
| R28(1Ch) | | LMTATKTH_HI | LATKTH15 | LATKTH14 | LATKTH13 | LATKTH12 | LATKTH11 | LATKTH10 | LATKTH9 | LATKTH8 | 7Fh |
| R29(1Dh) | | LMTATKTH_LO | LATKTH7 | LATKTH6 | LATKTH5 | LATKTH4 | LATKTH3 | LATKTH2 | LATKTH1 | LATKTH0 | FFh |
| R30(1Eh) | | LMTRELTH_HI | LRELTH15 | LRELTH14 | LRELTH13 | LRELTH12 | LRELTH11 | LRELTH10 | LRELTH9 | LRELTH8 | 00h |
| R31(1Fh) | | LMTRELTH_LO | LRELTH7 | LRELTH6 | LRELTH5 | LRELTH4 | LRELTH3 | LRELTH2 | LRELTH1 | LRELTH0 | 00h |
| R32(20h) | | GAINCTRL_HI | | | | zerodet1en1 | zerodet1en0 | step_time2 | step_time1 | step_time0 | 15h |
| R33(21h) | | GAINCTRL_LO | clr_latch | | step_10ms | stepped_change | disable_gain | auto_mute | change_mode | mute_mode | 05h |
| R34(22h) | | MUTE | | | | | | Mute | mute1 | mute0 | 00h |
| R35(23h) | | ATTEN | atten7 | atten6 | atten5 | atten4 | atten3 | atten2 | atten1 | atten0 | 00h |
| R36(24h) | | DC_COEF_SEL | | | | | | dc_coef_sel2 | dc_coef_sel1 | dc_coef_sel0 | 05h |
| R37(25h) | | HPF_COEF_SEL | | | | | | hp_coef_sel2 | hp_coef_sel1 | hp_coef_sel0 | 02h |
| R38(26h) | | BPF_COEF_SEL | | bph_coef_sel2 | bph_coef_sel1 | bph_coef_sel0 | | bpl_coef_sel2 | bpl_coef_sel1 | bpl_coef_sel0 | 32h |
| R39(27h) | | PWR Stage Test Left | Enable | TRC_ESD | STRENDRV | SCTHR_1 | SCTHR_0 | DEADTIME2 | DEADTIME1 | DEADTIME0 | 89h |
| R40(28h) | | Short Circuit Test Left | TEST_EN | SC_DIS | | FAULT_SC | | PNSEL | Force_SC | TEST | 00h |
| R41(29h) | | PWR Stage Test Right | Enable | TRC_ESD | STRENDRV | SCTHR_1 | SCTHR_0 | DEADTIME2 | DEADTIME1 | DEADTIME0 | 89h |
| R42(2Ah) | | Short Circuit Test Right | TEST_EN | SC_DIS | | FAULT_SC | | PNSEL | Force_SC | TEST | 00h |

Table 20. I2C Registers

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Register | Name | Remarks | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | Default |
|----------|--------|----------------------|--------------|--------------|------------|------------|------------|----------------------|---------------------------|---------------------------|---------|
| R43(2Bh) | | LDO LEVEL CONTROL | | | | | | Lv_QU AD_BIA S | Lv_reg_ cntrl_bit 1 | Lv_reg_ cntrl_bit 0 | 00h |
| R44(2Ch) | | | | | | | | | | | |
| R45(2Dh) | | | | | | | | | | | |
| R46(2Eh) | | | | | | | | | | | |
| R47(2Fh) | | | | | | | | | | | |
| R48(30h) | | EQRAM_READ[47:40] | EQRD4 7 | EQRD4 6 | EQRD4 5 | EQRD4 4 | EQRD4 3 | EQRD4 2 | EQRD4 1 | EQRD4 0 | 00h |
| R49(31h) | | EQRAM_READ[39:32] | EQRD3 9 | EQRD3 8 | EQRD3 7 | EQRD3 6 | EQRD3 5 | EQRD3 4 | EQRD3 3 | EQRD3 2 | 00h |
| R50(32h) | | EQRAM_READ[31:24] | EQRD3 1 | EQRD3 0 | EQRD2 9 | EQRD2 8 | EQRD2 7 | EQRD2 6 | EQRD2 5 | EQRD2 4 | 00h |
| R51(33h) | | EQRAM_READ[23:16] | EQRD2 3 | EQRD2 2 | EQRD2 1 | EQRD2 0 | EQRD1 9 | EQRD1 8 | EQRD1 7 | EQRD1 6 | 00h |
| R52(34h) | | EQRAM_READ[15:08] | EQRD1 5 | EQRD1 4 | EQRD1 3 | EQRD1 2 | EQRD1 1 | EQRD1 0 | EQRD0 9 | EQRD0 8 | 00h |
| R53(35h) | | EQRAM_READ[07:00] | EQRD0 7 | EQRD0 6 | EQRD0 5 | EQRD0 4 | EQRD0 3 | EQRD0 2 | EQRD0 1 | EQRD0 0 | 00h |
| R54(36h) | | EQRAM_WRITE[47:40] | EQWD4 7 | EQWD4 6 | EQWD4 5 | EQWD4 4 | EQWD4 3 | EQWD4 2 | EQWD4 1 | EQWD4 0 | 00h |
| R55(37h) | | EQRAM_WRITE[39:32] | EQWD3 9 | EQWD3 8 | EQWD3 7 | EQWD3 6 | EQWD3 5 | EQWD3 4 | EQWD3 3 | EQWD3 2 | 00h |
| R56(38h) | | EQRAM_WRITE[31:24] | EQWD3 1 | EQWD3 0 | EQWD2 9 | EQWD2 8 | EQWD2 7 | EQWD2 6 | EQWD2 5 | EQWD2 4 | 00h |
| R57(39h) | | EQRAM_WRITE[23:16] | EQWD2 3 | EQWD2 2 | EQWD2 1 | EQWD2 0 | EQWD1 9 | EQWD1 8 | EQWD1 7 | EQWD1 6 | 00h |
| R58(3Ah) | | EQRAM_WRITE[15:08] | EQWD1 5 | EQWD1 4 | EQWD1 3 | EQWD1 2 | EQWD1 1 | EQWD1 0 | EQWD0 9 | EQWD0 8 | 00h |
| R59(3Bh) | | EQRAM_WRITE[07:00] | EQWD0 7 | EQWD0 6 | EQWD0 5 | EQWD0 4 | EQWD0 3 | EQWD0 2 | EQWD0 1 | EQWD0 0 | 00h |
| R60(3Ch) | EQADDR | EQ_ADDR | | | EQADD 5 | EQADD 4 | EQADD 3 | EQADD 2 | EQADD 1 | EQADD 0 | 00h |
| R61(3Dh) | EQCTRL | EQRAM_CTRL | EQRAM _WR | EQRAM _RD | | | | | | | 00h |
| R62(3Eh) | | Reserved | | | | | | | | | |
| R63(3Fh) | DEVADR | I2C Device Address | ADDR7 | ADDR6 | ADDR5 | ADDR4 | ADDR3 | ADDR2 | ADDR1 | NA(R/W) | E2h |
| R64(40h) | | PortAPinWCntrlVRefEn | | | | | | VRef2 | VRef1 | VRef0 | 00h |
| R65(41h) | | PortAlnAmpLeftGain | | | | | | | AlnGain L1 | AlnGain L0 | 00h |
| R66(42h) | | PortAlnAmpRightGain | | | | | | | AlnGain R1 | AlnGain R0 | 00h |

Table 20. I2C Registers

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Register | Name | Remarks | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | Default |
|----------|------|-----------------------|------------|--------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---------|
| R67(43h) | | DMic0InAmpLeftGain | | | | | | | DMIC0 InGainL 1 | DMIC0 InGainL 0 | 00h |
| R68(44h) | | DMic0InAmpRightGain | | | | | | | DMIC0 InGainR 1 | DMIC0 InGainR 0 | 00h |
| R69(45h) | | ADCMuxOutAmpLeftGain | AMux MuteL | | AMux OutGain L5 | AMux OutGain L4 | AMux OutGain L3 | AMux OutGain L2 | AMux OutGain L1 | AMux OutGain L0 | 90h |
| R70(46h) | | ADCMuxOutAmpRightGain | AMux MuteR | | AMux OutGain R5 | AMux OutGain R4 | AMux OutGain R3 | AMux OutGain R2 | AMux OutGain R1 | AMux OutGain R0 | 90h |

Table 20. I2C Registers

Notes:

1 Registers not described in this map should be considered "reserved".

2.29.2.1. SPKVOL L/R Registers

Speaker (BTL) volume adjustment in Aux Audio Mode (Port D).

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|----------|------|---------|---|
| 0x01 / 0x02 verb F71/771 (Left) verb F72/772 (Right) verb 773 (Left and Right - write only) | 7:0 | VOL[7:0] | RW | 30 | +36 to -91.5dB in 0.75dB steps 0x00 = +36dB 0x01 = +35.25dB ... 0x2F = +0.75dB 0x30 = 0dB 0x31 = -0.75dB ... 0xA9 = -90.75 0xAA to 0xFE = -91.5dB 0xFF = mute |

Note: The speaker volume control is intended to be the same volume control as implemented in non Aux Audio mode but is controlled through the I2C interface rather than the HD Audio Bus.

2.29.2.2. AIC1 Register

Audio Interface (I2S) control in Aux Audio Mode

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|-------------|------|---------|--|
| 0x06 verb F76/776 | 7 | SCLKINV | RW | 0 | 0 =SCLK not inverted (data and LRCLK transition on falling edge of SCLK) 1 = invert SCLK (data and LRCLK transition on rising edge of SCLK) |
| | 6 | MS | RW | 1 | Master/Slave 0 = SCLK and LRCLK are inputs (slave mode) 1 = SCLK and LRCLK are outputs (master mode) |
| | 5 | LRSWAP | RW | 0 | Swap Left and Right Samples 0 = Left sample first in frame 1 = Right sample first in frame |
| | 4 | LRP | RW | 0 | Left/Right (I2S_LRCLK) Polarity 0 = default per format 1 = LRCLK inverted |
| | 3:2 | WL[1:0] | RW | 10 | Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = Reserved |
| | 1:0 | FORMAT[1:0] | RW | 10 | link format 00 = Right Justified 01 = Left Justified 10 = I2S 11 = reserved |

Note: The audio interface control is intended to be the same as implemented in non Aux Audio mode but is controlled through the I2C interface rather than the HD Audio Bus.

2.29.2.3. AIC2 Register

Audio Interface (I2S) control in Aux Audio Mode

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|-----------|------|---------|--|
| 0x07 verb F77/777 | 7 | TRI | RW | 0 | TRI=1 & MS = 0 (Slave mode) I2S_DOUT is hi-z (I2S_SCLK and I2S_LRCLK are inputs) TRI=1 & MS = 1(Master mode) I2S_DOUT, I2S_SCLK, and I2S_LRCLK are hi-z |
| | 6:3 | SCLK[3:0] | RW | 0000 | SCLK rate See table below |
| | 2:0 | SR[2:0] | RW | 100 | Sample Rate 000 = 44.1KHz 001 = 88.2KHz 010= Reserved 011 = Reserved 100 = 48KHz 101 = 96KHz 110 = 192KHz 111 = Reserved |

Note: The audio interface control is intended to be the same as implemented in non Aux Audio mode but is controlled through the I2C interface rather than the HD Audio Bus.

| SCLK[3:0] | Frequency (MHz) | PLL clock divisor | suggested sample rate | clocks/frame | Notes |
|-----------|-----------------|-------------------|-----------------------|--------------|---|
| 0000 | Auto | Auto | All | 64 | SCLK is always 64Fs (48KHz based rates have jitter) |
| 0001 | 12.288 | 147/16 | 192KHz | 64 | High jitter (<5nS) |
| 0010 | 6.144 | 147/32 | 96KHz | 64 | High jitter (<5nS) |
| 0011 | 3.072 | 147/64 | 48KHz | 64 | High jitter (<5nS) |
| 0100 | 11.2896 | 10 | 88.2KHz | 128 | |
| 0101 | 5.6448 | 20 | 88.2KHz | 64 | |
| 0110 | 2.8224 | 40 | 44.1KHz | 64 | |
| 0111 | | | | | reserved |
| 1000 | Auto | Auto | All | 64/84 | SCLK adjusts for sample rate. 44.1KHz based rates are 64Fs and 48KHz based rates are 84Fs |
| 1001 | 16.128 | 7 | 192KHz | 84 | |
| 1010 | 8.064 | 14 | 96KHz | 84 | |
| 1011 | 4.032 | 28 | 48KHz | 84 | |
| 1100 | 7.056 | 16 | 88.2KHz | 80 | |
| 1101 | 3.528 | 32 | 44.1KHz | 80 | |
| 1110 | 1.764 | 64 | 44.1KHz | 40 | |
| 1111 | | | | | reserved |

2.29.2.4. AIC3 Register

Audio Interface (I2S) control in Aux Audio Mode.

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|-----------|------|---------|---|
| 0x08 verb F78/778 | 7:6 | RSVD | RO | 00 | Reserved |
| | 5 | SAEN | RW | 0 | 1 = Input enabled for I2S Secondary Audio 0 = Input disabled for Secondary Audio |
| | 4 | AUXSWAP | RW | 0 | Swap Left and Right Samples of Aux Audio Output. 0 = Left sample first in frame 1 = Right sample first in frame |
| | 3 | MCLKMS | RW | 1 | MCLK master 0 = MCLK is an input 1 = MCLK is an output (not recommended in Aux Audio Mode since 24/12MHz rates cant be supported and 112MHz internal clock is imprecise but is useful for testing.) |
| | 2:0 | MCLK[2:0] | RW | 001 | MCLK rate 000 = 24MHz (HDA BitClk) 001 = 12MHz (HDA BitClk/2) 010 = 22.5792MHz 011 = 11.2896MHZ 100 = 5.6448MHZ 101 = 28.224MHz 110 = 14.112MHz 111 = 7.056MHz |

Note: The audio interface control is intended to be the same as implemented in non Aux Audio mode but is controlled through the I2C interface rather than the HD Audio Bus.

2.29.2.5. PWRM Register

Power management in Aux Audio Mode

92HD92

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|---------|------|---------|---|
| 0x09 verb F79/779 | 7 | RSVD | RO | 0 | Reserved |
| | 6 | RSVD | RO | 0 | Reserved |
| | 5 | RSVD | RO | 0 | Reserved |
| | 4 | HPPWD | RW | 0 | Headphone ports are forced off in Aux Audio Mode (including charge pump) |
| | 3 | SPKRON | RW | 0 | BTL (port D) is forced on in Aux Audio Mode |
| | 2 | DMICPWD | RW | 0 | DMIC powered down in Aux Audio Mode (including DAC) |
| | 1 | MCLKOut | RW | 1 | MCLK Output Enabler 0 = MCLK Output is disabled in master mode 1 = MCLK is an output in master mode (input in slave mode)) |
| | 0 | AUXEn | RW | 1* | 1 = Aux Audio Mode Enabled (on parts supporting Aux Audio Mode and will override HD Audio power state control to enable needed paths.) 0 = Aux Audio Mode disabled (power state controlled by HD Audio rules/controls only.) |

Note: The audio interface control is intended to be the same as implemented in non Aux Audio mode but is controlled through the I2C interface rather than the HD Audio Bus.

2.29.2.6. RESET Register

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------|-----|-------|------|---------|--|
| 0x0F RESET verb F7F/77F | 7:0 | RESET | RW | 0 | Writing causes registers to revert to their default values (similar to a function group reset) |

2.29.2.7. STATUS Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------|-----|--------------|------|---------|---|
| 0x10 STATUS verb F80/780 | 7 | limit1latch | RO | 0 | Latched version of limit1, clear via GAINCTRL_LO[7] |
| | 6 | limit0latch | RO | 0 | Latched version of limit0, clear via GAINCTRL_LO[7] |
| | 5:3 | Reserved | RO | 0x0 | RESERVED |
| | 2 | limit1 | RO | 0 | Set (1) if regz saturation after gain multiply for CH1. may change on a sample by sample basis. |
| | 1 | limit0 | RO | 0 | Set (1) if regz saturation after gain multiply for CH0. may change on a sample by sample basis. |
| | 0 | zerodet_flag | RO | 0 | Set when input zero detect of long string of zeroes. |

2.29.2.8. *INIT Register*

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|---------------------------------|-----|----------------------|------|---------|--|
| 0x11 CONFIG1 verb F81/781 | 7:4 | Reserved | RO | 0 | RESERVED |
| | 3 | anabeep_dcbyp | RW | 0 | 1 = bypass analog Beep DC filter |
| | 2:1 | anabeep_dc_coef f | RW | 0x2 | 0: dc_coef = 24'h004000; 1: dc_coef = 24'h001000; 2: dc_coef = 24'h000400; 3: dc_coef = 24'h000100; |
| | 0 | Initialize | RW | 0 | 1= Initialize/soft reset data path. Must be set when changing the config0 or config1 registers. |

2.29.2.9. *CONFIG Register*

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------|-----|-----------|------|---------|--|
| 0x12 CONFIG verb F82/782 | 7 | BPFBYB | RW | 0 | 1= Bypass MonoOut band-pass filter |
| | 6 | PREBYB | RW | 1 | 1= Bypass BTL EQ filter prescale |
| | 5 | EQBYB | RW | 1 | 1= Bypass BTL EQ filter |
| | 4 | BTL_dcbyp | RW | 0 | 1 = bypass BTL DC filter |
| | 3:1 | Reserved | RO | 0 | RESERVED |
| | 0 | HPFBYP | RW | 0 | 1= Bypass BTL high-pass filter (not DC removal filter) |

2.29.2.10. *PWM4 Register*

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|-----------------------|------|---------|---|
| 0x13 PWM4 verb F83/783 | 7 | sc_status_clear_right | RWC | 0 | Write once operation will clear sc_fault_status_right |
| | 6 | sc_status_clear_left | RWC | 0 | Write once operation will clear sc_fault_status_left |
| | 5 | Reserved | RO | 0 | RESERVED |
| | 4 | sc_Fault_status_right | RO | 0 | 1 = Fault occurs on right channel |
| | 3 | sc_Fault_status_left | RO | 0 | 1 = Fault occurs on left channel |
| | 2:1 | scdly_set | RW | 00 | Used for short circuit detection; designer will set the value |
| | 0 | evenbit | RW | 0 | 1=Noise Shaper output data are even |

2.29.2.11. PWM3 Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|---------|------|---------|---|
| 0x14 PWM3 verb F84/784 | 7:6 | outctrl | RW | 0 | pwm output muxing 0 = normal 1 = swap 0/1 2 = ch0 on both 3 = ch1 on both |
| | 5:0 | cvalue | RW | 0x2 | Tristate constant value filed, must be even and not 0 |

2.29.2.12. PWM2 Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|-------------|------|---------|--|
| 0x15 PWM2 verb F85/785 | 7:2 | dvalue | RW | 0x10 | dvalue constant field. |
| | 1 | pwm_outflip | RW | 0 | 1= swap pwm a/b output pair for all channels |
| | 0 | pwm_outmode | RW | 1 | 1= tristate, 0 = binary |

2.29.2.13. PWM1 Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|--------------|------|---------|---|
| 0x16 PWM1 verb F86/786 | 7 | Reserved | RO | 0 | RESERVED |
| | 6:2 | dithpos | RW | 0 | Dither position, where dither inserted after NS 0,1,2 = dither bits 2:0 4 = dither bits 3:1 5 = dither bits 4:1 ... 19 = dither bits 19:17 |
| | 1 | dither_range | RW | 0 | 1= dither -1 to +1, 0 = dither -3 to +3 |
| | 0 | dithclr | RW | 0 | 1 = disable dither |

2.29.2.14. PWM0 Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|---------------|------|---------|---|
| 0x17 PWM0 verb F87/787 | 7:6 | PhaseOffset | RW | 01 | PWM ch1 offset from ch0 at 8x sample rate by: 00 = 0 degrees 01 = 90 degrees 10 = 180 degrees 11 = NA |
| | 5 | clk320mode | R | 1 | 1 = PCA clock 320 mode 0 = PCA clock 294 mode |
| | 4 | roundup | RW | 1 | 1= roundup, 0 = truncate for quantizer |
| | 3 | bfclr | RW | 0 | 1 = disable binomial filter |
| | 2 | fourthorder | RW | 0 | 1 = fourth order binomial filter, 0 = 3rd order binomial filter |
| | 1 | add3_sel | RW | 0 | 1 = 24-bit Noise Shaper output (pre-quantizer), 0 = 8/9/10-bit quantizer output |
| | 0 | Btl_test_mode | RW | 0 | 1 = power stage test mode |

2.29.2.15. LMTCTRL Register

Control operation of the volume Limiter (Compressor).

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|------------|------|---------|---|
| 0x18 verb F88/788 | 7:4 | – | RO | 0 | Reserved for future use. |
| | 3 | zerocross | RW | 0 | 1 = only change limiter gain value on zero cross. |
| | 2:1 | stepsize | RW | 0 | Gain stepsize when incrementing or decrementing: 0 - 0.75 dB, 1 - 1.5 dB, 2 - 3.0 dB, 3 - 6.0 dB |
| | 0 | limiter_en | RW | 0 | 1 = enable limiter (compressor) |

2.29.2.16. LMTATKTIME (0x19), LMTHOLDTIME (0x1A), LMTRELTIME (0x1B) Registers

These 8-bit registers set the timer values between incrementing/decrementing the Compressor attenuation values. There is one register each for Attack, Hold, and Release times, the configuration parameters are the same for all three and are shown in the table below.

These registers reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------------|-----|------------|------|---------|--|
| 0x19 LMTATKTIME verb F89/789 | 7 | ATK10ms | RW | 0 | 1 = value in bits 6:0 is in 10ms units, otherwise 1ms units. |
| | 6:0 | LMTAT[6:0] | RW | 0 | Timer value in units of 1 or 10ms. |

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|-----------|------|---------|--|
| 0x1A LMTHOLDTIME verb F8A/78A | 7 | HOLD10ms | RW | 0 | 1 = value in bits 6:0 is in 10ms units, otherwise 1ms units. |
| | 6:0 | LMHT[6:0] | RW | 0 | Timer value in units of 1 or 10ms. |

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------------|-----|------------|------|---------|--|
| 0x1B LMTATKTIME verb F8B/78B | 7 | REL10ms | RW | 0 | 1 = value in bits 6:0 is in 10ms units, otherwise 1ms units. |
| | 6:0 | LMTRT[6:0] | RW | 0 | Timer value in units of 1 or 10ms. |

2.29.2.17. LMTATKTH (0x1D–LO, 0x1C–HI), LMTRELTH (0x1F–LO, 0x1E–HI) Registers

These 16-bit registers set the threshold values. When in attack phase and the Attack Threshold is exceeded the Compressor attenuation is incremented by stepsize (see LMTCTRL). When in release phase and the Release Threshold is not exceeded the Compressor attenuation is incremented by stepsize (but not above 0)

These registers reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|--------------|------|---------|--|
| 0x1C LMTATKTH_HI verb F8C/78C | 7:0 | LATKTH[15:8] | RW | 7F | 8'hFF would equal threshold level of +2.0dB. Each step below this 8-bit full scale value reduces threshold level by 0.0078 dB. |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|-------------|------|---------|---|
| 0x1D LMTATKTH_LO verb F8D/78D | 7:0 | LATKTH[7:0] | RW | FF | Always 0. It isn't necessary to provide threshold resolution to the point where these lower 8 bits would be used. |

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------------|-----|--------------|------|---------|--|
| 0x1E LMTARELTH_HI verb F8E/78E | 7:0 | LRELTH[15:8] | RW | 0 | 8'hFF would equal threshold level of +2.0dB. Each step below this 8-bit full scale value reduces threshold level by 0.0078 dB. |

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|-------------|------|---------|---|
| 0x1F LMTRELTH_LO verb F8F/78F | 7:0 | LRELTH[7:0] | RW | 0 | Always 0. It isn't necessary to provide threshold resolution to the point where these lower 8 bits would be used. |

2.29.2.18. GAINCTRL_HI Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|------------|------|---------|---|
| 0x20 GAINCTRL_HI verb F90/790 | 7:5 | Reserved | RO | 0 | RESERVED |
| | 4:3 | zerodetlen | RW | 0x2 | enable mute if input consecutive zeros exceeds this length: 00 = 32 01 = 1000 10 = 2000 11 = 4000 |
| | 2:0 | step_time | RW | 0x5 | step time units = 1<<step_time, units in GAINCTRL_LO bit 5 |

2.29.2.19. GAINCTRL_LO Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|----------------|------|---------|---|
| 0x21 GAINCTRL_LO verb F91/791 | 7 | clr_latch | RW | 0 | 1 = clear limit 0/1 latches, see STATUS register |
| | 6 | RSVD | RO | 0 | Reserved |
| | 5 | step_10ms | RW | 0 | 1 = units for step_time are 10ms 0 = units for step_time are 1ms |
| | 4 | stepped_change | RW | 0 | 1 = step volume progressively to new setting |
| | 3 | disable_gain | RW | 0 | 1 = disable all gain functions (bypass gain multiply) |
| | 2 | auto_mute | RW | 1 | 1 = auto mute if detect long strings of zeros on input |
| | 1 | change_mode | RW | 0 | 1 = change gain immediately 0 = change on zero cross |
| | 0 | mute_mode | RW | 1 | 1 = hard mute after reset, 0 = soft mute |

2.29.2.20. MUTE Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|------------------------------|-----|----------|------|---------|-----------------------|
| 0x22 MUTE verb F92/792 | 7:3 | Reserved | RO | 0x0 | RESERVED |
| | 2 | Mute | RW | 0 | 1 = mute all channels |
| | 1 | mute1 | RW | 0 | 1 = mute ch1 |
| | 0 | mute0 | RW | 0 | 1 = mute ch0 |

2.29.2.21. ATTEN Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------|-----|-------|------|---------|--|
| 0x23 ATTEN verb F93/793 | 7:0 | atten | RW | 0x0 | Attenuation. Each bit represents 0.5dB of attenuation to be applied to the channel. The range will be -125dB to 2dB as follows: 0x00: +2dB 0x01: +1.5dB 0x02: +1.0dB ... 0x47: -33.5dB 0x48: -34.0dB 0x49: -34.5dB ... 0xFE: -125dB 0xFF: Hard Master Mute |

2.29.2.22. DC_COEF_SEL Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-------------------------------------|-----|-------------|------|---------|---|
| 0x24 DC_COEF_SEL verb F94/794 | 7:3 | Reserved | RO | 0 | RESERVED |
| | 2:0 | dc_coef_sel | RW | 0x5 | 0:dc_coef = 24'h100000; //2 ⁻³ = 0.125 1:dc_coef = 24'h040000; 2:dc_coef = 24'h010000; 3:dc_coef = 24'h004000; 4:dc_coef = 24'h001000; 5:dc_coef = 24'h000400; 6:dc_coef = 24'h000100; //2 ⁻¹⁵ = 0.000330517 7:dc_coef = 24'h000040; //2 ⁻¹⁷ |

2.29.2.23. BTL High-Pass Filter COEF_SEL Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------------|-----|-------------|------|---------|--|
| 0x25 HPF_COEF_SEL verb F95/795 | 7:3 | Reserved | RO | 0 | RESERVED |
| | 2:0 | hp_coef_sel | RW | 0x2 | Select IIR coefficients for BTL amplifier high pass filter corner frequency 000 = 100Hz 001 = 200Hz 010 = 300Hz 011 = 400Hz 100 = 500Hz 101 = 750Hz 110 = 1000Hz 111 = 2000Hz |

2.29.2.24. Mono Band-Pass Filter COEF_SEL Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------------|-----|--------------|------|---------|--|
| 0x26 BPF_COEF_SEL verb F96/796 | 7 | Reserved | RO | 0 | RESERVED |
| | 6:4 | bph_coef_sel | RW | 0x3 | Select IIR coefficients for MonoOut band-pass filter lower corner frequency 000 = 63Hz 001 = 80Hz 010 = 100Hz 011 = 120Hz 100 = 150Hz 101 = 200Hz 110 = 315Hz 111 = 400Hz |
| | 3 | Reserved | RO | 0 | RESERVED |
| | 2:0 | bpl_coef_sel | RW | 0x2 | Select IIR coefficients for MonoOut band-pass filter upper corner frequency 000 = 150Hz 001 = 200Hz 010 = 250Hz 011 = 315Hz 100 = 400Hz 101 = 500Hz 110 = 630Hz 111 = 800Hz |

2.29.2.25. PortA PinWCntrlVRefEn Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|----------------------|-----|-------|------|---------|--|
| 0x40 PortA_VrefEn | 7:3 | RSVD | RO | 00000 | RESERVED |
| | 2:0 | Vref | RW | 000 | Vref selection for Port A. See VrefCntrl field of PinCap parameter for supported selections 000 = Hi-Z 001 = 50% 010 = GND 011 = Reserved 100 = 80% 101 = 100% 110 = Reserved 111 = Reserved |

2.29.2.26. PortA InAmpLeftGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|---------------------|-----|----------|------|---------|---|
| 0x41 PortA_GainL | 7:2 | RSVD | RO | 000000 | RESERVED |
| | 1:0 | AlnGainL | RW | 00 | Input gain step number for Port A. See InAmpCap parameter pertaining to this widget |

2.29.2.27. PortA InAmpRightGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|---------------------|-----|----------|------|---------|---|
| 0x42 PortA_GainR | 7:2 | RSVD | RO | 000000 | RESERVED |
| | 1:0 | AlnGainR | RW | 00 | Input gain step number for Port A. See InAmpCap parameter pertaining to this widget |

2.29.2.28. DMic0 InAmpLeftGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|---------------------|-----|--------------|------|---------|--|
| 0x43 DMic0_GainL | 7:2 | RSVD | RO | 000000 | RESERVED |
| | 1:0 | DMIC0InGainL | RW | 00 | Input gain step number for DMic0. See InAmpCap parameter pertaining to this widget |

2.29.2.29. DMIC0 InAmpRightGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|---------------------|-----|--------------|------|---------|--|
| 0x44 DMic0_GainR | 7:2 | RSVD | RO | 000000 | RESERVED |
| | 1:0 | DMIC0InGainR | RW | 00 | Input gain step number for DMic0. See InAmpCap parameter pertaining to this widget |

2.29.2.30. ADC0Mux OutAmpLeftGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-----------------------|-----|--------------|------|---------|--|
| 0x45 ADC0Mux_GainL | 7 | AMuxMuteL | RW | 1 | Amp Mute: 1=muted, 0=not muted |
| | 6 | RSVD | RO | 0 | RESERVED |
| | 5:0 | AMuxOutGainL | RW | 010000 | Output gain step number for ADC0Mux. See OutAmpCap parameter pertaining to this widget |

2.29.2.31. ADC0Mux OutAmpRightGain Register

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset

| Register Address | Bit | Label | Type | Default | Description |
|-----------------------|-----|--------------|------|---------|--|
| 0x46 ADC0Mux_GainR | 7 | AMuxMuteR | RW | 1 | Amp Mute: 1=muted, 0=not muted |
| | 6 | RSVD | RO | 0 | RESERVED |
| | 5:0 | AMuxOutGainR | RW | 010000 | Output gain step number for ADC0Mux. See OutAmpCap parameter pertaining to this widget |

2.29.2.32. BTL Class-D Power Stage Register Settings

This register reset by POR/DAFG/ULR.

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|----------|------|---------|---|
| 0x27 TEST and CONTROL Left verb F97/797 | 7 | ENABLE | RW | 1 | 1 = Enable BTL Power stage |
| | 6 | TRC_ESD | RO | 0 | 1 = ESD trigger detected 0 = No trigger |
| | 5 | STRENDRV | RW | 0 | 1 = Strengthen pre-drive 0 = Normal |
| | 4:3 | SCTHR | RW | 01 | Short circuit threshold current 00 = 10% of PVDD 01 = 14% of PVDD 10 = 16% of PVDD 11 = 20% of PVDD |
| | 2:0 | DEADTIME | RW | 001 | Dead time for output FETs 000 = 0.5ns 001 = 1.0ns 010 = 1.5ns 011 = 2ns 100 = 4ns 101 = 8ns 110 = 8ns 111 = 8ns |

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|----------|------|---------|--|
| 0x28 Short Circuit Left verb F98/798 | 7 | TEST_EN | RW | 0 | 1 = Enable short circuit test |
| | 6 | SC_DIS | RW | 0 | 1 = disable short circuit protection |
| | 5 | RSVD | RW | 0 | Reserved |
| | 4 | FAULT_SC | RO | 0 | 1 = Fault |
| | 3 | RSVD | RW | 0 | Reserved |
| | 2 | PNSEL | RW | 0 | 1=PFET tested, 0=NFET tested |
| | 1 | FORCE_SC | RW | 0 | 1 = force short circuit |
| | 0 | TEST | RW | 0 | 1 = Pos PFET / Neg NFET on, 0 = Pos NFET / Neg PFET on |

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| Register Address | Bit | Label | Type | Default | Description |
|---|-----|----------|------|---------|---|
| 0x29 TEST and CONTROL Right verb F99/799 | 7 | ENABLE | RW | 1 | 1 = Enable BTL Power stage |
| | 6 | TRC_ESD | RO | 0 | 1 = ESD trigger detected 0 = No trigger |
| | 5 | STRENDRV | RW | 0 | 1 = Strengthen pre-drive 0 = Normal |
| | 4:3 | SCTHR | RW | 01 | Short circuit threshold current 00 = 10% of PVDD 01 = 14% of PVDD 10 = 16% of PVDD 11 = 20% of PVDD |
| | 2:0 | DEADTIME | RW | 001 | Dead time for output FETs 000 = 0.5ns 001 = 1.0ns 010 = 1.5ns 011 = 2ns 100 = 4ns 101 = 8ns 110 = 8ns 111 = 8ns |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|----------|------|---------|--|
| 0x2A Short Circuit Right verb F9A/79A | 7 | TEST_EN | RW | 0 | 1 = Enable short circuit test |
| | 6 | SC_DIS | RW | 0 | 1 = disable short circuit protection |
| | 5 | RSVD | RW | 0 | Reserved |
| | 4 | FAULT_SC | RO | 0 | 1 = Fault |
| | 3 | RSVD | RW | 0 | Reserved |
| | 2 | PNSEL | RW | 0 | 1=PFET tested, 0=NFET tested |
| | 1 | FORCE_SC | RW | 0 | 1 = force short circuit |
| | 0 | TEST | RW | 0 | 1 = Pos PFET / Neg NFET on, 0 = Pos NFET / Neg PFET on |

2.29.2.33. LDO LEVEL CONTROL Register

This register reset by POR/DAFG/ULR

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|------------------|------|---------|---|
| 0x2B LDO LEVEL CONTROL verb F9B/79B | 7:3 | Reserved | RO | 0x0 | RESERVED |
| | 2 | Lv_QUAD_BIAS | RW | 0 | |
| | 1:0 | Lv_reg_cntrl_bit | RW | 0x0 | Two bits are defined to program the output of the 1.8V LDO 00 = normal operation (3.3V in to 1.8V out) 01 = 1.8V*1.1 = 1.98V 10 = 1.8V*0.9 = 1.62V 11 = power down LDO/bypass. When disabled, the DVDD_Core pin must be supplied with a nominal 1.8V from an external source. |

2.29.2.34. EQRAM

The EQ RAM is a 52 x 48-bit SRAM that contains the EQ coefficients.

This register reset by POR/DAFG/ULR OR when a BIST is run under certain conditions, contact IDT for more information. Writing to NID22h verb 77F will cause NOT generate a reset.

| Address | Channel RIGHT Coefficients (24bit) | Channel LEFT Coefficients (24bit) |
|------------|------------------------------------|-----------------------------------|
| EQRAM Bits | [47:24] | [23:00] |
| | based on 44.1Khz sample rate | |
| 0x00 | EQ_COEF_F0_B0 | EQ_COEF_F0_B0 |
| 0x01 | EQ_COEF_F0_B1 | EQ_COEF_F0_B1 |
| 0x02 | EQ_COEF_F0_B2 | EQ_COEF_F0_B2 |
| 0x03 | EQ_COEF_F0_A1 | EQ_COEF_F0_A1 |
| 0x04 | EQ_COEF_F0_A2 | EQ_COEF_F0_A2 |
| 0x05 | EQ_COEF_F1_B0 | EQ_COEF_F1_B0 |
| 0x06 | EQ_COEF_F1_B1 | EQ_COEF_F1_B1 |
| 0x07 | EQ_COEF_F1_B2 | EQ_COEF_F1_B2 |
| 0x08 | EQ_COEF_F1_A1 | EQ_COEF_F1_A1 |
| 0x09 | EQ_COEF_F1_A2 | EQ_COEF_F1_A2 |
| 0x0A | EQ_COEF_F2_B0 | EQ_COEF_F2_B0 |
| 0x0B | EQ_COEF_F2_B1 | EQ_COEF_F2_B1 |
| 0x0C | EQ_COEF_F2_B2 | EQ_COEF_F2_B2 |
| 0x0D | EQ_COEF_F2_A1 | EQ_COEF_F2_A1 |
| 0x0E | EQ_COEF_F2_A2 | EQ_COEF_F2_A2 |
| 0x0F | EQ_COEF_F3_B0 | EQ_COEF_F3_B0 |
| 0x10 | EQ_COEF_F3_B1 | EQ_COEF_F3_B1 |
| 0x11 | EQ_COEF_F3_B2 | EQ_COEF_F3_B2 |
| 0x12 | EQ_COEF_F3_A1 | EQ_COEF_F3_A1 |
| 0x13 | EQ_COEF_F3_A2 | EQ_COEF_F3_A2 |
| 0x14 | EQ_COEF_F4_B0 | EQ_COEF_F4_B0 |
| 0x15 | EQ_COEF_F4_B1 | EQ_COEF_F4_B1 |
| 0x16 | EQ_COEF_F4_B2 | EQ_COEF_F4_B2 |
| 0x17 | EQ_COEF_F4_A1 | EQ_COEF_F4_A1 |
| 0x18 | EQ_COEF_F4_A2 | EQ_COEF_F4_A2 |
| 0x19 | EQ_PRESCALE | EQ_PRESCALE |
| | based on 48Khz sample rate | |
| 0x1A | EQ_COEF_F0_B0 | EQ_COEF_F0_B0 |
| 0x1B | EQ_COEF_F0_B1 | EQ_COEF_F0_B1 |
| 0x1C | EQ_COEF_F0_B2 | EQ_COEF_F0_B2 |
| 0x1D | EQ_COEF_F0_A1 | EQ_COEF_F0_A1 |
| 0x1E | EQ_COEF_F0_A2 | EQ_COEF_F0_A2 |
| 0x1F | EQ_COEF_F1_B0 | EQ_COEF_F1_B0 |
| 0x20 | EQ_COEF_F1_B1 | EQ_COEF_F1_B1 |
| 0x21 | EQ_COEF_F1_B2 | EQ_COEF_F1_B2 |
| 0x22 | EQ_COEF_F1_A1 | EQ_COEF_F1_A1 |

| Address | Channel RIGHT Coefficients (24bit) | Channel LEFT Coefficients (24bit) |
|------------|------------------------------------|-----------------------------------|
| EQRAM Bits | [47:24] | [23:00] |
| 0x23 | EQ_COEF_F1_A2 | EQ_COEF_F1_A2 |
| 0x24 | EQ_COEF_F2_B0 | EQ_COEF_F2_B0 |
| 0x25 | EQ_COEF_F2_B1 | EQ_COEF_F2_B1 |
| 0x26 | EQ_COEF_F2_B2 | EQ_COEF_F2_B2 |
| 0x27 | EQ_COEF_F2_A1 | EQ_COEF_F2_A1 |
| 0x28 | EQ_COEF_F2_A2 | EQ_COEF_F2_A2 |
| 0x29 | EQ_COEF_F3_B0 | EQ_COEF_F3_B0 |
| 0x2A | EQ_COEF_F3_B1 | EQ_COEF_F3_B1 |
| 0x2B | EQ_COEF_F3_B2 | EQ_COEF_F3_B2 |
| 0x2C | EQ_COEF_F3_A1 | EQ_COEF_F3_A1 |
| 0x2D | EQ_COEF_F3_A2 | EQ_COEF_F3_A2 |
| 0x2E | EQ_COEF_F4_B0 | EQ_COEF_F4_B0 |
| 0x2F | EQ_COEF_F4_B1 | EQ_COEF_F4_B1 |
| 0x30 | EQ_COEF_F4_B2 | EQ_COEF_F4_B2 |
| 0x31 | EQ_COEF_F4_A1 | EQ_COEF_F4_A1 |
| 0x32 | EQ_COEF_F4_A2 | EQ_COEF_F4_A2 |
| 0x33 | EQ_PRESCALE | EQ_PRESCALE |

The EQRAM is programmed indirectly through the Control Bus in the following manner:

- 1) Write the 48-bit write data to the EQRAM_WRITE register
- 2) Write the target address to the EQ_ADDRESS register
- 3) Set bit 7 of the EQRAM_CTRL register

The write will occur when the EQRAM is not being accessed by the DSP audio processing routines. When complete the hardware will automatically clear this bit.

Reading back from the EQRAM is done in the following manner:

- 1) Write target address to EQ_ADDR register
 - 2) Set bit 6 of the EQRAM_CTRL register
- When the hardware completes the read it will automatically clear this bit.
- 3) When bit 6 of the EQRAM_CTRL register has been cleared, read the 48bit data from the EQRAM_READ register.

2.29.2.35. EQRAM Read Data (0x30–0x35), EQRAM Write Data (0x36–3B) Registers

These two 48-bit registers (addressed as 12 8-bit registers) are 48-bit data holding registers used when doing indirect writes/reads to the EQRAM.

These registers reset by POR/DAFG/ULR

]The EQRAM_WRITE will also reset by writing to NID22h verb 77F]

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|-------------|------|---------|--|
| 30h EQRAM_READ[47:40] verb FA0/7A0 | 7:0 | EQRD[47:40] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

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| Register Address | Bit | Label | Type | Default | Description |
|--|-----|-------------|------|---------|--|
| 31h EQRAM_READ[39:32] verb FA1/7A1 | 7:0 | EQRD[39:32] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|-------------|------|---------|--|
| 32h EQRAM_READ[31:24] verb FA2/7A2 | 7:0 | EQRD[31:24] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|-------------|------|---------|--|
| 33h EQRAM_READ[23:16] verb FA3/7A3 | 7:0 | EQRD[23:16] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|------------|------|---------|--|
| 34h EQRAM_READ[15:8] verb FA4/7A4 | 7:0 | EQRD[15:8] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|-----------|------|---------|--|
| 35h EQRAM_READ[7:0] verb FA5/7A5 | 7:0 | EQRD[7:0] | RW | 0x00 | 48-bit data register, contains the contents of the most recent EQRAM address read from the RAM. The address read will have been specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|-------------|------|---------|---|
| 36h EQRAM_WRITE[47:40] verb FA6/7A6 | 7:0 | EQWD[47:40] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|-------------|------|---------|---|
| 37h EQRAM_WRITE[39:32] verb FA7/7A7 | 7:0 | EQWD[39:32] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|-------------|------|---------|---|
| 38h EQRAM_WRITE[31:24] verb FA8/7A8 | 7:0 | EQWD[31:24] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|-------------|------|---------|---|
| 39h EQRAM_WRITE[23:16] verb FA9/7A9 | 7:0 | EQWD[23:16] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|--|-----|------------|------|---------|---|
| 3Ah EQRAM_WRITE[15:8] verb FAA/7AA | 7:0 | EQWD[15:8] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

| Register Address | Bit | Label | Type | Default | Description |
|---|-----|-----------|------|---------|---|
| 3Bh EQRAM_WRITE[7:0] verb FAB/7AB | 7:0 | EQWD[7:0] | RW | 0x00 | 48-bit data register, contains the values to be written to the EQRAM. The address written will have be specified by the EQRAM Address fields. |

2.29.2.36. EQRAM Address Register

This 8-bit register provides the address to the internal RAM when doing indirect writes/reads to the EQRAM

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|-----------------------------------|-----|------------|------|---------|---|
| 3Ch EQRAM_ADDR verb FAC/7AC | 7:6 | RSVD | RO | 0x00 | Reserved |
| | 5:0 | EQADD[5:0] | RW | 0x00 | Contains the address (between 0x00 and 0x33) of the EQRAM to be accessed by a read or write. This is not a byte address--it is the address of the 48-bit data item to be accessed from the EQRAM. |

2.29.2.37. EQRAM Control Register

This control register provides the write/read enable when doing indirect writes/reads to the EQRAM.

This register reset by POR/DAFG/ULR. Writing to NID22h verb 77F will also cause reset.

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------------|-----|----------|------|---------|--|
| 3Dh EQRAM_CONTROL verb FAD/7AD | 7 | EQRAM_wr | RW | 0 | 1 = write to EQRAM, cleared by HW when done |
| | 6 | EQRAM_rd | RW | 0 | 1 = read from EQRAM, cleared by HW when done |
| | 5:0 | RSVD | RO | 0 | Reserved |

2.29.2.38. Device Address Register

This 8-bit register provides slave address for the device on the control interface.

| Register Address | Bit | Label | Type | Default | Description |
|--------------------------------|-----|-------------|------|-------------|--|
| 3Fh DEV_ADR verb FAF/7AF | 7:1 | DEVADR[7:1] | RW | 1110 001 | Contains the 7-bit device address used when accessing the CODEC in Aux Audio Mode. The lsb is ignored and reads back 0. (D0 is the read/write bit) |
| | 0 | DEVADR[0] | RO | 0 | This bit is not used. |

3. CHARACTERISTICS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD94. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Pin | Maximum Rating |
|---------------------------------------|------|---|
| Analog maximum supply voltage | AVdd | 6 Volts |
| Digital maximum supply voltage | DVdd | 5.5 Volts |
| | PVdd | 6 Volts |
| VREFOUT output current | | 5 mA |
| Voltage on any pin relative to ground | | Vss - 0.3 V to Vdd + 0.3 V |
| Operating temperature | | 0 °C to +70 °C -40 °C to +85°C (INDUSTRIAL TEMP, see part number list) |
| Storage temperature | | -55 °C to +125 °C |
| Soldering temperature | | Soldering temperature information for all available in the package section of this datasheet. |

Table 18. Electrical Specification: Maximum Ratings

3.1.2. Recommended Operating Conditions

| Parameter | | Min. | Typ. | Max. | Units |
|-------------------------------|------------------------------|-------|------|-------|-------|
| Power Supplies | DVDD_Core | 1.6 | 1.8 | 1.98 | V |
| | DVDD_IO (3.3V signaling) | 3.135 | 3.3 | 3.465 | V |
| | DVDD_IO (1.5V signaling) | 1.418 | 1.5 | 1.583 | V |
| Power Supply Voltage | Digital - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | Analog - 5 V | 4.75 | 5 | 5.25 | V |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Case Temperature | T _{case} | | | +90 | °C |
| | T _{case} Industrial | | | +110 | °C |

Table 19. Recommended Operating Conditions

92HD94

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

ESD: The 92HD94 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD94 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

3.2. 92HD94 Analog Performance Characteristics (PRELIMINARY)

($T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$, $AV_{\text{dd}} = 4.75\text{V}$ (4.5-5.25V) or $3.3\text{V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{V} \pm 5\%$ or $1.8\text{V} \pm 10\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0dB FS = 1Vrms for $AV_{\text{dd}} = 4.75\text{V}$ and 0.71Vrms for $AV_{\text{dd}} = 3.3\text{V}$, 10K Ω //50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--------|------|--------|--------|
| Digital to Analog Converters | | | | | |
| Resolution | | | 24 | | Bits |
| Dynamic Range ¹ : PCM to All Analog Outputs | -60dB FS signal level, Analog Mixer disabled | | 98 | | dB |
| SNR ² - DAC to All Line-Out Ports | Analog Mixer Disabled, PCM data | | 98 | | dB |
| THD+N ³ - DAC to All Line-Out Ports | Analog Mixer Disabled, -3dB FS Signal, PCM data | | 89 | | dBr |
| SNR ² - DAC to All Headphone Ports | Analog Mixer Disabled, 10K Ω load, PCM data | | 98 | | dB |
| THD+N ³ - DAC to All Headphone Ports | Analog Mixer Disabled, -3dB FS Signal, 10K Ω load, PCM data | | 87 | | dBr |
| SNR ² - DAC to All Headphone Ports | Analog Mixer Disabled, 32 Ω load, PCM data | | 98 | | dB |
| THD+N ³ - DAC to All Headphone Ports | Analog Mixer Disabled, -3dB FS Signal, 32 Ω load, PCM data | | 73 | | dBr |
| Any Analog Input (ADC) to DAC Crosstalk | 10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output. | -65 | - | - | dB |
| Any Analog Input (ADC) to DAC Crosstalk | 1KHz Signal Frequency. see above | -65 | - | - | dB |
| DAC L/R crosstalk | DAC to LO or HP 20-15KHz into 10K Ω load | 70 | 73 | | dB |
| DAC L/R crosstalk | DAC to HP 20-15KHz into 32 Ω load | 65 | 68 | | dB |
| Gain Error | Analog Mixer Disabled | | | 0.5 | dB |
| Interchannel Gain Mismatch | Analog Mixer Disabled | | | 0.5 | dB |
| D/A Digital Filter Pass Band ⁴ | | 20 | - | 21,000 | Hz |
| D/A Digital Filter Pass Band Ripple ⁵ | | | | 0.125 | +/- dB |
| D/A Digital Filter Transition Band | | 21,000 | - | 31,000 | Hz |
| D/A Digital Filter Stop Band | | 31,000 | - | - | Hz |
| D/A Digital Filter Stop Band Rejection ⁶ | | -100 | - | - | dB |
| D/A Out-of-Band Rejection ⁷ | | -55 | - | - | dB |
| Group Delay (48KHz sample rate) | | - | - | 1 | ms |
| Attenuation, Gain Step Size DIGITAL | | - | 0.75 | - | dB |

Table 20. 92HD94 Analog Performance Characteristics

92HD94

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|------------|-----|-----|-----------|
| DAC Offset Voltage | | - | 10 | 20 | mV |
| Deviation from Linear Phase | | - | 1 | 10 | deg. |
| Analog Outputs | | | | | |
| Full Scale All Mono/Line-Outs | DAC PCM Data | 1.00 | - | - | Vrms |
| Full Scale All Mono/Line-Outs | DAC PCM Data | 2.83 | - | - | Vp-p |
| All Headphone Capable Outputs | 32Ω load | 40 | 60 | - | mW (peak) |
| Amplifier output impedance | Mono/Line Outputs Headphone Outputs | 150 0.1 | | | Ohms |
| External load Capacitance | Mono/Line Outputs Headphone Outputs | | 220 | | pF |
| Analog inputs | | | | | |
| Full Scale Input Voltage | 0dB Boost @4.75V (input voltage required for 0dB FS output) | 1.05 | - | - | Vrms |
| All Analog Inputs with boost | 10dB Boost | 0.320 | - | - | Vrms |
| All Analog Inputs with boost | 20dB Boost | 0.105 | - | - | Vrms |
| All Analog Inputs with boost | 30dB Boost | 0.032 | - | - | Vrms |
| Boost Gain Accuracy | | -2 | | 2 | dB |
| Input Impedance | | - | 50 | - | KΩ |
| Input Capacitance | | - | 15 | - | pF |
| Analog Mixer | | | | | |
| Dynamic Range: PCM to All Analog Outputs | -60dB FS signal level Analog Beep enabled all other mixer inputs mute | | 95 | | dB |
| SNR ² - All Line-Inputs to all Line Outputs | All inputs unmuted, single line input driven by ATE. | | 90 | | dB |
| THD+N ³ - All Line-Inputs to all Line Outputs | 0dB Full Scale Input on one input, all others silent. | | 83 | | dBr |
| SNR ² - DAC to All Ports | Analog Mixer Enabled, PCM data, all others inputs mute. | | 98 | | dB |
| THD+N ³ - DAC to All Ports | Analog Mixer Enabled, 0dB FS Signal, PCM data, all others inputs unmute/silent | | 85 | | dBr |
| Attenuation, Gain Step Size ANALOG | | - | 1.5 | - | dB |
| Analog to Digital Converter | | | | | |
| Resolution | | | 24 | | Bits |
| Full Scale Input Voltage | 0dB Boost (input voltage required to generate 0dBFS per AES 17) | 1.05 | | | |
| Dynamic Range ¹ , All Analog Inputs to A/D | High Pass Filter Enabled, -60dB FS, No boost | | 94 | | dB |
| Full Scale Input Voltage | 20dB Boost (input voltage required to generate 0dBFS per AES 17) | 0.105 | | | |
| Dynamic Range ¹ , All Analog Inputs to A/D | 20dB Boost High Pass Filter Enabled, -60dB FS | | 90 | | dB |
| THD+N ³ All Analog Inputs to A/D | High Pass Filter enabled, -3dB FS signal level | | 83 | | dB |

Table 20. 92HD94 Analog Performance Characteristics

92HD94

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--------|------|--------|--------|
| THD+N ³ All Analog Inputs to A/D | 20dB Boost, High Pass Filter enabled, -3dB FS signal level | | 80 | | dB |
| Analog Frequency Response ⁸ | | 10 | - | 30,000 | Hz |
| A/D Digital Filter Pass Band ⁴ | | 20 | - | 21,000 | Hz |
| A/D Digital Filter Pass Band Ripple ⁵ | | | | 0.1 | +/- dB |
| A/D Digital Filter Transition Band | | 21,000 | - | 31,000 | Hz |
| A/D Digital Filter Stop Band | | 31,000 | - | - | Hz |
| A/D Digital Filter Stop Band Rejection ⁶ | | -100 | - | - | dB |
| Group Delay | 48 KHz sample rate | - | - | 1 | ms |
| Any unselected analog Input to ADC Crosstalk | 10KHz Signal Frequency | -65 | - | - | dB |
| Any unselected analog Input to ADC Crosstalk | 1KHz Signal Frequency | -65 | - | - | dB |
| ADC L/R crosstalk | Any selected input to ADC 20-15Khz | -65 | | | dB |
| DAC to ADC crosstalk | DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz | -65 | | | dB |
| Spurious Tone Rejection ⁹ | | - | -100 | - | dB |
| Attenuation, Gain Step Size (analog) | | - | 1.5 | - | dB |
| Interchannel Gain Mismatch ADC | | - | - | 0.5 | dB |
| Power Supply | | | | | |
| Power Supply Rejection Ratio | 10kHz | - | -60 | - | dB |
| Power Supply Rejection Ratio | 1kHz | - | -70 | - | dB |
| D0 Didd ¹⁰ | 3.3V | | 25 | | mA |
| D0 Aidd ¹⁰ | 5V | | 66 | | mA |
| D0 Didd ¹¹ | 3.3V | | 17 | | mA |
| D0 Aidd ¹¹ | 5V | | 54 | | mA |
| D1 Didd ¹² | 3.3V | | 10 | | mA |
| D1 Aidd ¹² | 5V | | 30 | | mA |
| D2 Didd | 3.3V | | 8 | | mA |
| D2 Aidd | 5V | | 7 | | mA |
| D3 (Beep enabled) Didd ¹³ | 3.3V | | 2 | | mA |
| D3 (Beep enabled) Aidd ¹³ | 5V | | 6 | | mA |
| D3 Didd ¹³ | 3.3V | | 2 | | mA |
| D3 Aidd ¹³ | 5V | | 4 | | mA |
| D3cold Didd ¹³ | 3.3V | | 1.3 | | mA |
| D3cold Aidd ¹³ | 5V | | 3.5 | | mA |
| Vendor D4 Didd | 3.3V | | 1.1 | | mA |
| Vendor D4 Aidd | 5V | | 3.5 | | mA |

Table 20. 92HD94 Analog Performance Characteristics

92HD94

SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|------------|-----|-------------|-----|-------|
| Vendor D5 Didd | 3.3V | | 1 | | mA |
| Vendor D5 Aidd | 5V | | 0.3 | | mA |
| Voltage Reference Outputs | | | | | |
| VREFOut ¹⁴ | | - | 0.5 X AVdd | - | V |
| VREFOut Drive | | | 1.6 | | mA |
| VREFILT (VAG) | | | 0.45 X AVdd | | V |
| Phased Locked Loop | | | | | |
| PLL lock time | | | 96 | 200 | usec |
| PLL (or HD Audio Bit CLK) 24MHz clock jitter | | | 150 | 500 | psec |
| ESD / Latchup | | | | | |
| IEC1000-4-2 | | 1 | | | Level |
| JESD22-A114-B | | 2 | | | Class |
| JESD22-C101 | | 4 | | | Class |

Table 20. 92HD94 Analog Performance Characteristics

- 1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured "A weighted" over 20 Hz to 20 kHz bandwidth
- 2.Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
- 3.TH+N ratio as defined in AES17 and outlined in AES6id,non-weighted, over 20 Hz to 20 kHz bandwidth.Results at the jack are dependent on external components and will likely be 1 - 2dB worse.
- 4.Peak-to-Peak Ripple over Passband meets ± 0.125 dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
- 5.Peak-to-Peak Ripple over Passband meets ± 0.125 dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
- 6.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
- 7.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8. ± 1 dB limits for Line Output & 0 dB gain, at -20dBV
- 9.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.
- 10.All functions/converters active, pin complexes enabled, two FDX streams, line (10Kohm) loads. Add 24mA analog current per stereo 32 ohm headphone.
- 11.One stereo DAC and corresponding pin widgets enabled (playback mode)
- 12.Mixer enabled
- 13.Idle measurement D3 set for minimum clicks/pops (biases and min. amps. on)
- 14.Can be set to 0.5 or 0.8 AVdd.

3.3. Class-D BTL Amplifier Performance

| Parameter | Min | Typ | Max | Unit |
|---|-----|-------|-----|---------|
| Output Power (BTL 4 ohm, 5V, <1% THD+N) | 2 | | | W |
| Output Power (BTL 4 ohm, 5V, <10% THD+N) | | 3 | | W |
| Amplifier Efficiency η (4 Ω , 5V, 2W) | | 88 | | % |
| THD+N (BTL 4 Ω , 5V, FS) | | | 1 | % |
| THD+N (BTL 4 Ω , 5V, -3dBFS) | | 0.3 | | % |
| Frequency Response | 20 | - | 20K | Hz |
| PWM frequency | | 352.8 | | KHz |
| Output voltage noise (4 Ω , 5V) | | 65 | | μ V |
| Idle current | | 3.6 | | mA |
| Shutdown current | | 0 | | mA |

Table 21. Class-D BTL Amplifier Performance

3.4. Capless Headphone Supply Characteristics

| Parameter | Min | Typ | Max | Unit |
|------------------------------------|-----|-----|-----|------|
| LDO idle current | | 1 | 2 | mA |
| Capless Headphone Amp idle current | | 2 | 3 | mA |
| Charge Pump idle current | | 4 | 6 | mA |
| Charge Pump shutdown time | | 1 | | mS |
| Charge Pump start-up time | | 10 | | mS |
| Frequency | | 384 | | KHz |
| C1/C2 cap value | | 2.2 | | uF |

Table 22. Capless Headphone Supply

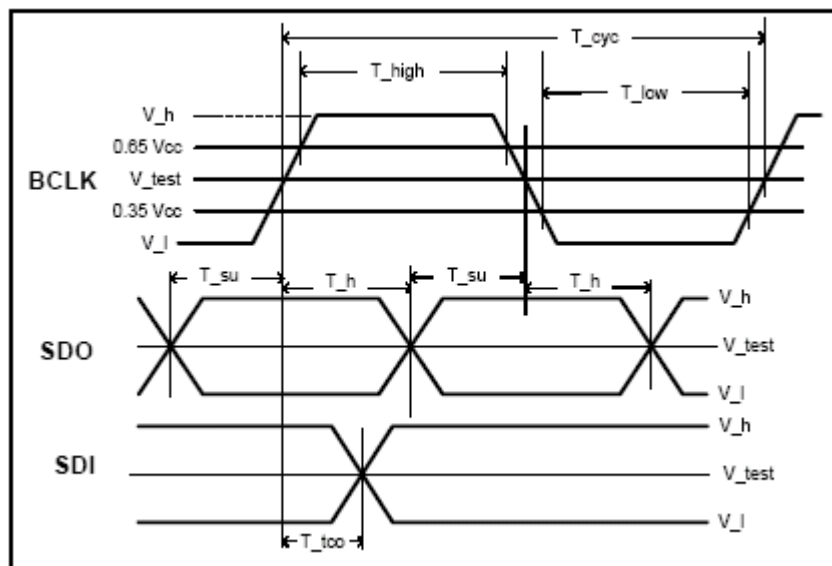
3.5. AC Timing Specs

3.5.1. HD Audio Bus Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|-----------------|--|-------------------|---------|-------|---------|-------|
| BCLK Frequency | Average BCLK frequency | | 23.9976 | 24.0 | 24.0024 | Mhz |
| BCLK Period | Period of BCLK including jitter | T _{cyc} | 41.163 | 41.67 | 42.171 | ns |
| BCLK High Phase | High phase of BCLK | T _{high} | 17.5 | | 24.16 | ns |
| BCLK Low Phase | Low phase of BCLK | T _{low} | 17.5 | | 24.16 | ns |
| BCLK jitter | BCLK jitter | | | 150 | 500 | ps |
| SDI delay | Time after rising edge of BCLK that SDI becomes valid | T _{tco} | 3 | | 11 | ns |
| SDO setup | Setup for SDO at both rising and falling edges of BCLK | T _{su} | 5 | | | ns |
| SDO hold | Hold for SDO at both rising and falling edges of BCLK | T _h | 5 | | | ns |

Table 23. HD Audio Bus Timing

Figure 11. HD Audio Bus Timing



3.5.2. SPDIF Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|-------------------------|--|-------------------|--------|--------|--------|-------|
| SPDIF_OUT Frequency | highest rate of encoded signal 64 times the sample rate | | 2.8224 | 3.072 | 12.288 | MHz |
| SPDIF_OUT unit interval | 1/(128 times the sample rate) | UI | 177.15 | 162.76 | 40.69 | ns |
| SPDIF_OUT jitter | SPDIF_OUT jitter | | | | 4.43 | ns |
| SPDIF_OUT rise time | | T _{rise} | | | 15 | ns |
| SPDIF_OUT fall time | | T _{fall} | | | 15 | ns |

Table 24. SPDIF Timing

3.5.3. Digital Microphone Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|--------------------|---|-----------------------|--------|--------|--------|-------|
| DMIC_CLK Frequency | Average DMIC_CLK frequency | | 1.176 | 2.352 | 4.704 | MHz |
| DMIC_CLK Period | Period of DMIC_CLK | T _{dmic_cyc} | 850.34 | 425.17 | 212.59 | ns |
| DMIC_CLK jitter | DMIC_CLK jitter | | | | 5000 | ps |
| DMIC Data setup | Setup for the microphone data at both rising and falling edges of DMIC_CLK | T _{dmic_su} | 5 | | | ns |
| DMIC Data hold | Hold for the microphone data at both rising and falling edges of DMIC_CLK | T _{dmic_h} | 5 | | | ns |

Table 25. Digital Mic timing

3.5.4. GPIO Characteristics

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|--|---|--------------------------------------|--------------|-----|---------------|-------|
| Input High Voltage ¹ | input level at or above which a 1 is reliably recorded | V _{ih} | 0.6 x VDD | | | V |
| Input Low Voltage ¹ | input level at or below which a 0 is reliably recorded. VDD may be DVDD or AVDD | V _{il} | | | 0.35 x VDD | V |
| Output High Voltage | i _{out} = 4mA VDD may be DVDD or AVDD depending on pin | V _{oh} | 0.9 x VDD | | | V |
| Output Low Voltage | i _{out} = -4mA VDD may be DVDD or AVDD depending on pin | V _{ol} | | | 0.1 x VDD | V |
| Input rise/fall time | transition time between 10% and 90% of supply | T _{rise} /T _{fall} | | | 10 | ns |
| Input/Tristate High Leakage Current | V _{in} = VDD VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present) | | | 0.5 | | uA |
| Input/Tristate Low Leakage Current | V _{in} = 0 VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present) | | | -50 | | uA |

Table 26. GPIO Characteristics

1.High peak currents during dynamic switching of the Class-D PWM Outputs can result in Ground Rail Bounce. The amount of Ground Bounce should be kept below 0.35 x VDD for all Inputs, including internal logic which is tied to DVDD_CORE.

3.5.5. I2S Interface Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|--------------------|--|---------|-----|--------|------|-------|
| I2S_MCLK Frequency | MCLK frequency (256Fs) | | | 12.288 | | MHz |
| I2S_SCLK Frequency | SCLK frequency (64Fs) | | | 3.072 | | MHz |
| I2S_SCLK jitter | DMIC_CLK jitter | | | | 4000 | ps |
| I2S Data setup | Setup for input and output data relative to I2S_SCLK | Ti2s_su | 5 | | | ns |
| I2S Data hold | Hold for input and output data relative to I2S_SCLK | Ti2s_h | 5 | | | ns |

Table 29. I2S Interface Timing

4. FUNCTIONAL BLOCK DIAGRAM

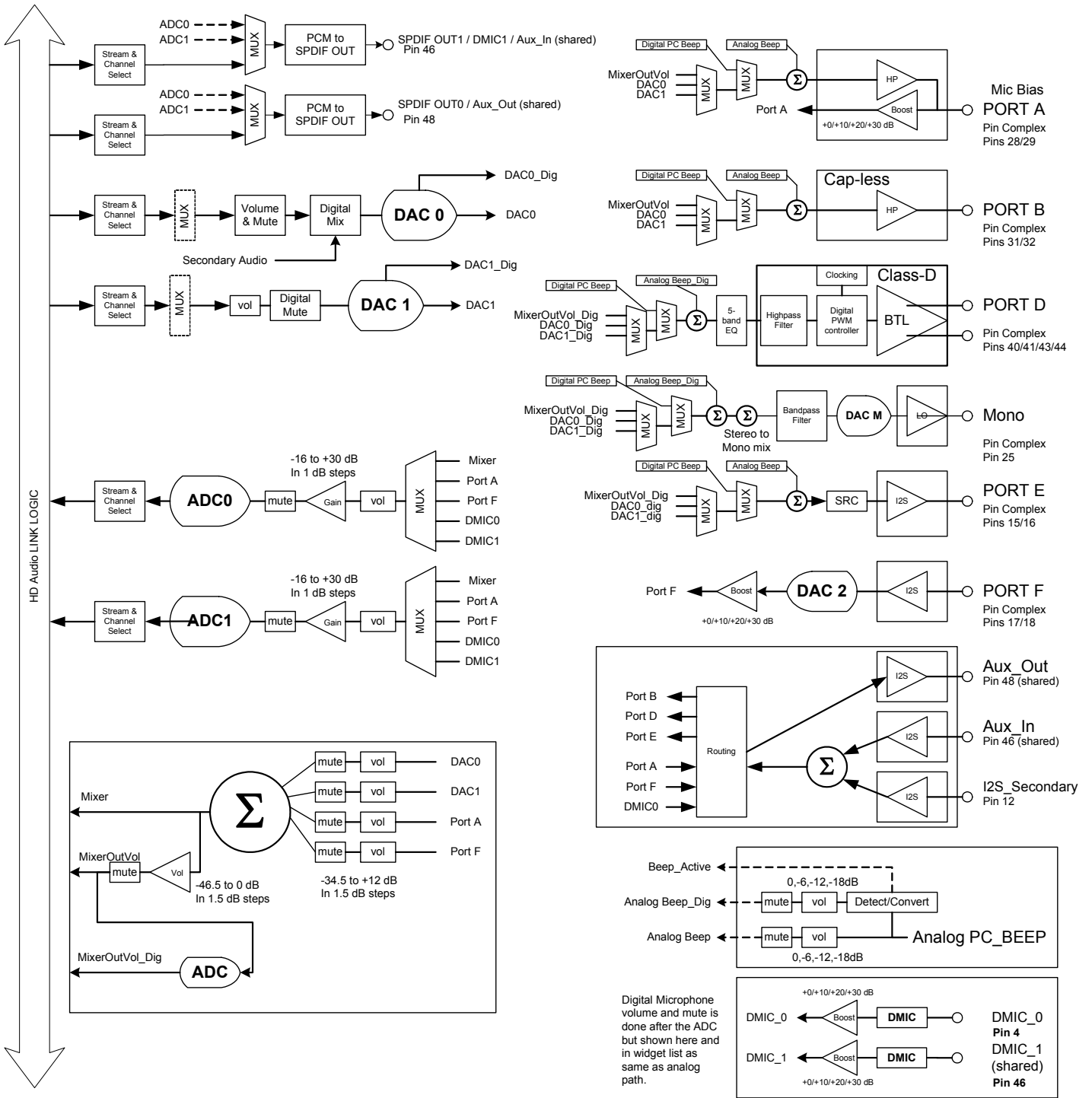


Figure 22. Functional Block Diagram

5. WIDGET DIAGRAM

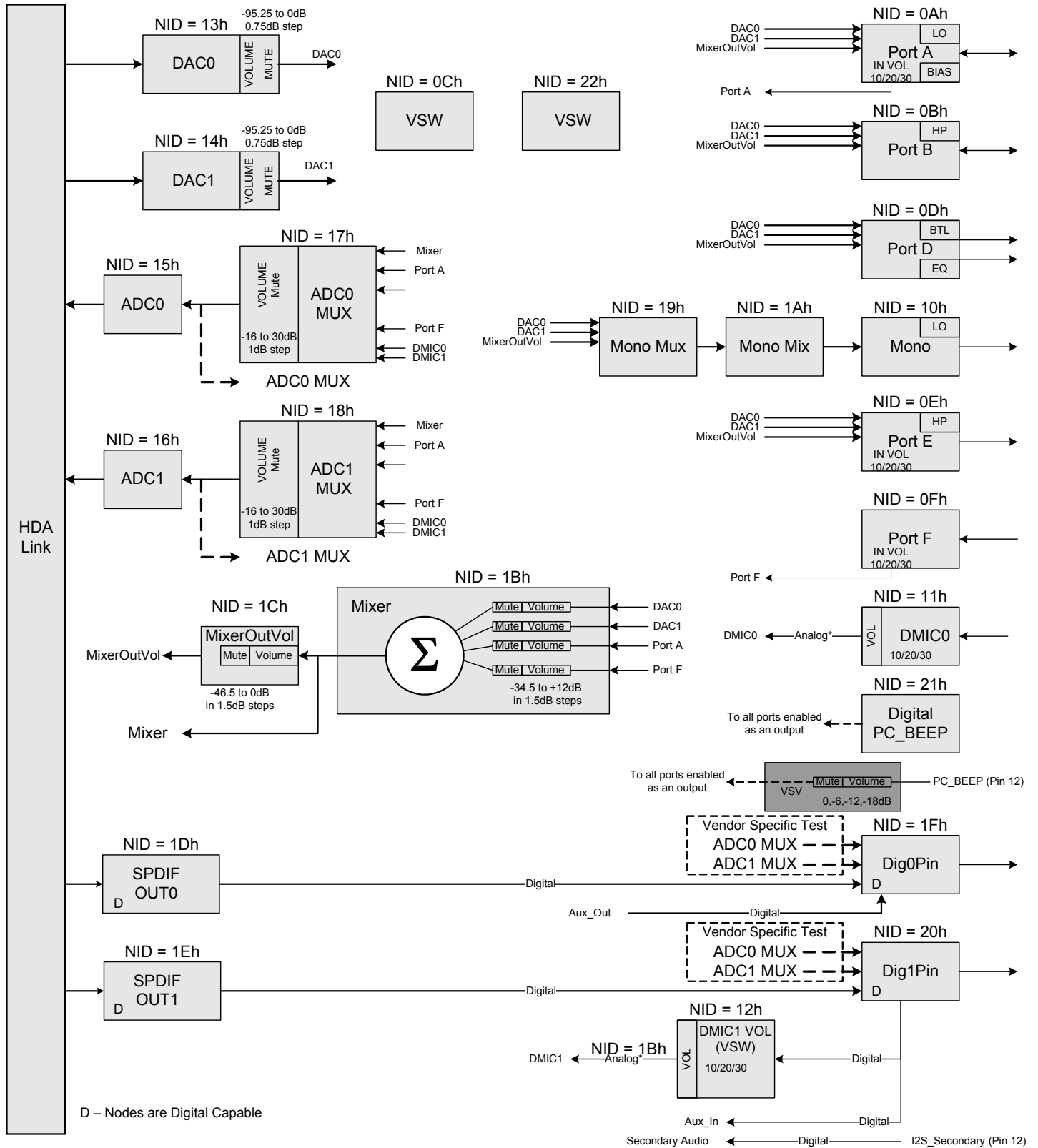


Figure 23. Widget Diagram

6. PORT AND PIN CONFIGURATIONS

6.1. Port Configurations

Mobile

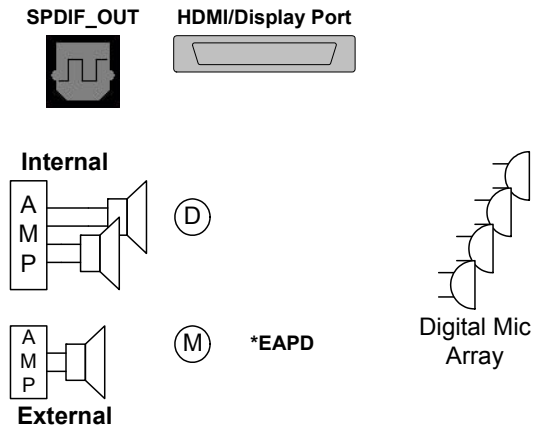
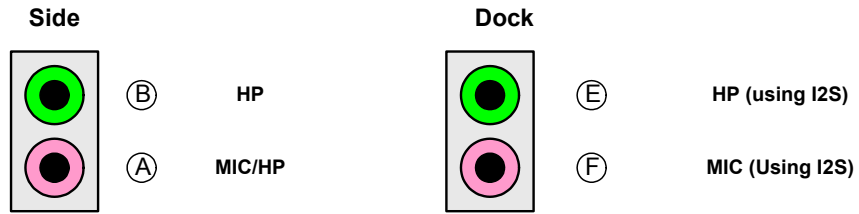


Figure 24. Port Configurations

6.2. Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Desktop implementation with 2 jacks in front and 3 jacks in rear. The internal speaker is redirected from the front (green) headphone jack. An internal microphone is present.

| Pin Name | Port | Location | Device | Connection | Color | Misc | Assoc. | Seq |
|------------|---------------------|------------------------|----------------------|------------------|------------|------------------------|--------|-----|
| PortAPin | Connect to Jack 00b | Mainboard Front 2h | Mic In Ah | 1/8 inch Jack 1h | Pink 9h | Jack Detect Override=0 | 2h | 0h |
| PortBPin | Connect to Jack 00b | Mainboard Front 2h | HP Out 2h | 1/8 inch Jack 1h | Green 4h | Jack Detect Override=0 | 1h | Fh |
| PortCPin | NA | | | | | | | |
| PortDPin | Internal 10b | NA 010000b | Speaker 1h | Other Analog 7h | Unknown 0h | Jack Detect Override=1 | 1h | 0h |
| PortEPin | Connect to Jack 00b | Mainboard Rear 1h | HP Out 2h | 1/8 inch Jack 1h | Green 4h | Jack Detect Override=0 | 5h | 0h |
| PortFPin | Connect to Jack 00b | Mainboard Rear 1h | Line In 8h | 1/8 inch Jack 1h | Blue 3h | Jack Detect Override=0 | 2h | Eh |
| MonoOutPin | No Connect 01b | NA 000000b | Other Fh | Unknown 0h | Unknown 0h | Jack Detect Override=0 | Fh | 0h |
| DigOutPin0 | Connect to Jack 00b | Mainboard Rear 000001b | SPDIF Out 4h | optical 5h | Black 1h | Jack Detect Override=1 | 6h | 0h |
| DigOutPin1 | Connect to Jack 10b | Internal 011000b | Digital Other Out 5h | Other Digital 6h | Unknown 0h | Jack Detect Override=1 | 7h | 0h |
| DigMic0Pin | Internal 10b | Internal 010000b | Mic In Ah | ATAPI 3h | Unknown 0h | Jack Detect Override=1 | 3h | 0h |

Table 31. Pin Configuration Default Settings

Figure 25.

7. WIDGET INFORMATION

| Bits [39:32] | Bits [31:28] | BITS [27:20] | BITS[19:16] | BITS [15:0] |
|--------------|---------------|--------------|-----------------|-----------------------|
| Reserved | CODEC Address | NID | Verb ID (4-bit) | Payload Data (16-bit) |

Table 32. Command Format for Verb with 4-bit Identifier

| Bits [39:32] | Bits [31:28] | BITS [27:20] | BITS[19:8] | BITS [7:0] |
|--------------|---------------|--------------|------------------|----------------------|
| Reserved | CODEC Address | NID | Verb ID (12-bit) | Payload Data (8-bit) |

Table 33. Command Format for Verb with 12-bit Identifier

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in the tables below. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

| Bit [35] | Bit [34] | BITS [33:32] | BITS[31:0] |
|-------------------|-----------|--------------|------------|
| Valid (Valid = 1) | UnSol = 0 | Reserved | Response |

Table 34. Solicited Response Format

| Bit [35] | Bit [34] | BITS [33:32] | BITS[31:28] | BITS [27:0] |
|-------------------|-----------|--------------|-------------|-------------|
| Valid (Valid = 1) | UnSol = 1 | Reserved | Tag | Response |

Table 35. Unsolicited Response Format

7.1. Widget List

| ID | Widget Name | Description |
|-----|-------------|--|
| 00h | Root | Root Node |
| 01h | AFG | Audio Function Group |
| 0Ah | Port A | Port A Pin Widget (Headphone, Line IN/OUT, MIC) |
| 0Bh | Port B | Port B Pin Widget (Capless Headphone) |
| 0Ch | Port C | Port C Pin Widget -- Not Available |
| 0Dh | Port D | Port D Pin Widget (Class-D BTL output) |
| 0Eh | Port E | Port E Pin Widget (Line OUT (I2S)) |
| 0Fh | Port F | Port F Pin Widget (Line IN, MIC) |
| 10h | MonoOut | MonoOut Pin Widget (Output Only) |
| 11h | DigMic0 | Digital Microphone 0 Pin Widget |
| 12h | DigMic1 Vol | Vendor Specific Widget - D-Mic1 volume (D pin to A mux connection) |
| 13h | DAC0 | Stereo Output Converter to DAC |
| 14h | DAC1 | Stereo Output Converter to DAC |
| 15h | ADC0 | Stereo Input Converter to ADC |
| 16h | ADC1 | Stereo Input Converter to ADC |
| 17h | ADC0Mux | ADC0 Mux with volume and mute |
| 18h | ADC1Mux | ADC1 Mux with volume and mute |
| 19h | Mono_Mux | Mono output source select |
| 1Ah | Mono_Mix | Stereo to mono conversion |
| 1Bh | Mixer | Input Mixer (Input Ports, DACs, Analog PC_Beep) |
| 1Ch | MixerOutVol | Volume control for analog mixer |
| 1Dh | SPDIFOut0 | Stereo Output for SPDIF_Out |
| 1Eh | SPDIFOut1 | Second Stereo Output for SPDIF_Out |
| 1Fh | Dig0Pin | First Digital Output Pin (pin48) |
| 20h | Dig1Pin | Second Digital Output Pin / DMIC Input Pin (pin 46) |
| 21h | PCBeep | Digital PC Beep |
| 22h | VSW | Vendor Defined Widget |

Table 36. Widget List

7.2. Reset Key

| Abbreviation | Description |
|--------------|--|
| POR | Power On Reset. |
| SAFG | Single AFG Reset - One single write to the Reset Verb in the AFG Node. |
| DAFG | Double AFG Reset - Two consecutive Single AFG Resets with only idle frames (if any) and no Link Resets between. |
| S&DAFG | Single And Double AFG Reset - Either one will cause reset. |
| LR | Link Reset - Level sensitive reset anytime the HDA Reset is set low. |
| ELR | Exiting Link Reset - Edge sensitive reset any time the HDA Reset transitions from low to high. |
| ULR | Unexpected Link Reset - Level sensitive reset anytime the HDA Reset is set low when the ClkStopOK indicator is currently set to 0. |
| PS | Power State Change - Reset anytime the Actual Power State changes for the Widget in question. |

7.3. Root (NID = 00h): VendorID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------|-----|-----------|-------|
| Vendor | 31:16 | R | 111Dh | N/A |
| | Vendor ID. | | | |
| DeviceFix | 15:8 | R | see below | N/A |
| | Device ID. | | | |
| DeviceProg | 7:0 | R | see below | N/A |
| | Device ID. | | | |

| | |
|-----------|--------|
| Device | 92HD92 |
| Device ID | 76E2h |

7.3.1. Root (NID = 00h): RevID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Major | 23:20 | R | 1h | N/A (Hard-coded) |
| | Major rev number of compliant HD Audio spec. | | | |
| Minor | 19:16 | R | 0h | N/A (Hard-coded) |
| | Minor rev number of compliant HD Audio spec. | | | |
| RevisionFix | 15:12 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| RevisionProg | 11:8 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| SteppingFix | 7:4 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |
| SteppingProg | 3:0 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |

7.3.2. Root (NID = 00h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| StartNID | 23:16 | R | 01h | N/A (Hard-coded) |
| | Starting node number (NID) of first function group | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 01h | N/A (Hard-coded) |
| | Total number of nodes | | | |

7.4. AFG (NID = 01h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StartNID | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Starting node number for function group subordinate nodes. | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 19h | N/A (Hard-coded) |
| | Total number of nodes. | | | |

7.4.1. AFG (NID = 01h): FGType

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:9 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| UnSol | 8 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response supported: 1 = yes, 0 = no. | | | |
| NodeType | 7:0 | R | 1h | N/A (Hard-coded) |
| | Function group type: 00h = Reserved 01h = Audio Function Group 02h = Vendor Defined Modem Function Group 03h-7Fh = Reserved 80h-FFh = Vendor Defined Function Group | | | |

7.4.2. AFG (NID = 01h): AFGCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0008h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd3 | 31:17 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| BeepGen | 16 | R | 1h | N/A (Hard-coded) |
| | Beep generator present: 1 = yes, 0 = no. | | | |
| Rsvd2 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| InputDelay | 11:8 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link. | | | |
| Rsvd1 | 7:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| OutputDelay | 3:0 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin. | | | |

7.4.3. AFG (NID = 01h): PCMCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

7.4.4. AFG (NID = 01h): StreamCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 0h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

7.4.5. AFG (NID = 01h): InAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 0h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 27h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-----------------------------|------|-----|---------|------------------|
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| Indicates which step is 0dB | | | | |

7.4.6. AFG (NID = 01h): PwrStateCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Fh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| EPSS | 31 | R | 1h | N/A (Hard-coded) |
| Extended power states support: 1 = yes, 0 = no. | | | | |
| ClkStop | 30 | R | 1h | N/A (Hard-coded) |
| D3 clock stop support: 1 = yes, 0 = no. | | | | |
| S3D3ColdSup | 29 | R | 1h | N/A (Hard-coded) |
| Codec state intended during system S3 state: 1 = D3Hot, 0 = D3Cold. | | | | |
| Rsvd | 28:5 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| D3ColdSup | 4 | R | 1h | N/A (Hard-coded) |
| D3Cold power state support: 1 = yes, 0 = no. | | | | |
| D3Sup | 3 | R | 1h | N/A (Hard-coded) |
| D3 power state support: 1 = yes, 0 = no. | | | | |
| D2Sup | 2 | R | 1h | N/A (Hard-coded) |
| D2 power state support: 1 = yes, 0 = no. | | | | |
| D1Sup | 1 | R | 1h | N/A (Hard-coded) |
| D1 power state support: 1 = yes, 0 = no. | | | | |
| D0Sup | 0 | R | 1h | N/A (Hard-coded) |
| D0 power state support: 1 = yes, 0 = no. | | | | |

7.4.7. AFG (NID = 01h): GPIOCnt

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0011h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| GPIWake | 31 | R | 1h | N/A (Hard-coded) |
| | Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin. | | | |
| GPIUnsol | 30 | R | 1h | N/A (Hard-coded) |
| | GPIO unsolicited response support: 1 = yes, 0 = no. | | | |
| Rsvd | 29:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumGPIs | 23:16 | R | 00h | N/A (Hard-coded) |
| | Number of GPI pins supported by function group. | | | |
| NumGPOs | 15:8 | R | 00h | N/A (Hard-coded) |
| | Number of GPO pins supported by function group. | | | |
| NumGPIOs | 7:0 | R | 05h | N/A (Hard-coded) |
| | Number of GPIO pins supported by function group. | | | |

7.4.8. AFG (NID = 01h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 02h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 7Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 7Fh | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.4.9. AFG (NID = 01h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd3 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Function Group have been reset. Cleared by PwrState 'Get' to this Widget. | | | |
| ClkStopOK | 9 | R | 1h | POR - DAFG - ULR |
| | Bit clock can currently be removed: 1 = yes, 0 = no. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 6:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 2:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.4.10. AFG (NID = 01h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.4.11. AFG (NID = 01h): GPIO

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 715h |
| Get | F1500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Data4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |

7.4.12. AFG (NID = 01h): GPIOEn

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 716h |
| Get | F1600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Mask4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |

7.4.13. AFG (NID = 01h): GPIODir

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 717h |
| Get | F1700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Control4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO4: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Control2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |

7.4.14. AFG (NID = 01h): GPIOWakeEn

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 718h |
| Get | F1800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| W4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| W1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |

7.4.15. AFG (NID = 01h): GPIOUnsol

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 719h |
| Get | F1900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EnMask4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO4. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| EnMask0 | 0 | RW | 0h | POR - DAFG - ULR |
| Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state. | | | | |

7.4.16. AFG (NID = 01h): GPIOSticky

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 71Ah |
| Get | F1A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Mask4 | 4 | RW | 0h | POR - DAFG - ULR |
| GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | | |
| Mask3 | 3 | RW | 0h | POR - DAFG - ULR |
| GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | | |

7.4.17. AFG (NID = 01h): SubID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | 723h | 722h | 721h | 720h |

7.4.17. AFG (NID = 01h): SubID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Get | F2300h / F2200h / F2100h / F2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|-------|
| Subsys3 | 31:24 | RW | 00h | POR |
| | Subsystem ID (byte 3) | | | |
| Subsys2 | 23:16 | RW | 00h | POR |
| | Subsystem ID (byte 2) | | | |
| Subsys1 | 15:8 | RW | 01h | POR |
| | Subsystem ID (byte 1) | | | |
| Assembly | 7:0 | RW | 00h | POR |
| | Assembly ID (Not applicable to codec vendors). | | | |

7.4.18. AFG (NID = 01h): GPIOIrty

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 770h |
| Get | F7000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| GP4 | 4 | RW | 1h | POR - DAFG - ULR |
| | GPIO4 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| GP3 | 3 | RW | 1h | POR - DAFG - ULR |
| | GPIO3 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |
| GP2 | 2 | RW | 1h | POR - DAFG - ULR |
| | GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |
| GP1 | 1 | RW | 1h | POR - DAFG - ULR |
| | GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |
| GP0 | 0 | RW | 1h | POR - DAFG - ULR |
| | GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected | | | |

7.4.19. AFG (NID = 01h): GPIODrive

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 771h |
| Get | F7100h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OD4 | 4 | RW | 0h | POR - DAFG - ULR |
| | GPIO4 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD3 | 3 | RW | 0h | POR - DAFG - ULR |
| | GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD2 | 2 | RW | 0h | POR - DAFG - ULR |
| | GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD1 | 1 | RW | 0h | POR - DAFG - ULR |
| | GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD0 | 0 | RW | 0h | POR - DAFG - ULR |
| | GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0, float for 1). | | | |

7.4.20. AFG (NID = 01h): DMic

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 778h |
| Get | F7800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mono1 | 5 | RW | 0h | POR |
| | DMic1 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel). | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|-------|
| Mono0 | 4 | RW | 0h | POR |
| | DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel). | | | |
| PhAdj | 3:2 | RW | 0h | POR |
| | Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge 1h = left data center of high/right data center of low 2h = left data falling edge/right data rising edge 3h = left data center of low/right data center of high | | | |
| Rate | 1:0 | RW | 2h | POR |
| | Selects the DMic clock rate: 0h = 4.704MHz 1h = 3.528MHz 2h = 2.352MHz 3h = 1.176MHz. | | | |

7.4.21. AFG (NID = 01h): DACMode

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 780h |
| Get | F8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 8 | RW | 0h | POR |
| | Internal DAC left channel and right channel swap. 0h = not swap, 1h = swap. | | | |
| SDMSettleDisable | 7 | RW | 0h | POR |
| | SDM wait-to-settle disable: 1 = at mute, the SDM switches to the mute pattern immediately 0 = at mute, the SDM switches to the mute pattern after settling (can take up to ~45ms) | | | |

| Field Name | Bits | R/W | Default | Reset |
|-----------------|--|-----|---------|-------|
| SDMCoeffSel | 6 | RW | 0h | POR |
| | DAC SDM coefficient select (stages 1, 2, 3): 1 = 1/16, 1/2, 1/4 0 = 1/16, 1/4, 1/2 | | | |
| SDMLFHalf | 5 | RW | 0h | POR |
| | DAC SDM local feedback coefficient select: 1 = 1/4096, 0 = 1/2048. | | | |
| SDMLFDisable | 4 | RW | 0h | POR |
| | DAC SDM local feedback disable: 1 = local feedback disabled, 0 = local feedback enabled. | | | |
| InvertValid | 3 | RW | 0h | POR |
| | DAC Valid Invert: 1 = 7.056MHz valid strobe is inverted, 0 = 7.056MHz valid strobe is not inverted. | | | |
| InvertData | 2 | RW | 0h | POR |
| | DAC Data Invert: 1 = 1-bit outputs are inverted, 0 = 1-bit outputs are not inverted. | | | |
| Atten6dBDisable | 1 | RW | 1h | POR |
| | Disable built-in -6dB digital attenuation: 1 = -6dB disabled, 0 = -6dB enabled. | | | |
| Fade | 0 | RW | 1h | POR |
| | DAC Gain Fade Enable: 1 = gain will be slowly faded from old value to new value (~10ms) 0 = gain will jump immediately to new value. | | | |

7.4.22. AFG (NID = 01h): ADCMode

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 784h |
| Get | F8400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|----------|------------------|
| Rsvd2 | 31:4 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------|
| InvertValid | 3 | RW | 0h | POR |
| ADC Valid Invert: 1 = 14.112MHz valid strobe is inverted, 0 = 14.112MHz valid strobe is not inverted. | | | | |
| InvertData | 2 | RW | 0h | POR |
| ADC Data Invert: 1 = 1-bit inputs are inverted, 0 = 1-bit inputs are not inverted. | | | | |
| ADCClkDelay | 1 | RW | 0h | POR |
| Delay ADC clock. | | | | |
| DACClkDelay | 0 | RW | 0h | POR |
| Delay DAC clock. | | | | |

7.4.23. AFG (NID = 01h): PortUse

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7C0h |
| Get | FC00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|----------|------------------|
| Rsvd | 31:7 | R | 0000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Mono | 6 | RW | 1h | POR |
| 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | | |
| PortF | 5 | RW | 1h | POR |
| 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | | |
| PortE | 4 | RW | 1h | POR |
| 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | | |
| PortD | 3 | RW | 1h | POR |
| 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|-------|
| PortC | 2 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortB | 1 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortA | 0 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable. | | | |

7.4.24. AFG (NID = 01h): ComJack

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | 7C7h | 7C6h |
| Get | FC700h/FC600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|--|-----|-----------|------------------|
| Rsvd3 | 31:14 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| DebounceTime | 13:12 | RW | 1h | POR |
| | Combo Jack debounce time set. 2'h0 = 0.1ms; 2'h1 = 125ms; 2'h2 = 500ms; 2'h3 = 1s." | | | |
| Rsvd2 | 11 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| RbCon | 10:8 | RW | 4h | POR |
| | Combo jack detection reference voltage 000 = 0.18*AVDD 001 = 0.16*AVDD 010 = 0.14*AVDD 011 = 0.12*AVDD 100 = 0.10*AVDD 101 = 0.08*AVDD 110 = 0.06*AVDD 111 = 0.04*AVDD | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| MasterPort | 7:5 | RW | 0h | POR |
| | Port tied to the jack presence detection switch 000 = Port A 001 = Port B 010 = Port C 011 = Port D 100 = Port E 101 = Port F | | | |
| Rsvd1 | 4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SlavePort | 3:1 | RW | 0h | POR |
| | Port used as microphone input When combo jack detection is enabled, Port presence detection as shown in the pin complex is not sensed directly by the sense input but is inferred by the load placed on the Vref_Output associated with the port 000 = Port A 001 = Port B 010 = Port C 011 = Port D; 100 = Port E 101 = Port F | | | |
| Det-en | 0 | R | 0h | POR |
| | 0h = disable combo jact detection 1h = enable combo jact detection | | | |

7.4.25. AFG (NID = 01h): VSPwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7D8h |
| Get | FD800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|-----------|
| D5 | 1 | RW | 0h | POR - ELR |
| | Vendor specific D5 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If set, this bit overrides the D4 bit (bit 0). Includes the power savings of D4, but additionally powers down GPIO pins, the VAG amp, and the HP amps. Exits this power state via POR or rising edge of Link Reset. | | | |
| D4 | 0 | RW | 0h | POR - ELR |
| | Vendor specific D4 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If the D5 bit (bit 1) is set, this bit is overridden. Includes the power savings of D3cold, but additionally powers down the HDA interface (no responses). Exit this power state via POR or rising edge of Link Reset. | | | |

7.4.26. AFG (NID = 01h): AnaPort

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | 7EDh | 7ECh |
| Get | FEC00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------|-----|----------|------------------|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| MonoPwD | 6 | RW | 0h | POR |
| | Power down Mono Output. | | | |
| FPwD | 5 | RW | 0h | POR |
| | Power down Port F. | | | |
| EPwD | 4 | RW | 0h | POR |
| | Power down Port E. | | | |
| DPwD | 3 | RW | 0h | POR |
| | Power down Port D. | | | |
| CPwD | 2 | RW | 0h | POR |
| | Power down Port C. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------|-----|---------|-------|
| BPwd | 1 | RW | 0h | POR |
| | Power down Port B. | | | |
| APwd | 0 | RW | 0h | POR |
| | Power down Port A. | | | |

7.4.27. AFG (NID = 01h): AnaBTL

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | 7F6h | 7F5h | 7F4h |
| Get | FF400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|------------------|
| Rsvd6 | 31:22 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SCStableTimeSel | 21:22 | RW | 0h | POR |
| | The programmed time window for short circuit detect. This is available on WB silicon revisions and beyond. Prior silicon revisions, these bits are reserved. | | | |
| TSOverrideHiz | 19 | RW | 0h | POR |
| | Override Hiz for the BTL amplifier power stage circuit: set to 1 to Hiz, set back to 0 to normal mode | | | |
| TSTestMode | 18 | RW | 0h | POR |
| | Temp sense test mode select, 0=normal operation, 1=sensor will trip at ambient temperature. | | | |
| TSForcePwd | 17 | RW | 1h | POR |
| | Temp sense force powerdown select 0=BTL will not be muted and powered down even if it is still overheating when the volume is 0h 1=BTL will be muted and powered down even if it is still overheating when the volume is 0h | | | |
| TSInstantCutMode | 16 | RW | 0h | POR |
| | Temp sense instant cut mode 0=Two trip points used to smoothly adjust the volume 1=One single trip point used to set volume to wither 0 or max value (TI mode) | | | |

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| Field Name | Bits | R/W | Default | Reset |
|----------------|--|-----|---------|-------|
| TSWait | 15:12 | RW | 3h | POR |
| | Temperature sensing wait time between volume increments 0h = 2ms (polling at 2ms) 1h = 4ms (polling at 4ms) 2h = 8ms (polling at 8ms) 3h = 16ms (polling at 16ms) 4h = 32ms (polling at 16ms) 5h = 64ms (polling at 16ms) 6h = 128ms (polling at 16ms) 7h = 256ms (polling at 16ms) 8h = 512ms (polling at 16ms) 9h = 1.024s (polling at 16ms) Ah = 2.048s (polling at 16ms) Bh = 4.096s (polling at 16ms) Ch = 8.192s (polling at 16ms) Dh = 16.384s (polling at 16ms) Eh = 32.768s (polling at 16ms) Fh = 65.536s (polling at 16ms). | | | |
| TSTripHish | 11:9 | RW | 3h | POR |
| | Temp sense high trip point setting: 0h = 125 Degrees C 1h = 140 Degrees C 2h = 155 Degrees C 3h = 170 Degrees C 4h = 185 C 5h = 200 C 6h = 215 C 7h = Reserved | | | |
| TSOverrideRest | 8 | RW | 0h | POR |
| | Override reset for the BTL amplifier Temp sense circuit: set to 1 to recalculate, set back to 0 to latch the value | | | |
| TSTripLow | 7:5 | RW | 2h | POR |
| | Temp sense low trip point setting: 0h = 110 Degrees C 1h = 125 Degrees C 2h = 140 Degrees C 3h = 155 Degrees C 4h = 170 C 5h = 185 C 6h = 200 C 7h = 215 C | | | |
| Rsvd1 | 4:0 | R | 0h | NA |
| | Reserved | | | |

7.4.28. AFG (NID = 01h): AnaBTLStatus

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | FF700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd | 31:20 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TSTripHigh | 19 | R | 0h | POR |
| | Temp sense high trip point status | | | |
| TSTripLow | 18 | R | 0h | POR |
| | Temp sense low trip point status | | | |
| TSMute | 17 | R | 0h | POR |
| | Temp sense forced mute status for BTL amplifier | | | |
| TSPwd | 16 | R | 0h | POR |
| | Temp sense forced powerdown status for BTL amplifier | | | |
| TSLeftVol | 15:8 | R | 0h | POR |
| | Temp sense volume status for the BTL amplifier: 00000000b..11111111b = Range specified for SPKVol field. | | | |
| TSRightVol | 7:0 | R | 0h | POR |
| | Temp sense volume status for the BTL amplifier: 00000000b..11111111b = Range specified for SPKVol field. | | | |

7.4.29. AFG (NID = 01h): AnaCapless

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | 7FAh | 7F9h | 7F8h |
| Get | FF800h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------------------|---|-----|---------|------------------|
| Rsvd2 | 31:26 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRegSCDet | 25 | R | 0h | POR |
| | Capless regulator short circuit detect indicator. | | | |
| ChargePumpSCDet | 24 | R | 0h | POR |
| | Capless charge pump short circuit detect indicator. | | | |
| VRegSel | 23:20 | RW | 5h | POR |
| | Capless regulator output voltage multiply ratio Bits [3..2] Reserved Bits [1..0]: 00b = 2*Vbg 01b = 2.1*Vbg 10b = 2.2*Vbg 11b = 2.3*Vbg | | | |
| VRegSCRstB | 19 | RW | 0h | POR |
| | Capless regulator short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| VRegGndShort | 18 | RW | 0h | POR |
| | Ground the capless regulator output. | | | |
| VRegPwd | 17 | RW | 0h | POR |
| | Capless regulator powerdown. | | | |
| ChargePumpSCRstB | 16 | RW | 0h | POR |
| | Capless charge pump short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| ChargePumpHiZ | 15 | RW | 0h | POR |
| | Hi-Z the capless charge pump outputs. | | | |
| ChargePumpPwd | 14 | RW | 0h | POR |
| | Capless charge pump powerdown. | | | |
| ChargePumpSplyDetOverride | 13 | RW | 0h | POR |
| | Capless charge pump supply detect override. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------|
| ChargePumpFreqBypass | 12 | RW | 1h | POR |
| Capless charge pump frequency reg bypass. | | | | |
| ChargePumpClkRate | 11:8 | RW | 8h | POR |
| Capless charge pump clock rate: 0000b = 800.0kHz (24MHz/30) 0001b = 750.0kHz (24MHz/32) 0010b = 706.9kHz (24MHz/34) 0011b = 666.7kHz (24MHz/36) 0100b = 631.6kHz (24MHz/38) 0101b = 600.0kHz (24MHz/40) 0110b = 571.4kHz (24MHz/42) 0111b = 545.5kHz (24MHz/44) 1000b = 800.0kHz (24MHz/30) 1001b = 857.1kHz (24MHz/28) 1010b = 923.1kHz (24MHz/26) 1011b = 1.000MHz (24MHz/24) 1100b = 1.091MHz (24MHz/22) 1101b = 1.200MHz (24MHz/20) 1110b = 1.333MHz (24MHz/18) 1111b = 1.500MHz (24MHz/16) | | | | |
| ChargePumpClkDiv | 7:5 | RW | 4h | POR |
| Capless charge pump analog clock divider: 001b = No divide 010b = Divide by 2, 50% duty cycle 100b = Divide by 4, 50% duty cycle 110b = Divide by 2, 75% duty cycle 011b = Divide by 4, 75% duty cycle 111b = Divide by 4, 87.5% duty cycle Other values undefined | | | | |
| ChargePumpClkSel | 4 | RW | 0h | POR |
| Capless charge pump clock select: 0 = ring oscillator, 1 = charge pump clock defined by AFGCaplessChargePumpClkRate[3:0] field below. | | | | |
| PadGnd | 3 | RW | 0h | POR |
| Ground the output pad of the capless amplifiers. | | | | |
| InputGnd | 2 | RW | 0h | POR |
| Ground the input to the capless output amplifiers. | | | | |
| Rsvd1 | 1 | R | 0h | NA |
| Reserved | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------|
| AntiPopBypass | 0 | RW | 0h | POR |
| 0 = Enable anti-pop on the capless headphone; 1 = bypass anti-pop on the capless headphone. | | | | |

7.4.30. AFG (NID = 01h): Reset

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7FFh |
| Get | FFF00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd1 | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Execute | 7:0 | W | 00h | N/A (Hard-coded) |
| Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The codec should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response. | | | | |

7.4.31. AFG (NID = 01h): DAC3OutAmp (Mono Out Volume)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7B6hh |
| Get | FB600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:8 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter of AFG) | | | |

7.4.32. AFG (NID = 01h): DAC5OutAmpLeft (AuxMode)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7B7hh |
| Get | FB700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:8 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter of AFG) | | | |

7.4.33. AFG (NID = 01h): DAC5OutAmpRight (AuxMode)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7B8hh |
| Get | FB800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:8 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter of AFG) | | | |

7.4.34. AFG (NID = 01h): ADC4OutAmpLeft (AuxMode)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7B9hh |
| Get | FB900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:8 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted | | | |
| Gain | 6:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter of AFG) | | | |

7.4.35. AFG (NID = 01h): ADC4OutAmpRight (AuxMode)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7BAhh |
| Get | FBA00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd | 31:8 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted | | | |
| Gain | 6:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter of AFG) | | | |

7.4.34. AFG (NID = 01h): I2Sctrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 7C8h |
| Get | FC800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------------|--|-----|----------|------------------|
| Rsvd2 | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| ForcePortf2Spdif0 | 5 | RW | 0h | POR |
| | Force I2S input to PortF to SPDIFOut0 for test purpose | | | |
| Rsvd1 | 4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| ForcePortf2PortB | 3 | RW | 0h | POR |
| | In I2S mode, the DAC2 output is routed to PortB to verified DAC2 | | | |
| I2Cdebug | 2 | RW | 0h | POR |
| | I2C bus debug mode | | | |
| BitExactSelDAC | 1 | RW | 0h | POR |
| | I2S bit exact mode select data source. 0h = data from DAC0, 1h = data from DAC1. | | | |
| BitExact | 0 | RW | 0h | POR |
| | 0h = disable I2S bit exact mode 1h = enable I2S exact mode. | | | |

7.4.33. AFG (NID = 01h): EAPD

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 788h |
| Get | F8800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd5 | 31:19 | R | 00000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPESDInv | 18 | RW | 0h | POR |
| | YA silicon: called AuxSDInv Port E HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| HPESDMode | 17 | RW | 1h | POR |
| | YA silicon and before: Reserved Port E HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| HPESD | 16 | RW | 0h | POR |
| | YA silicon and before: Reserved Port E HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd4 | 15 | R | 0 | N/A (Hard-coded) |
| | Reserved. | | | |
| HPBSDInv | 14 | RW | 0h | POR |
| | Port B HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| HPBSDMode | 13 | RW | 1h | POR |
| | Port B HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| HPBSD | 12 | RW | 0h | POR |
| | Port B HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd3 | 11 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPASDInv | 10 | RW | 0h | POR |
| | Port A HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| HPASDMode | 9 | RW | 1h | POR |
| | Port A HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| HPASD | 8 | RW | 0h | POR |
| | Port A HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BTLSDInv | 6 | RW | 0h | POR |
| | BTL Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high | | | |
| BTLSDMode | 5 | RW | 1h | POR |
| | BTL Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled | | | |
| BTLSD | 4 | RW | 0h | POR |
| | BTL Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|-------|
| PinMode | 1:0 | RW | 0h | POR |
| EAPD Pin Mode: 00b = Open Drain I/O (Value at pin is wired-AND of EAPD bit & external signal) 01b = CMOS Output (Value of EAPD bit is forced at pin) 1xb = CMOS Input (External signal controls internal amps, EAPD bit ignored) | | | | |

7.4.34. AFG (NID = 01h): ComboJackTime (Available only on WB revision and beyond)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | 7CAh | 7C9h |
| Get | FCA00h/FC900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------------|---|-----|----------|------------------|
| Rsvd3 | 31:16 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| bouncertimer_bypass | 15 | RW | 0h | POR |
| | 0 = all the combjack debounce time in normal; 1 = all the combjack debounce time in simulation mode(debounce time is short). | | | |
| t_delay_slave_port_usr | 14:12 | RW | 3h | POR |
| | 000 = 2frame 001 =4frame 010 =8frame 011 =16frame 100 = 32frame 101 =64frame 110 = 128frame 111 = 256frame | | | |
| t_stable | 11:8 | RW | 7h | POR |
| | 0000 = 0.1ms 0001 =0.5ms 0010 =1ms 0011 =2ms 0100 = 4ms 0101 =8ms 0110 = 16ms 0111 = 32ms 1000 = 64ms 1001 =128ms;1010 =256ms;1011 =512ms 1100 = 1024ms 1101 =1024ms 1110 = 1024ms 1111 = 1024ms | | | |
| RSVD2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------------------|--|-----|---------|------------------|
| t_long_realtime_detect | 6:4 | RW | 5h | POR |
| | 000 = 2s 001 =4s 010 =8s 011 =16s 100 = 32s 101 =64s 110 = 128s 111 = infinite | | | |
| RSVD1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved | | | |
| t_delay_verfout | 2:0 | RW | 3h | POR |
| | 000 = 0.1ms 001 =50ms 010 = 125ms 011 =250ms 100 = 500ms 101 = 1s 110 = 2s 111 = 4s | | | |

7.5. PortA (NID = 0Ah): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.5.1. PortA (NID = 0Ah): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.5.2. PortA (NID = 0Ah): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.5.3. PortA (NID = 0Ah): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

7.5.4. PortA (NID = 0Ah): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.5.5. PortA (NID = 0Ah): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.5.6. PortA (NID = 0Ah): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.5.7. PortA (NID = 0Ah): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.5.8. PortA (NID = 0Ah): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved | | | |

7.5.9. PortA (NID = 0Ah): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.5.10. PortA (NID = 0Ah): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

7.5.11. PortA (NID = 0Ah): EAPDBTLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.5.12. PortA (NID = 0Ah): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 02h | POR |
| | Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | Ah | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 9h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 2h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Fh | POR |
| | Sequence. | | | |

7.6. PortB (NID = 0Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

7.6.1. PortB (NID = 0Bh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| EAPD support: 1 = yes, 0 = no. | | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.6.2. PortB (NID = 0Bh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.6.3. PortB (NID = 0Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

7.6.4. PortB (NID = 0Bh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.6.5. PortB (NID = 0Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.6.6. PortB (NID = 0Bh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 5:0 | RW | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.6.7. PortB (NID = 0Bh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.6.8. PortB (NID = 0Bh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

7.6.9. PortB (NID = 0Bh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.6.10. PortB (NID = 0Bh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 02h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |
| Device | 23:20 | RW | 2h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|----------------|---|-----|---------|-------|
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | |
| Color | 15:12 | RW | 4h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 1h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Fh | POR |
| | Sequence. | | | |

7.7. (NID = 0Ch): Vendor Reserved

7.8. PortD (NID = 0Dh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.8.1. PortD (NID = 0Dh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 1h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 0h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.8.2. PortD (NID = 0Dh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.8.3. PortD (NID = 0Dh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

7.8.4. PortD (NID = 0Dh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.8.5. PortD (NID = 0Dh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.8.6. PortD (NID = 0Dh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 5:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.8.7. PortD (NID = 0Dh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.8.8. PortD (NID = 0Dh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |

7.8.8. PortD (NID = 0Dh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 2h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 10h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 1h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 7h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 1h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.9. PortE (NID = 0Eh): WCap (I2S Output)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.9.1. PortE (NID = 0Eh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.9.2. PortE (NID = 0Eh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.9.3. PortE (NID = 0Eh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

7.9.4. PortE (NID = 0Eh): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 780h |
| Get | F8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------------------------|--|-----|-----------|------------------|
| Rsvd1 | 31:8 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| Amp mute: 1 = muted, 0 = not muted | | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.9.5. PortE (NID = 0Eh): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 781h |
| Get | F8100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------------------------|--|-----|-----------|------------------|
| Rsvd1 | 31:8 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| Amp mute: 1 = muted, 0 = not muted | | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.9.6. PortE (NID = 0Eh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.9.7. PortE (NID = 0Eh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.9.8. PortE (NID = 0Eh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | R | 0h | N/A (Hard-coded) |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.9.9. PortE (NID = 0Eh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicted response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.9.10. PortE (NID = 0Eh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

7.9.11. PortE (NID = 0Eh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------|-----|---------|------------------|
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

7.9.12. PortE (NID = 0Eh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 01h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

92HD93**SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO**

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 0h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

92HD93**SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO**

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 4h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 5h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.10. PortF (NID = 0Fh): WCap (I2S Input)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.10.1. PortF (NID = 0Fh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.10.2. PortF (NID = 0Fh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.10.3. PortF (NID = 0Fh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL0 | 7:0 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |

7.10.4. PortF (NID = 0Fh): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.10.5. PortF (NID = 0Fh): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.10.6. PortF (NID = 0Fh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.10.7. PortF (NID = 0Fh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.10.8. PortF (NID = 0Fh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved | | | |

7.10.9. PortF (NID = 0Fh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.10.10. PortF (NID = 0Fh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

7.10.11. PortF (NID = 0Fh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.10.12. PortF (NID = 0Fh): InVolLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 790h |
| Get | F9000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Volume mute, 1=mute, 0 not muted | | | |
| Gain | 6:0 | RW | 00h | POR - DAFG - ULR |
| | 0 to -95.25dB in 0.75dB steps.Both headphone and BTL output paths are adjusted | | | |

7.10.13. PortF (NID = 0Fh): InVolRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 791h |
| Get | F9100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|---------|------------------|
| Rsvd1 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Volume mute, 1=mute, 0 not muted | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| Gain | 6:0 | RW | 00h | POR - DAFG - ULR |
| 0 to -95.25dB in 0.75dB steps.Both headphone and BTL output paths are adjusted | | | | |

7.10.14. PortF (NID = 0Fh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 01h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 8h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 3h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 2h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Eh | POR |
| | Sequence. | | | |

7.11. MonoOut (NID = 10h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 0h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.11.1. MonoOut (NID = 10h): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 0h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.11.2. MonoOut (NID = 10h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.11.3. MonoOut (NID = 10h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Ah | N/A (Hard-coded) |
| | MonoMix Summing widget (0x1A) | | | |

7.11.4. MonoOut (NID = 10h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.11.5. MonoOut (NID = 10h): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd1 | 5:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.11.6. MonoOut (NID = 10h): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------------|---|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 1h | POR |
| | Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 00h | POR |
| | Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | Fh | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 0h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | Fh | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.12. DMic0 (NID = 11h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.12.1. DMic0 (NID = 11h): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| VRefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 0h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HPhnDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.12.2. DMic0 (NID = 11h): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.12.3. DMic0 (NID = 11h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.12.4. DMic0 (NID = 11h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.12.5. DMic0 (NID = 11h): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|----------|------------------|
| Rsvd2 | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.12.6. DMic0 (NID = 11h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.12.7. DMic0 (NID = 11h): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

7.12.8. DMic0 (NID = 11h): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 2h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 10h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | Ah | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 3h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 3h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.13. DMic1Vol (NID = 12h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | Fh | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.13.1. DMic1Vol (NID = 12h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.13.2. DMic1Vol (NID = 12h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 20h | N/A (Hard-coded) |
| | Dig1Pin Pin widget (0x20) | | | |

7.13.3. DMic1Vol (NID = 12h): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.13.4. DMic1Vol (NID = 12h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.13.5. DMic1Vol (NID = 12h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.14. DAC0 (NID = 13h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.14.1. DAC0 (NID = 13h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmpIRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.14.2. DAC0 (NID = 13h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.14.3. DAC0 (NID = 13h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.14.4. DAC0 (NID = 13h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.14.5. DAC0 (NID = 13h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

7.14.6. DAC0 (NID = 13h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.15. DAC1 (NID = 14h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.15.1. DAC1 (NID = 14h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.15.2. DAC1 (NID = 14h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.15.3. DAC1 (NID = 14h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.15.4. DAC1 (NID = 14h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|-----------------|
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| Current power state setting for this widget. | | | | |

7.15.5. DAC1 (NID = 14h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | | |

7.15.6. DAC1 (NID = 14h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

7.16. ADC0 (NID = 15h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.16.1. ADC0 (NID = 15h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.16.2. ADC0 (NID = 15h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 20h | N/A (Hard-coded) |
| | ADC0Mux Selector widget (0x17) | | | |

7.16.3. ADC0 (NID = 15h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.16.4. ADC0 (NID = 15h): ProcState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

7.16.5. ADC0 (NID = 15h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.16.6. ADC0 (NID = 15h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

7.17. ADC1 (NID = 1Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.17.1. ADC1 (NID = 1Bh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.17.2. ADC1 (NID = 1Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 18h | N/A (Hard-coded) |
| | ADC1Mux widget (0x18) | | | |

7.17.3. ADC1 (NID = 1Bh): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| SmpIRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.17.4. ADC1 (NID = 1Bh): ProcState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

7.17.5. ADC1 (NID = 1Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.17.6. ADC1 (NID = 1Bh): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

7.18. ADC0Mux (NID = 17h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvr | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.18.1. ADC0Mux (NID = 17h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 05'h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.18.2. ADC0Mux (NID = 17h): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---------------------|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL5 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL4 | 7:0 | R | 12h | N/A (Hard-coded) |
| | DMIC1 widget (0x12) | | | |

7.18.3. ADC0Mux (NID = 17h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 11h | N/A (Hard-coded) |
| | DMIC0 widget (0x11) | | | |
| ConL2 | 23:16 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) | | | |
| ConL1 | 15:8 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

7.18.4. ADC0Mux (NID = 17h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 03h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 2Eh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 10h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.18.5. ADC0Mux (NID = 17h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.18.6. ADC0Mux (NID = 17h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.18.7. ADC0Mux (NID = 17h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.18.8. ADC0Mux (NID = 17h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.18.9. ADC0Mux (NID = 17h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.19. ADC1Mux (NID = 18h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.19.1. ADC1Mux (NID = 18h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 05h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.19.2. ADC1Mux (NID = 18h): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---------------------|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ConL5 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| ConL4 | 7:0 | R | 12h | N/A (Hard-coded) |
| | DMIC1 widget (0x12) | | | |

7.19.3. ADC1Mux (NID = 18h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 11h | N/A (Hard-coded) |
| | DMIC0 widget (0x11) | | | |
| ConL2 | 23:16 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) | | | |
| ConL1 | 15:8 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

7.19.4. ADC1Mux (NID = 18h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 03h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| NumSteps | 14:8 | R | 2Eh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 10h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.19.5. ADC1Mux (NID = 18h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.19.6. ADC1Mux (NID = 18h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.19.7. ADC1Mux (NID = 18h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.19.8. ADC1Mux (NID = 18h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.19.9. ADC1Mux (NID = 18h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|-----------|------------------|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.20. MonoMux (NID = 19h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.20.1. MonoMux (NID = 19h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 03h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.20.2. MonoMux (NID = 19h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x22) | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

7.20.3. MonoMux (NID = 19h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|----------------------------------|-----|----------|------------------|
| Rsvd | 31:2 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

7.20.4. MonoMux (NID = 19h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.21. MonoMix (NID = 1Ah): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 2h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 0h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

7.21.1. MonoMix (NID = 1Ah): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

7.21.2. MonoMix (NID = 1Ah): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 19h | N/A (Hard-coded) |
| | MonoMux Selector widget (0x19) | | | |

7.21.3. MonoMix (NID = 1Ah): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.22. Mixer (NID = 1Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 2h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.22.1. Mixer (NID = 1Bh): InAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 17h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.22.2. Mixer (NID = 1Bh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.22.3. Mixer (NID = 1Bh): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------|-----|---------|------------------|
| ConL7 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL6 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL5 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ConL4 | 7:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.22.4. Mixer (NID = 1Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| ConL3 | 31:24 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F). Uses InAmpLeft3/InAmpRight3 controls. | | | |
| ConL2 | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A). Uses InAmpLeft2/InAmpRight2 controls. | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 widget (0x14). Uses InAmpLeft1/InAmpRight1 controls. | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 widget (0x13). Uses InAmpLeft0/InAmpRight0 controls. | | | |

7.22.5. Mixer (NID = 1Bh): InAmpLeft0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.6. Mixer (NID = 1Bh): InAmpRight0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.7. Mixer (NID = 1Bh): InAmpLeft1

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 361h |
| Get | B2001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.8. Mixer (NID = 1Bh): InAmpRight1

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 351h |
| Get | B0001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.9. Mixer (NID = 1Bh): InAmpLeft2

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 362h |
| Get | B2002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.10. Mixer (NID = 1Bh): InAmpRight2

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 352h |
| Get | B0002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.11. Mixer (NID = 1Bh): InAmpLeft3

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 363h |
| Get | B2003h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.12. Mixer (NID = 1Bh): InAmpRight3

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 353h |
| Get | B0003h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.13. Mixer (NID = 1Bh): InAmpLeft4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 364h |
| Get | B2004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.14. Mixer (NID = 1Bh): InAmpRight4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 354h |
| Get | B0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.15. Mixer (NID = 1Bh): InAmpLeft5

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 365h |
| Get | B2005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.16. Mixer (NID = 1Bh): InAmpRight5

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 355h |
| Get | B0005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

7.22.17. Mixer (NID = 1Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.23. MixerOutVol (NID = 1Ch): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

7.23.1. MixerOutVol (NID = 1Ch): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

7.23.2. MixerOutVol (NID = 1Ch): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

7.23.3. MixerOutVol (NID = 1Ch): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-----------------------------|------|-----|---------|------------------|
| Offset | 6:0 | R | 1Fh | N/A (Hard-coded) |
| Indicates which step is 0dB | | | | |

7.23.4. MixerOutVol (NID = 1Ch): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| Amp mute: 1 = muted, 0 = not muted. | | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | | |

7.23.5. MixerOutVol (NID = 1Ch): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------------------------------|------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| Amp mute: 1 = muted, 0 = not muted. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.23.6. MixerOutVol (NID = 1Ch): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.24. SPDIFOut0 (NID = 1Dh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 4h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 1h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.24.1. SPDIFOut0 (NID = 1Dh): PCMCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

7.24.2. SPDIFOut0 (NID = 1Dh): StreamCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 1h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

7.24.3. SPDIFOut0 (NID = 1Dh): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--------------------------------|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 00h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 00h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.24.4. SPDIFOut0 (NID = 1Dh): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| FrmtNonPCM | 15 | RW | 0h | POR - DAFG - ULR |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.24.5. SPDIFOut0 (NID = 1Dh): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.24.6. SPDIFOut0 (NID = 1Dh): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.24.7. SPDIFOut0 (NID = 1Dh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.24.8. SPDIFOut0 (NID = 1Dh): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

7.24.9. SPDIFOut0 (NID = 1Dh): DigCnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | 73Fh | 73Eh | 70Eh | 70Dh |
| Get | F0E00h / F0D00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| KeepAlive | 23 | RW | 0h | POR - DAFG - ULR |
| | Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3. | | | |
| Rsvd1 | 22:15 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| CC | 14:8 | RW | 00h | POR - DAFG - ULR |
| | CC: Category Code. | | | |
| L | 7 | RW | 0h | POR - DAFG - ULR |
| | L: Generation Level. | | | |
| PRO | 6 | RW | 0h | POR - DAFG - ULR |
| | PRO: Professional. | | | |
| AUDIO | 5 | RW | 0h | POR - DAFG - ULR |
| | /AUDIO: Non-Audio. | | | |
| COPY | 4 | RW | 0h | POR - DAFG - ULR |
| | COPY: Copyright. | | | |
| PRE | 3 | RW | 0h | POR - DAFG - ULR |
| | PRE: Preemphasis. | | | |
| VCFG | 2 | RW | 0h | POR - DAFG - ULR |
| | VCFG: Validity Config. | | | |
| V | 1 | RW | 0h | POR - DAFG - ULR |
| | V: Validity. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| DigEn | 0 | RW | 0h | POR - DAFG - ULR |
| Digital enable: 1 = converter enabled, 0 = converter disable. | | | | |

7.25. SPDIFOut1 (NID = 1Eh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| Reserved. | | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 4h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 1h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.25.1. SPDIFOut1 (NID = 1Eh): PCMCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |

92HD94**SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO**

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

7.25.2. SPDIFOut1 (NID = 1Eh): StreamCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|-----------|------------------|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 1h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

7.25.3. SPDIFOut1 (NID = 1Eh): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 00h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 00h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.25.4. SPDIFOut1 (NID = 1Eh): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 2h |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--------------|---|-----|---------|------------------|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| FrmtNonPCM | 15 | RW | 0h | POR - DAFG - ULR |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmpIRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---------------|---|-----|---------|------------------|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

7.25.5. SPDIFOut1 (NID = 1Eh): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.25.6. SPDIFOut1 (NID = 1Eh): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.25.7. SPDIFOut1 (NID = 1Eh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.25.8. SPDIFOut1 (NID = 1Eh): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

7.25.9. SPDIFOut1 (NID = 1Eh): DigCnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | 73Fh | 73Eh | 70Eh | 70Dh |
| Get | F0E00h / F0D00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| KeepAlive | 23 | RW | 0h | POR - DAFG - ULR |
| | Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3. | | | |
| Rsvd1 | 22:15 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| CC | 14:8 | RW | 00h | POR - DAFG - ULR |
| | CC: Category Code. | | | |
| L | 7 | RW | 0h | POR - DAFG - ULR |
| | L: Generation Level. | | | |
| PRO | 6 | RW | 0h | POR - DAFG - ULR |
| | PRO: Professional. | | | |
| AUDIO | 5 | RW | 0h | POR - DAFG - ULR |
| | /AUDIO: Non-Audio. | | | |
| COPY | 4 | RW | 0h | POR - DAFG - ULR |
| | COPY: Copyright. | | | |
| PRE | 3 | RW | 0h | POR - DAFG - ULR |
| | PRE: Preemphasis. | | | |
| VCFG | 2 | RW | 0h | POR - DAFG - ULR |
| | VCFG: Validity Config. | | | |
| V | 1 | RW | 0h | POR - DAFG - ULR |
| | V: Validity. | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| DigEn | 0 | RW | 0h | POR - DAFG - ULR |
| Digital enable: 1 = converter enabled, 0 = converter disable. | | | | |

7.26. Dig0Pin (NID = 1Fh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| Reserved. | | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvr | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvr | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.26.1. Dig0Pin (NID = 1Fh): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

7.26.2. Dig0Pin (NID = 1Fh): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

7.26.3. Dig0Pin (NID = 1Fh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Dh | N/A (Hard-coded) |
| | SPDIFOut0 Converter widget (0x1D) | | | |

7.26.4. Dig0Pin (NID = 1Fh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.26.5. Dig0Pin (NID = 1Fh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd1 | 5:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.26.6. Dig0Pin (NID = 1Fh): UnsolicitedResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

7.26.7. Dig0Pin (NID = 1Fh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|-------|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|------|-----|-----------|------------------|
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| Reserved. | | | | |

7.26.8. Dig0Pin (NID = 1Fh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 0h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 1h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 4h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 5h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 1h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 6h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.27. Dig1Pin (NID = 20h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| Number of sample delays through widget. | | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| Left/right swap support: 1 = yes, 0 = no. | | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| Power state support: 1 = yes, 0 = no. | | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| Digital stream support: 1 = yes (digital), 0 = no (analog). | | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| Connection list present: 1 = yes, 0 = no. | | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| Unsolicited response support: 1 = yes, 0 = no. | | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| Processing state support: 1 = yes, 0 = no. | | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| Striping support: 1 = yes, 0 = no. | | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| Stream format override: 1 = yes, 0 = no. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| Amplifier capabilities override: 1 = yes, no. | | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| Output amp present: 1 = yes, 0 = no. | | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| Input amp present: 1 = yes, 0 = no. | | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | | |

7.27.1. Dig1Pin (NID = 20h): PinCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|-------|-----|---------|------------------|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| Reserved. | | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| EAPD support: 1 = yes, 0 = no. | | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no) | | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| Reserved. | | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| Balanced I/O support: 1 = yes, 0 = no. | | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| Input support: 1 = yes, 0 = no. | | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| Output support: 1 = yes, 0 = no. | | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| Headphone amp present: 1 = yes, 0 = no. | | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| Presence detection support: 1 = yes, 0 = no. | | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| Trigger required for impedance sense: 1 = yes, 0 = no. | | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| Impedance sense support: 1 = yes, 0 = no. | | | | |

7.27.2. Dig1Pin (NID = 20h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| Number of NID entries in connection list. | | | | |

7.27.3. Dig1Pin (NID = 20h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------------------------------|-----|---------|------------------|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Eh | N/A (Hard-coded) |
| | SPDIFOut1 Converter widget (0x1E) | | | |

7.27.4. Dig1Pin (NID = 20h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

7.27.5. Dig1Pin (NID = 20h): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|----------|------------------|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

7.27.6. Dig1Pin (NID = 20h): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|-----------------------------------|---------------------|--------------------|-------------------|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| PortConnectivity | 31:30 | RW | 2h | POR |
| Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | | |
| Location | 29:24 | RW | 18h | POR |
| Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|---|-------|-----|---------|-------|
| Device | 23:20 | RW | 5h | POR |
| Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other | | | | |
| ConnectionType | 19:16 | RW | 6h | POR |
| Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other | | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|-------|
| Color | 15:12 | RW | 0h | POR |
| | Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 7h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

7.28. DigBeep (NID = 21h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|-------------|--|-----|---------|------------------|
| Rsvd4 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 7h | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Rsvd3 | 19:11 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no." | | | |
| Rsvd2 | 9:4 | R | 0h | N/A (Hard-coded) |
| | Reserved | | | |
| AmpParOvr | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

7.28.1. DigBeep (NID = 21h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 17h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 03h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

7.28.2. DigBeep (NID = 21h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|---|-----|---------|------------------|
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

7.28.3. DigBeep (NID = 21h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---------------|--|-----|---------|------------------|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|-----------------|
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| Current power state setting for this widget. | | | | |

7.28.4. DigBeep (NID = 21h): Gen

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 70Ah |
| Get | F0A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|--|------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Divider | 7:0 | RW | 00h | POR - DAFG - LR |
| Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). | | | | |

7.28.5. DigBeep (NID = 21h): Gain

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 77Ah |
| Get | F7A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|------|-----|---------|------------------|
| Rsvd | 31:3 | R | 000000h | N/A (Hard-coded) |
| Reserved. | | | | |
| Divider | 2:0 | RW | 05h | POR - DAFG - LR |
| Digital PC Beep Gain adjust in digital side 0h = -9dB, 1h = -6dB, 2h = -3dB, 3h = 0dB, 4h = +3db, 5h = +6db | | | | |

7.29. I2C (NID = 22h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|--|-----|---------|------------------|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | Fh | N/A (Hard-coded) |
| | Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 0h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|-------------|---|-----|---------|------------------|
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

7.29.1. I2C (NID = 22h): Cntrl0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|-----|---------------------|---------------------|--------------------|-------------------|
| Set | | | | 770h:&7AFh |
| Get | F7700h: 7AF0h | | | |

| Field Name | Bits | R/W | Default | Reset |
|------------|-----------|-----|---------|------------------|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |

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| Field Name | Bits | R/W | Default | Reset |
|------------|-------------------------------------|-----|---------|------------------|
| Value | 7:0 | RW | 0h | POR - DAFG - ULR |
| | Contrl register value of I2C module | | | |

8. PINOUT AND PACKAGING

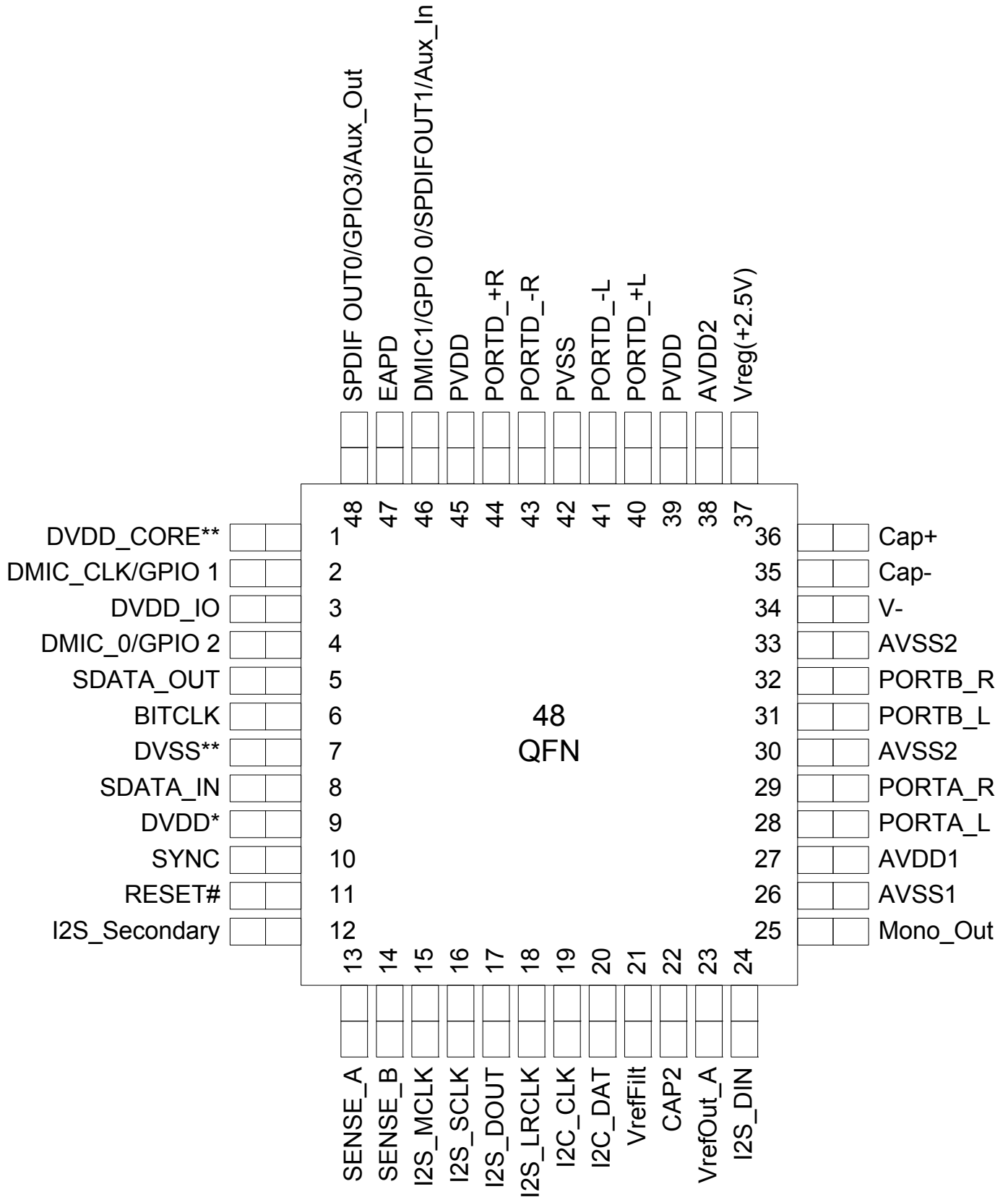


Figure 26. 48QFN Pin Assignment

92HD92**SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO****8.0.1. 48QFN Pin Table**

| Pin Name | Pin Function | I/O | Internal Pull-up/Pull-down | 48 pin location |
|----------------|--|--------------|----------------------------|-----------------|
| DVDD_CORE | 1.5V Digital Core Regulator Filter Cap | O(Digital) | None | 1 |
| DMIC_CLK/GPIO1 | Digital Mic Clock Output/GPIO1 | I/O(Digital) | 60K Pull-down | 2 |
| DVDD_IO | Reference Voltage (1.5V or 3.3V) | I(Digital) | None | 3 |
| DMIC0/GPIO2 | Digital Mic 01 Input/GPIO2 | I/O(Digital) | 60K Pull-down | 4 |
| SDATA_OUT | HD Audio Serial Data output from controller | I/O(Digital) | None | 5 |
| BITCLK | HD Audio Bit Clock | I(Digital) | None | 6 |
| DVSS | Digital Ground | I(Digital) | None | 7 |
| SDATA_IN | HD Audio Serial Data Input to controller | O(Digital) | None | 8 |
| DVDD | Digital Vdd= 3.3V | I(Digital) | None | 9 |
| SYNC | HD Audio Frame Sync | I(Digital) | None | 10 |
| RESET# | HD Audio Reset | I(Digital) | None | 11 |
| I2S_Secondary | Secondary Audio Input | I(Digital) | 60K Pull-down | 12 |
| SENSE_A | Jack insertion detection Ports A,B, SPDIFOUT0 | I(Analog) | None | 13 |
| SENSE_B | Jack insertion detection Ports E,F, DMIC0, SPDIFOUT1 (DMIC1) | I(Analog) | None | 14 |
| I2S_MCLK | Master Clock for I2S port | I/O(Digital) | 60K Pull-down | 15 |
| I2S_SCLK | Shift Clock for I2S port | I/O(Digital) | 60K Pull-down | 16 |
| I2S_DOUT | Data output for I2S port (port E) | O(Digital) | 60K Pull-down | 17 |
| I2S_LRCLK | Left/Right strobe for I2S port (Fs) | I/O(Digital) | 60K Pull-down | 18 |
| I2C_CLK | Aux Mode Control Port Clock | I(Digital) | | 19 |
| I2C_DAT | Aux Mode Control Port Data | I/O(Digital) | | 20 |
| VREFFILT | Analog Virtual Ground | O(Analog) | None | 21 |
| CAP2 | Reference filter Cap | O(Analog) | None | 22 |
| VREFOUT-A | Reference Voltage out drive (intended for mic bias) | O(Analog) | None | 23 |
| I2S_DIN | Data input for I2S port (port F) | I(Digital) | 60K Pull-down | 24 |
| MONO_OUT | Mono output | O(Analog) | None | 25 |
| AVSS1 | Analog Ground | I(Analog) | None | 26 |
| AVDD1 | Analog Vdd=5.0V or 3.3V | I(Analog) | None | 27 |
| PORTA_L (HP0) | Port A Output Left | I/O(Analog) | None | 28 |
| PORTA_R (HP0) | Port A Output Right | I/O(Analog) | None | 29 |
| AVSS | Analog Ground | I(Analog) | None | 30 |
| PORTB_L (HP1) | Port B Output Left | I/O(Analog) | None | 31 |
| PORTB_R (HP1) | Port B Output Right | I/O(Analog) | None | 32 |
| AVSS | Analog Ground | I(Analog) | None | 33 |
| V- | Negative analog supply | O(Analog) | None | 34 |
| CAP- | Charge pump cap - | O(Analog) | None | 35 |
| CAP+ | Charge pump cap + | O(Analog) | None | 36 |

Table 37. Pin Table

92HD92**SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO**

| Pin Name | Pin Function | I/O | Internal Pull-up/Pull-down | 48 pin location |
|-----------------------------|--|---------------|----------------------------|-----------------|
| VREG | Linear Regulator Output (2.5V) filter cap | O(Analog) | None | 37 |
| AVDD2 | Analog Supply for VREG | I(Analog) | None | 38 |
| PVDD | Analog Supply for Class-D amp | I(Analog) | None | 39 |
| PORTD_+L | BTL amp Left + | O(Analog) | None | 40 |
| PORTD_-L | BTL amp Left - | O(Analog) | None | 41 |
| PVSS | Analog Ground | I(Analog) | None | 42 |
| PORTD_-R | BTL amp Right - | O(Analog) | None | 43 |
| PORTD_+R | BTL amp Right + | O(Analog) | None | 44 |
| PVDD | Analog Supply for Class-D amp | I(Analog) | None | 45 |
| DMIC1/GPIO/SPDIFOUT1/Aux_In | Digital Microphone input, SPDIF Output, or GPIO0 | I/O(Digital) | 60K Pull-down | 46 |
| EAPD | EAPD | I/O (Digital) | 60K Pull-up | 47 |
| SPDIFOUT0/Aux_Out | SPDIF0 | O(Digital) | 60K pull-down | 48 |

Table 37. Pin Table

8.0.2. 48QFN Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95

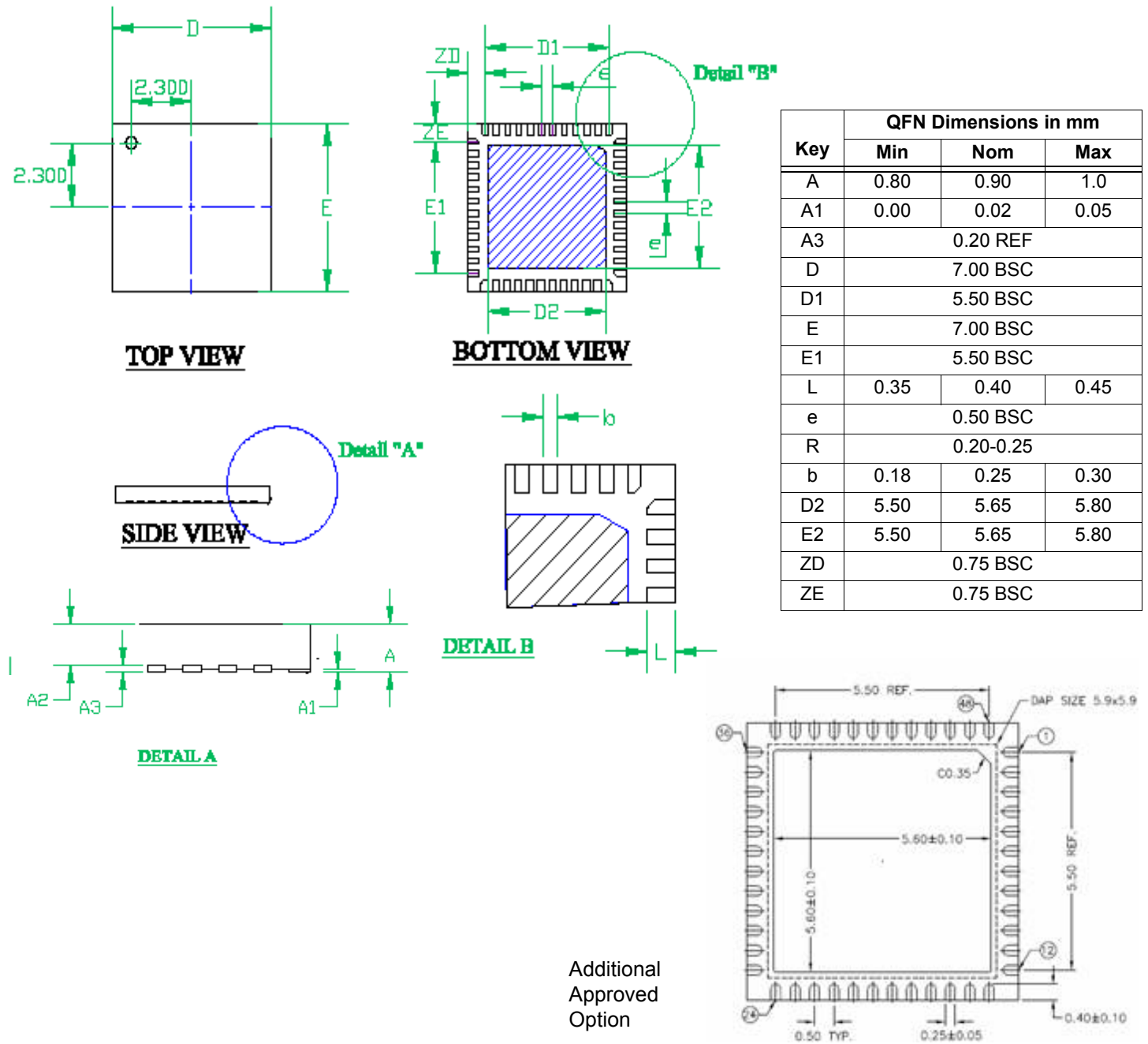


Figure 27. 48QFN Package Diagram

8.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices” (www.jedec.org/download).

| Profile Feature | Pb Free Assembly |
|---|--|
| Average Ramp-Up Rate ($T_{s_{max}} - T_p$) | 3 °C / second max |
| Preheat: Temperature Min ($T_{s_{min}}$) Temperature Max ($T_{s_{max}}$) Time ($t_{s_{min}} - t_{s_{max}}$) | 150 °C 200 °C 60 - 180 seconds |
| Time maintained above: Temperature (T_L) Time (t_L) | 217 °C 60 - 150 seconds |
| Peak / Classification Temperature (T_p) | See “Package Classification Reflow Temperatures” |
| Time within 5 °C of actual Peak Temperature (t_p) | 20 - 40 seconds |
| Ramp-Down rate | 6 °C / second max |
| Time 25 °C to Peak Temperature | 8 minutes max |

Note: All temperatures refer to topside of the package, measured on the package body surface.

Table 38. Standard Reflow Profile



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10. DOCUMENT REVISION HISTORY

| Revision | Date | Description of Change |
|----------|----------------|--|
| 0.5 | January 2010 | Initial release |
| 0.8 | March 2010 | Added widget details, front page feature bullet updates |
| 0.85 | June 2010 | Port E updated to add HPhnEn R/W bit in the Pin Cntrl widget and as HPCapable in the widget capabilities. Aux mode section updated to include additional information. |
| 0.9 | September 2010 | Added changes for YA silicon revision (ZA/ZB prior settings referenced) AFG EAPD bit added for PortE Headphone control. AFG ComJack bits added to select debounce time. Removed SCS support. Updated SPKVOL L/R step size to .75dB and changed register address from 04/05h to 01/02h. Added 3rd I2C register for updating speaker L and R volume at the same time (to match HDA implementation). Additional I2C register bits added/reordered to R17, R19, R39, R40, R41, R42. I2C Register R64 to R70 added. Removed pull up from pins 19/20. Updated conditions of performance characteristics, added HDA signalling voltage to condition for power measurements. Default changed on BTL/HD_Mode from 0 to 1. Updated Record Path behavior label for Aux mode. Added Pin Configuration Default Settings. Corrected Combo Jack diagram. |
| 0.91 | October 2010 | Updated LDO Level Control values. Corrected step size and thermal trip in BTL section. Clarified AuxMode section wording related to D3Cold entry. Added description text for High pass and Mono band pass filter features. |
| 0.92 | May 2011 | Corrected Sense A/B description and table. |
| 0.93 | June 2011 | Corrected front page bullet for BTL voltage and removed blank section 3. |
| 1.0 | October 2011 | Corrected Left vs Right channel for the EQ coefficients to match silicon. Updated electrical characteristics for typical values. Removed Preliminary. Removed comments related to ZA and ZB silicon since they were non-production. Added WB silicon widget items: ComboJackTiming in the AFG and ScStableTimeSel added to AFG AnaBTL. Added PVDD value for the digital maximum supply voltage and footnote to the GPIO characteristics for the Input Low and High Voltage. Added missing EAPD widget details. |
| 1.1 | January 2012 | Updated I2C registers with reset information. |
| 1.2 | March 2012 | Added ComboJackTime widget details and updated EAPD widget details. |
| 1.3 | June 2012 | Added THD+N setting to Class D Output power and 3W typical line. |
| 1.4 | February 2013 | Added Industrial temp package option for revisions WC and beyond. |

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SINGLE CHIP PC AUDIO SYSTEM, CODEC+SPEAKER AMPLIFIER+CAPLESS HP+LDO



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