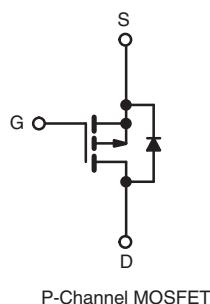
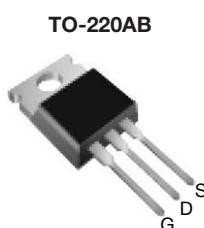


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 100	
$R_{DS(on)}$ (Ω)	$V_{GS} = - 10$ V	0.20
Q_g (Max.) (nC)	61	
Q_{gs} (nC)	14	
Q_{gd} (nC)	29	
Configuration	Single	



P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC


RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRF9540PbF SiHF9540-E3
SnPb	IRF9540 SiHF9540

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 100	
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	- 19	A
		- 13	
Pulsed Drain Current ^a	I_{DM}	- 72	
Linear Derating Factor		1.0	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	640	mJ
Repetitive Avalanche Current ^a	I_{AR}	- 19	A
Repetitive Avalanche Energy ^a	E_{AR}	15	mJ
Maximum Power Dissipation	P_D	150	W
Peak Diode Recovery dV/dt ^c	dV/dt	- 5.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = - 25$ V, starting $T_J = 25$ °C, $L = 2.7$ mH, $R_g = 25 \Omega$, $I_{AS} = - 19$ A (see fig. 12).

c. $I_{SD} \leq - 19$ A, $dI/dt \leq 200$ A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

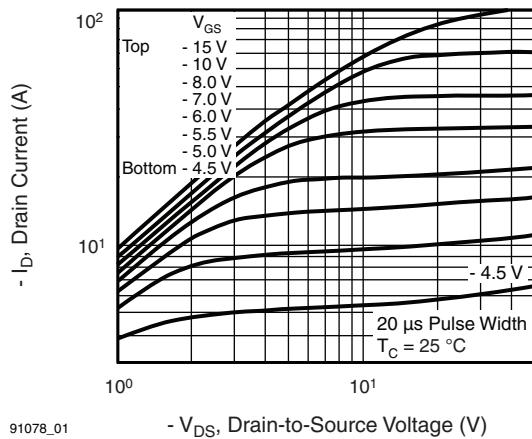
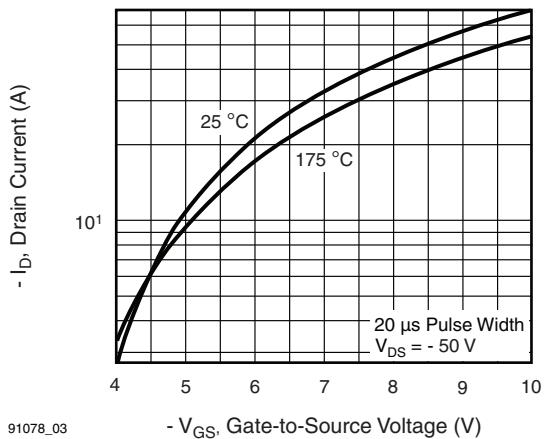
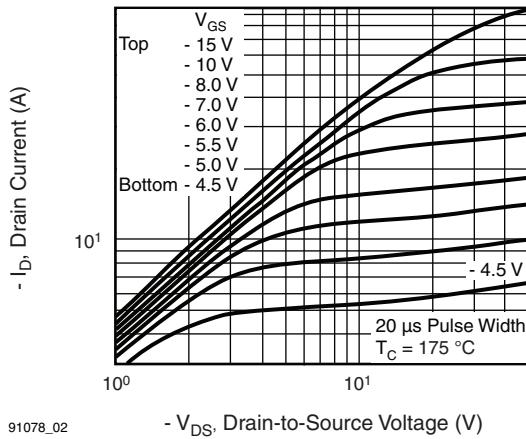
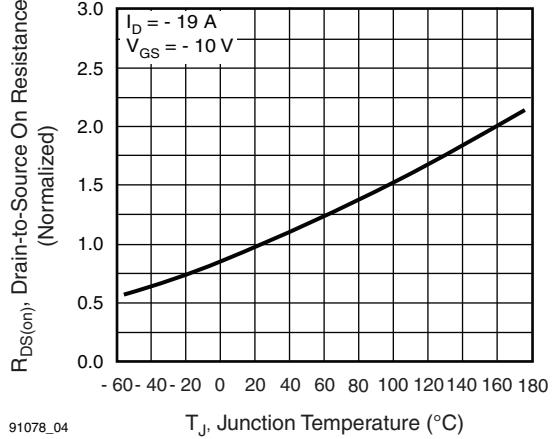
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

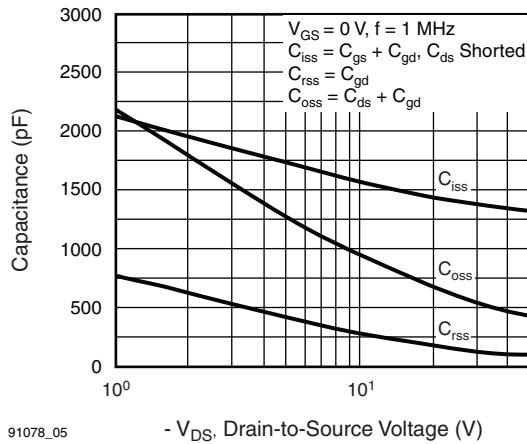
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = -250 \mu\text{A}$		-100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = -1 \text{ mA}$		-	-0.087	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	-100	μA
		$V_{DS} = -80 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 150^\circ\text{C}$		-	-	-500	
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}$	$I_D = -11 \text{ A}^b$	-	-	0.20	Ω
Forward Transconductance	g_{fs}	$V_{DS} = -50 \text{ V}$, $I_D = -11 \text{ A}^b$		6.2	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = -25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	1400	-	pF
Output Capacitance	C_{oss}			-	590	-	
Reverse Transfer Capacitance	C_{rss}			-	140	-	
Total Gate Charge	Q_g	$V_{GS} = -10 \text{ V}$	$I_D = -19 \text{ A}$, $V_{DS} = -80 \text{ V}$, see fig. 6 and 13 ^b	-	-	61	nC
Gate-Source Charge	Q_{gs}			-	-	14	
Gate-Drain Charge	Q_{gd}			-	-	29	
Turn-On Delay Time	$t_{d(on)}$			-	16	-	
Rise Time	t_r	$V_{DD} = -50 \text{ V}$, $I_D = -19 \text{ A}$, $R_g = 9.1 \Omega$, $R_D = 2.4 \Omega$, see fig. 10 ^b		-	73	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	34	-		
Fall Time	t_f		-	57	-		
Internal Drain Inductance	L_D		-	4.5	-	nH	
Internal Source Inductance	L_S	Between lead, 6 mm (0.25") from package and center of die contact		-	7.5		-
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-19	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	-72	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}$, $I_S = -19 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	-5.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_F = -19 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	130	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.35	0.70	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

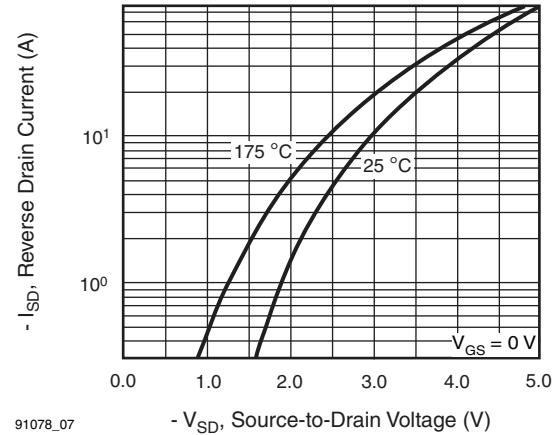
b. Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ C$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ C$

Fig. 4 - Normalized On-Resistance vs. Temperature



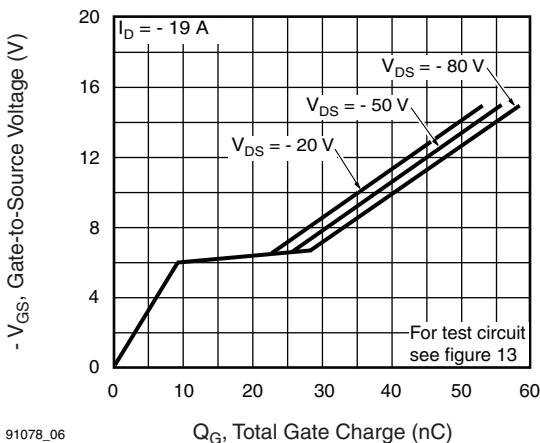
91078_05 - V_{DS} , Drain-to-Source Voltage (V)

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



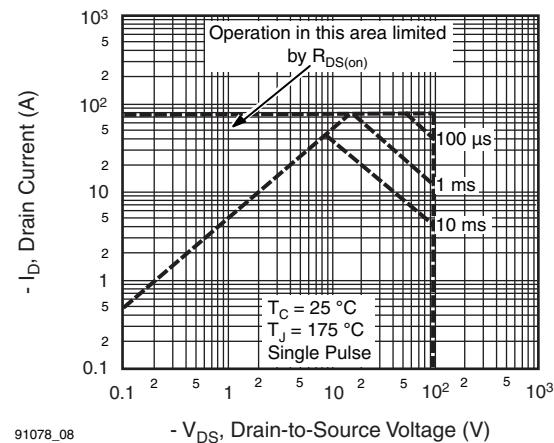
91078_07 - V_{SD} , Source-to-Drain Voltage (V)

Fig. 7 - Typical Source-Drain Diode Forward Voltage



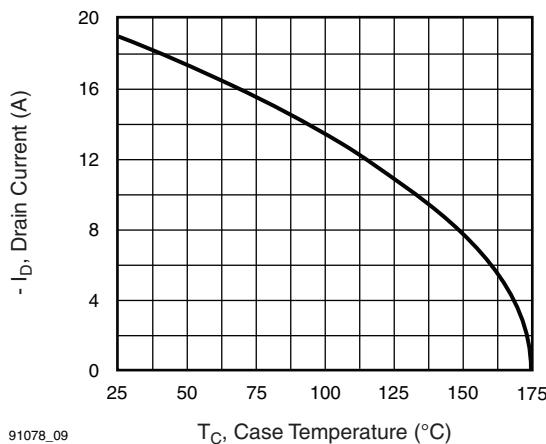
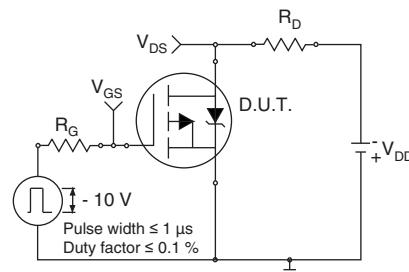
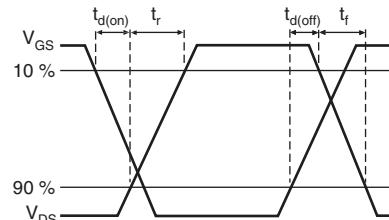
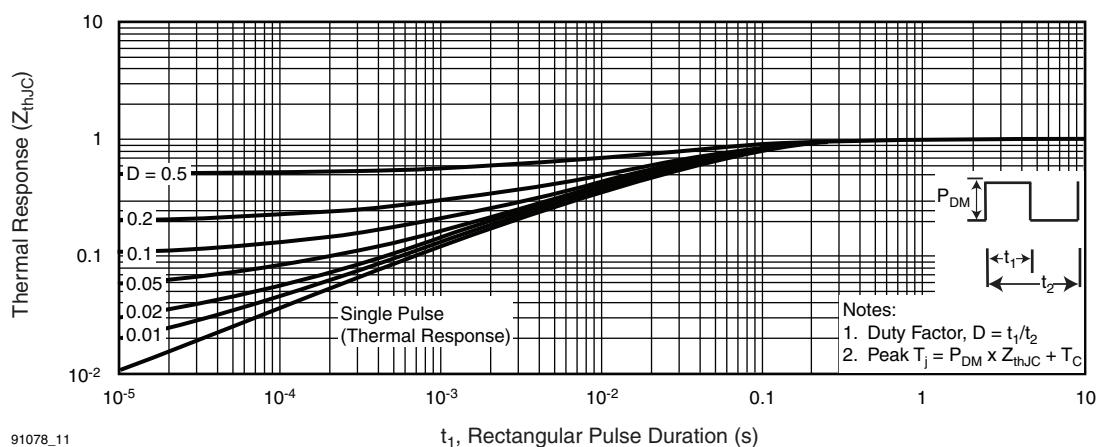
91078_06 Q_G , Total Gate Charge (nC)

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



91078_08 - V_{DS} , Drain-to-Source Voltage (V)

Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

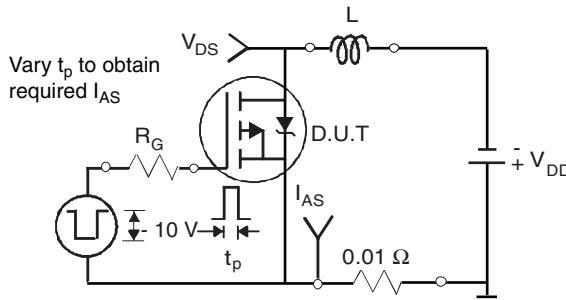


Fig. 12a - Unclamped Inductive Test Circuit

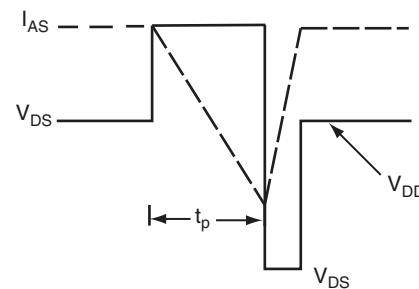


Fig. 12b - Unclamped Inductive Waveforms

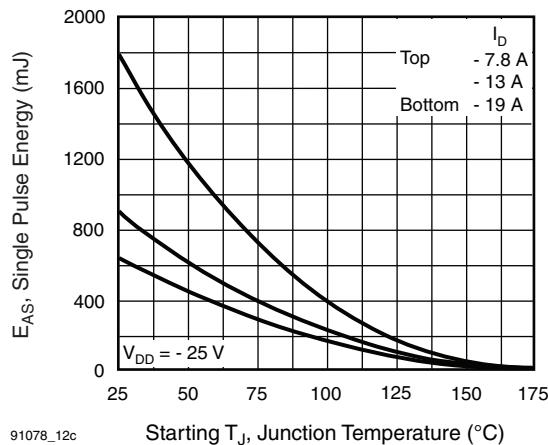


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

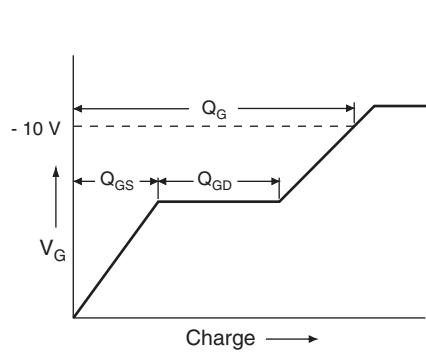


Fig. 13a - Basic Gate Charge Waveform

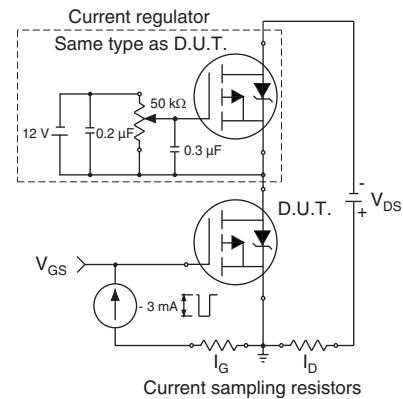
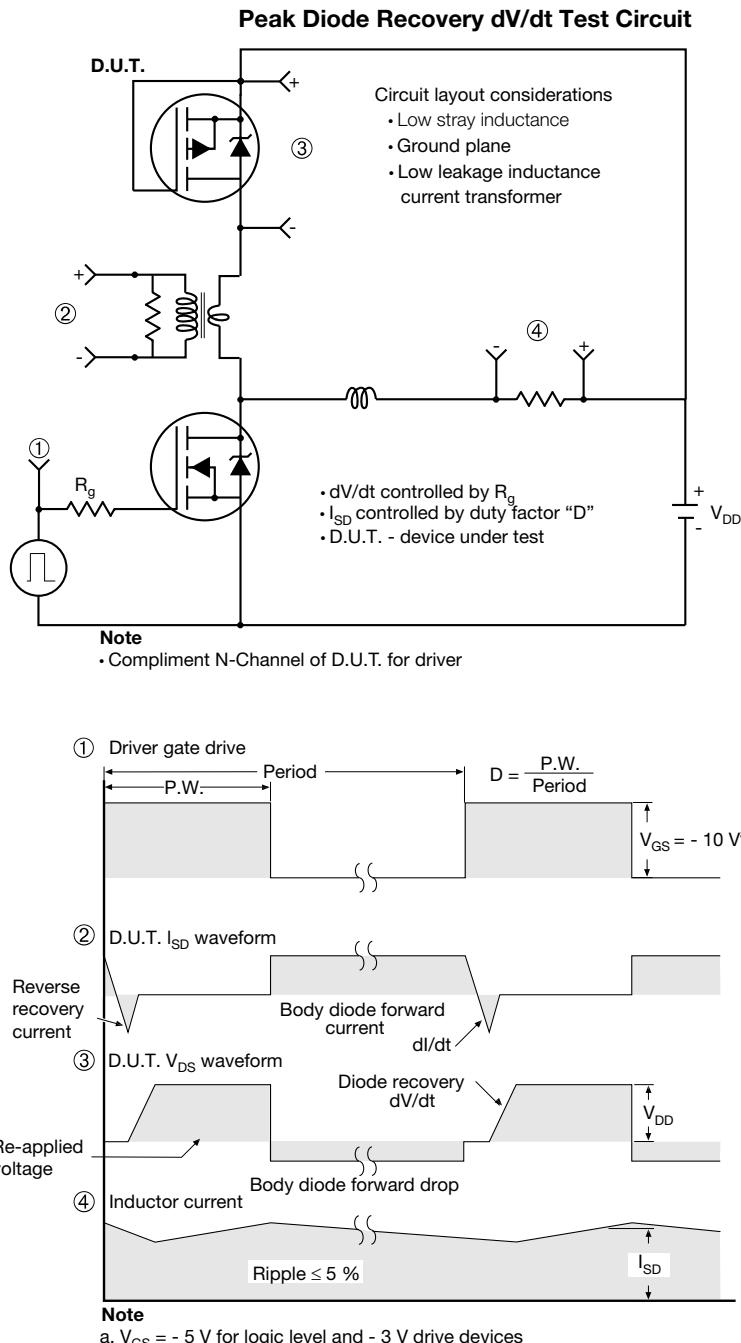
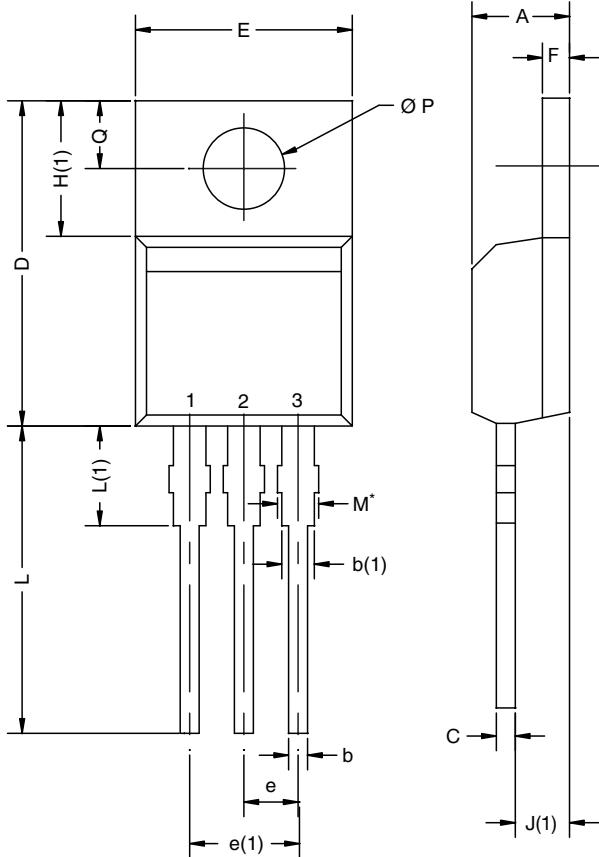


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For P-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91078.

TO-220AB

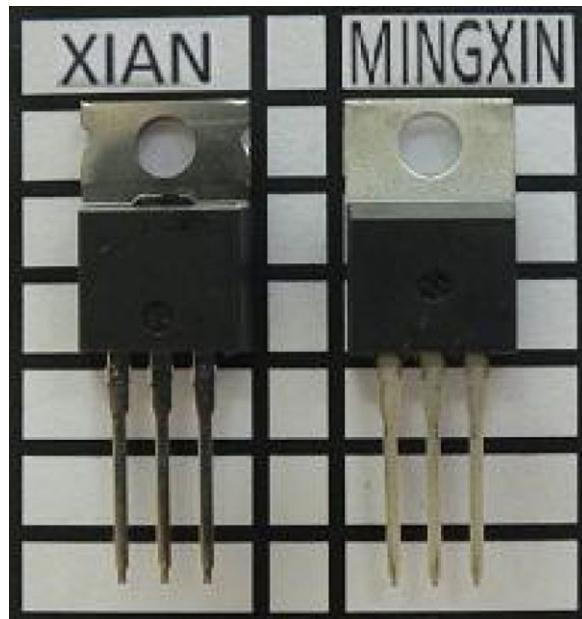


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

- Xi'an and Mingxin actual photo





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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Экспресс доставка в любую точку России;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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