

### Characteristics

Parameter	Rating	Units
AC Operating Voltage	20-240	$V_{rms}$
Load Current		
With 5°C/W Heat Sink	20	$A_{rms}$
No Heat Sink	5	
On-State Voltage Drop	1.1	$V_P$ (at $I_L=2A_P$ )
Blocking Voltage	800	$V_P$
Thermal Impedance, Junction-to-Case, $\theta_{JC}$	0.35	°C/W

### Features

- Load Current up to  $20A_{rms}$  with 5°C/W Heat Sink
- 800V<sub>P</sub> Blocking Voltage
- 5mA Control Current
- Zero-Cross Switching
- Isolated, Low Thermal Impedance Ceramic Pad for Heat Sink Applications
- 2500V<sub>rms</sub> Isolation, Input to Output
- DC Control, AC Output
- Optically Isolated
- Low EMI and RFI Generation
- High Noise Immunity
- Flammability Rating UL 94 V-0

### Applications

- Programmable Control
- Process Control
- Power Control Panels
- Remote Switching
- Gas Pump Electronics
- Contactors
- Large Relays
- Solenoids
- Motors
- Heaters

### Approvals

- UL 508 Recognized Component: File E69938

### Description

CPC1998J is an AC Solid State Switch utilizing dual power SCR outputs. This device also includes zero-cross turn-on circuitry and is specified with an 800V<sub>P</sub> blocking voltage.

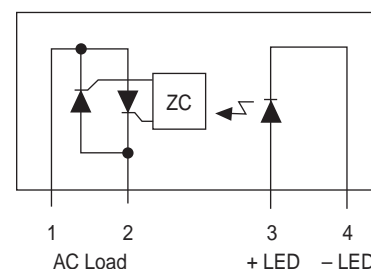
Tightly controlled zero-cross circuitry ensures low noise switching of AC loads by minimizing the generation of transients. The optically coupled input and output circuits provide exceptional noise immunity and 2500V<sub>rms</sub> of isolation between the control and the output. As a result, the CPC1998 is well suited for industrial environments where electromagnetic interference would disrupt the operation of plant facility communications and control systems.

The unique i4-PAC package pioneered by IXYS allows Solid State Relays to achieve the highest load current and power ratings. This package features a unique IXYS process in which the silicon chips are soft soldered onto the Direct Copper Bond (DCB) substrate instead of the traditional copper leadframe. The DCB ceramic, the same substrate used in high power modules, not only provides 2500V<sub>rms</sub> isolation but also very low junction-to-case thermal impedance (0.35 °C/W).

### Ordering Information

Part	Description
CPC1998J	i4-PAC Package (25 per tube)

### Pin Configuration



## 1 Specifications

### 1.1 Absolute Maximum Ratings @ 25°C

Symbol	Min	Max	Units
Blocking Voltage	-	800	V <sub>P</sub>
Reverse Input Voltage	-	5	V
Input Control Current	-	50	mA
Peak (10ms)	-	1	A
Input Power Dissipation <sup>1</sup>	-	150	mW
Total Power Dissipation <sup>2</sup>	-	3.5	W
I <sup>2</sup> t for Fusing (1/2 Sine Wave, 60Hz)	-	200	A <sup>2</sup> s
Isolation Voltage, Input to Output	-	2500	V <sub>rms</sub>
ESD, Human Body Model	-	8	kV
Operational Temperature	- 40	+85	°C
Storage Temperature	- 40	+125	°C

<sup>1</sup> Derate linearly 1.33mW / °C.

<sup>2</sup> Free air, no heat sink.

*Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

*Typical values are characteristic of the device at +25°C, and are the result of engineering evaluations. They are provided for information purposes only, and are not part of the manufacturing testing requirements.*

### 1.2 Electrical Characteristics @ 25°C

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
<b>Output Characteristics</b>						
Load Current	No Heat Sink, V <sub>L</sub> =20-240V <sub>rms</sub> T <sub>C</sub> =25°C	I <sub>L</sub>	0.1	-	5	A <sub>rms</sub>
Continuous			0.1	-	50	
Maximum Surge Current	1/2 Sine Wave, 60Hz	I <sub>P</sub>	-	-	150	A
Off-State Leakage Current	V <sub>L</sub> =800V	I <sub>LEAK</sub>	-	-	100	μA <sub>P</sub>
On-State Voltage Drop <sup>1</sup>	I <sub>L</sub> =2A <sub>P</sub>	-	-	0.85	1.1	V <sub>P</sub>
Off-State dV/dt	I <sub>F</sub> =0mA	dV/dt	1000	-	-	V/μs
Switching Speeds	I <sub>F</sub> =5mA	t <sub>on</sub>	-	-	0.5	cycles
Turn-On		t <sub>off</sub>	-	-	0.5	
Zero-Cross Turn-On Voltage <sup>2</sup>	1 <sup>st</sup> half-cycle	-	-	5	20	V
	subsequent half-cycle	-	-	-	5	
Holding Current	-	I <sub>H</sub>	-	44	50	mA
Latching Current	-	I <sub>L</sub>	-	48	75	mA
Operating Frequency	-	-	20	-	500	Hz
Load Power Factor for Guaranteed Turn-On <sup>3</sup>	f=60Hz	PF	0.25	-	-	-
<b>Input Characteristics</b>						
Input Control Current to Activate <sup>4</sup>	I <sub>L</sub> =1A Resistive, f=60Hz	I <sub>F</sub>	-	-	5	mA
Input Dropout Voltage	-	-	0.8	-	-	V
Input Voltage Drop	I <sub>F</sub> =5mA	V <sub>F</sub>	0.9	1.2	1.5	V
Reverse Input Current	V <sub>R</sub> =5V	I <sub>R</sub>	-	-	10	μA
<b>Input/Output Characteristics</b>						
Capacitance, Input-to-Output	V <sub>IO</sub> =0V, f=1MHz	C <sub>IO</sub>	-	-	3	pF

<sup>1</sup> Tested at a peak value equivalent.

<sup>2</sup> Zero-cross first half-cycle @ < 100Hz.

<sup>3</sup> Snubber circuits may be required at low power factors.

<sup>4</sup> For high-noise environments, or high-frequency operation (>60Hz), or for applications with a high inductive load, a minimum LED drive current of 10mA is recommended.

## 2 Thermal Characteristics

Parameter	Conditions	Symbol	Rating	Units
Thermal Impedance (Junction to Case)	-	$\theta_{JC}$	0.35	$^{\circ}\text{C/W}$
Thermal Impedance (Junction to Ambient)	Free Air	$\theta_{JA}$	33	$^{\circ}\text{C/W}$
Junction Temperature (Operating)	-	$T_J$	-40 to +125	$^{\circ}\text{C}$

### 2.1 Thermal Management

Device high current characterization was performed using Kunze heat sink KU 1-159, phase change thermal interface material KU-ALC 5, and transistor clip KU 4-499/1. This combination provided an approximate junction-to-ambient thermal impedance of 12.5 $^{\circ}\text{C/W}$ .

### 2.2 Heat Sink Calculation

Higher load currents are possible by using lower thermal impedance heat sink combinations.

#### Heat Sink Rating

$$\theta_{CA} = \frac{(T_J - T_A)}{P_D} - \theta_{JC}$$

$T_J$  = Junction Temperature ( $^{\circ}\text{C}$ ),  $T_J \leq 125^{\circ}\text{C}$  \*

$T_A$  = Ambient Temperature ( $^{\circ}\text{C}$ )

$\theta_{JC}$  = Thermal Impedance, Junction to Case ( $^{\circ}\text{C/W}$ ) = 0.35 $^{\circ}\text{C/W}$

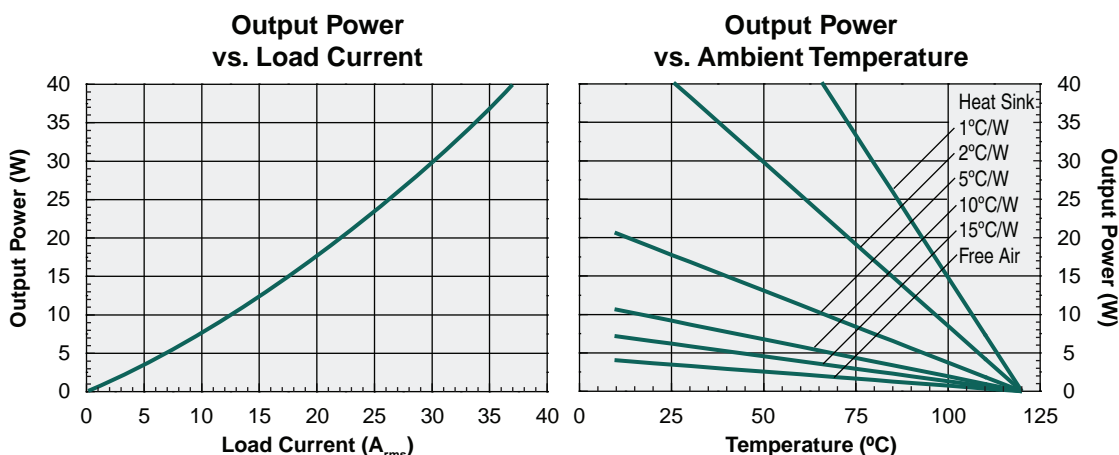
$\theta_{CA}$  = Thermal Impedance of Heat Sink & Thermal Interface Material, Case to Ambient ( $^{\circ}\text{C/W}$ )

$P_D$  = On-State Voltage ( $V_{rms}$ ) • Load Current ( $A_{rms}$ )

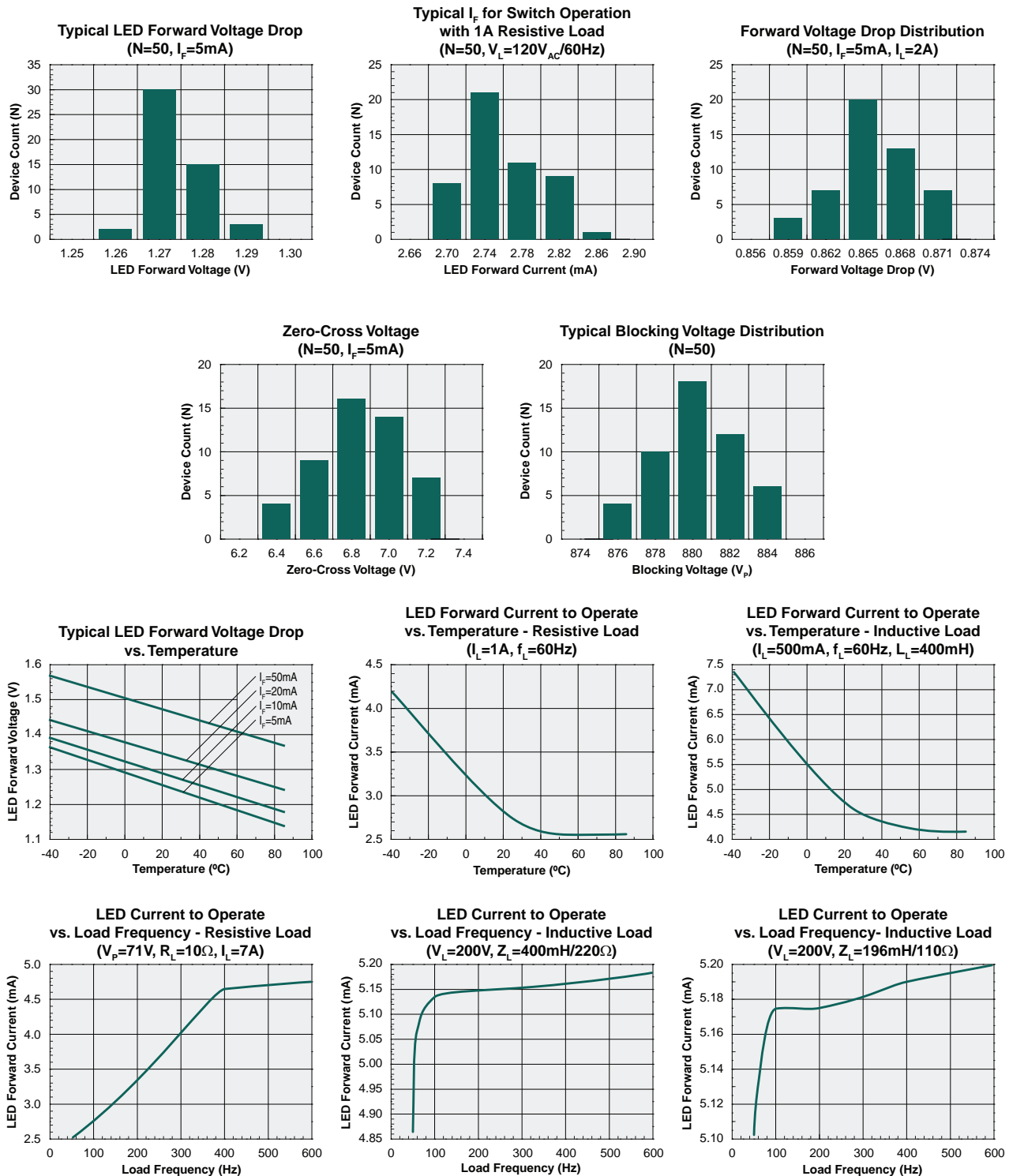
\* Elevated junction temperature reduces semiconductor lifetime.

**NOTE:** The exposed surface of the DCB substrate is not to be soldered.

### 2.3 Thermal Performance Data

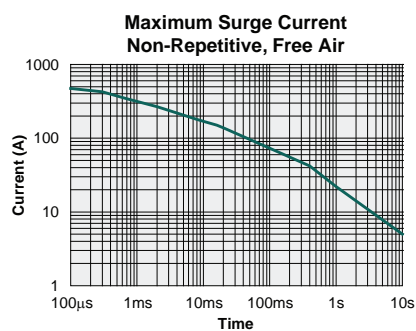
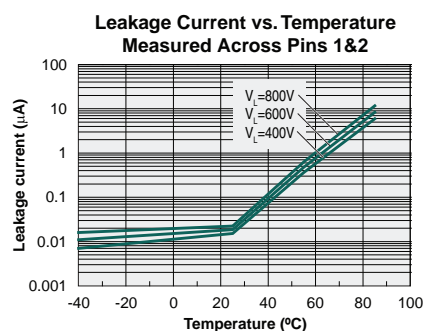
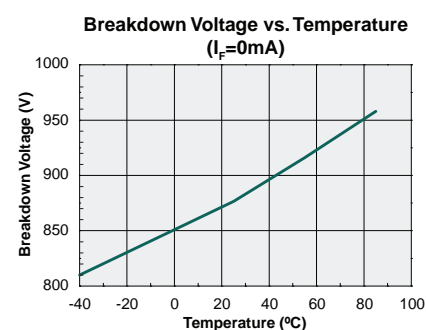
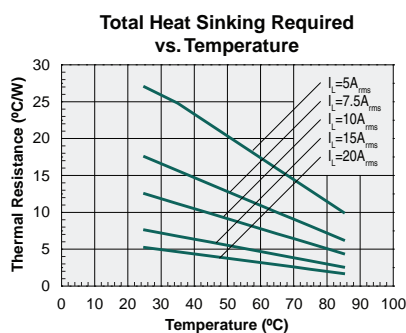
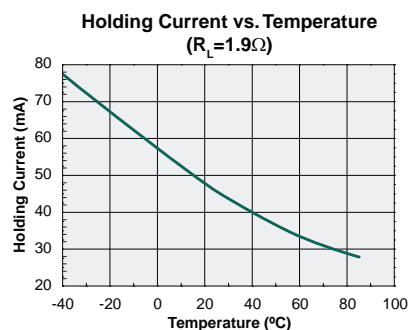
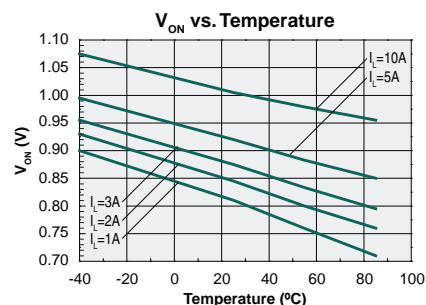
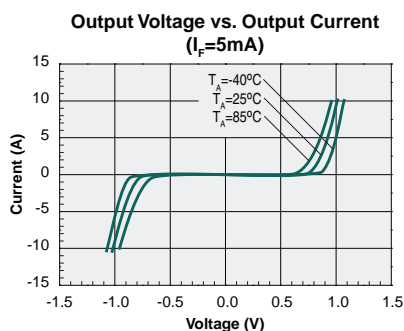
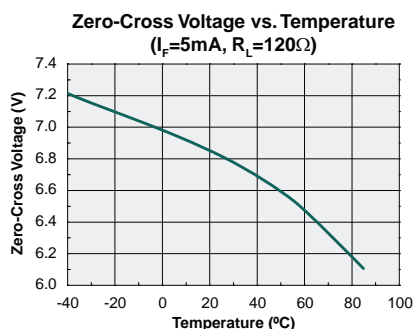


### 3 Performance Data\*



\*Unless otherwise noted, data presented in these graphs is typical of device operation at  $25^{\circ}\text{C}$ .

For guaranteed parameters not indicated in the written specifications, please contact our application department.



\*Unless otherwise noted, data presented in these graphs is typical of device operation at 25°C.  
For guaranteed parameters not indicated in the written specifications, please contact our application department.

## 4 Manufacturing Information

### 4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
CPC1998J	MSL 1

### 4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

### 4.3 Soldering Profile

Provided in the table below is the Classification Temperature ( $T_C$ ) of this product and the maximum dwell time the body temperature of this device may be ( $T_C - 5$ )°C or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of **J-STD-020** must be observed.

Device	Classification Temperature ( $T_C$ )	Dwell Time ( $t_p$ )	Max Reflow Cycles
CPC1998J	245°C	30 seconds	1

**NOTE:** The exposed surface of the DCB substrate is not to be soldered.

### 4.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.



Technical drawing of a DCB substrate showing top, side, and bottom views with dimensions in mm and inches.

**Top View Dimensions:**

- Overall width:  $19.914 \pm 0.254$  (0.784 ± 0.010)
- Overall height:  $20.879 \pm 0.254$  (0.822 ± 0.010)
- Distance from top edge to mounting holes:  $20.396 \pm 0.508$  (0.803 ± 0.020)
- Distance between mounting holes:  $15.240 \pm 0.508$  (0.600 ± 0.020)
- Distance from bottom edge to mounting holes:  $2.362 \pm 0.381$  (0.093 ± 0.015)
- Distance from side edge to mounting holes:  $3.810 \pm 0.254$  (0.150 ± 0.010)

**Side View Dimensions:**

- Overall thickness:  $5.029 \pm 0.127$  (0.198 ± 0.005)
- Distance from top edge to mounting holes:  $1.181 \pm 0.076$  (0.047 ± 0.003)
- Distance from bottom edge to mounting holes:  $0.635 \pm 0.076$  (0.025 ± 0.003)
- Distance from side edge to mounting holes:  $2.794 \pm 0.127$  (0.110 ± 0.005)

**Bottom View Dimensions:**

- Overall width:  $17.221 \pm 0.254$  (0.678 ± 0.010)
- Overall height:  $15.317 \pm 0.254$  (0.603 ± 0.010)
- Distance from top edge to mounting holes:  $1.930 \pm 0.381$  (0.076 ± 0.015)
- Distance between mounting holes:  $1.270$  TYP (0.050 TYP)

**Notes:**

- DCB Substrate
- NOTE: Not to be soldered
- DIMENSIONS mm (inches)

**NOTE:** Metallized external surface of DCB substrate maintains 2500V<sub>rms</sub> isolation to device internal structure and all external pins.

Specification: DS-CPC1998-R06  
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- Защита от снятия компонента с производства.



#### Как с нами связаться

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