

## Internal 3.5A MOSFET Switching Regulator IC for Buck Converter

### ■ GENERAL DESCRIPTION

The **NJW4196** is a buck converter with **40V/3.5A** MOSFET.

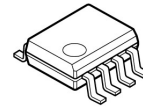
The transient response when a supply voltage rises from a reduced voltage is improved than conventional current mode products, therefore the **NJW4196** provides stable regulation characteristic even if application which an operating voltage fluctuates.

External Clock Synchronization function synchronizes oscillating frequency with external clock input.

Also, it has a soft start function, an external clock synchronization, an over current protection and a thermal shutdown circuit.

It is suitable for supplying power to a Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

### ■ PACKAGE OUTLINE



**NJW4196GM1**

### ■ FEATURES

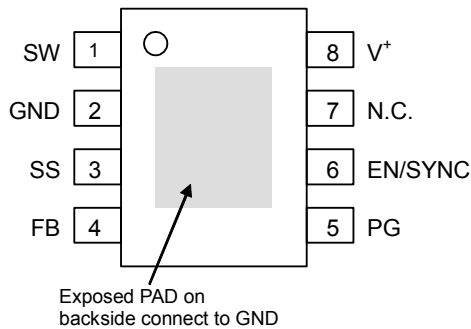
- Fast supply voltage transient response from a reduced voltage
- External Clock Synchronization
- Wide Operating Voltage Range      4.45V to 40V
- Switching Current                      5A min.
- Oscillating Frequency                A ver. Fixed 450kHz typ.  
    J ver . Adjustable TBD(100kHz) to TBD
- PWM Control
- Maximum Duty Cycle 100%
- Correspond to Ceramic Capacitor (MLCC)
- Adjustable Soft Start Function
- UVLO (Under Voltage Lockout)
- Over Current Protection (Hiccup type)
- Thermal Shutdown Protection
- Power Good Function
- Standby Function
- Package Outline                        NJW4196GM1 : HSOP8

### ■ PRODUCT CLASSIFICATION

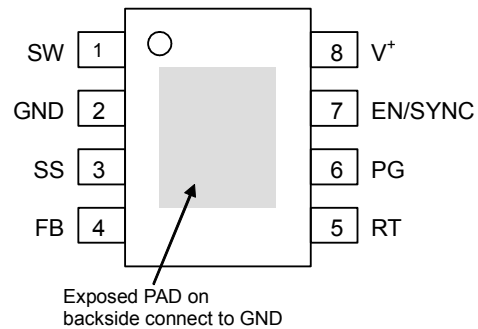
Part Number	Version	Oscillating Frequency	Operating Temperature Range
NJW4196GM1-A	A	Fixed 450kHz typ.	General Spec. -40°C to +125°C
NJW4196GM1-J (U.D.)	J	Adjustable TBD(100kHz) to TBD	General Spec. -40°C to +125°C

# NJW4196

## ■ PIN CONFIGURATION



**NJW4196GM1-A**

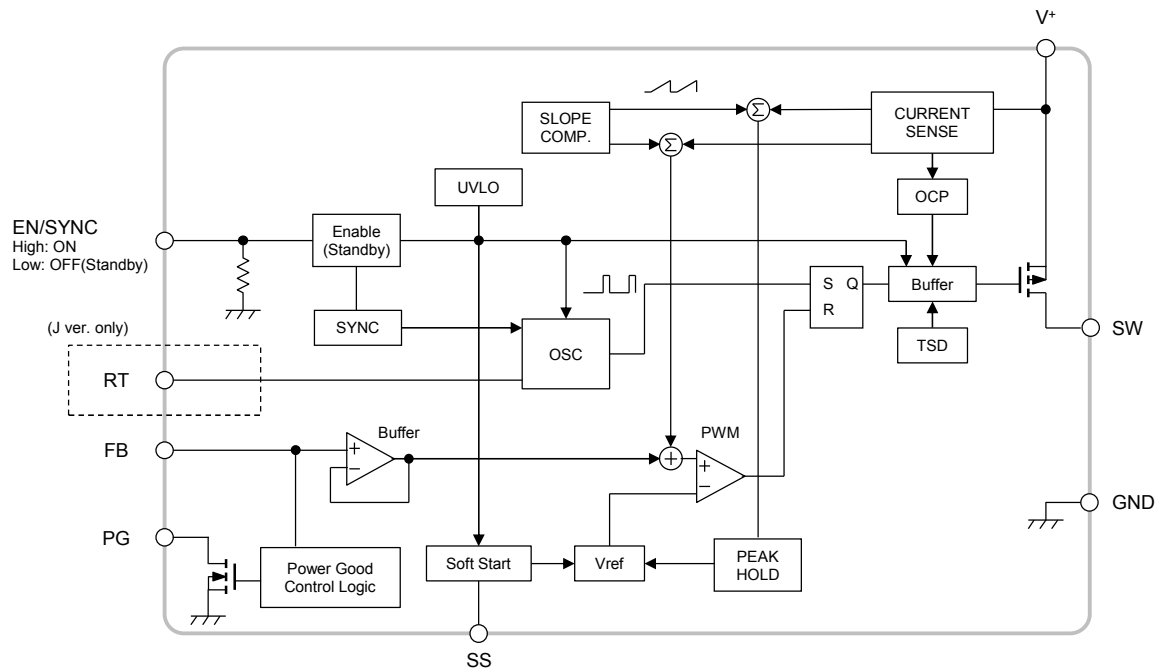


**NJW4196GM1-J  
(U.D.)**

## ■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER		FUNCTION
	A version	J version (U.D.)	
SW	1	1	Switch Output pin of Power MOSFET
GND	2	2	GND pin
SS	3	3	Soft Start timer setting pin. Soft start time is set by an external capacitor.
FB	4	4	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the FB pin become 1V.
RT	—	5	Oscillating Frequency Setting pin with an external Timing Resistor. Oscillating Frequency should set between TBD(100kHz) and TBD. (Only J version)
PG	5	6	Power Good pin. An open drain output that goes high impedance when the FB pin voltage is stable around $\pm 15\%$ .
EN/SYNC	6	7	Standby Control pin The EN/SYNC pin internally pulls down with 500k $\Omega$ . Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
N.C.	7	—	Non Connection (Only A version)
V <sup>+</sup>	8	8	Power Supply pin for Power Line
Exposed PAD	—	—	Connect to GND

## ■ BLOCK DIAGRAM



# NJW4196

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	-0.3~+45	V
V <sup>+</sup> - SW pin Voltage	V <sub>V-SW</sub>	+45	V
FB pin Voltage	V <sub>FB</sub>	-0.3~+6	V
PG pin Voltage	V <sub>PG</sub>	-0.3~+6	V
EN/SYNC pin Voltage	V <sub>EN/SYNC</sub>	-0.3~+45	V
Power Dissipation	P <sub>D</sub>	HSOP8      860 (*1) 2,900 (*2)	mW
Junction Temperature Range	T <sub>j</sub>	-40 to +150	°C
Operating Temperature Range	T <sub>opr</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-50 to +150	°C

(\*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(\*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)

Depending on conditions of the application, NJW4196 may not apply a max output current of it by a limit of the power consumption.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sup>+</sup>	4.45	–	40	V
Power Good pin Voltage	V <sub>PG</sub>	0	–	5.5	V
Timing Resistor (*3)	R <sub>T</sub>	TBD	–	TBD	kΩ
Oscillating Frequency (*3)	f <sub>osc</sub>	TBD (100)	–	TBD	kHz
External Clock Input Range	f <sub>SYNC</sub>	440	–	600	kHz
A version		0.9×f <sub>osc</sub>	–	1.3×f <sub>osc</sub>	
J version (U.D.)					

(\*3): Apply only the J version.

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+=V_{EN/SYNC}=12V$ ,  $T_a=25^\circ C$ , J version:  $R_T=TBD\ k\Omega$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Under Voltage Lockout Block</b>						
ON Threshold Voltage	$V_{T\_ON}$	$V^+=L \rightarrow H$	4.05	4.25	4.45	V
OFF Threshold Voltage	$V_{T\_OFF}$	$V^+=H \rightarrow L$	4.0	4.15	4.3	V
Hysteresis Voltage	$V_{HYS}$		70	100	—	mV

### Soft Start Block

Charge Current	$I_{CHG}$		3.5	4.0	4.5	$\mu A$
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### Oscillator Block

Oscillating Frequency (*4)	$f_{OSC\_A}$		405	450	495	kHz
Oscillating Frequency 1 (*5)	$f_{OSC1\_J}$	$R_T=TBDk\Omega$	270	300	330	kHz
Oscillating Frequency 2 (*5)	$f_{OSC2\_J}$	$R_T=TBDk\Omega$	TBD	TBD	TBD	kHz
Oscillating Frequency deviation (Supply voltage)	$f_{DV}$	$V^+=4.45V$ to $40V$	—	1	—	%
Oscillating Frequency deviation (Temperature)	$f_{DT}$	$T_a=-40^\circ C$ to $+85^\circ C$	—	5	—	%

(\*4): A version

(\*5): J version (U.D.)

### Buffer Block

Reference Voltage	$V_B$		-1.0%	1	+1.0%	V
Threshold Voltage	$V_{TH}$	$I_{SW}=3A$	-2.0%	1	+2.0%	V
Input Bias Current	$I_B$		-0.1	—	0.1	$\mu A$

### PWM Compare Block

Maximum Duty Cycle	$M_{AX}D_{UTY}$	$V_{FB}=0.9V$	—	—	100	%
Minimum ON Time	$t_{ON-min}$		—	125	185	ns

### OCP Block

COOL DOWN Time	$t_{COOL}$		—	75	—	ms
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### Output Block

Output ON Resistance	$R_{ON}$	$I_{SW}=3A$	—	0.125	0.25	$\Omega$
Switching Current Limit	$I_{LIM}$		5	6.5	8	A
SW Leak Current	$I_{LEAK}$	$V_{EN/SYNC}=0V$ , $V^+=40V$ , $V_{SW}=0V$	—	—	5	$\mu A$

### Standby Control / Sync Block

EN/SYNC pin High Threshold Voltage	$V_{TH\_EN/SYNC}$	$V_{EN/SYNC}=L \rightarrow H$	1.6	—	$V^+$	V
EN/SYNC pin Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC}=H \rightarrow L$	0	—	0.5	V
Input Bias Current (EN/SYNC pin)	$I_{EN/SYNC}$	$V_{EN/SYNC}=12V$	—	235	340	$\mu A$

# NJW4196

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+ = V_{EN/SYNC} = 12V$ ,  $T_a = 25^\circ C$ , J version:  $R_T = TBD\ k\Omega$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Good Block						
High Level Detection Voltage	$V_{THH\_PG}$	Measured at FB pin	110	115	120	%
Low Level Detection Voltage	$V_{THL\_PG}$	Measured at FB pin	80	85	90	%
Hysteresis Region	$V_{HYS\_PG}$		–	2	–	%
Power Good ON Resistance	$R_{ON\_PG}$	$I_{PG} = 10mA$	–	45	60	$\Omega$
Leak Current at OFF State	$I_{LEAK\_PG}$	$V_{PG} = 6V$	–	–	0.1	$\mu A$

## General Characteristics

Quiescent Current	$I_{DD}$	$R_L = \text{no load}, V_{FB} = 0.9V$	–	3.5	4.2	mA
Standby Current	$I_{DD\_STB}$	$V_{EN/SYNC} = 0V$	–	–	3	$\mu A$

## ■ THERMAL CHARACTERISTICS

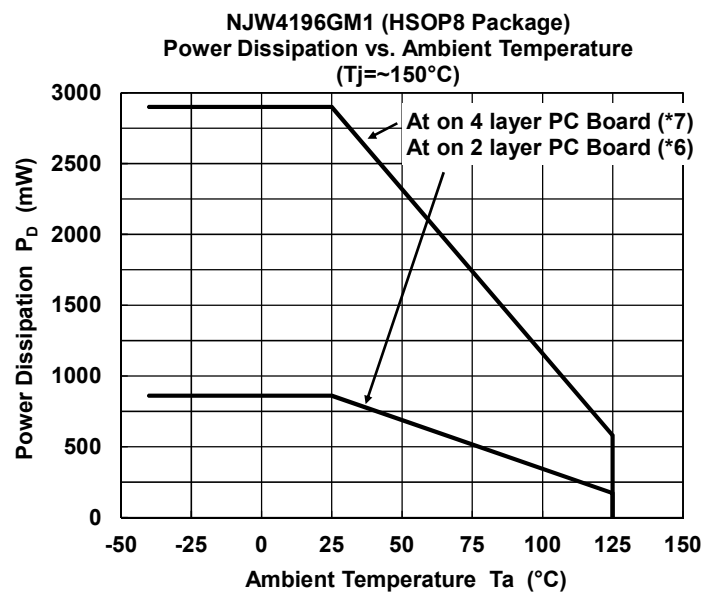
PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance	$\theta_{ja}$	145 (*6)	$^\circ C/W$
		43 (*7)	
Junction-to-Top of package characterization parameter	$\psi_{jt}$	28 (*6)	$^\circ C/W$
		12 (*7)	

(\*6): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

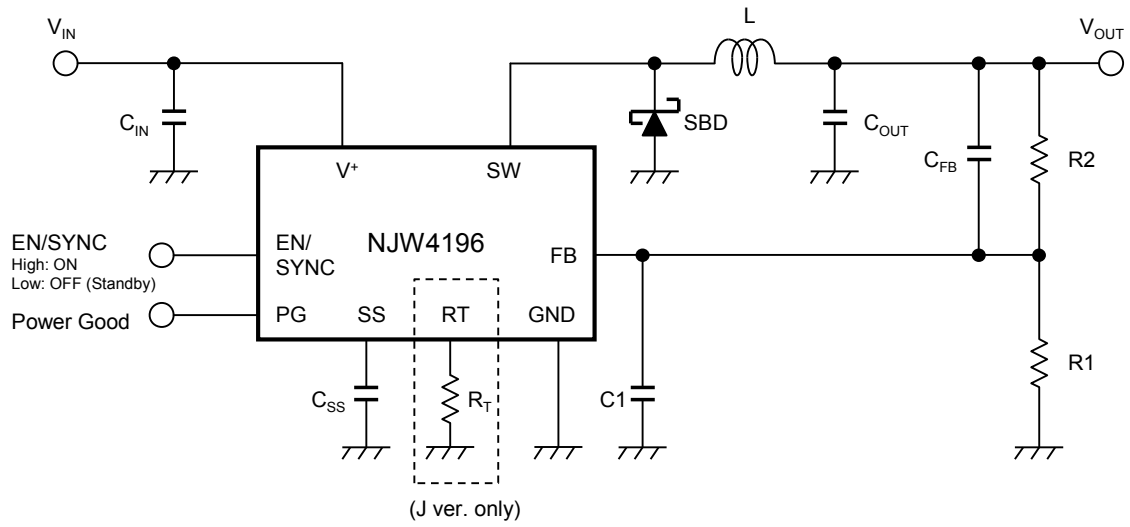
(\*7): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)

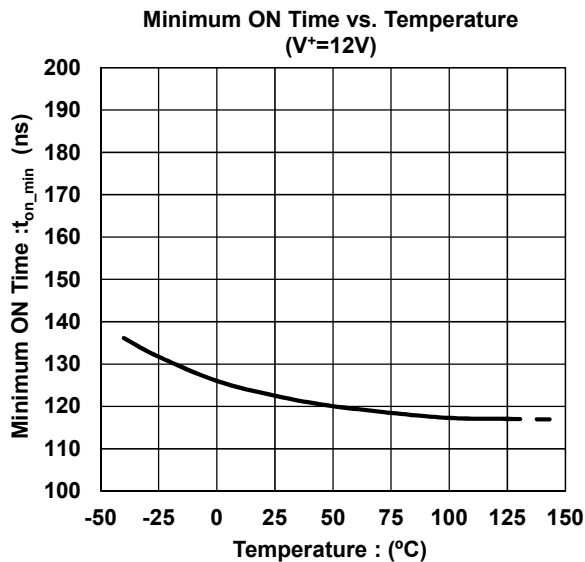
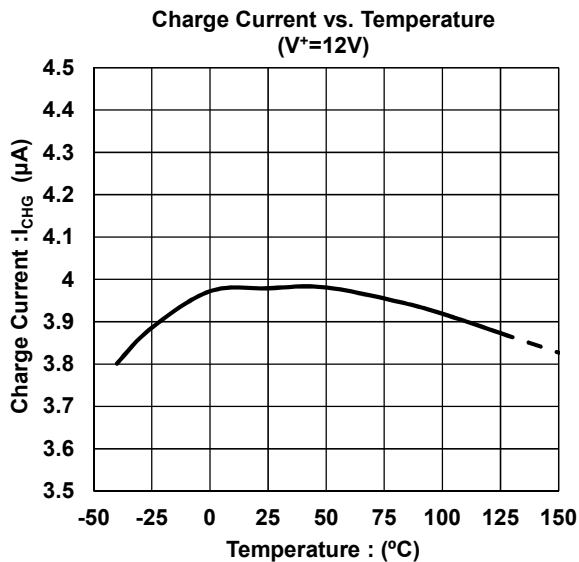
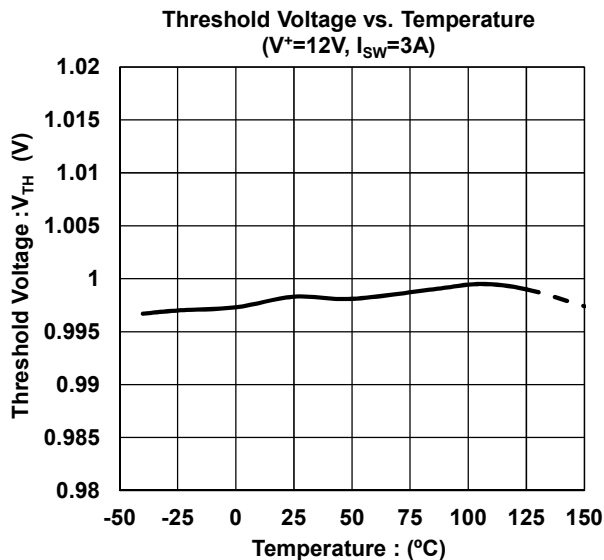
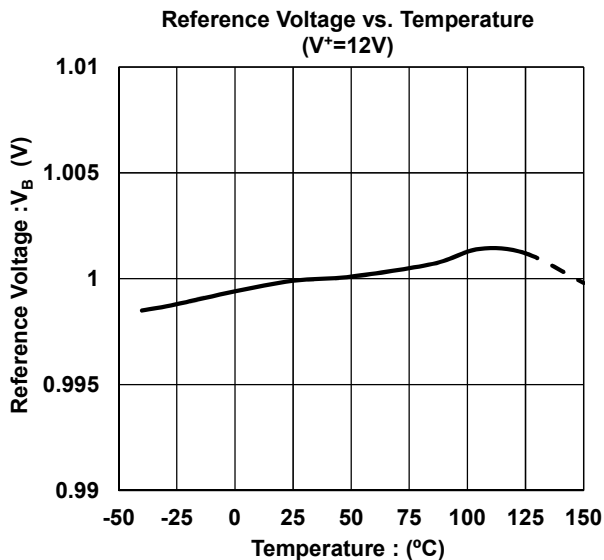
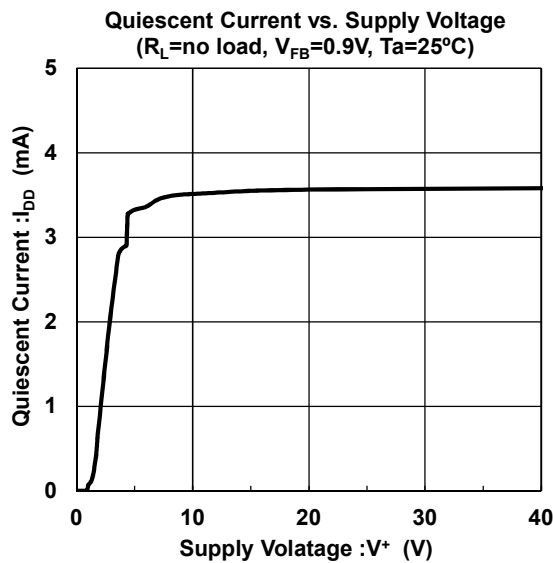
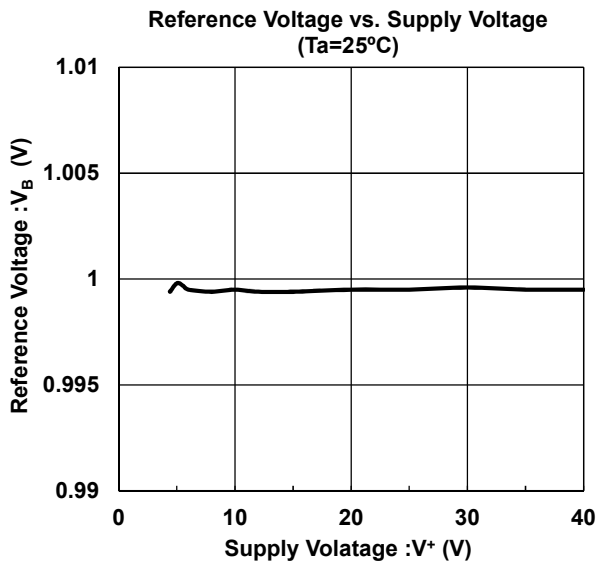
## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



## ■ TYPICAL APPLICATIONS

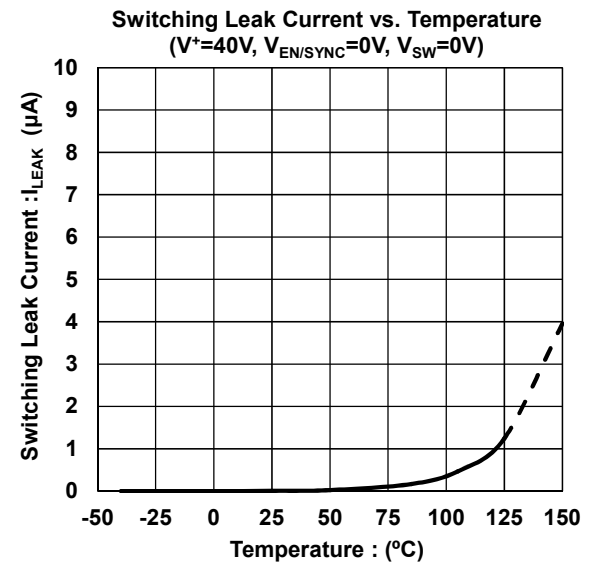
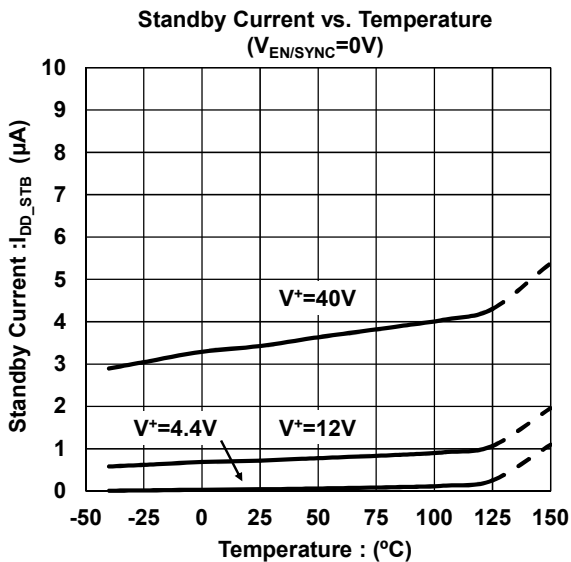
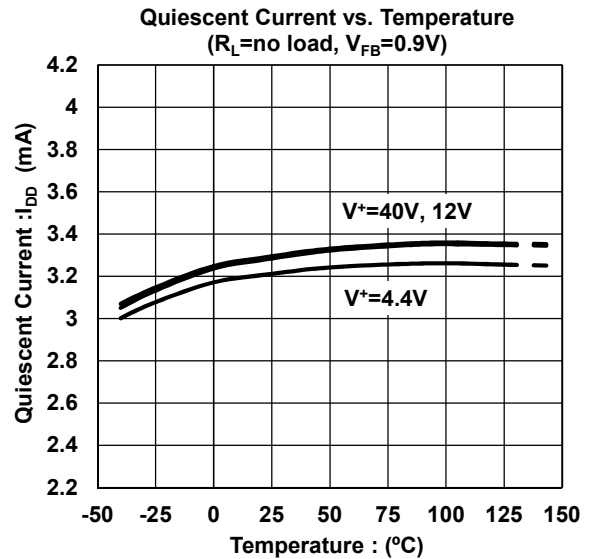
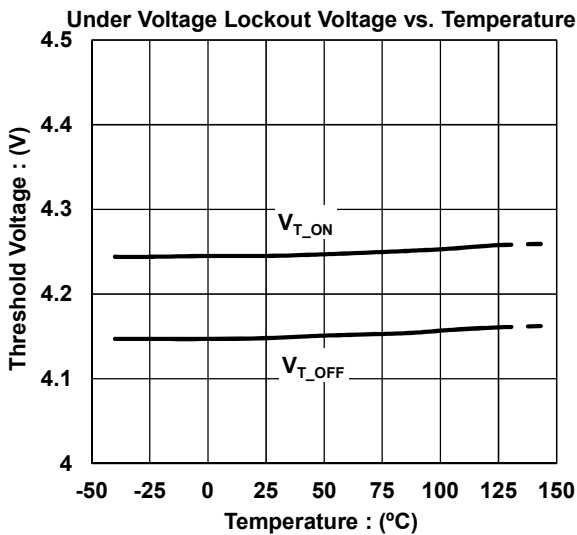
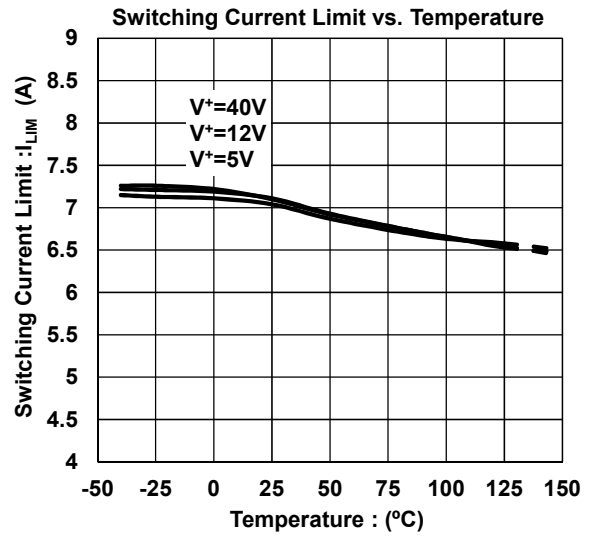
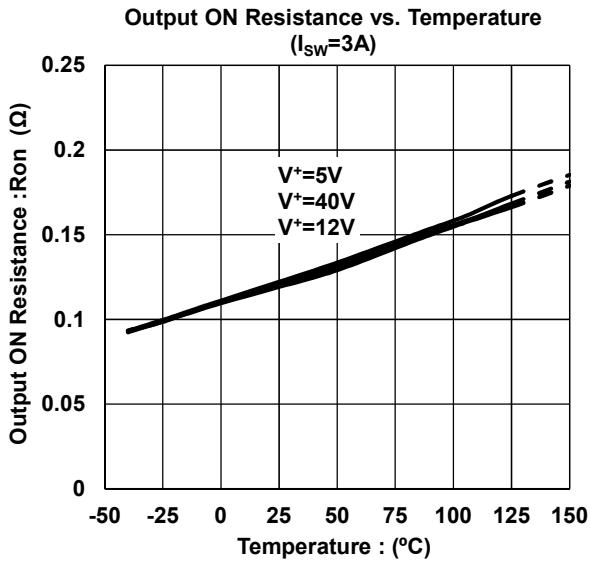


## ■ TYPICAL CHARACTERISTICS (A, J version)

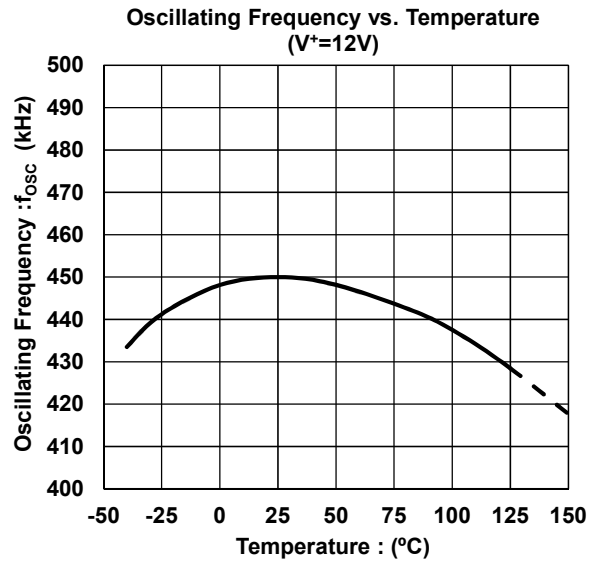
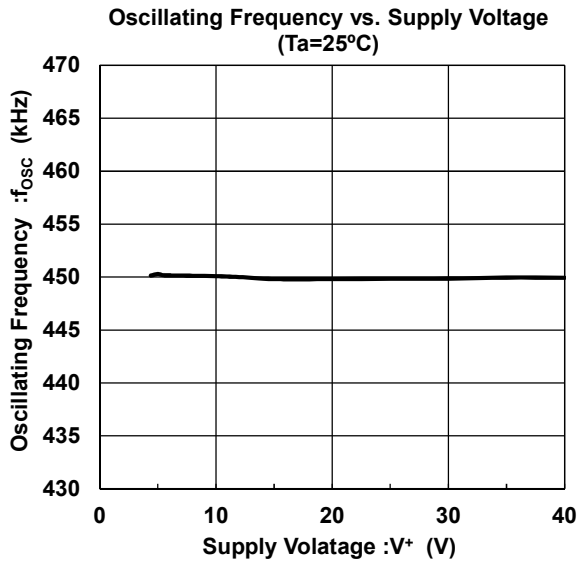




## ■ TYPICAL CHARACTERISTICS (A, J version)



## ■ TYPICAL CHARACTERISTICS (A version)



# MEMO

**[CAUTION]**

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