

MRF10502



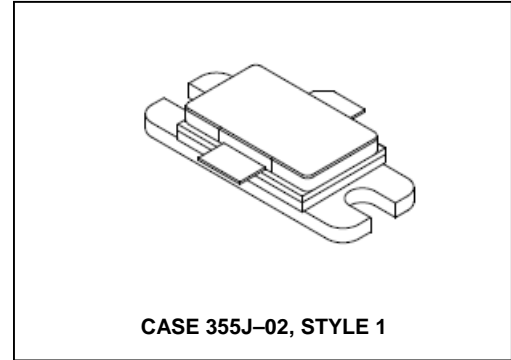
Microwave Pulse Power Silicon NPN Transistor
500W (peak), 1025–1150MHz

M/A-COM Products
 Released - Rev. 07.07

Product Image

Designed for 1025–1150 MHz pulse common base amplifier applications such as TCAS, TACAN and Mode-S transmitters.

- Guaranteed performance @ 1090 MHz
 Output power = 500 W peak
 Gain = 8.5 dB min, 9.0 dB (typ.)
- 100% tested for load mismatch at all phase angles with 10:1 VSWR
- Hermetically sealed industry package
- Silicon nitride passivated
- Gold metalized, emitter ballasted for long life and resistance to metal migration
- Internal input and output matching
- Characterized with 10 μ s, 1% duty cycle pulses



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CES}	65	Vdc
Collector–Base Voltage	V _{CBO}	65	Vdc
Emitter–Base Voltage	V _{EBO}	3.5	Vdc
Collector Current — Peak (1)	I _C	29	Adc
Total Device Dissipation @ T _C = 25°C (1), (2) Derate above 25°C	P _D	1460 8.3	Watts W/°C
Storage Temperature Range	T _{stg}	–65 to +200	°C
Junction Temperature	T _J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case (3)	R _{θJC}	0.12	°C/W

NOTES:

1. Under pulse RF operating conditions.
2. These devices are designed for RF operation. The total device dissipation rating applies only when the devices are operated as pulsed RF amplifiers.
3. Thermal Resistance is determined under specified RF operating conditions by infrared measurement techniques. (Worst case θ_{JC} value measured @ 32 μ s, 2%.)

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage (I _C = 60 mAdc, V _{BE} = 0)	V _{(BR)CES}	65	—	—	Vdc
Collector–Base Breakdown Voltage (I _C = 60 mAdc, I _E = 0)	V _{(BR)CBO}	65	—	—	Vdc
Emitter–Base Breakdown Voltage (I _E = 10 mAdc, I _C = 0)	V _{(BR)EBO}	3.5	—	—	Vdc
Collector Cutoff Current (V _{CB} = 36 Vdc, I _E = 0)	I _{CBO}	—	—	25	mAdc

ON CHARACTERISTICS

DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	20	—	—	—
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FUNCTIONAL TESTS

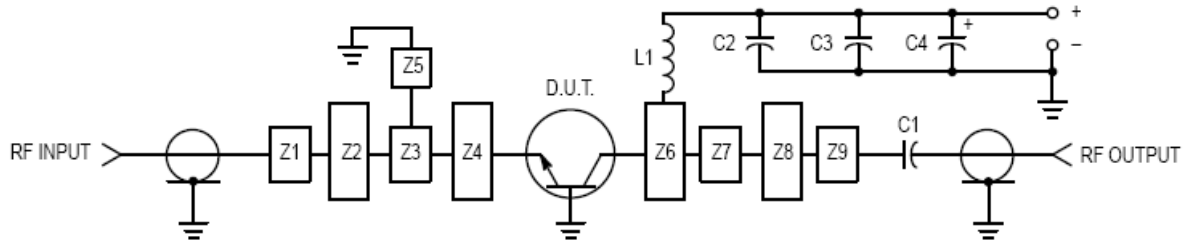
Common–Base Amplifier Power Gain (V _{CC} = 50 Vdc, P _{out} = 500 W Peak, f = 1090 MHz)	G _{PB}	8.5	9.0	—	dB
Collector Efficiency (V _{CC} = 50 Vdc, P _{out} = 500 W Peak, f = 1090 MHz)	η	40	45	—	%
Load Mismatch (V _{CC} = 50 Vdc, P _{out} = 500 W Peak, f = 1090 MHz, VSWR = 10:1 All Phase Angles)	ψ	No Degradation in Output Power			

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- C1 — 82 pF 100 Mil Chip Capacitor
- C2 — 39 pF 100 Mil Chip Capacitor
- C3 — 0.1 μ F
- C4 — 100 μ F, 100 Vdc, Electrolytic
- L1 — 3 Turns #18 AWG, 1/8" ID, 0.18 Long

- Z1–Z9 — Microstrip, See Details
- Board Material — Teflon, Glass Laminate
- Dielectric Thickness = 0.030"
- $\epsilon_r = 2.55$, 2 Oz. Copper

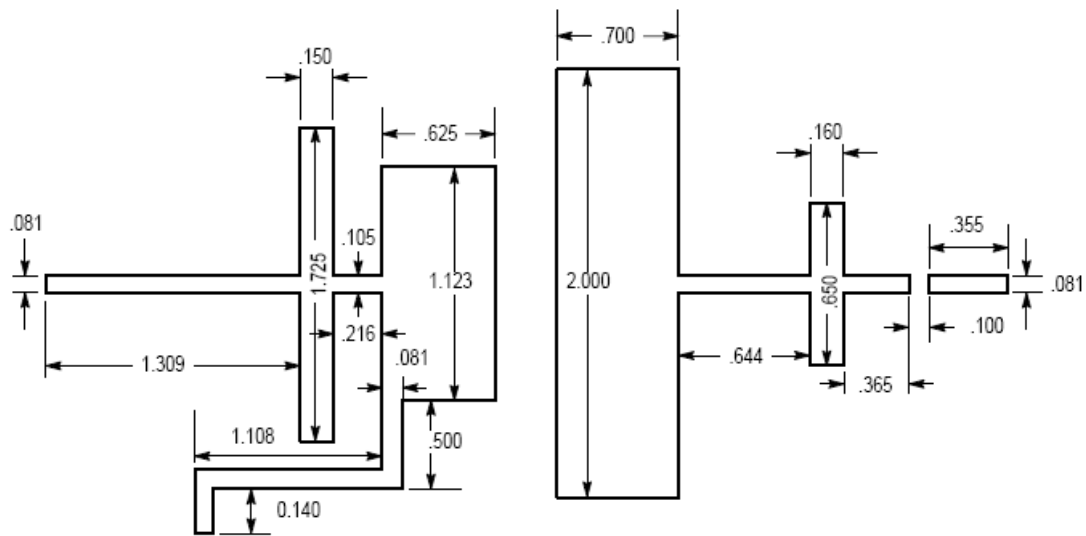


Figure 1. Test Circuit

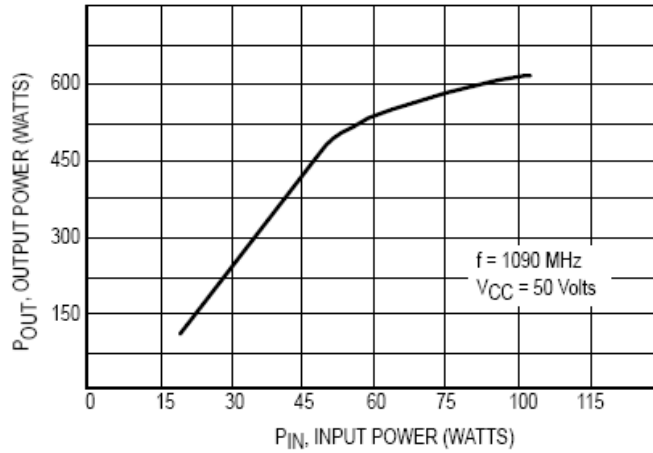
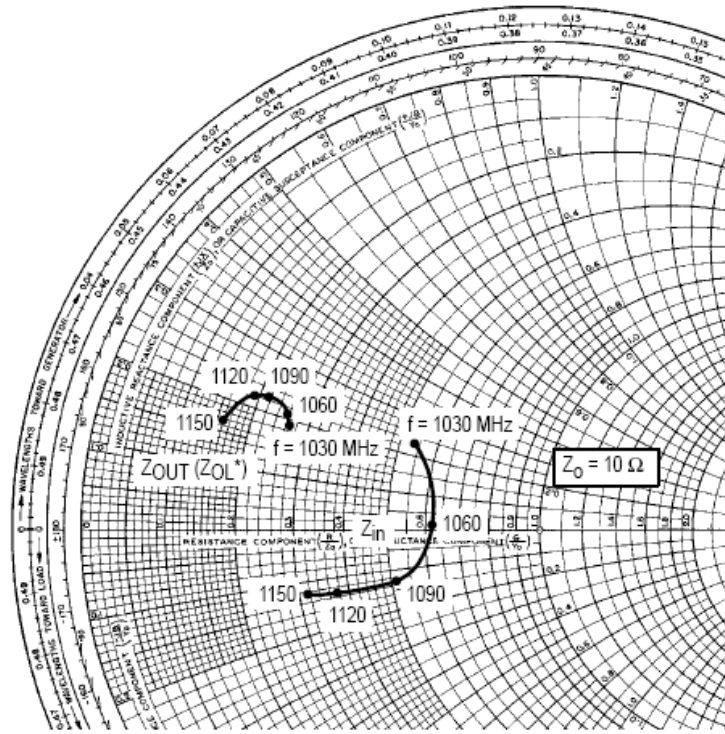


Figure 2. Output Power versus Input Power



$P_{OUT} = 500 \text{ W Pk}$ $V_{CC} = 50 \text{ V}$

f MHz	Z_{in} OHMS	$Z_{OL}^* (Z_{OUT})$ OHMS
1030	$5.3 + j2.25$	$2.6 + j1.89$
1060	$6.2 + j0.2$	$2.56 + j2.0$
1090	$5.2 - j1.4$	$2.12 + j2.2$
1120	$3.7 - j1.35$	$1.9 + j2.15$
1150	$3.15 - j1.3$	$1.6 + j1.62$

Z_{OL}^* is the conjugate of the optimum load impedance into which the device operates at a given output power voltage and frequency.

Figure 3. Series Equivalent Input/Output Impedances

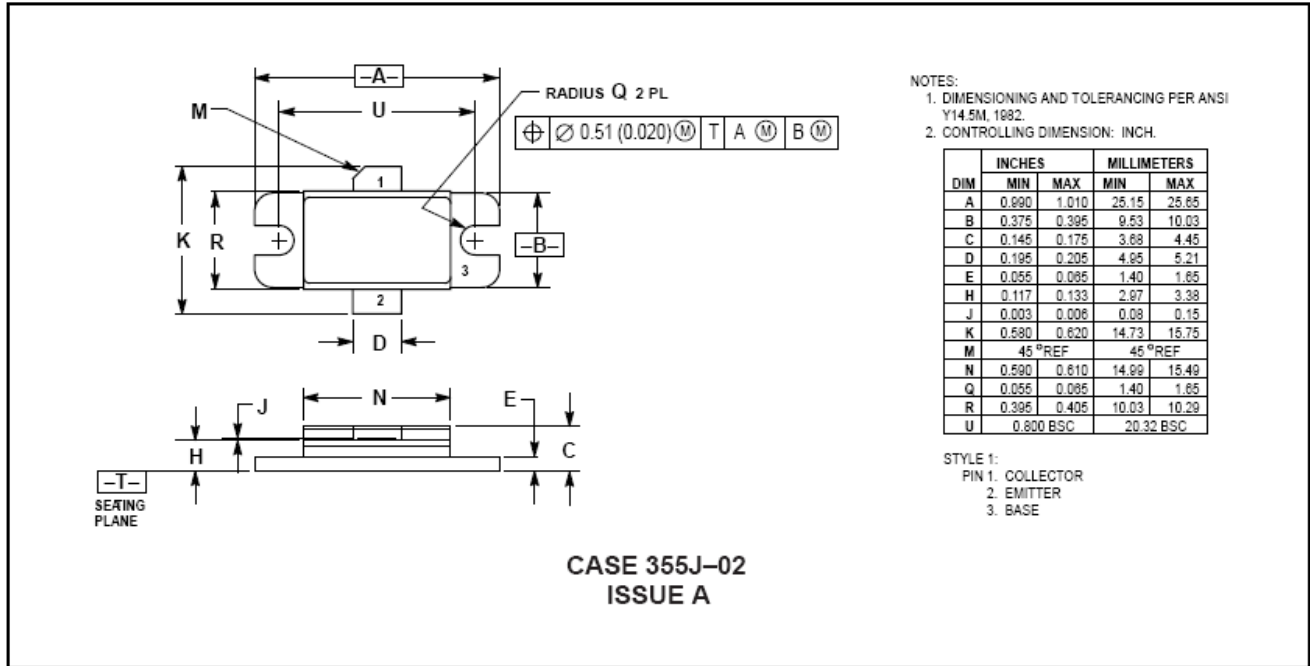
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