PLL Frequency Synthesizer

Data Sheet

ADF4107

FEATURES

- 7.0 GHz bandwidth
- 2.7 V to 3.3 V power supply
- Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
- Programmable dual-modulus prescaler 8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- Programmable antibacklash pulse width
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode

APPLICATIONS

- Broadband wireless access
- Satellite systems
- Instrumentation
- Wireless LANs
- Base stations for wireless radio

GENERAL DESCRIPTION

The ADF4107 frequency synthesizer can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual-modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R counter), allows selectable REF_{IN} frequencies at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

FUNCTIONAL BLOCK DIAGRAM

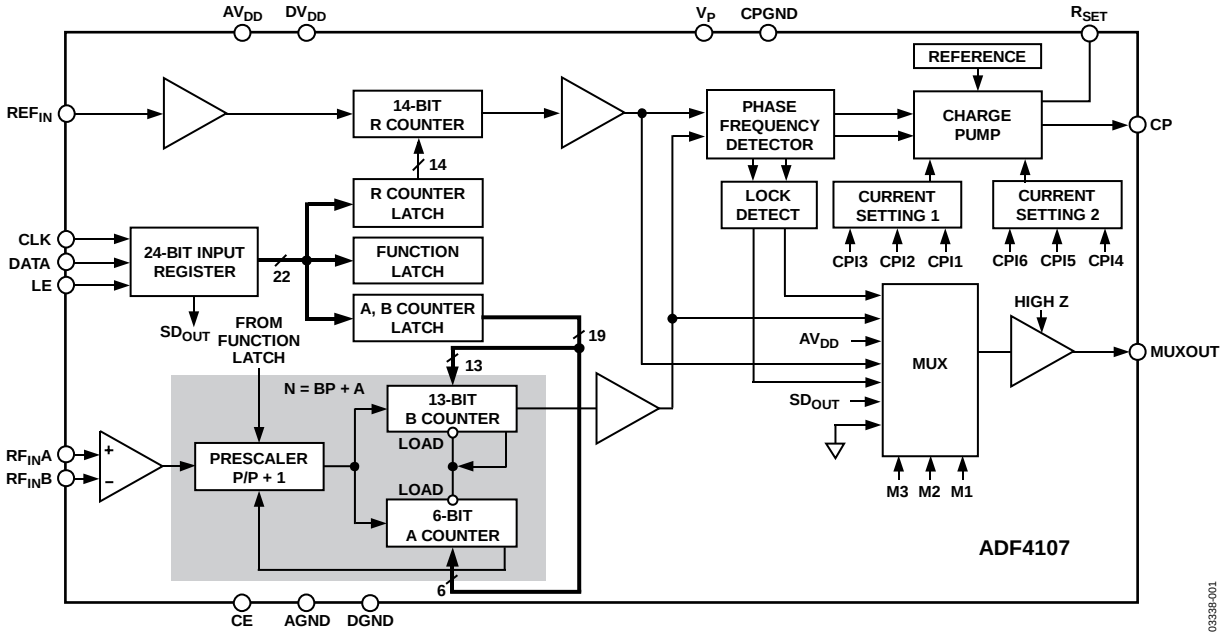


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/13—Rev. C to Rev. D

Changed $RF_{IN}A$ to $RF_{IN}B$ Parameter from ±320 mV to ±600 mV, Table 3 ... 5
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

11/12—Rev. B to Rev. C

Changed EVAL-ADF411xEBZ1 to EV-ADF411XSD1Z ... 4
Changes to Table 3 ... 5
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

9/11—Rev. A to Rev. B

Changes to Normalized Phase Noise Floor (PNSYNTH) Parameter, Table 1 ... 3
Added Normalized 1/f Noise (PN1_f) Parameter and Endnote 11, Table 1 ... 3
Changed EVAL-ADF4107EB1 to EVAL-ADF411xEBZ1 ... 4
Changes to Figure 4 and Table 4 ... 6
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

4/07—Rev. 0 to Rev. A

Updated Format ... Universal
Changes to REFIN Characteristics Section ... 3
Changes to Noise Characteristics Section ... 4
Changes to Absolute Maximum Ratings Section ... 5
Changes to Figure 23 ... 12
Changes to Ordering Guide ... 20

5/03—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	B Chips[2] (Typ)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency (RF_{IN})[3]	1.0/7.0	1.0/7.0	GHz min/max	See Figure 18 for input circuit
RF Input Sensitivity	−5/+5	−5/+5	dBm min/max	
Maximum Allowable Prescaler Output Frequency[4]	300	300	MHz max	
REF_{IN} CHARACTERISTICS				
REF_{IN} Input Frequency	20/250	20/250	MHz min/max	For f < 20 MHz, ensure slew rate >50 V/µs
REF_{IN} Input Sensitivity[5]	0.8/V_{DD}	0.8/V_{DD}	V p-p min/max	Biased at $AV_{DD}/2$[6]
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[7]	104	104	MHz max	ABP = 0,0 (2.9 ns antibacklash pulse width)
CHARGE PUMP				Programmable; see Figure 25
I_{CP} Sink/Source				
High Value	5	5	mA typ	With R_{SET} = 5.1 kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With R_{SET} = 5.1 kΩ
R_{SET} Range	3.0 to 11	3.0 to 11	kΩ typ	See Figure 25
I_{CP} Three-State Leakage	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}	1.5	1.5	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5 V
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{IH}, Input High Voltage	1.4	1.4	V min	
V_{IL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}, I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	1.4	1.4	V min	Open-drain output chosen; 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	V_{DD} − 0.4	V_{DD} − 0.4	V min	CMOS output chosen
I_{OH}	100	100	µA max	
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	AV_{DD}/5.5	V min/V max	$AV_{DD} \le V_P \le 5.5$ V
I_{DD}[8] (AI_{DD} + DI_{DD})	17	15	mA max	15 mA typ
I_P	0.4	0.4	mA max	T_A = 25°C
Power-Down Mode[9] (AI_{DD} + DI_{DD})	10	10	µA typ	
NOISE CHARACTERISTICS				
Normalized Phase Noise Floor (PN_{SYNTH})[10]	−223	−223	dBc/Hz typ	PLL loop BW = 500 kHz, measured at 100 kHz offset
Normalized 1/f Noise (PN_{1_f})[11]	−122	−122	dBc/Hz typ	10 kHz offset; normalized to 1 GHz

Parameter	B Version[1]	B Chips[2] (Typ)	Unit	Test Conditions/Comments
Phase Noise Performance[12]				@ VCO output
900 MHz Output[13]	−93	−93	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
6400 MHz Output[14]	−76	−76	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
6400 MHz Output[15]	−83	−83	dBc/Hz typ	@ 1 kHz offset and 1 MHz PFD frequency
Spurious Signals				
900 MHz Output[13]	−90/−92	−90/−92	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
6400 MHz Output[14]	−65/−70	−65/−70	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
6400 MHz Output[15]	−70/−75	−70/−75	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD frequency

[1] Operating temperature range (B version) is −40°C to +85°C.
[2] The B chip specifications are given as typical values.
[3] Use a square wave for lower frequencies, below the minimum stated.
[4] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[5] $AV_{DD} = DV_{DD} = 3$ V.
[6] AC-coupling ensures $AV_{DD}/2$ bias.
[7] Guaranteed by design. Sample tested to ensure compliance.
[8] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 32; $RF_{IN} = 7.0$ GHz.
[9] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3.3$ V; R = 16,383; A = 63; B = 891; P = 32; $RF_{IN} = 7.0$ GHz.
[10] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value) and 10 log(F_{PFD}). $PN_{SYNTH} = PN_{TOT} - 20\log N - 10\log F_{PFD}$.
[11] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by $PN = PN_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[12] The phase noise is measured with the EV-ADF411xSD1Z evaluation board and the HP8562E spectrum analyzer. The spectrum analyzer provides the REF_{IN} for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
[13] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; offset frequency = 1 kHz; $f_{RF} = 900$ MHz; N = 4500; loop BW = 20 kHz.
[14] $f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; offset frequency = 1 kHz; $f_{RF} = 6400$ MHz; N = 32,000; loop BW = 20 kHz.
[15] $f_{REFIN} = 10$ MHz; $f_{PFD} = 1$ MHz; offset frequency = 1 kHz; $f_{RF} = 6400$ MHz; N = 6400; loop BW = 100 kHz.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3$ V ± 10%, $AV_{DD} \le V_P \le 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted. [1]

Table 2.

Parameter	Limit[2] (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK setup time
t_2	10	ns min	DATA to CLOCK hold time
t_3	25	ns min	CLOCK high duration
t_4	25	ns min	CLOCK low duration
t_5	10	ns min	CLOCK to LE setup time
t_6	20	ns min	LE pulse width

[1] Guaranteed by design but not production tested.
[2] Operating temperature range (B Version) is −40°C to +85°C.

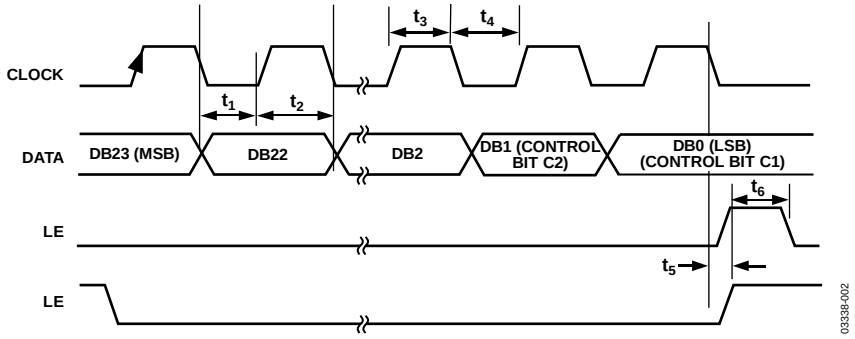


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±600 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

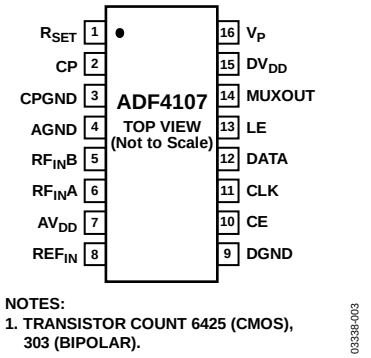


Figure 3. Pin Configuration, TSSOP

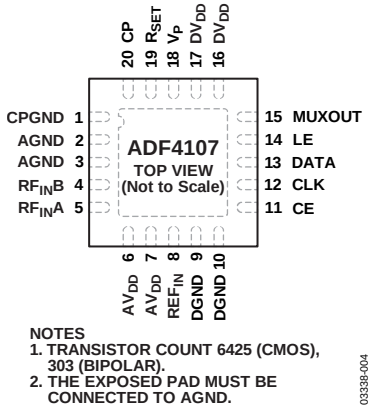


Figure 4. Pin Configuration, LFCSP

Table 4. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $I_{CP\,MAX} = \frac{25.5}{R_{SET}}$ so, with R_{SET} = 5.1 kΩ, $I_{CP\,MAX}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this pin provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 18.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This voltage may range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of V_{DD}/2 and a dc equivalent input resistance of 100 kΩ. See Figure 17. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This voltage should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5 V and used to drive a VCO with a tuning range of up to 5 V.
		EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ UNIT: GHz KEYWORD: R
PARAM TYPE: S IMPEDANCE: 50Ω
DATA FORMAT: MA

Freq.	MagS11	AngS11	Freq.	MagS11	AngS11
0.500	0.89148	-17.2820	3.800	0.44800	-130.399
0.600	0.88133	-20.6919	3.900	0.45223	-135.744
0.700	0.87152	-24.5386	4.000	0.45555	-142.766
0.800	0.85855	-27.3228	4.100	0.45313	-149.269
0.900	0.84911	-31.0698	4.200	0.45622	-154.884
1.000	0.83512	-34.8623	4.300	0.45555	-159.680
1.100	0.82374	-38.5574	4.400	0.46108	-164.916
1.200	0.80871	-41.9093	4.500	0.45325	-168.452
1.300	0.79176	-45.6990	4.600	0.45054	-173.462
1.400	0.77205	-49.4185	4.700	0.45200	-176.697
1.500	0.75696	-52.8898	4.800	0.45043	178.824
1.600	0.74234	-56.2923	4.900	0.45282	174.947
1.700	0.72239	-60.2584	5.000	0.44287	170.237
1.800	0.69419	-63.1446	5.100	0.44909	166.617
1.900	0.67288	-65.6464	5.200	0.44294	162.786
2.000	0.66227	-68.0742	5.300	0.44558	158.756
2.100	0.64758	-71.3530	5.400	0.45417	153.195
2.200	0.62454	-75.5658	5.500	0.46038	147.721
2.300	0.59466	-79.6404	5.600	0.47128	139.760
2.400	0.55932	-82.8246	5.700	0.47439	132.657
2.500	0.52256	-85.2795	5.800	0.48604	125.782
2.600	0.48754	-85.6298	5.900	0.50637	121.110
2.700	0.46411	-86.1854	6.000	0.52172	115.400
2.800	0.45776	-86.4997	6.100	0.53342	107.705
2.900	0.44859	-88.8080	6.200	0.53716	101.572
3.000	0.44588	-91.9737	6.300	0.55804	97.5379
3.100	0.43810	-95.4087	6.400	0.56362	93.0936
3.200	0.43269	-99.1282	6.500	0.58268	89.2227
3.300	0.42777	-102.748	6.600	0.59248	86.3300
3.400	0.42859	-107.167	6.700	0.61066	83.0856
3.500	0.43365	-111.883	6.800	0.61830	80.8843
3.600	0.43849	-117.548	6.900	0.61633	78.0872
3.700	0.44475	-123.856	7.000	0.61673	75.3727

03338-005

Figure 5. Parameter Data for the RF Input

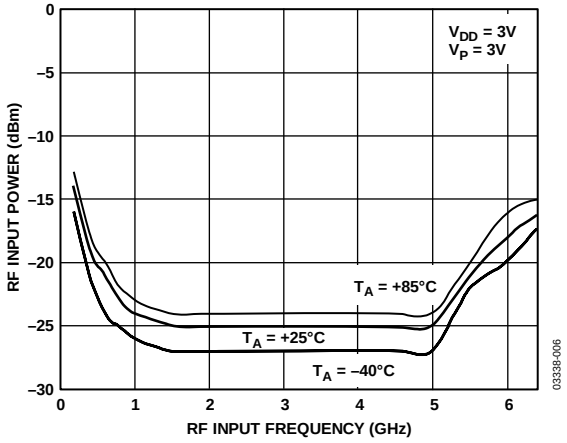


Figure 6. Input Sensitivity

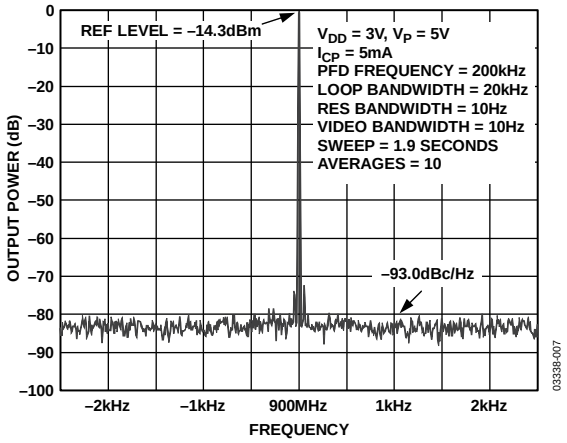


Figure 7. Phase Noise (900 MHz, 200 kHz, 20 kHz)

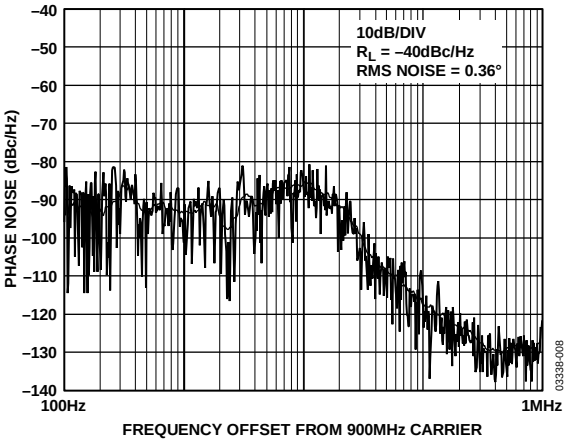


Figure 8. Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz)

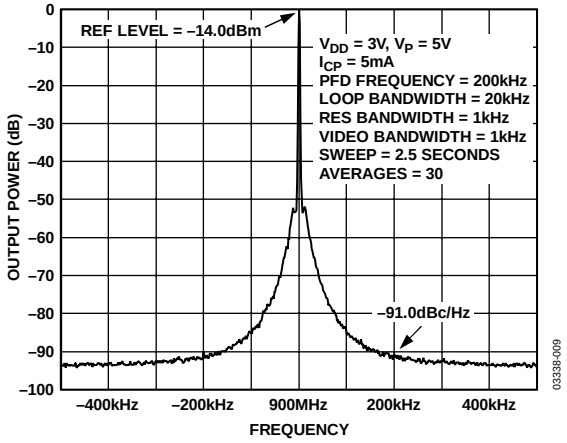


Figure 9. Reference Spurs (900 MHz, 200 kHz, 20 kHz)

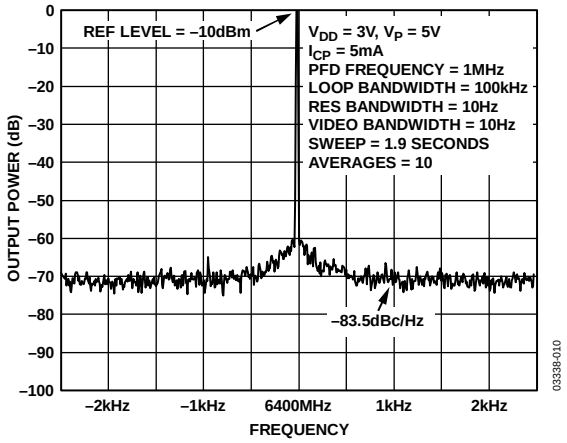


Figure 10. Phase Noise (6.4 GHz, 1 MHz, 100 kHz)

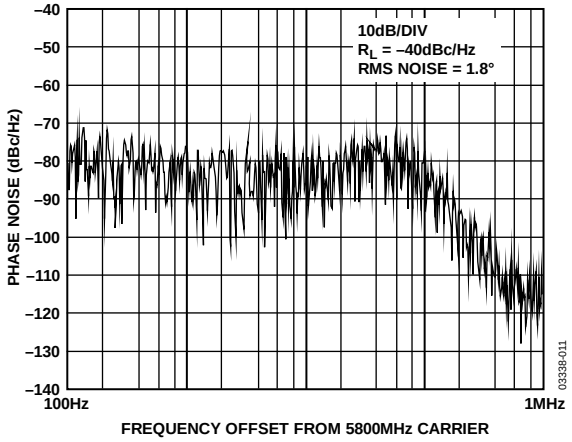


Figure 11. Integrated Phase Noise (6.4 GHz, 1 MHz, 100 kHz)

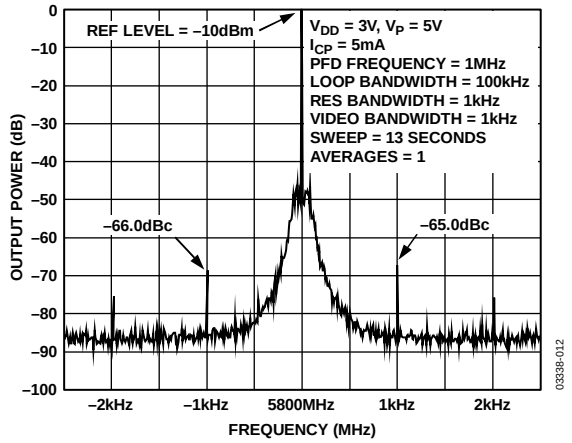


Figure 12. Reference Spurs (6.4 GHz, 1 MHz, 100 kHz)

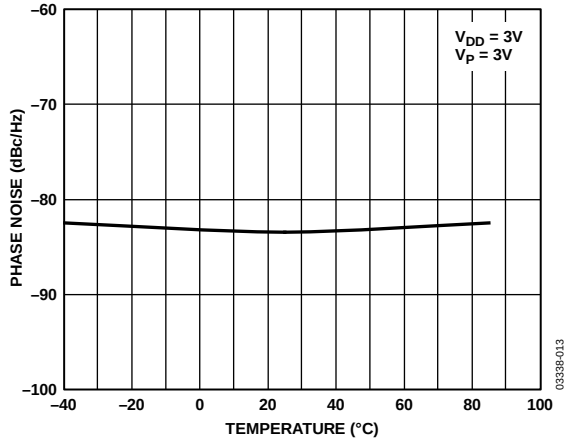


Figure 13. Phase Noise (6.4 GHz, 1 MHz, 100 kHz) vs. Temperature

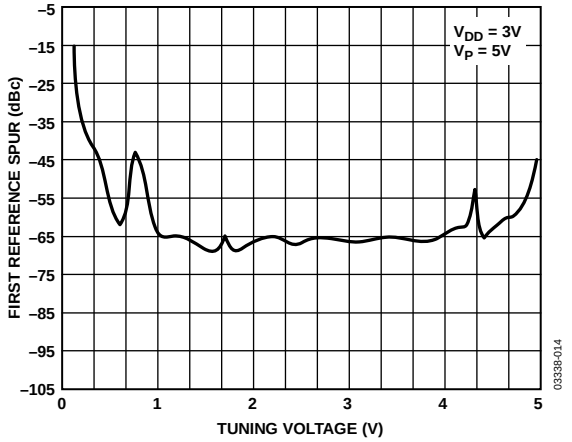


Figure 14. Reference Spurs vs. V_{TUNE} (6.4 GHz, 1 MHz, 100 kHz)

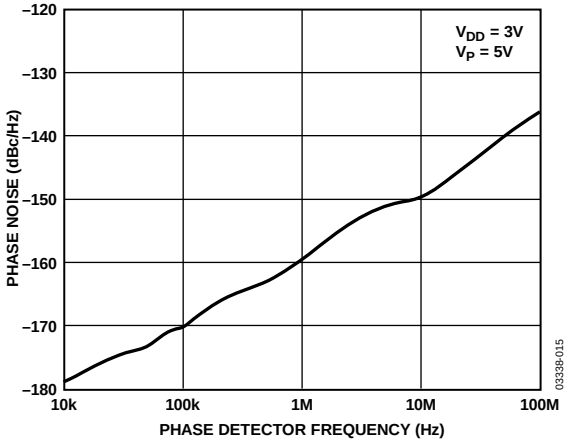


Figure 15. Phase Noise (Referred to CP Output) vs. PFD Frequency

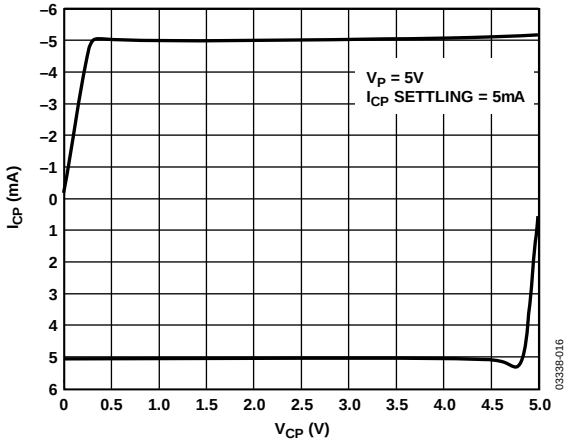


Figure 16. Charge Pump Output Characteristics

FUNCTIONAL DESCRIPTION

REFERENCE INPUT STAGE

The reference input stage is shown in Figure 17. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

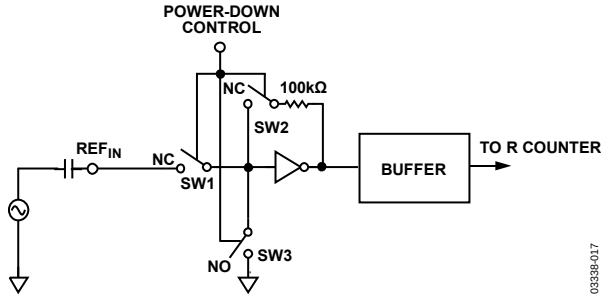


Figure 17. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 18. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

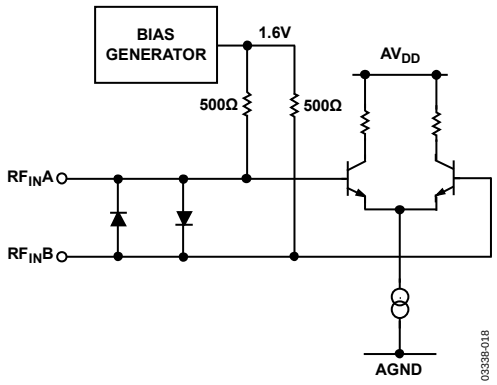


Figure 18. RF Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and CMOS B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. A minimum divide ratio is possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value, and is given by: $(P^2 - P)$.

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).
P is the preset modulus of dual-modulus prescaler (8/9, 16/17).
B is the preset divide ratio of binary 13-bit counter (3 to 8191).
A is the preset divide ratio of binary 6-bit swallow counter (0 to 63).
f_{REFIN} is the external reference frequency oscillator.

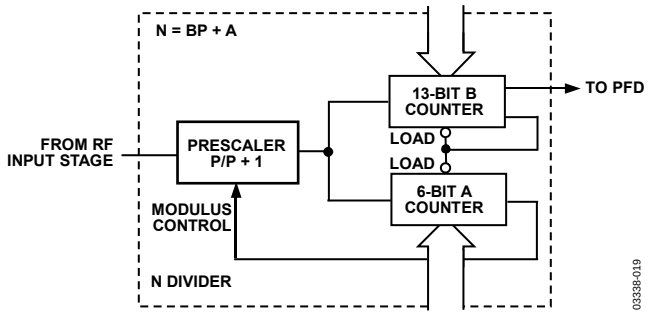


Figure 19. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. Use of the minimum antibacklash pulse width is not recommended. See Figure 23.

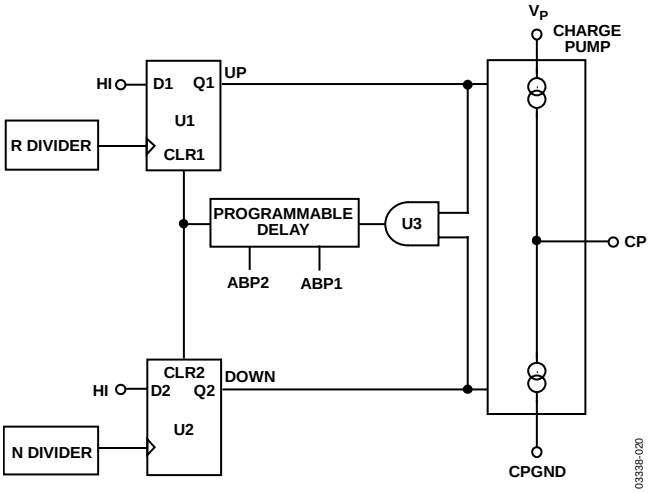


Figure 20. PFD Simplified Schematic and Timing (in Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4107 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 25 shows the full truth table. Figure 21 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When the lock detect precision (LDP) bit in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output becomes high with narrow, low going pulses.

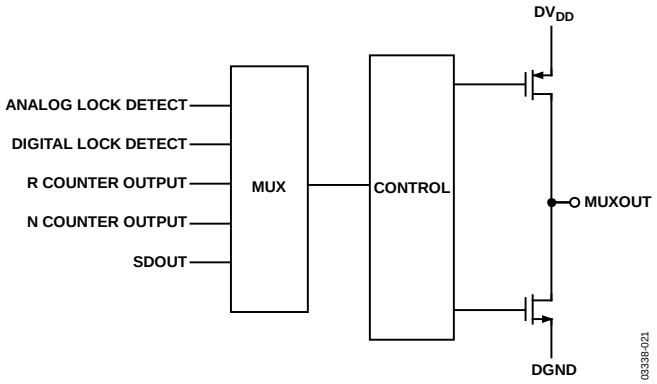


Figure 21. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4107 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Figure 22 shows a summary of how the latches are programmed.

Table 5. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

LATCH SUMMARY

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

03338-022

Figure 22. Latch Summary

REFERENCE COUNTER LATCH MAP

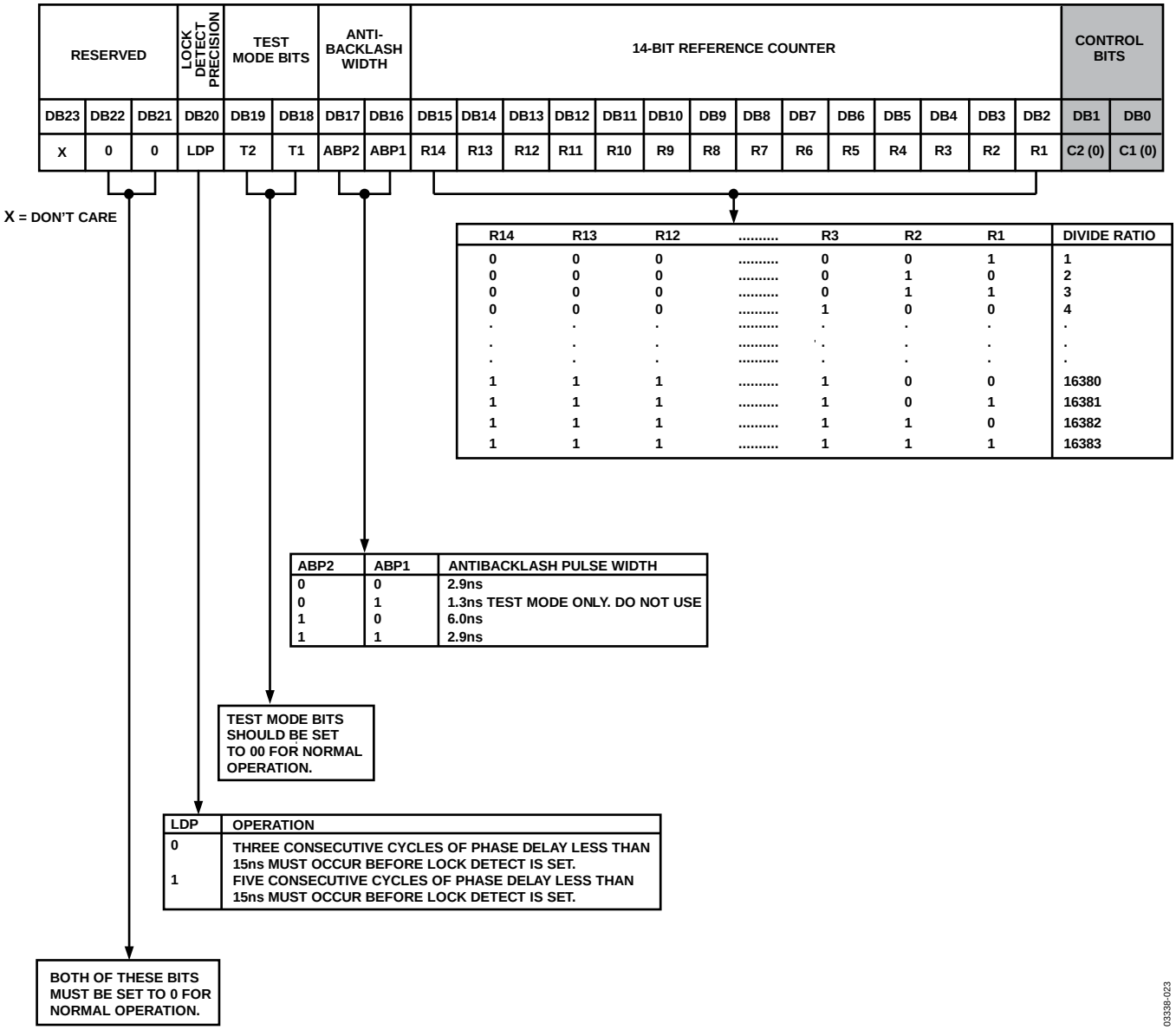


Figure 23. Reference Counter Latch Map

AB COUNTER LATCH MAP

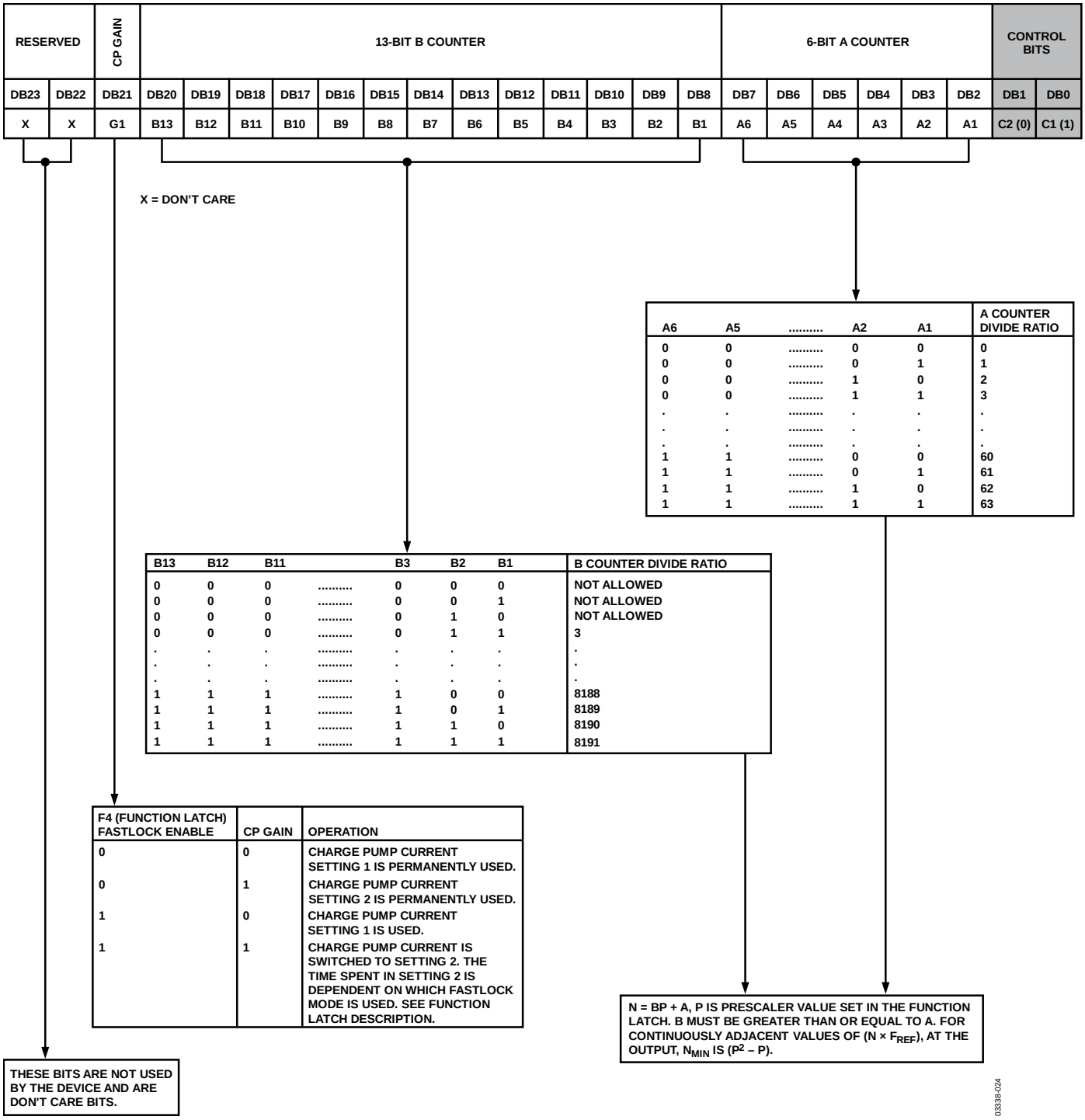


Figure 24. AB Counter Latch Map

FUNCTION LATCH MAP

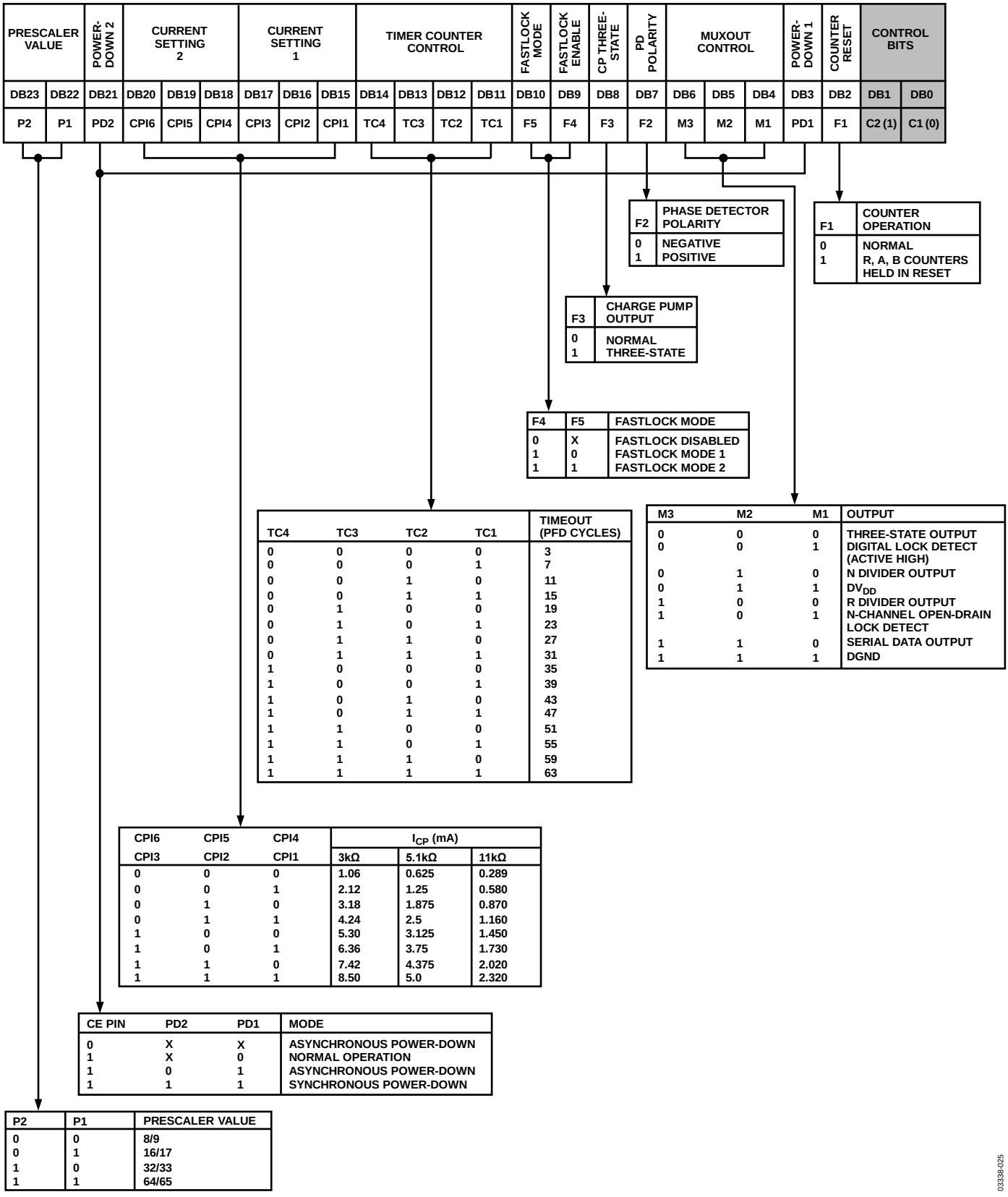


Figure 25. Function Latch Map

INITIALIZATION LATCH MAP

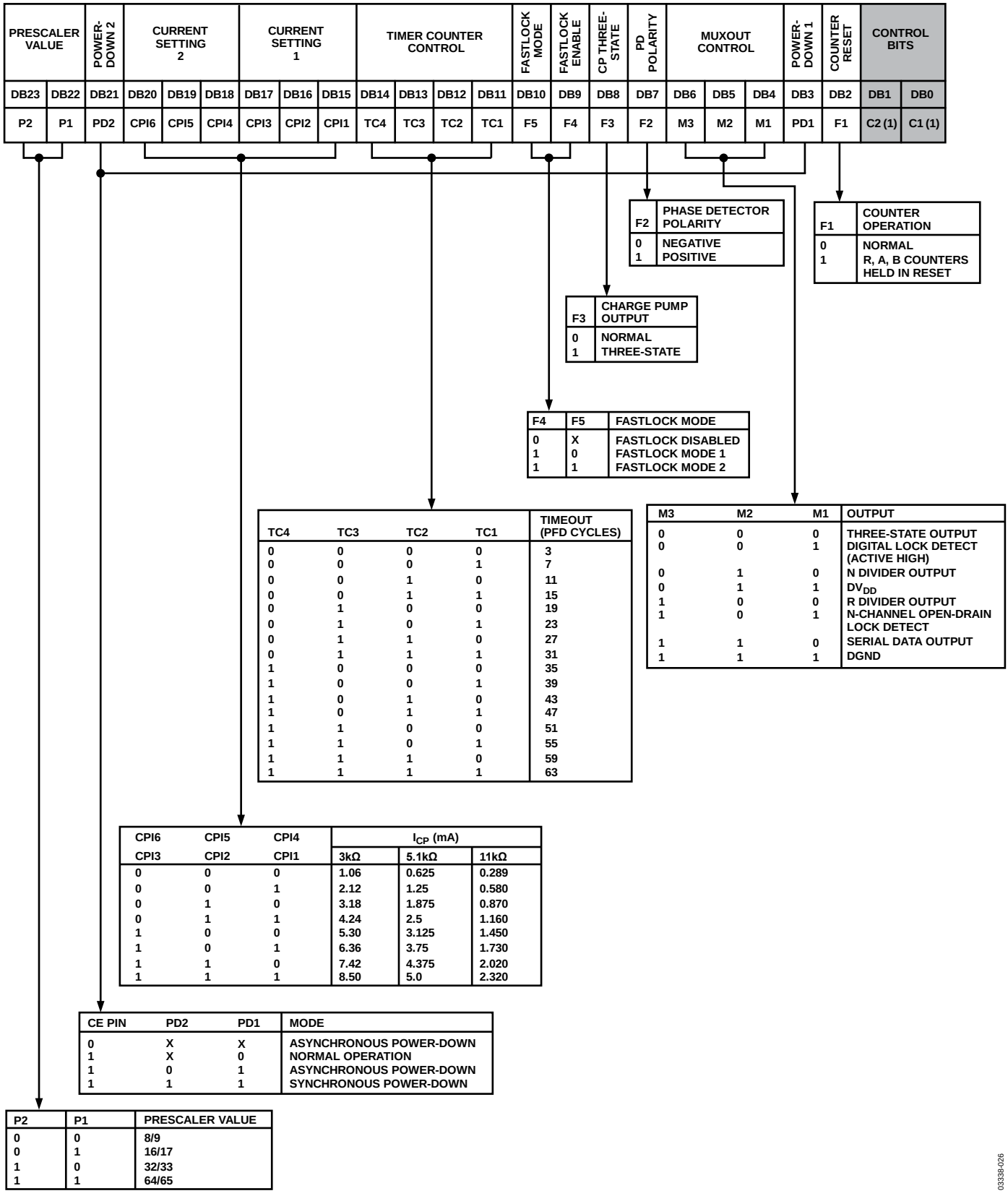


Figure 26. Initialization Latch Map

FUNCTION LATCH

The on-chip function latch is programmed with C2 and C1 set to 1 and 0, respectively. Figure 25 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into PD1 (on condition that a 1 has also been loaded to PD2), then the device goes into power-down on the occurrence of the next charge pump event.

When a power-down is activated (either in synchronous or asynchronous mode, including CE pin-activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4107. Figure 25 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Fastlock is enabled only when this bit is 1.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the AB counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 to TC1, the CP gain bit in the AB counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 25 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed).

The normal sequence of events is as follows:

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, it must be decided how long the secondary current is to stay active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Figure 25.

To program a new output frequency, the user simply programs the AB counter latch with new values for A and B. At the same time, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the AB counter latch is reset to 0 and is ready for the next time that the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Figure 25.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

PD Polarity

This bit sets the phase detector polarity bit. See Figure 25.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

The initialization latch is programmed when C2 and C1 are set to 1 and 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed an additional internal reset pulse is applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this will not trigger the internal reset pulse.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initially powering up the device, there are three ways to program the device.

Initialization Latch Method

1. Apply V_{DD}.
2. Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Next, do a function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.
4. Then do an R load (00 in two LSBs).
5. Then do an AB load (01 in two LSBs).
6. When the initialization latch is loaded, the following occurs:

a. The function latch contents are loaded.
b. An internal pulse resets the R, AB, and timeout counters to load-state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
c. Latching the first AB counter data after the initialization word activates the same internal reset pulse. Successive AB loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the AB counter latch (01).
6. Bring CE high to take the device out of power-down. The R and AB counters resume counting in close alignment.

Note that after CE goes high, a duration of 1 µs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down in order to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in two LSBs).
4. Do an AB counter load (01 in two LSBs).
5. Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

APPLICATIONS

LOCAL OSCILLATOR FOR LMDS BASE STATION TRANSMITTER

Figure 27 shows the ADF4107 being used with a VCO to produce the LO for an LMDS base station.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical base station system has either a TCXO or an OCXO driving the reference input without any 50 Ω termination.

To have a channel spacing of 1 MHz at the output, the 10 MHz reference input must be divided by 10, using the on-chip reference divider of the ADF4107.

The charge pump output of the ADF4107 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45°.

Other PLL system specifications are:

K_D = 5.0 mA
K_V = 80 MHz/V
Loop bandwidth = 70 kHz
F_{PFD} = 1 MHz
N = 6300
Extra reference spur attenuation = 10 dB

All of these specifications are needed and used to derive the loop filter component values shown in Figure 27.

Figure 27 gives a typical phase noise performance of −83 dBc/Hz at 1 kHz offset from the carrier. Spurs are better than −70 dBc.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer, and drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in lock. In Figure 27, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock detect signal.

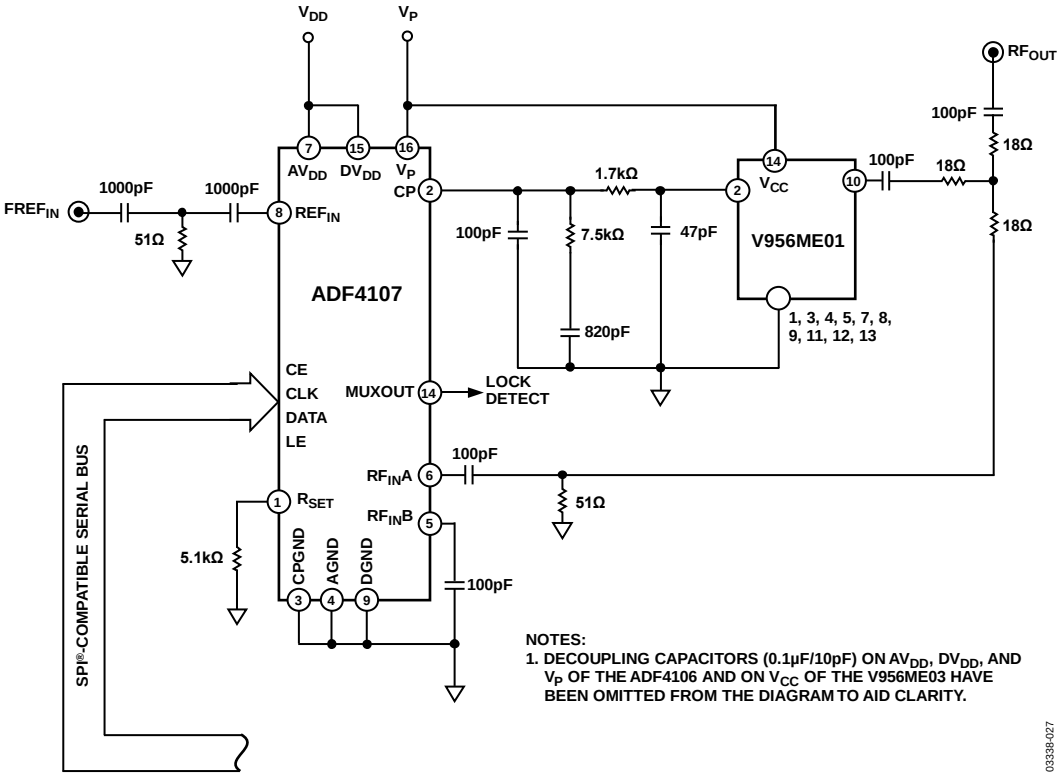


Figure 27. 6.3 GHz Local Oscillator Using the ADF4107

INTERFACING

The ADF4107 has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 28 shows the interface between the ADF4107 and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4107 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4107, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

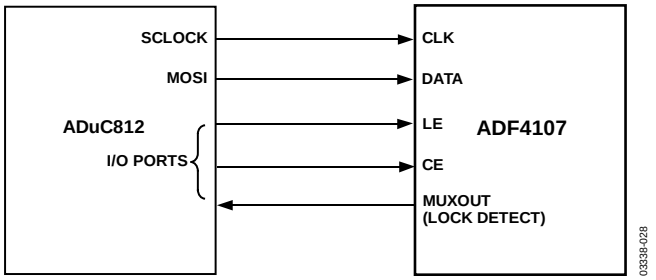


Figure 28. ADuC812 to ADF4107 Interface

ADSP-2181 Interface

Figure 29 shows the interface between the ADF4107 and the ADSP21xx digital signal processor. The ADF4107 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

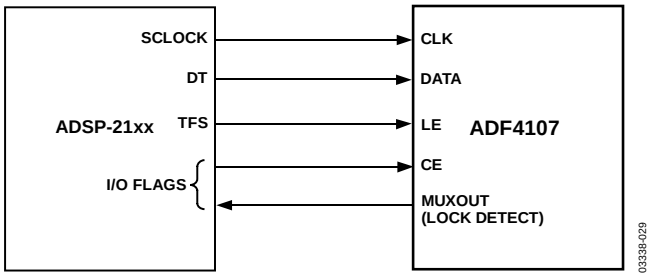


Figure 29. ADSP-21xx to ADF4107 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

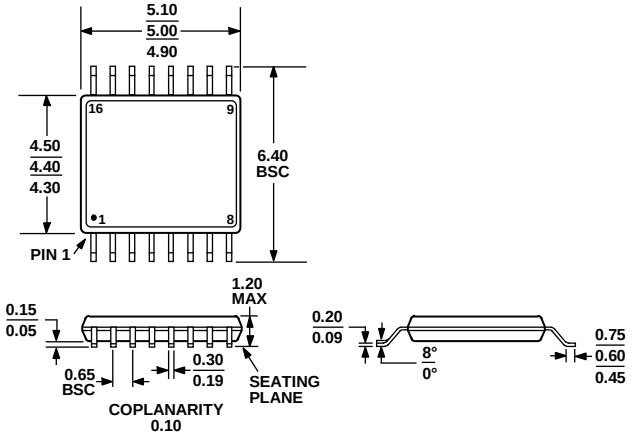
The lands on the chip scale package (CP-20-6) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via.

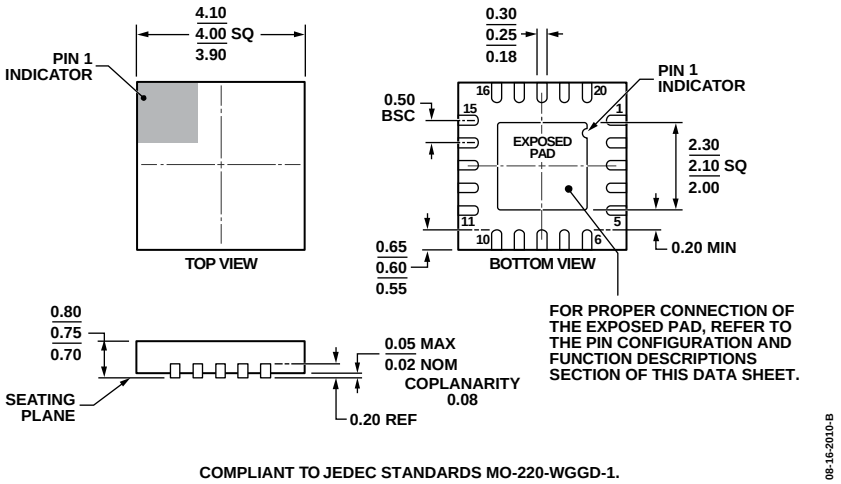
The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 31. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4107BRU	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BRU-REEL	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BRU-REEL7	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BRUZ	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BRUZ-REEL	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BRUZ-REEL7	−40°C to + 85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4107BCPZ	−40°C to + 85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4107BCPZ-REEL	−40°C to + 85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4107BCPZ-REEL7	−40°C to + 85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
EV-ADF411XSD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

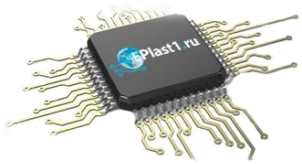
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.