TLE4291

Low Drop Out Linear Voltage Regulator

TLE4291E

Data Sheet

Rev. 1.1, 2012-12-03

Automotive Power

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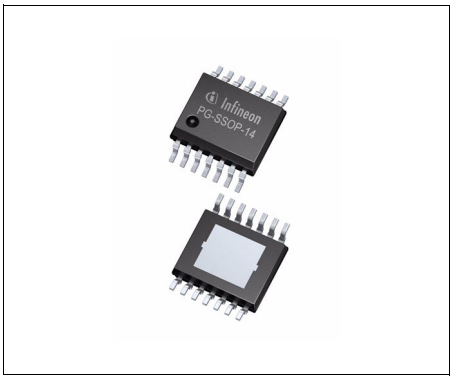
Low Drop Out Linear Voltage Regulator **TLE4291E**

5 V Fixed Output Voltage

1 Overview



PG-SSOP-14 EP

Features

- Output Voltage 5 V ± 2%
- Output Current up to 450 mA
- Very low Current Consumption
- Power-on and Undervoltage Reset with Programmable Delay Time
- Integrated Standard Watchdog
- Reset Low Down to V_Q = 1 V
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Input Voltage Range from -42 V to 45 V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE4291 is a monolithic integrated low-dropout voltage regulator in a PG-SSOP-14 EP exposed pad package, especially designed for automotive applications. An input voltage up to 42 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 450 mA. It is short-circuit protected by the implemented current limitation and has an integrated overtemperature shutdown. The integrated reset and watchdog function makes it suitable for supplying microprocessor systems in automotive environments. The watchdog and the power-on reset delay timing can be programmed by the external delay capacitor.

Type	Package	Marking
TLE4291E	PG-SSOP-14 EP	TLE4291

2 Block Diagram

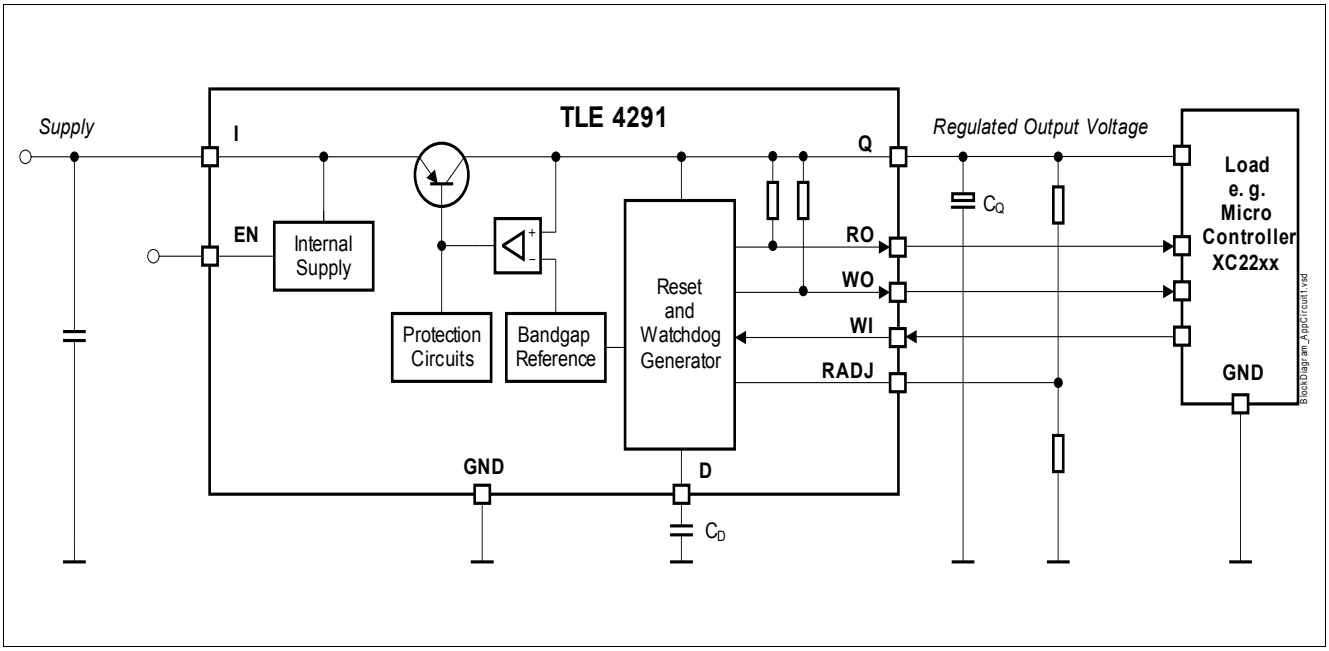


Figure 1 Block Diagram and Simplified Application Circuit

3 Pin Configuration

3.1 Pin Assignment

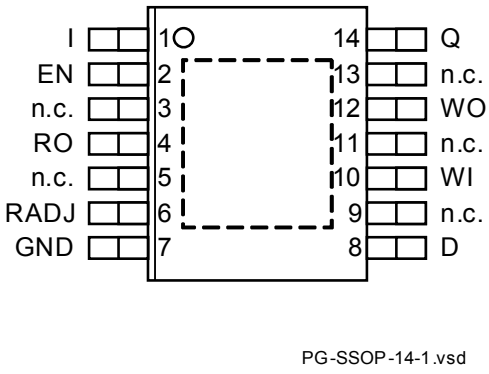


Figure 2 Pin Configuration PG-SSOP-14 EP

3.2 Pin Definitions and Functions

[11]

Pin	Symbol	Function
1	I	**Regulator Input and IC Supply** For compensating line influences, a capacitor to GND close to the IC pins is recommended.
2	EN	**Enable** High signal enables the regulator; Low signal disables the regulator; Connect to I, if the enable function is not needed.
3	n.c.	**Not Connected** Internally not connected; Connection to PCB GND recommended.
4	RO	**Reset Output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the reset function is not needed.
5	n.c.	**Not Connected** Internally not connected; Connection to PCB GND recommended.
6	RADJ	**Reset Switching Threshold Adjust** For reset threshold adjustment connect to a voltage divider from output Q to GND. For triggering the reset at the internally determined threshold, connect this pin directly to GND. Connect directly to GND if the reset function is not needed.
7	GND	**Ground** Interconnect the GND pins on PCB. Connect to heat sink area.

Pin	Symbol	Function
8	D	**Reset Delay and Watchdog Timing** Connect a ceramic capacitor D (pin 6) to GND for reset delay and watchdog timing adjustment. Leave only open if both, the reset and the watchdog function are not needed.
9	n.c.	**Not Connected** Internally not connected; Connection to PCB GND recommended.
10	WI	**Watchdog Input** Positive edge triggered input, usable for microcontroller monitoring. Connect to GND if the watchdog function is not needed.
11	n.c.	**Not Connected** Internally not connected; Connection to PCB GND recommended
12	WO	**Watchdog Output** Open collector output with an internal pull-up resistor to the output Q. An additional external pull-up resistor to the output Q is optional. Leave open if the watchdog function is not needed.
13	n.c.	**Not Connected** Internally not connected; Connection to PCB GND recommended.
14	Q	**5 V Regulator Output** Block to GND with a capacitor close to the IC pins, respecting capacitance and ESR requirements given in the **Chapter 4.2**.
	PAD	**Heat sink** connect to PCB heat sink area and GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply Voltage	V_I	-42	45	V	–
4.1.2	Enable Input EN	V_{EN}	-42	45	V	–
4.1.3	Regulator Output	V_Q	-1	7	V	–
4.1.4	Watchdog Input	V_{WI}	-0.3	7	V	–
4.1.5	Watchdog Output	V_{WO}	-0.3	7	V	–
4.1.6	Reset Adjust	V_{RADJ}	-0.3	7	V	–
4.1.7	Reset Output	V_{RO}	-0.3	7	V	–
4.1.8	Reset Delay	V_D	-0.3	7	V	–
Temperatures						
4.1.9	Junction Temperature	T_j	-40	150	°C	–
4.1.10	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility PG-SSOP-14 EP						
4.1.11	ESD Resistivity to GND	V_{ESD}	-4	4	kV	HBM[2)]
4.1.12	ESD Resistivity to GND	V_{ESD}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to AEC-Q100-002-JESD 22-A114

3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage Range for Normal Operation	V_I	$V_Q + V_{dr}$	42	V	1)
4.2.2	Extended Input Voltage Range	V_I	3.3	42	V	2)
4.2.3	Junction Temperature	T_j	-40	150	°C	–
4.2.4	Output Capacitor Requirements	C_Q	22	–	µF	3)
4.2.5		ESR_{CQ}	–	3		4)

1) For specification of the output voltage V_Q and the drop out voltage V_{dr}, see **Chapter 5 Voltage Regulator**.
2) The output voltage will follow the input voltage, but is outside the specified range.
For details see **Chapter 5 Voltage Regulator**.
3) The minimum output capacitance is applicable for a worst case capacitance tolerance of 30%
4) Relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	7	–	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	43	–	K/W	2)
4.3.3			–	120	–	K/W	Footprint only[3)]
4.3.4			–	59	–	K/W	300 mm^2 heatsink area on PCB[3)]
4.3.5			–	49	–	K/W	600 mm^2 heatsink area on PCB[3)]

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. Saturation control as a function of the load current prevents any oversaturation of the pass element. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Chapter 4.2** table "Functional Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 28 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore reduce the IC lifetime.

The TLE4291 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

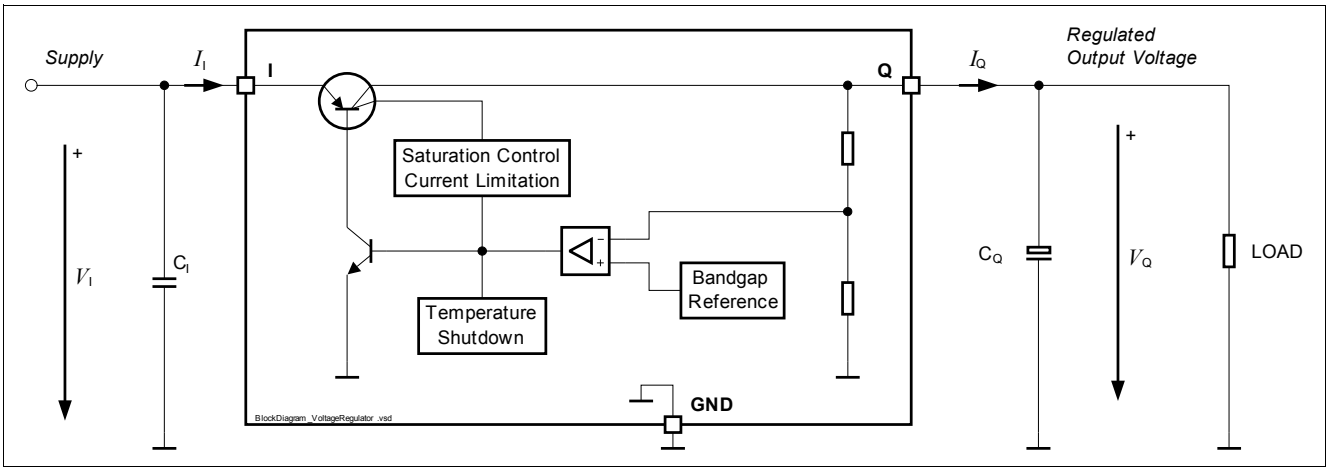


Figure 3 Block Diagram Voltage Regulator Circuit

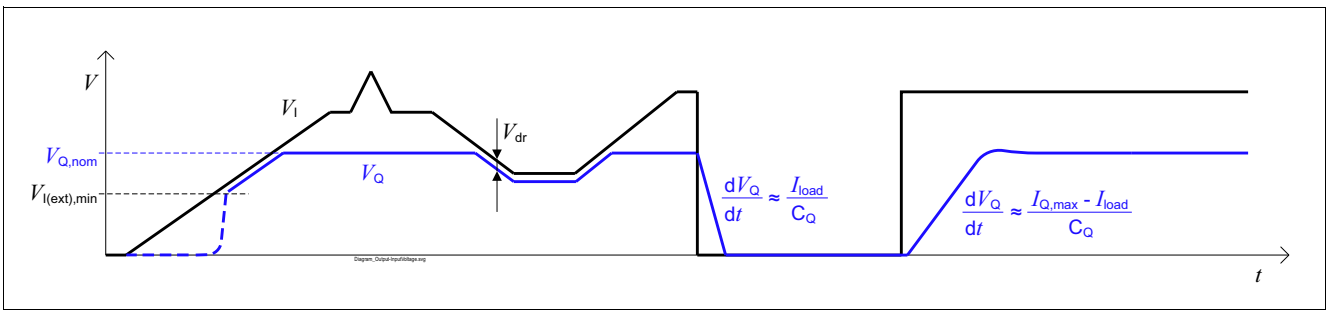


Figure 4 Output Voltage vs. Input Voltage

5.2 Electrical Characteristics Voltage Regulator

Electrical Characteristics: Voltage Regulator

V_I = 13.5V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, direction of currents as shown in **Figure 3** (unless otherwise specified)

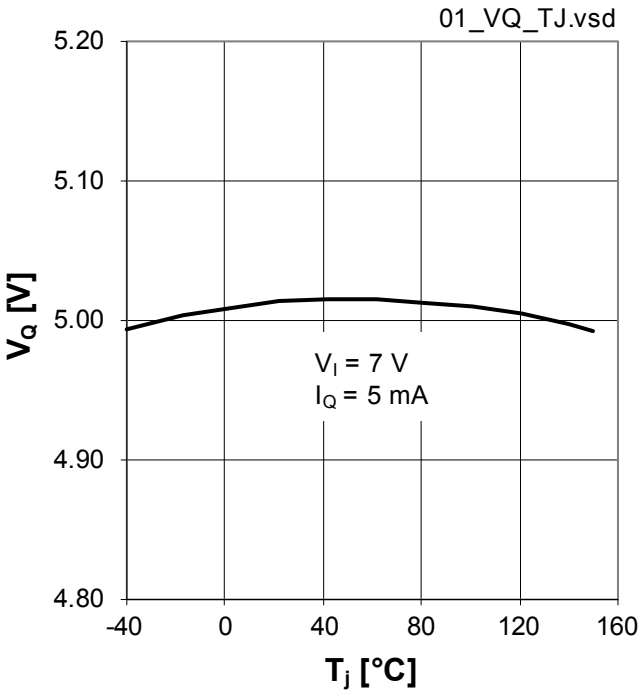
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Output Voltage	V_Q	4.9	5.0	5.1	V	1 mA < I_Q < 450 mA 9 V < V_I < 28 V
5.2.2	Output Voltage	V_Q	4.9	5.0	5.1	V	1 mA < I_Q < 400 mA 6 V < V_I < 28 V
5.2.3	Output Voltage	V_Q	4.85	5.0	5.15	V	1 mA < I_Q < 200 mA 6 V < V_I < 40 V
5.2.4	Output Current Limitation	$I_{Q,max}$	451	–	1100	mA	V_Q =4.8 V
5.2.5	Load Regulation steady-state	$dV_{Q,load}$	-30	-15	–	mV	I_Q = 5 mA to 400 mA; V_I = 8 V
5.2.6	Line Regulation steady-state	$dV_{Q,line}$	–	5	15	mV	V_I = 8 V to 32 V; I_Q = 5 mA
5.2.7	Power Supply Ripple Rejection	$PSRR$	60	65	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp[1)]
5.2.8	Drop Out Voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	250	mV	I_Q = 100 mA[2)]
5.2.9			–	250	500	mV	I_Q = 300 mA[2)]
5.2.10	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[1)]

1) Parameter not subject to production test; specified by design.

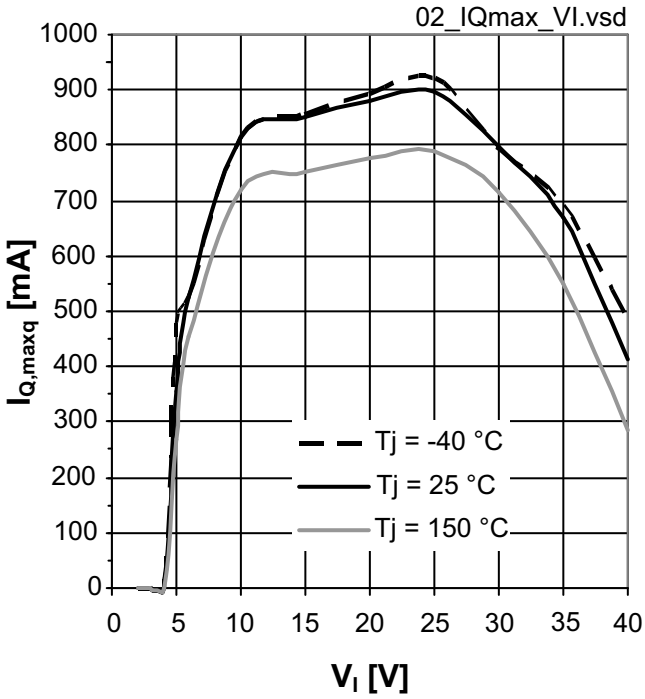
2) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

5.3 Typical Performance Characteristics Voltage Regulator

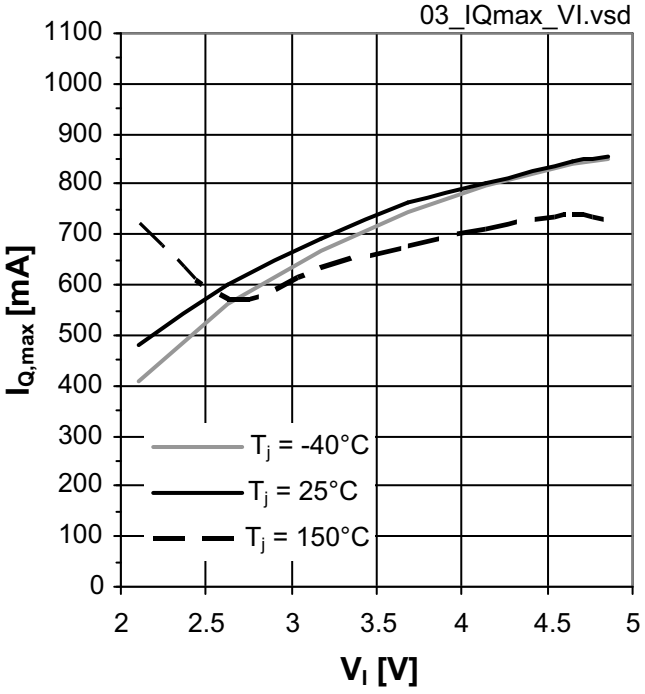
Output Voltage V_Q versus Junction Temperature T_j



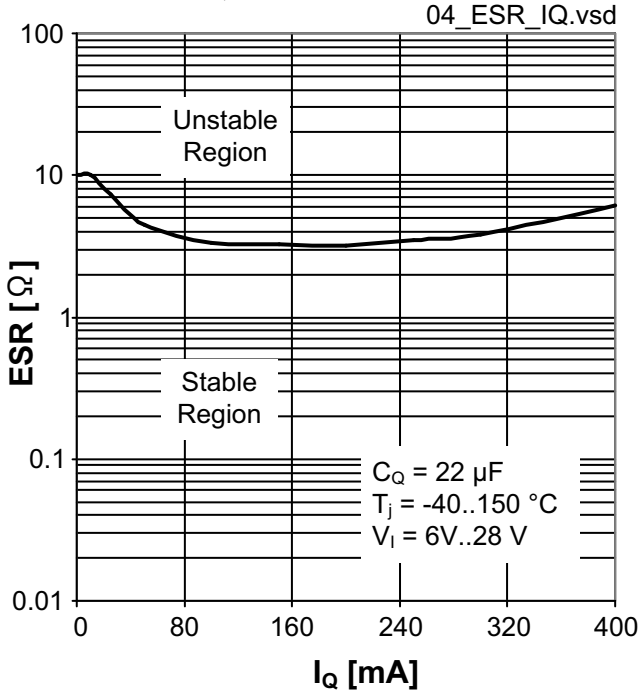
Output Current I_Q versus Input Voltage V_I



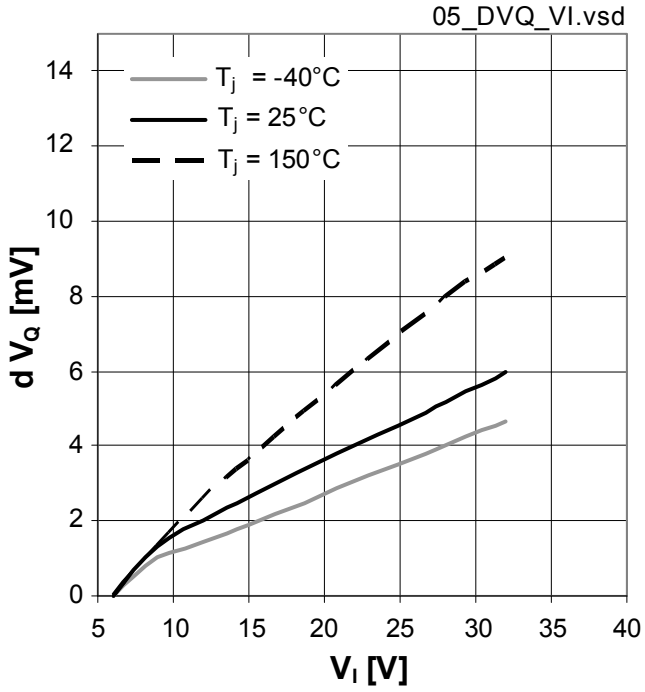
Output Current I_Q versus Input Voltage V_I



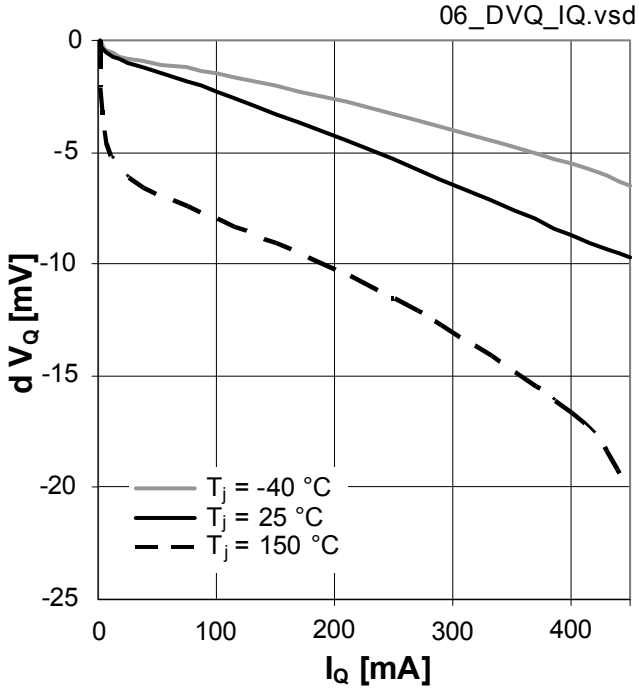
Output Capacitor Series Resistor ESR(C_Q) versus Output Current I_Q



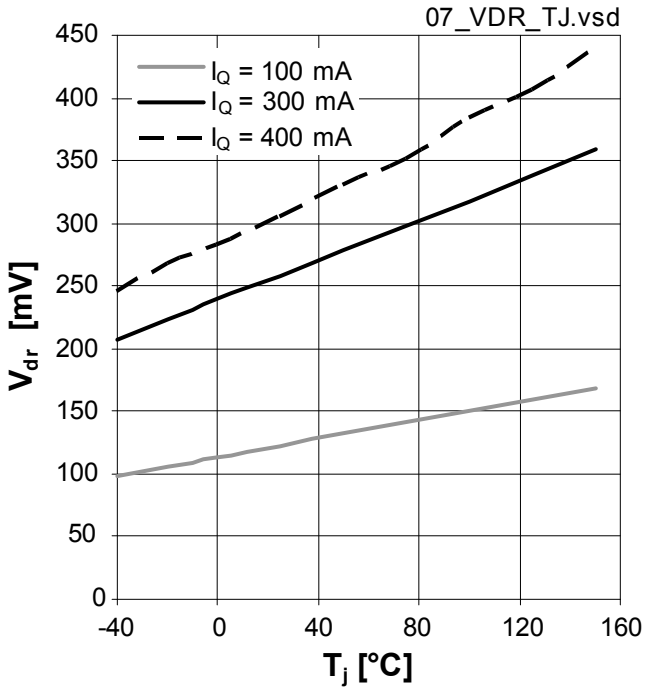
Line Regulation d$V_{Q,line}$ versus Input Voltage Change dV_I



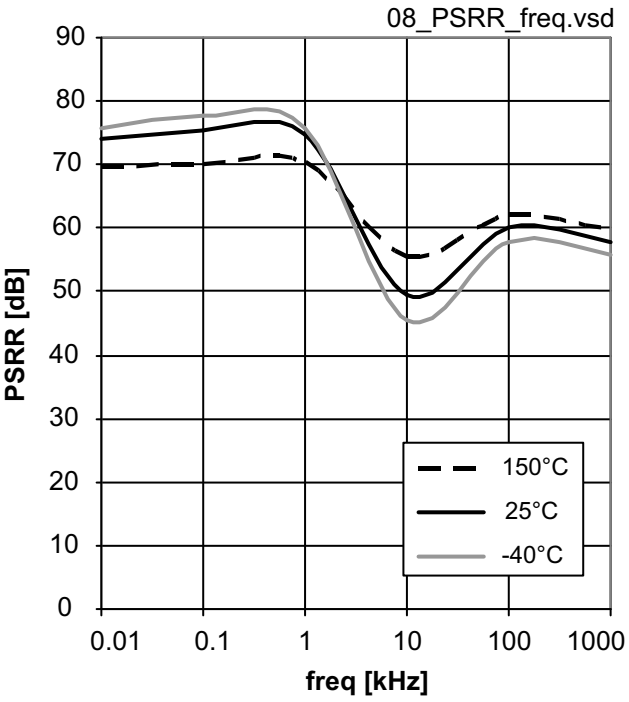
Load Regulation d$V_{Q,line}$ versus Output Current Change dI_Q



Dropout Voltage V_{dr} versus Output Current I_Q



Power Supply Ripple Rejection *PSRR*



6 Current Consumption

6.1 Electrical Characteristics Current Consumption

Electrical Characteristics: Current Consumption

V_I = 13.5V, T_j = -40 °C to +150 °C,

all voltages with respect to ground, directions of currents as shown in **Figure 5** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Current Consumption $I_{q,OFF} = I_I$	$I_{q,OFF}$	–	2	5	µA	$V_{EN} = 0$ V; $T_j \leq 105$°C
6.1.2	Current Consumption $I_q = I_I - I_Q$	I_q	–	220	300	µA	$V_{EN} = 5$V; $I_Q = 1$mA; $T_j \leq 85$ °C
6.1.3			–	–	350	µA	$V_{EN} = 5$V; $I_Q = 1$mA; $T_j \leq 105$ °C
6.1.4			–	6	15	mA	$V_{EN} = 5$V; I_Q = 250 mA
6.1.5			–	16	30	mA	$V_{EN} = 5$V; I_Q = 400 mA

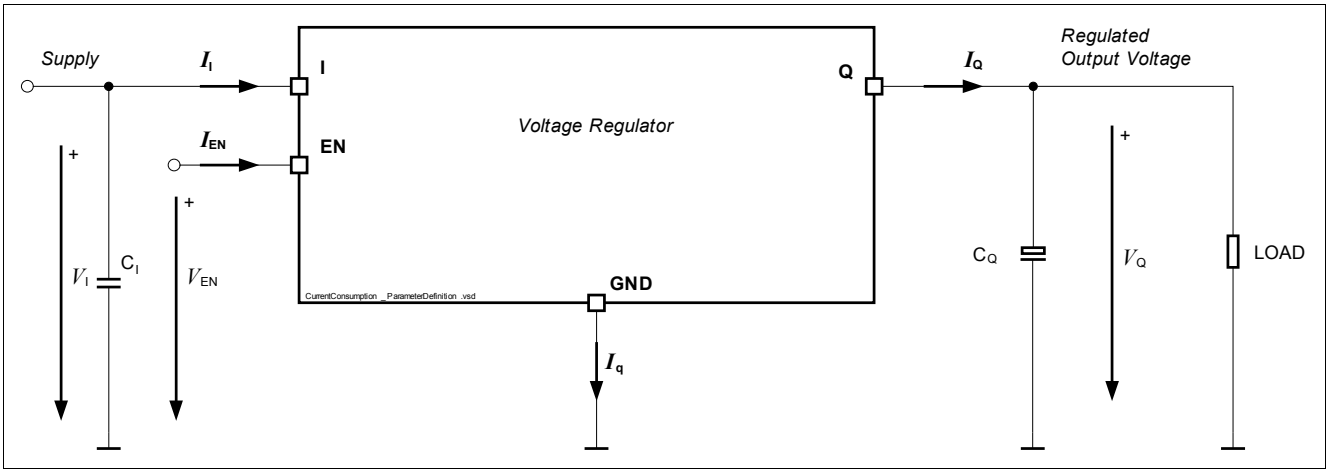
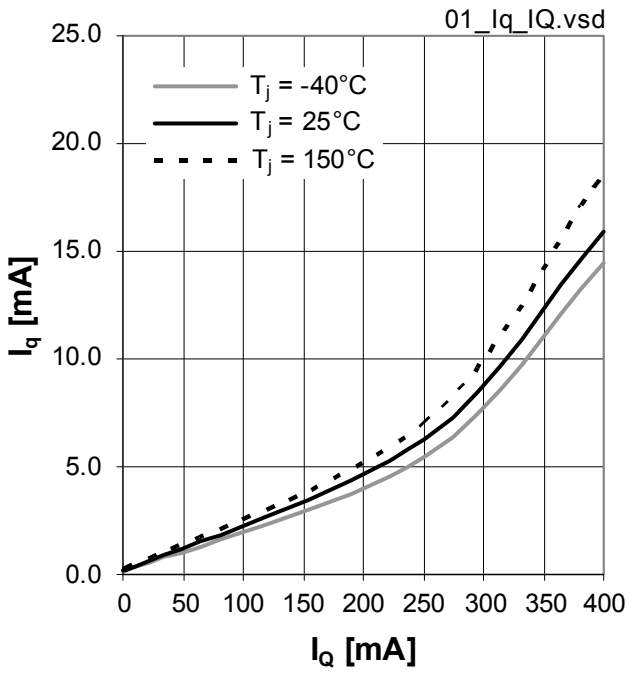


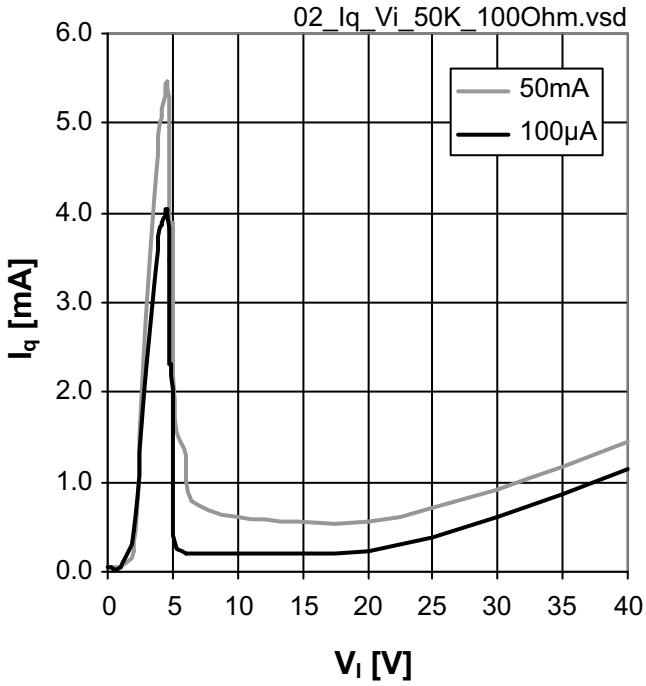
Figure 5 Parameter Definition

6.2 Typical Performance Characteristics Current Consumption

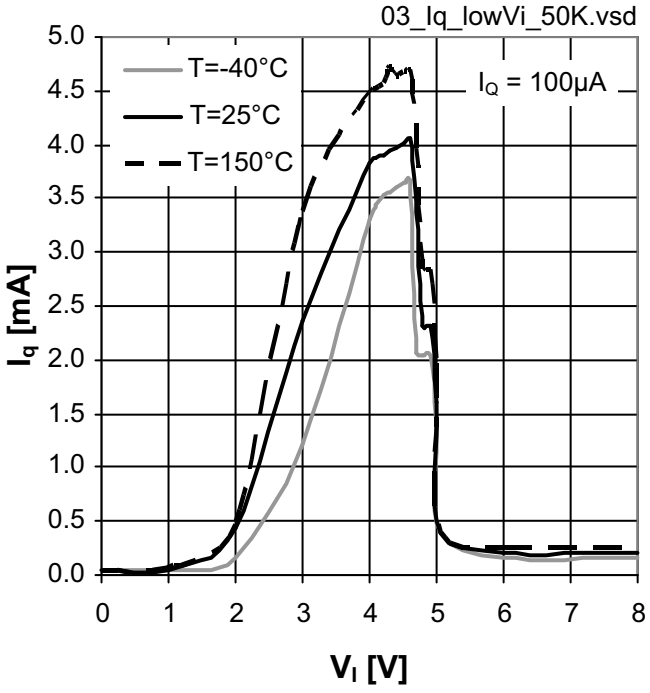
Current Consumption I_q versus Output Current I_Q



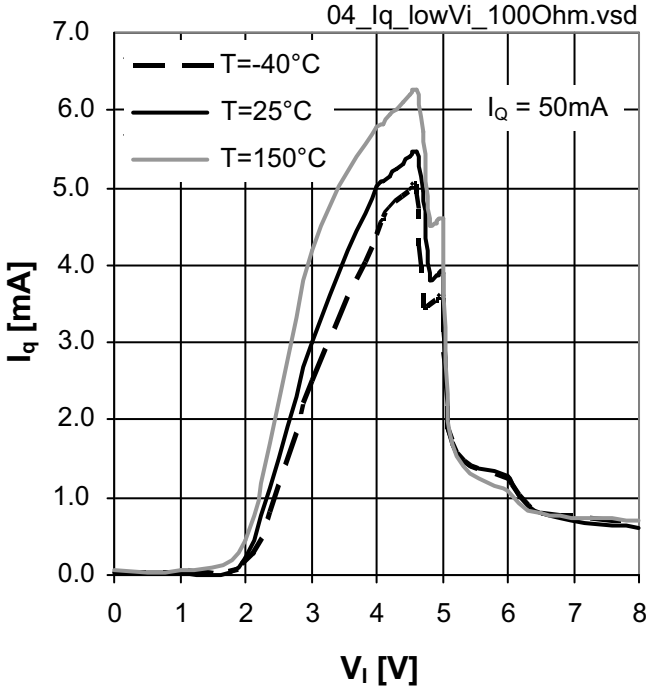
Current Consumption I_q versus Input Voltage V_I



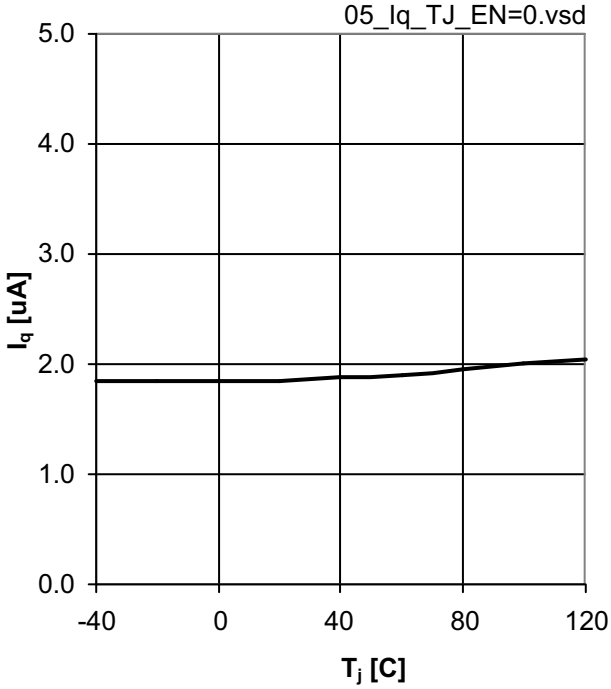
Current Consumption I_q versus Input Voltage V_I



Current Consumption I_q versus Input Voltage V_I



Current Consumption I_q versus Junction Temperature T_j Regulator disabled



7 Enable Function

7.1 Description Enable Function

The TLE4291 can be turned on or turned off via the EN Input. With voltage levels higher than $V_{EN,high}$ applied to the EN Input the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The Enable Input has an build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input.

7.2 Electrical Characteristics Enable Function

Electrical Characteristics: Enable Function

V_I = 13.5V, T_j = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.1	Enable Low Signal Valid	$V_{EN,low}$	–	–	0.8	V	–
7.2.2	Enable High Signal Valid	$V_{EN,high}$	2	–	–	V	V_Q settled
7.2.3	Enable Threshold Hysteresis	$V_{EN,hyst}$	30	–	–	mV	–
7.2.4	Enable Input current	I_{EN}	–	–	2	µA	V_{EN} = 5 V
7.2.5	Enable internal pull-down resistor	R_{EN}	3	4.5	6	MΩ	–

8 Reset Function

8.1 Description Reset Function

The reset function provides several features:

Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output “RO” to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-On Reset Delay Time

The power-on reset delay time $t_{d,PWR\text{-}ON}$ allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the reset switching threshold until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{d,PWR\text{-}ON}$ is defined by an external delay capacitor C_D connected to pin “D” which is charged up by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

In case a power-on reset delay time $t_{d,PWR\text{-}ON}$ different from the value for C_D = 100nF is required, the delay capacitor’s value can be derived from the specified value given in **Item 8.2.13**:

$$C_D = 100\text{nF} \times t_{d,PWR\text{-}ON} / t_{d,PWR\text{-}ON,100nF} \quad (1)$$

with

- $t_{d,PWR\text{-}ON}$: Desired power-on reset delay time
- $t_{d,PWR\text{-}ON,100nF}$: Power-on reset delay time specified in **Item 8.2.13**
- C_D: Delay capacitor required.

The formula is valid for $C_D \geq$ 10nF. For precise timing calculations consider also the delay capacitor’s tolerance.

Reset Reaction Time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,lo}$, the delay capacitor C_D is discharged rapidly. Once the delay capacitor’s voltage has reached the lower delay switching threshold $V_{DST,lo}$, the reset output “RO” will be set to “low”.

Additionally to the delay capacitor discharge time $t_{rr,d}$, an internal reaction time $t_{rr,int}$ applies. Hence, the total reset reaction rime $t_{rr,total}$ becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \quad (2)$$

with

- $t_{rr,total}$: Total reset reaction time
- $t_{rr,int}$: Internal reset reaction time; see **Item 8.2.14**.
- $t_{rr,d}$: Delay capacitor discharge time. For a capacitor C_D different from the value specified in **Item 8.2.15**, see typical performance graphs.

Reset Output “RO”

The reset output “RO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “RO” signal is desired, an external pull-up resistor to the output “Q” can be connected. Since the maximum “RO” sink current is limited, the optional external resistor $R_{RO,ext}$ must not below as specified in **Item 8.2.7**.

Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin "RADJ". For selecting the default threshold connect pin "RADJ" to GND. The reset adjustment range is given in **Item 8.2.5**.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows

$$V_{RT,lo,new} = V_{RADJ,th} \times (R_{ADJ,1} + R_{ADJ,2}) / R_{ADJ,2} \quad (3)$$

with

- $V_{RT,lo,new}$: Desired undervoltage reset switching threshold.
- $R_{ADJ,1}$, $R_{ADJ,2}$: Resistors of the external voltage divider, see **Figure 6**.
- $V_{RADJ,th}$: Reset adjust switching threshold given in **Item 8.2.4**.

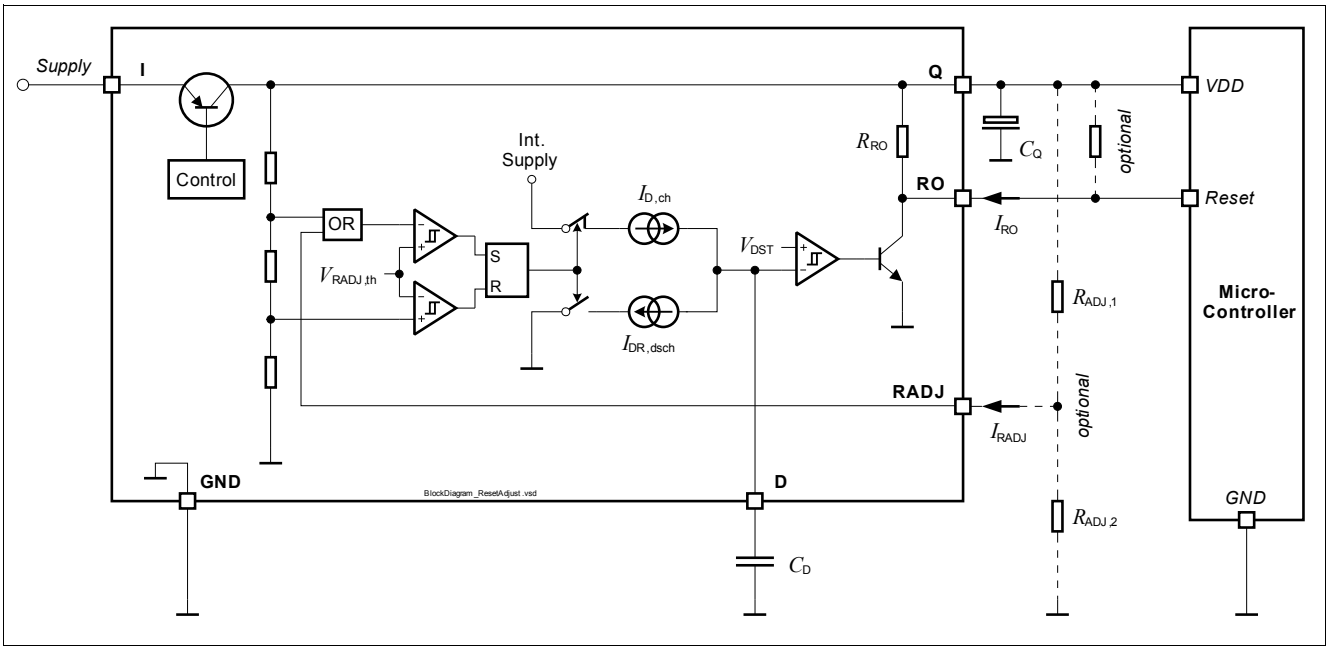


Figure 6 Block Diagram Reset Circuit

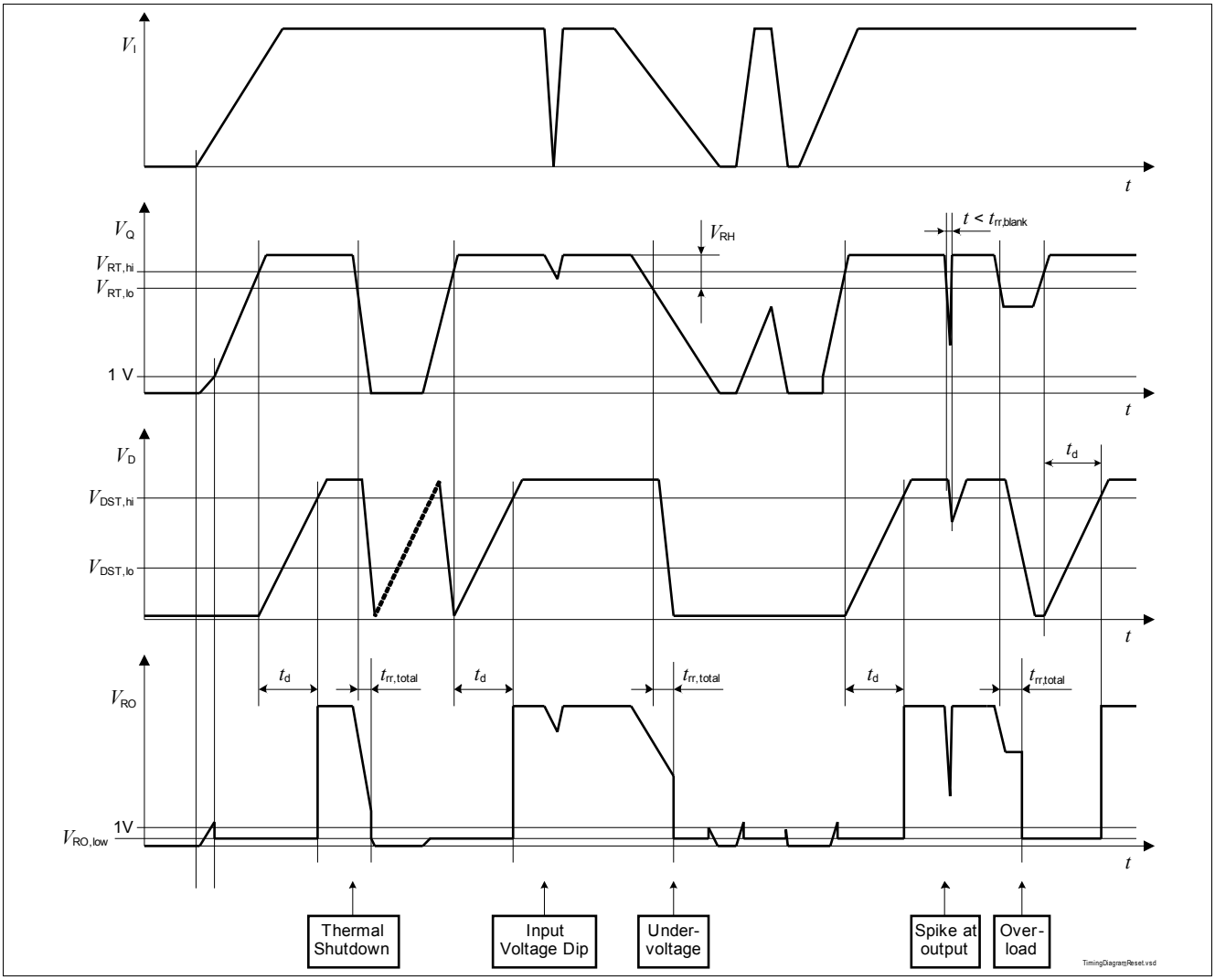


Figure 7 Timing Diagram Reset

8.2 Electrical Characteristics Reset Function

Electrical Characteristics: Reset Function

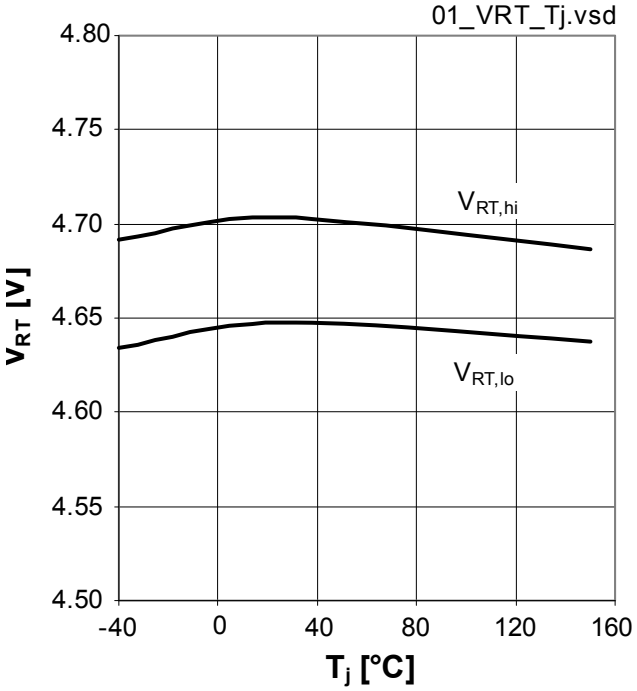
V_I = 13.5V, T_j = -40 °C to +150 °C,
all voltages with respect to ground, direction of currents as shown in **Figure 6** (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output Undervoltage Reset Comparator Default Values (Pin RADJ = GND)							
8.2.1	Output Undervoltage Reset Lower Switching Threshold	$V_{RT,lo}$	4.5	4.65	4.8	V	V_Q decreasing RADJ = GND
8.2.2	Output Undervoltage Reset Upper Switching Threshold	$V_{RT,hi}$	4.55	4.7	4.85	V	V_Q increasing RADJ = GND
8.2.3	Output Undervoltage Reset Headroom	V_{RH}	200	350	–	mV	Calculated Value: V_Q - $V_{RT,lo}$ I_Q = 50 mA RADJ = GND
Reset Threshold Adjustment							
8.2.4	Reset Adjust Lower Switching Threshold	$V_{RADJ,th}$	1.26	1.36	1.44	V	3.2 V ≤ V_Q < 5 V
8.2.5	Reset Adjustment Range [1]	$V_{RT,range}$	3.50	–	4.65	V	–
Reset Output RO							
8.2.6	Reset Output Low Voltage	$V_{RO,low}$	–	0.1	0.4	V	1 V ≤ V_Q ≤ $V_{RT,low}$; no external $R_{RO,ext}$
8.2.7	Reset Output External Pull-up Resistor to Q	$R_{RO,ext}$	5.6	–	–	kΩ	1 V ≤ V_Q ≤ $V_{RT,low}$; V_{RO} = 0.4 V
8.2.8	Reset Output Internal Pull-up Resistor	R_{RO}	20	30	40	kΩ	internally connected to Q
Reset Delay Timing							
8.2.9	Upper Delay Switching Threshold	$V_{DST,hi}$	–	0.9	–	V	–
8.2.10	Lower Delay Switching Threshold	$V_{DST,lo}$	–	0.25	–	V	–
8.2.11	Delay Capacitor Charge Current	$I_{D,ch}$	–	6.5	–	µA	V_D = 0.6 V
8.2.12	Delay Capacitor Reset Discharge Current	$I_{DR,dsch}$	–	70	–	mA	V_D = 0.6 V
8.2.13	Power-on Reset Delay Time	$t_{d,PWR,ON,100nF}$	8	13.5	18	ms	Calculated value; C_D = 100 nF [2]
8.2.14	Internal Reset Reaction Time	$t_{rr,int}$	–	9	15	µs	C_D = 0 nF
8.2.15	Delay Capacitor Discharge Time	$t_{rr,d}$	–	1.9	3	µs	C_D = 100 nF [2]
8.2.16	Total Reset Reaction Time	$t_{rr,total}$	–	11	18	µs	Calculated Value: $t_{rr,d,100nF}$ + $t_{rr,int}$; C_D = 100 nF [2]

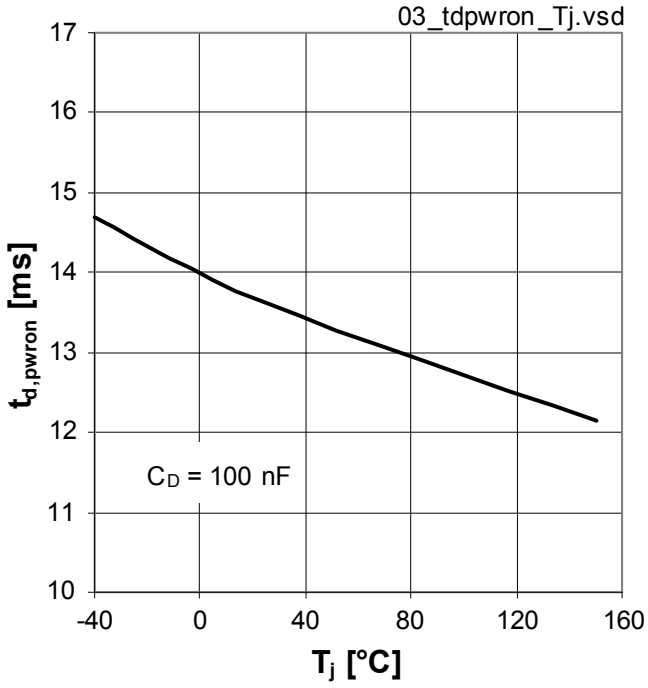
1) Related Parameter V_{RT} is scaled linear when the Reset Switching Threshold is modified.
2) For programming a different delay and reset reaction time, see **Chapter 8.1** for calculation.

8.3 Typical Performance Characteristics Reset Function

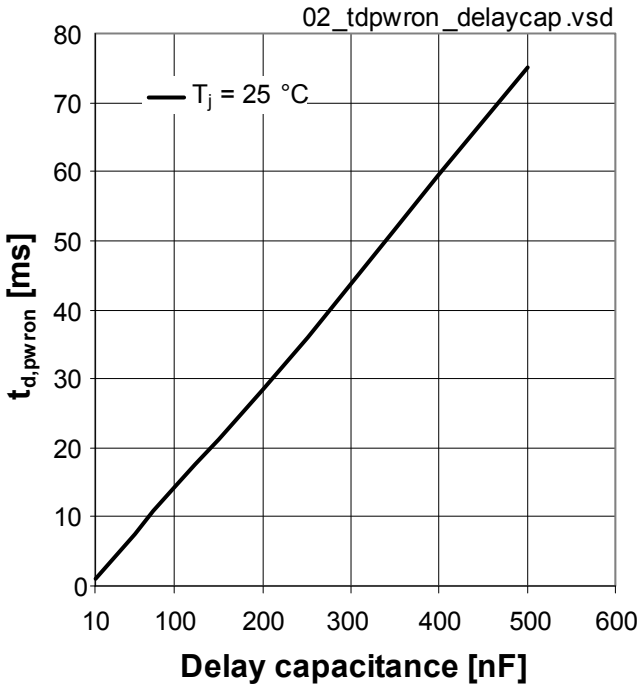
Undervoltage Reset Switching Threshold $V_{RT,hi}$/ $V_{RT,lo}$ vs. Junction Temperature T_j



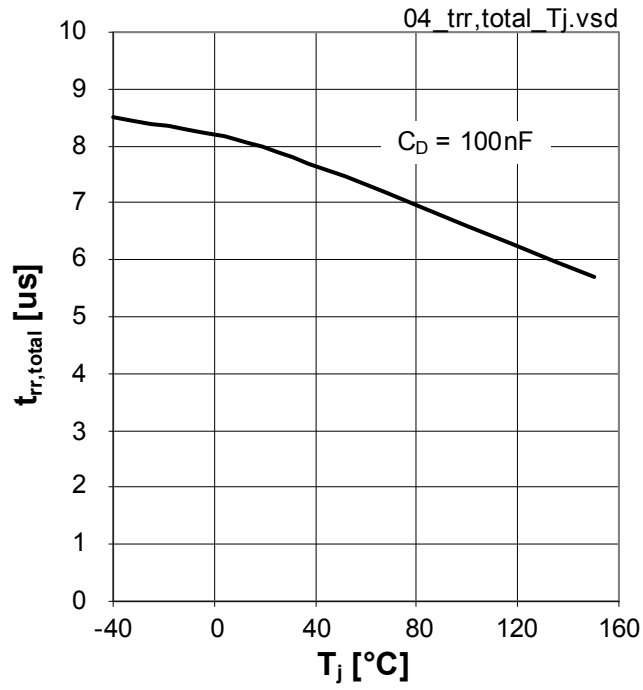
Power On Reset Delay Time t_{RD} versus Junction Temperature T_j



Power On Reset Delay Time t_{RD} versus Delay Capacitance C_D



Total Reset Reaction Time $t_{rr,total}$ versus Junction Temperature T_j



9 Watchdog Function

9.1 Description

The TLE4291 features a programmable watchdog timing.

The watchdog function monitors a microcontroller, including time base failures. In case of a missing rising edge within a certain pulse repetition time, the watchdog output is set to ‘low’. The programming of the expected watchdog pulse repetition time can be easily done by an external reset delay capacitor.

The watchdog output “WO” is separated from the reset output “RO”. Hence, the watchdog output might be used as an interrupt signal for the microcontroller independent from the reset signal. It is possible to interconnect pin “WO” and pin “RO” in order to establish a wire-or function with a dominant low signal.

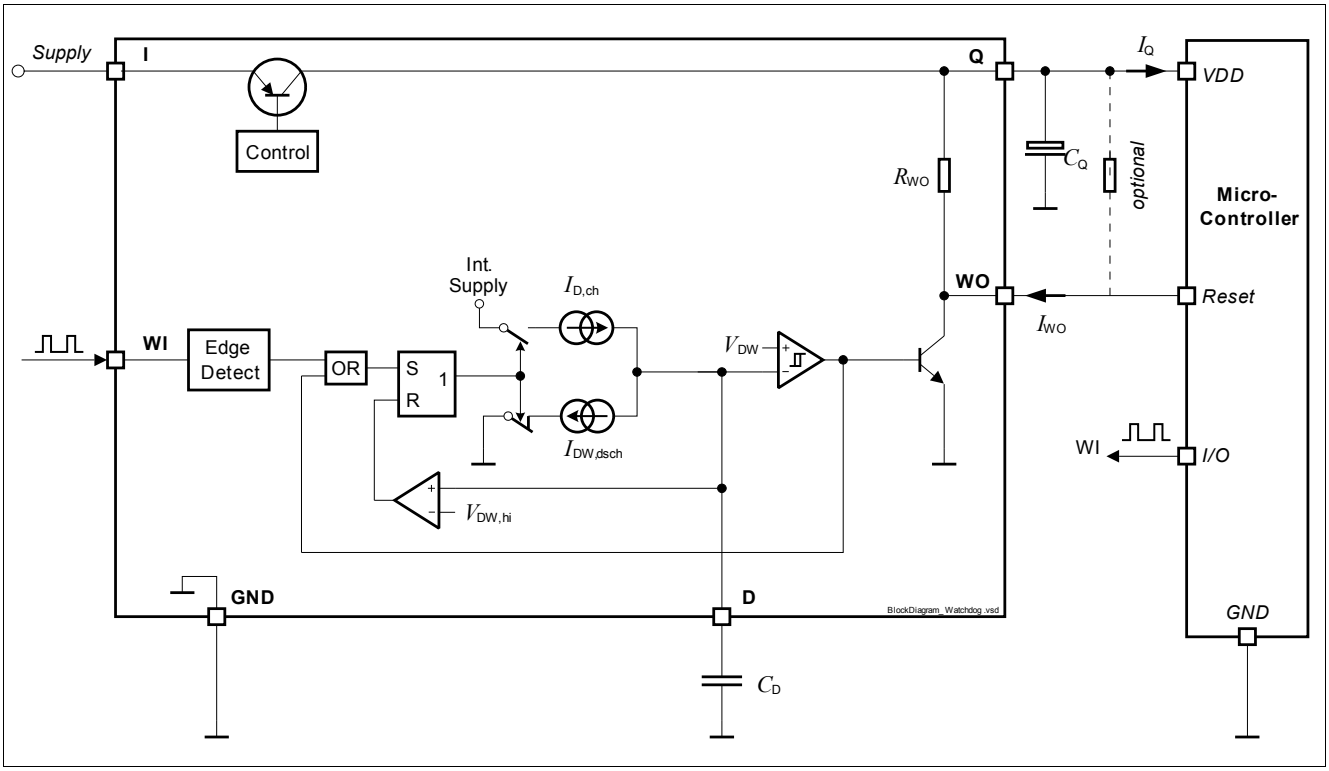


Figure 8 Block Diagram Watchdog Circuit

Watchdog Output “WO”

The watchdog output “WO” is an open collector output with an integrated pull-up resistor. In case a lower-ohmic “WO” signal is desired, an external pull-up resistor to the output “Q” can be connected. Since the maximum “WO” sink current is limited, the optional external resistor $R_{WO,ext}$ needs to be sized to comply with the watchdog output sink current (see **Item 9.2.8** and **Item 9.2.9**).

Watchdog Input “WI”

The watchdog is triggered by an positive edge at the watchdog input “WI”. The signal is filtered by a bandpass filter and therefore its amplitude and slope has to comply with the specification **9.2.11** to **9.2.14**. For details on the test pulse applied, see **Figure 9**.

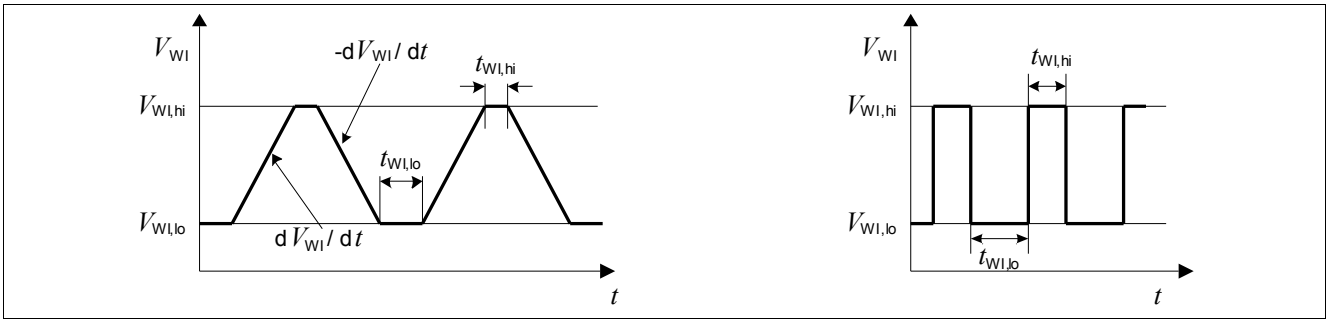


Figure 9 Test Pulses Watchdog Input WI

Watchdog Timing

Positive edges at the watchdog input pin “WI” are expected within the watchdog trigger time frame $t_{WI,tr}$, otherwise a low signal at pin “WO” is generated. If a watchdog low signal at pin “WO” is generated, it remains low for $t_{WD,lo}$. All watchdog timings are defined by charging and discharging the capacitor C_D at pin “D”. Thus, the watchdog timing can be programmed by selecting C_D. For timing details see also **Figure 10**.

In case a watchdog trigger time period $t_{WI,tr}$ different from the value for C_D = 100nF is required, the delay capacitor’s value can be derived from the specified value given in **Item 9.2.5**:

$$C_D = 100nF \times t_{WI,tr} / t_{WI,tr,100nF} \quad (4)$$

The watchdog output low time $t_{WD,lo}$ and the watchdog period $t_{WD,p}$ then becomes:

$$t_{WD,lo} = t_{WD,lo,100nF} \times C_D / 100nF \quad (5)$$

$$t_{WD,p} = t_{WI,tr} + t_{WD,lo} \quad (6)$$

The formula is valid for $C_D \geq 10nF$. For precise timing calculations consider also the delay capacitor’s tolerance.

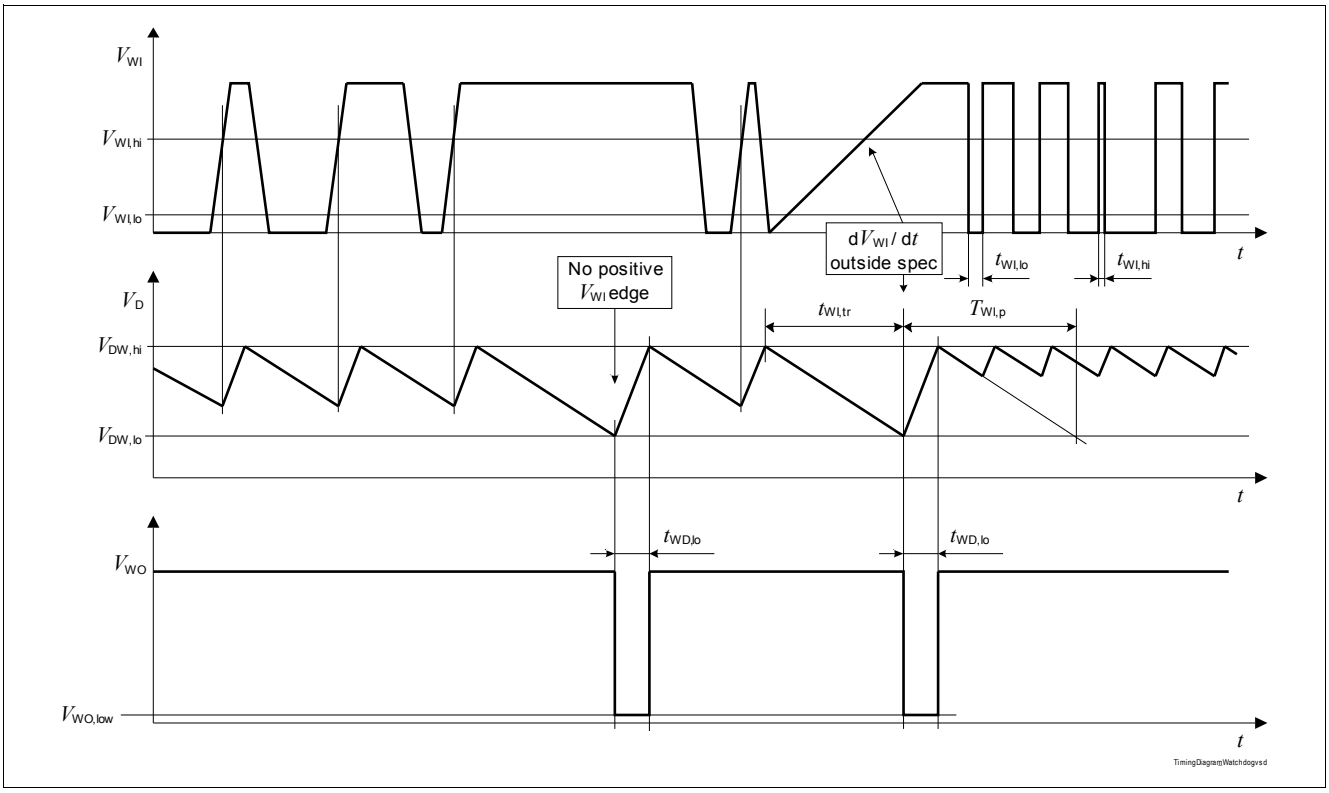


Figure 10 Timing Diagram Watchdog

9.2 Electrical Characteristics Watchdog Function

Electrical Characteristics Watchdog Function

V_I = 13.5V, T_j = -40 °C to +150 °C,
all voltages with respect to ground, direction of currents as shown in **Figure 8** (unless otherwise specified).

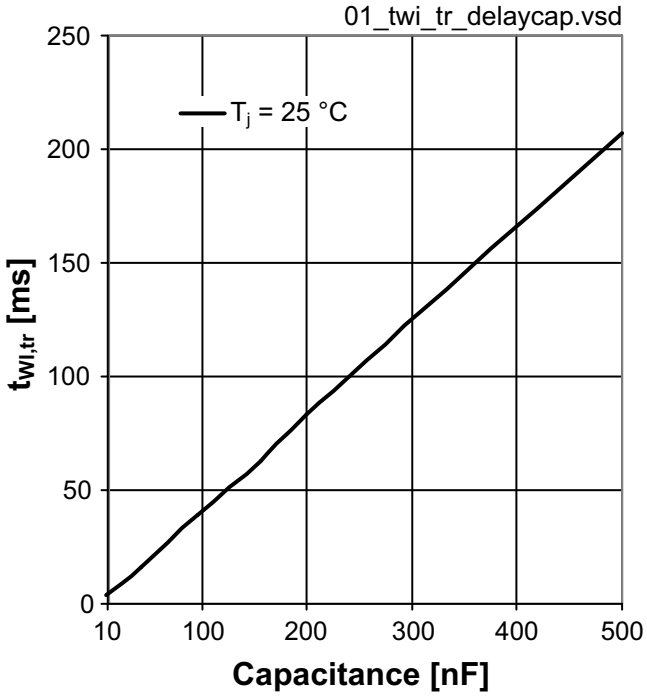
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Watchdog Timing							
9.2.1	Delay Capacitor Charge Current	I_D	–	6.5	–	µA	V_D = 0.6 V
9.2.2	Delay capacitor watchdog discharge current	$I_{DW,disch}$	–	1.4	–	µA	V_D = 0.6 V
9.2.3	Upper watchdog timing threshold	$V_{DW,hi}$	–	0.9	–	V	–
9.2.4	Lower watchdog timing threshold	$V_{DW,lo}$	–	0.35	–	V	–
9.2.5	Watchdog Trigger Time	$t_{WI,tr,100nF}$	24	40	58	ms	Calculated value; C_D = 100 nF 1)
9.2.6	Watchdog Output Low Time	$t_{WD,lo,100nF}$	6	8	12	ms	Calculated value; C_D = 100 nF 1); $V_Q > V_{RT,lo}$
9.2.7	Watchdog Period	$t_{WD,p,100nF}$	30	48	70	ms	Calculated value; $t_{WI,tr,100nF} + t_{WD,lo,100nF}$; C_D = 100 nF 1)
Watchdog Output WO							
9.2.8	Watchdog Output Low Voltage	$V_{WO,low}$	–	0.1	0.4	V	I_{WO} = 1 mA; V_{WI} = 0 V
9.2.9	Watchdog Output Maximum Sink Current	$I_{WO,max}$	1.5	13	30	mA	V_{WO} = 0.8 V; V_{WI} = 0 V
9.2.10	Watchdog Output Internal Pull-up Resistor	R_{WO}	20	30	40	kΩ	–
Watchdog Input WI							
9.2.11	Watchdog Input Low Signal Valid	$V_{WI,lo}$	–	–	0.8	V	2)
9.2.12	Watchdog Input High Signal Valid	$V_{WI,hi}$	2.6	–	–	V	2)
9.2.13	Watchdog Input High Signal Pulse Length	$t_{WI,hi}$	0.5	–	–	µs	$V_{WI} \geq V_{WI,hi}$ 2)
9.2.14	Watchdog Input Low Signal Pulse Length (Slewrate ≥ 1 V/µs)	$t_{WI,lo}$	2	–	–	µs	$V_{WI} \leq V_{WI,lo}$ 2); $dV_{WI}/dt \geq 1$ V/µs
9.2.15	Watchdog Input Low Signal Pulse Length (Slewrate ≥ 5 V/µs)	$t_{WI,lo}$	0.5	–	–	µs	$V_{WI} \leq V_{WI,lo}$ 2); $dV_{WI}/dt \geq 5$ V/µs $V_{WI,hi} \geq 4$ V

1) For programming a different watchdog timing, see **Chapter 9.1**.

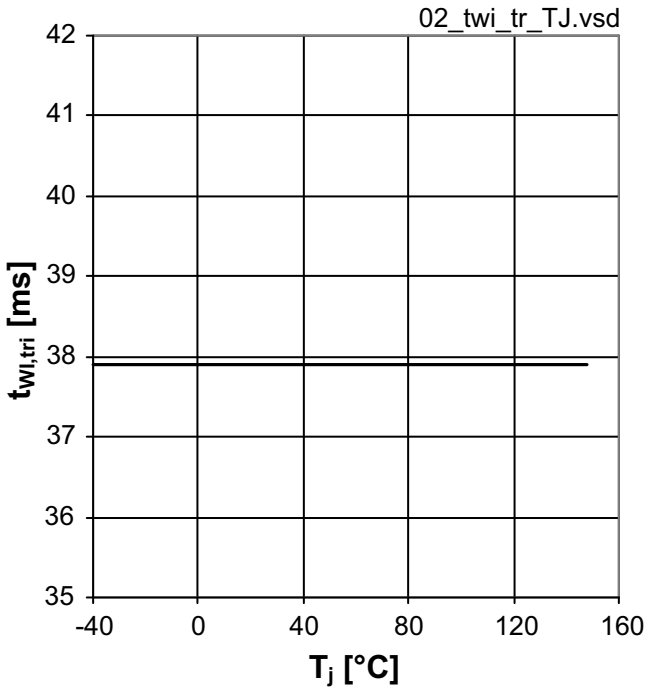
2) For details on the test pulse applied, see **Figure 9**.

9.3 Typical Performance Characteristics Standard Watchdog Function

Watchdog Trigger Time $t_{WI,tr}$ versus Delay Capacitance C_D



Watchdog Trigger Time $t_{WI,tr}$ versus Junction Temperature



10 Package Outlines

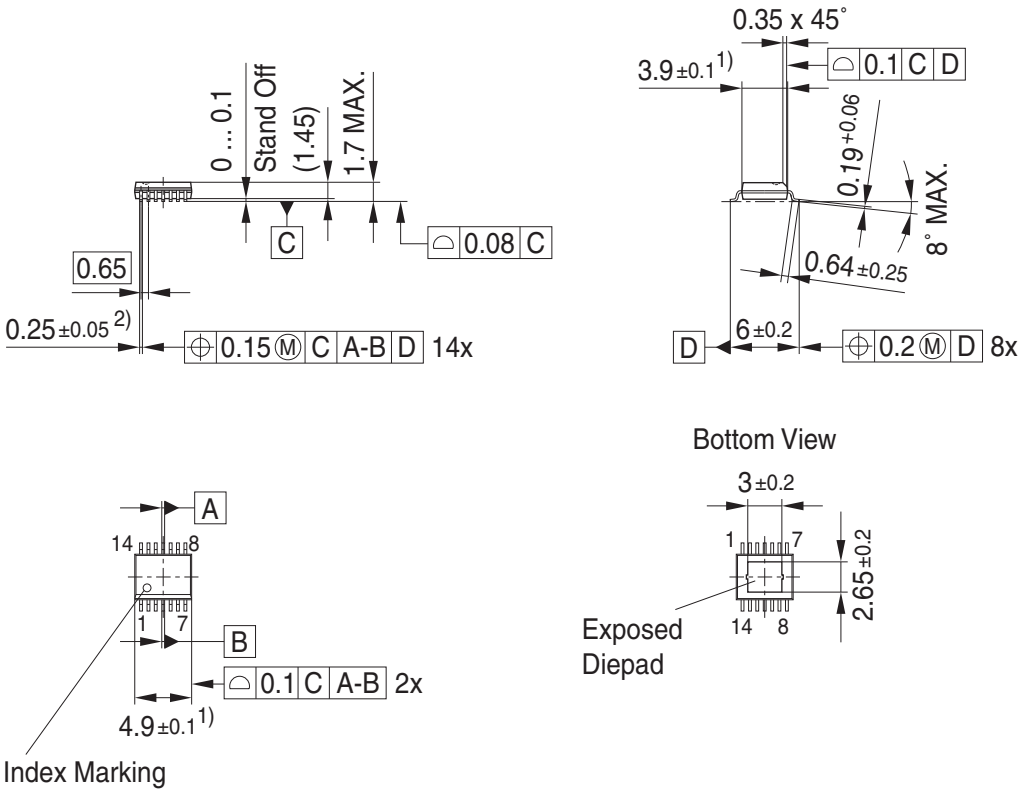


Figure 11 PG-SSOP-14 EP

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on packages, please visit our website:
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Dimensions in mm

11 Revision History

Revision	Date	Changes
1.1	2012-12-03	**Page 23**: **Figure 9**: Definition in **Test Pulses Watchdog Input WI** extended with low signal pulse length. Definition of frequency deleted according to the new specification of the watchdog input signal with high and low time. **Page 23**: **Figure 10**: Definition of watchdog input signal frequency deleted and definition for watchdog input low time added. **Page 24**: Specification for “Watchdog Input WI” corrected: Specification for watchdog input low time as replacement for watchdog input signal frequency. Slewrate specification moved to condition for watchdog input low time. **Page 24**: **9.2.14**: Specification of minimum watchdog input low time for slewrates ≥ 1 V/µs. **Page 24**: **9.2.15**: Specification of minimum watchdog input low time for slewrates ≥ 5 V/µs.
1.0	2011-06-07	Data Sheet

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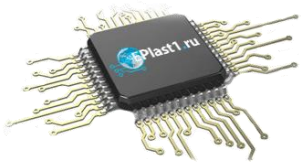

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