

NVMFD5489NL

Power MOSFET

60 V, 65 mΩ, 12 A, Dual N-Ch Logic Level

Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- 175°C Operating Temperature
- NVMFD5489NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage			V _{GS}	± 20	V
Continuous Drain Current R _{ΨJ-mb} (Notes 1, 2, 3, 4)	Steady State	T _{mb} = 25°C	I _D	12	A
		T _{mb} = 100°C		8.8	
Power Dissipation R _{ΨJ-mb} (Notes 1, 2, 3)	Steady State	T _{mb} = 25°C	P _D	23.4	W
		T _{mb} = 100°C		11.7	
Continuous Drain Current R _{θJA} (Notes 1, 3 & 4)	Steady State	T _A = 25°C	I _D	4.5	A
		T _A = 100°C		3.2	
Power Dissipation R _{θJA} (Notes 1 & 3)	Steady State	T _A = 25°C	P _D	3.0	W
		T _A = 100°C		1.5	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	62	A
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	°C
Source Current (Body Diode)			I _S	22	A
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _{L(pk)} = 19.5 A, L = 0.1 mH, R _G = 25 Ω)			E _{AS}	19	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Mounting Board (top) – Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	6.4	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	50	
Junction-to-Ambient – Steady State (min footprint)		161	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

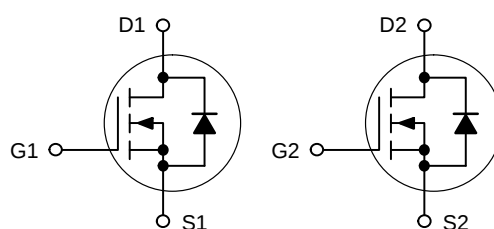


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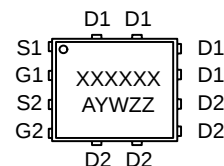
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	65 mΩ @ 10 V	12 A
	79 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



XXXXXX = 5489NL
(NVMFD5489NL) or
5489LW
(NVMFD5489NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NVMFD5489NLT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5489NLT3G	DFN8 (Pb-Free)	5000/ Tape & Reel
NVMFD5489NLWFT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5489NLWFT3G	DFN8 (Pb-Free)	5000/ Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFD5489NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to 25°C $I_D = 250\text{ }\mu\text{A}$		67		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V},$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C $I_D = 250\text{ }\mu\text{A}$		4.86		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		52	65	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$		66	79	

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		330		pF
Output Capacitance	C_{oss}			80		
Reverse Transfer Capacitance	C_{rss}			39		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 6\text{ A}$		12.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.31		
Gate-to-Source Charge	Q_{GS}			1.3		
Gate-to-Drain Charge	Q_{GD}			4.74		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 6\text{ A}, R_G = 2.5\text{ }\Omega$		7		ns
Rise Time	t_r			11		
Turn-Off Delay Time	$t_{d(off)}$			31		
Fall Time	t_f			21		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$	0.83	1.2	V
			$T_J = 125^\circ\text{C}$	0.71		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 10\text{ A}$		24.2		ns
Charge Time	t_a			20.2		
Discharge Time	t_b			4.0		
Reverse Recovery Charge	Q_{RR}			26.5		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	L_D			0.005		
Gate Inductance	L_G			1.84		
Gate Resistance	R_G			12		Ω

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

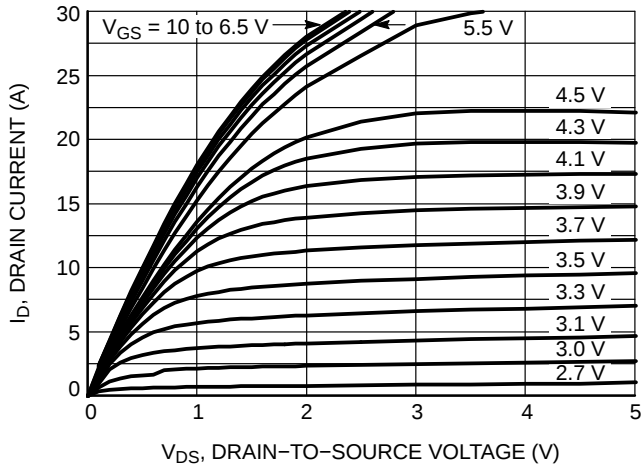


Figure 1. On-Region Characteristics

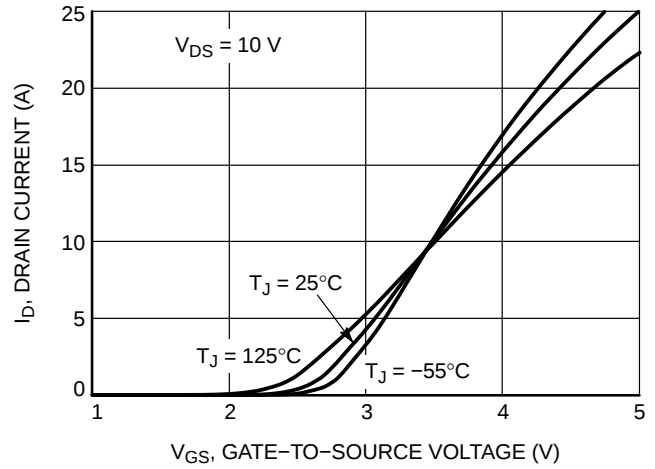


Figure 2. Transfer Characteristics

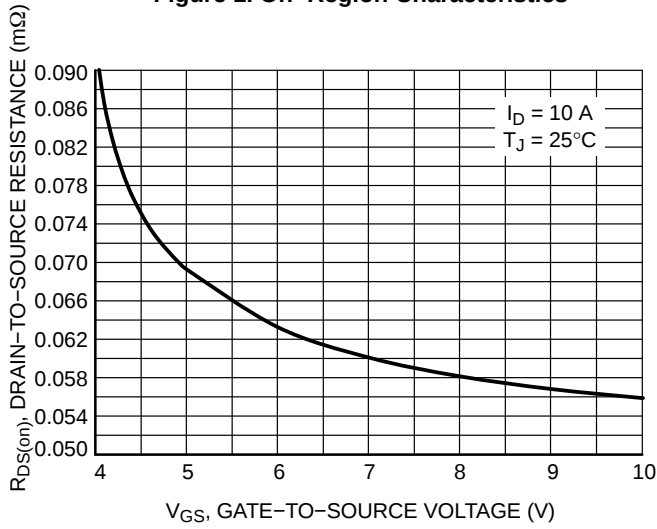


Figure 3. On-Resistance vs. V_{GS}

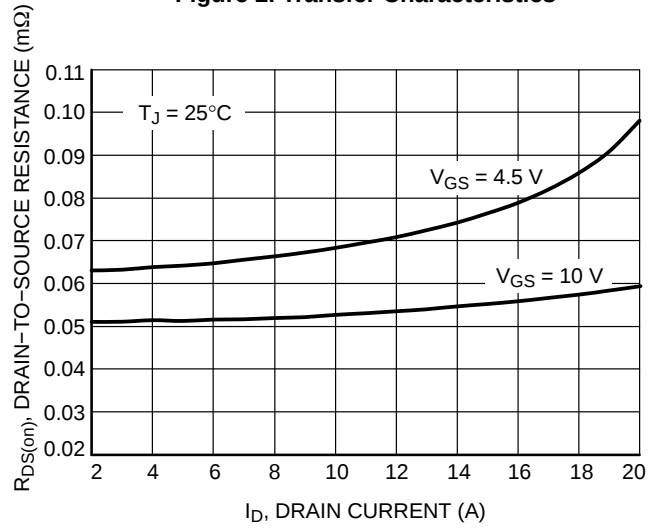


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

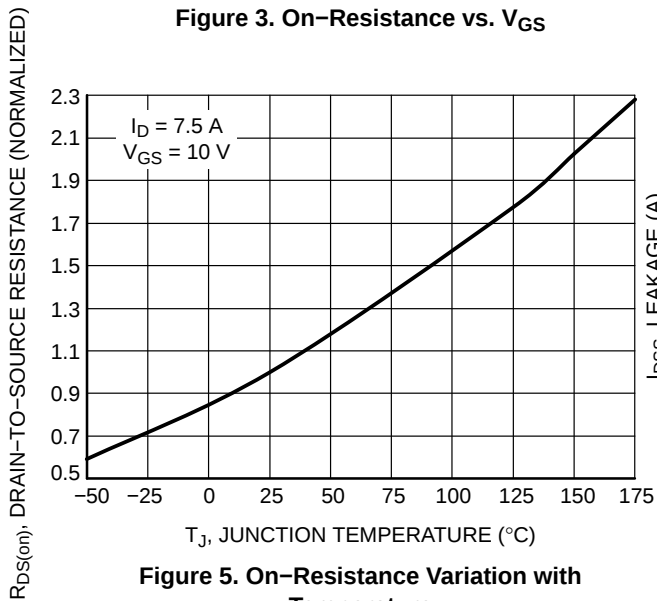


Figure 5. On-Resistance Variation with Temperature

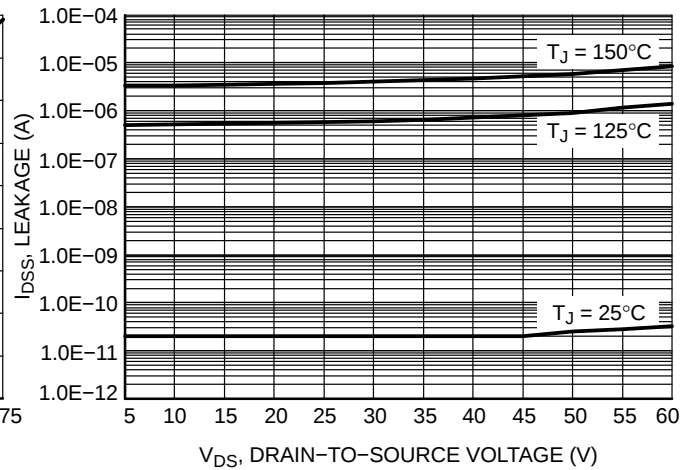


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

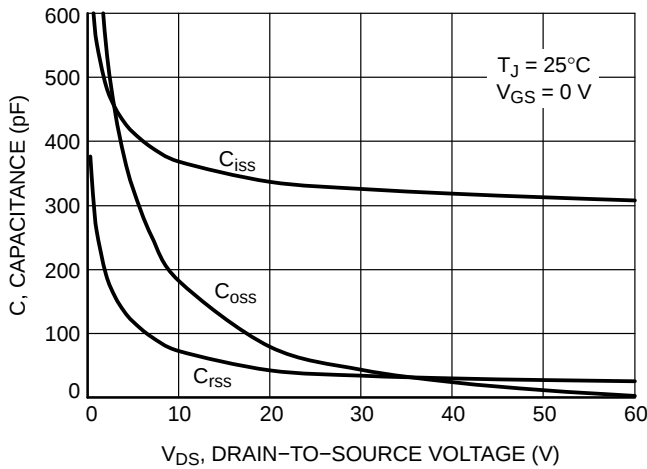


Figure 7. Capacitance Variation

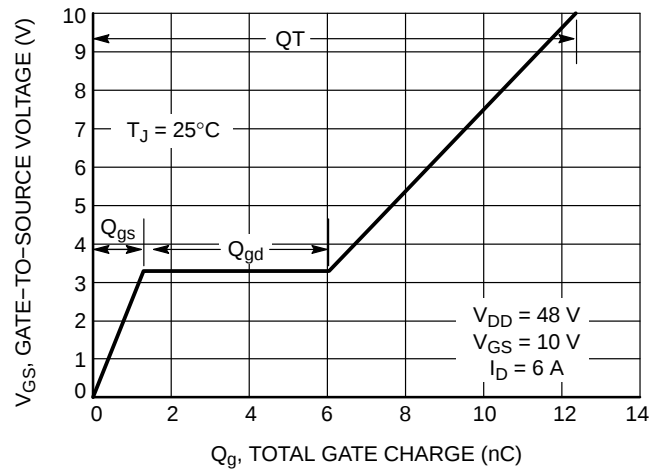


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

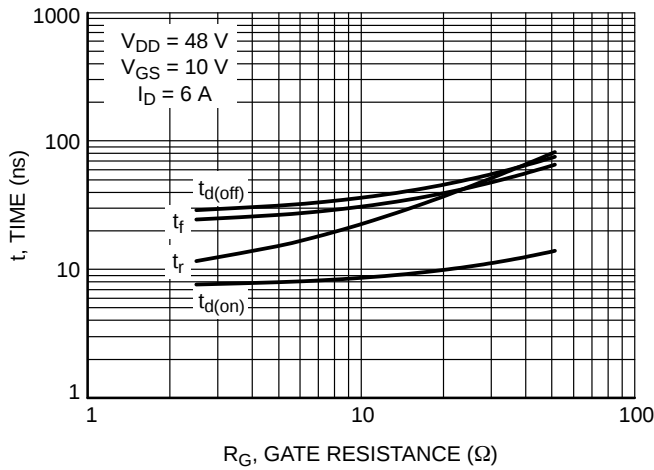


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

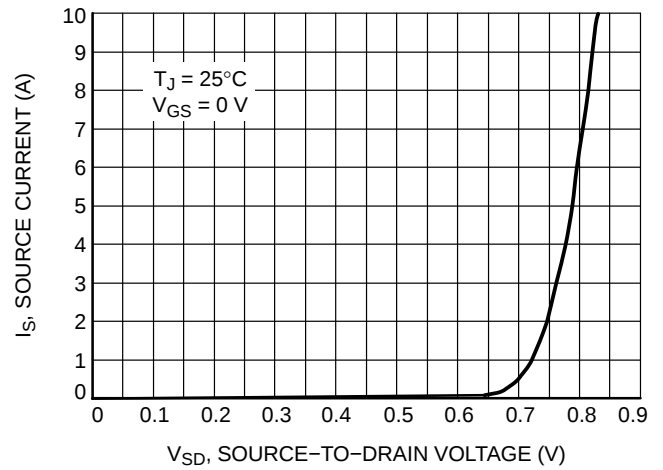


Figure 10. Diode Forward Voltage vs. Current

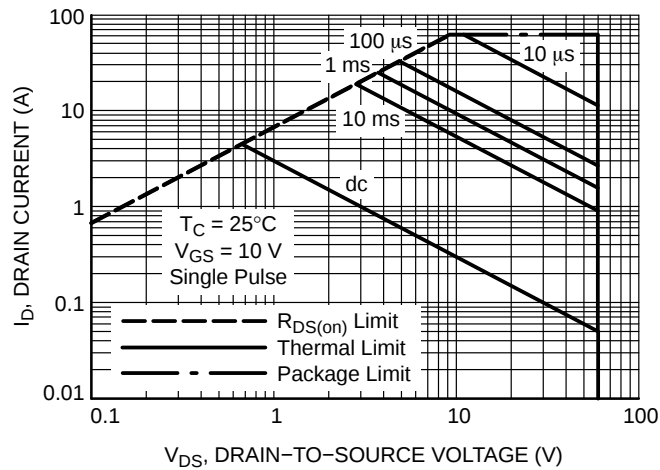


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

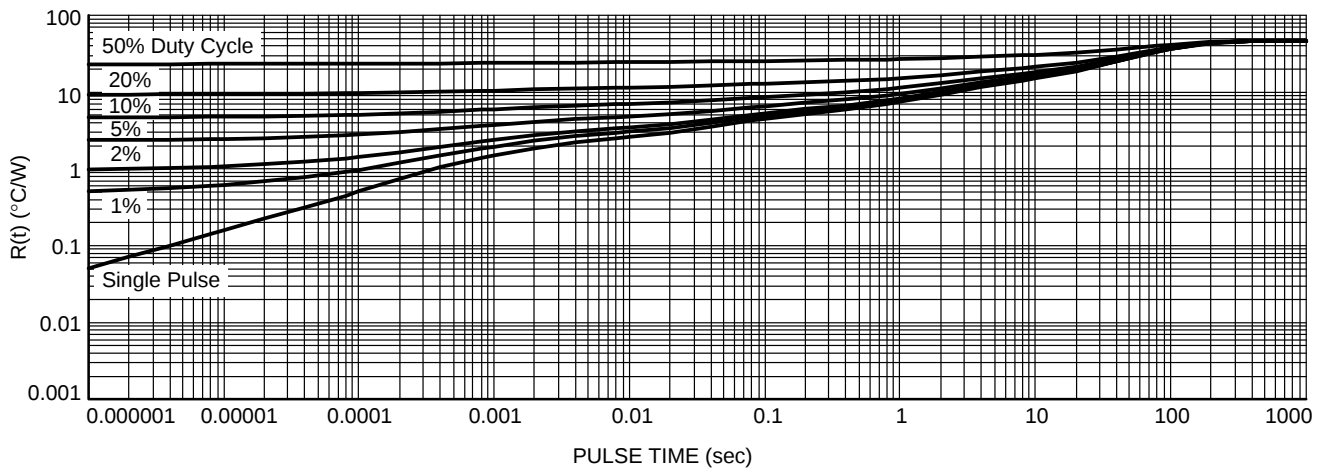
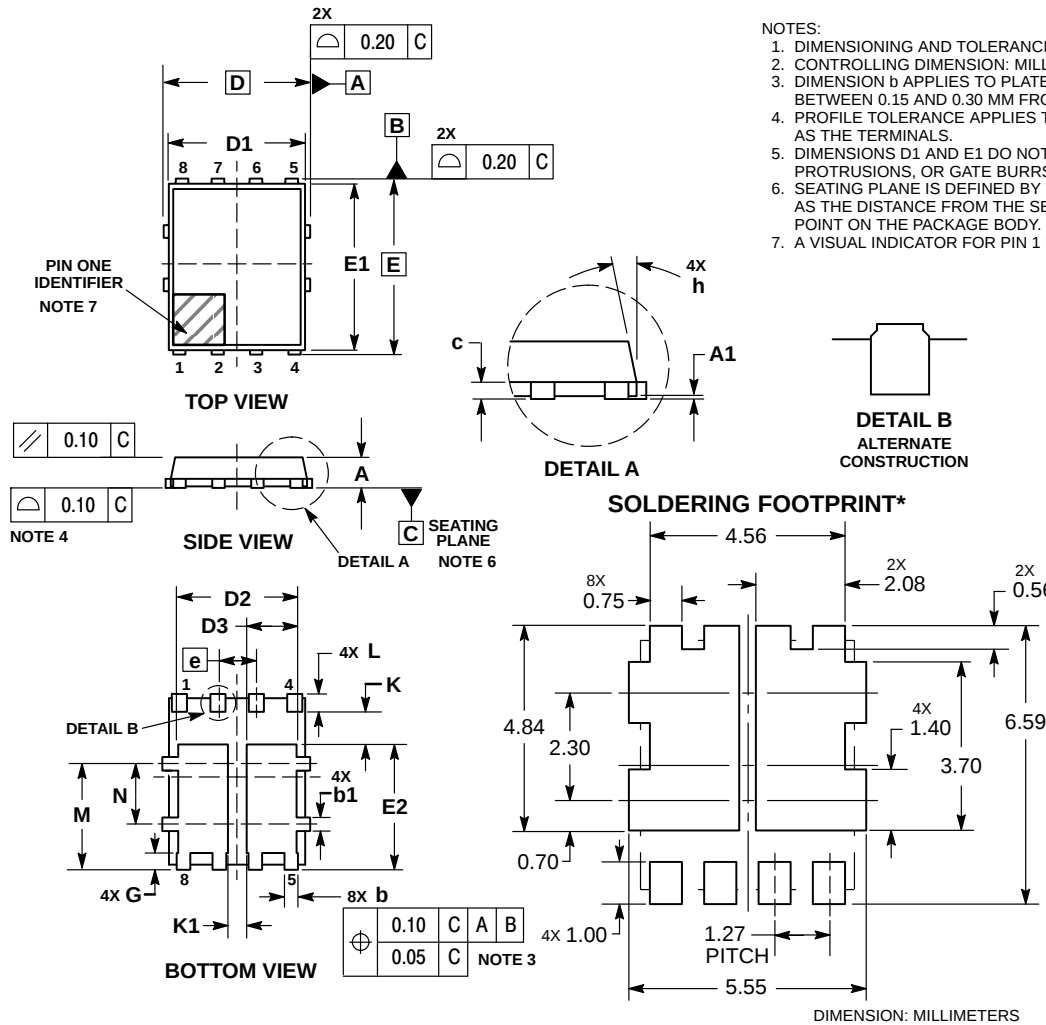


Figure 12. Thermal Response

NVMFD5489NL

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual) CASE 506BT ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
 4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
 7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Техническая поддержка проекта;
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