LPC15xx

32-bit ARM Cortex-M3 microcontroller; up to 256 kB flash and 36 kB SRAM; FS USB, CAN, RTC, SPI, USART, I2C

Rev. 1.1 — 29 April 2015 Product data sheet

1. General description

The LPC15xx are ARM Cortex-M3 based microcontrollers for embedded applications featuring a rich peripheral set with very low power consumption. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration.

The LPC15xx operate at CPU frequencies of up to 72 MHz. The ARM Cortex-M3 CPU incorporates a 3-stage pipeline and uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. The ARM Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branching.

The LPC15xx includes up to 256 kB of flash memory, 32 kB of ROM, a 4 kB EEPROM, and up to 36 kB of SRAM. The peripheral complement includes one full-speed USB 2.0 device, two SPI interfaces, three USARTs, one Fast-mode Plus I^2C-bus interface, one C_CAN module, PWM/timer subsystem with four configurable, multi-purpose State Configurable Timers (SCTimer/PWM) with input pre-processing unit, a Real-time clock module with independent power supply and a dedicated oscillator, two 12-channel/12-bit, 2 Msamples/s ADCs, one 12-bit, 500 kSamples/s DAC, four voltage comparators with internal voltage reference, and a temperature sensor. A DMA engine can service most peripherals.

For additional documentation related to the LPC15xx parts, see Section 17 “References”.

2. Features and benefits

- System:
  - ARM Cortex-M3 processor (version r2p1), running at frequencies of up to 72 MHz.
  - ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - Serial Wire Debug (SWD) with four breakpoints and two watchpoints.
  - Single-cycle multiplier supported.
  - Memory Protection Unit (MPU) included.
- Memory:
  - Up to 256 kB on-chip flash programming memory with 256 Byte page write and erase.
  - Up to 36 kB SRAM.
  - 4 kB EEPROM.

- ROM API support:
  - Boot loader with boot options from flash or external source via USART, C_CAN, or USB
  - USB drivers
  - ADC drivers
  - SPI drivers
  - USART drivers
  - I2C drivers
  - Power profiles and power mode configuration with low-power mode configuration option
  - DMA drivers
  - C_CAN drivers
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
  - Simple DMA engine with 18 channels and 20 programmable input triggers.
  - High-speed GPIO interface with up to 76 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, open-drain mode, input inverter, and programmable digital glitch filter.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight external inputs.
  - Two GPIO grouped port interrupts.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - Quadrature Encoder Interface (QEI).
- Configurable PWM/timer/motor control subsystem:
  - Up to four 32-bit counter/timers or up to eight 16-bit counter/timers or combinations of 16-bit and 32-bit timers.
  - Up to 28 match outputs and 22 configurable capture inputs with input multiplexer.
  - Up to 28 PWM outputs total.
  - Dither engine for improved average resolution of pulse edges.
  - Four State Configurable Timers (SCTimers) for highly flexible, event-driven timing and PWM applications.
  - SCT Input Pre-processor Unit (SCTIPU) for processing timer inputs and immediate handling of abort situations.
  - Integrated with ADC threshold compare interrupts, temperature sensor, and analog comparator outputs for motor control feedback using analog signals.
- Special-application and simple timers:
  - 24-bit, four-channel, multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Repetitive interrupt timer for general purpose use.
  - Windowed Watchdog timer (WWDT).
  - High-resolution 32-bit Real-time clock (RTC) with selectable 1 s or 1 ms time resolution running in the always-on power domain. RTC can be used for wake-up from all low power modes including Deep power-down.

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- Analog peripherals:
  - Two 12-bit ADC with up to 12 input channels per ADC and with multiple internal and external trigger inputs and sample rates of up to 2 Msamples/s. Each ADC supports two independent conversion sequences. ADC conversion clock can be the system clock or an asynchronous clock derived from one of the three PLLs.
  - One 12-bit DAC.
  - Integrated temperature sensor and band gap internal reference voltage.
  - Four comparators with external and internal voltage references (ACMP0 to 3). Comparator outputs are internally connected to the SCTimer/PWMs and ADCs and externally to pins. Each comparator output contains a programmable glitch filter.
- Serial interfaces:
  - Three USART interfaces with DMA, RS-485 support, autobaud, and with synchronous mode and 32 kHz mode for wake-up from Deep-sleep and Power-down modes. The USARTs share a fractional baud-rate generator.
  - Two SPI controllers.
  - One I^2C-bus interface supporting fast mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode.
  - One C_CAN controller.
  - One USB 2.0 full-speed device controller with on-chip PHY.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - Watchdog oscillator with a frequency range of 503 kHz.
  - 32 kHz low-power RTC oscillator with 32 kHz, 1 kHz, and 1 Hz outputs.
  - System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
  - Two additional PLLs for generating the USB and SCTimer/PWM clocks.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - APIs provided for optimizing power consumption in active and sleep modes and for configuring Deep-sleep, Power-down, and Deep power-down modes.
  - Wake-up from Deep-sleep and Power-down modes on activity on USB, USART, SPI, and I2C peripherals.
  - Wake-up from Sleep, Deep-sleep, Power-down, and Deep power-down modes from the RTC alarm or wake-up interrupts.
  - Timer-controlled self wake-up from Deep power-down mode using the RTC high-resolution/wake-up 1 kHz timer.
  - Power-On Reset (POR).
  - BrownOut Detect BOD).
- JTAG boundary scan modes supported.
- Unique device serial number for identification.

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- Single power supply 2.4 V to 3.6 V.
- Temperature range −40 °C to +105 °C.
- Available as LQFP100, LQFP64, and LQFP48 packages.

3. Applications

- Motor control
- Motion drives
- Digital power supplies
- Industrial and medical
- Solar inverters
- Home appliances
- Building and factory automation

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1549JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1549JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1549JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1548JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1548JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1547JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC1519JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1519JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1518JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC1518JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC1517JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

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4.1 Ordering options

Table 2. Ordering options for LPC15xx

Type number	Flash/ kB	EEPROM/ kB	Total SRAM/ kB	USB	USART	I^2C	SPI	C_CAN	SCTimer/ PWM	12-bit ADC0/1 channels	DAC	GPIO
LPC1549JBD100	256	4	36	yes	3	1	2	1	4	12/12	1	76
LPC1549JBD64	256	4	36	yes	3	1	2	1	4	12/12	1	44
LPC1549JBD48	256	4	36	yes	3	1	2	1	4	9/7	1	30
LPC1548JBD100	128	4	20	yes	3	1	2	1	4	12/12	1	76
LPC1548JBD64	128	4	20	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD64	64	4	12	yes	3	1	2	1	4	12/12	1	44
LPC1547JBD48	64	4	12	yes	3	1	2	1	4	9/7	1	30
LPC1519JBD100	256	4	36	no	3	1	2	1	4	12/12	1	78
LPC1519JBD64	256	4	36	no	3	1	2	1	4	12/12	1	46
LPC1518JBD100	128	4	20	no	3	1	2	1	4	12/12	1	78
LPC1518JBD64	128	4	20	no	3	1	2	1	4	12/12	1	46
LPC1517JBD64	64	4	12	no	3	1	2	1	4	12/12	1	46
LPC1517JBD48	64	4	12	no	3	1	2	1	4	9/7	1	32

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5. Marking

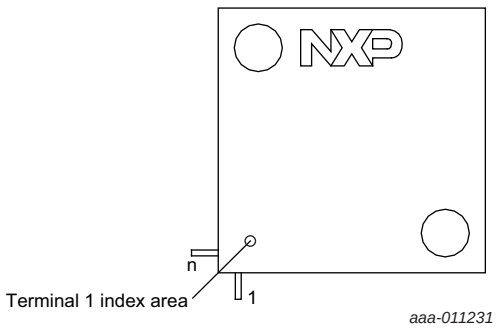

Fig 1. LQFP64/100 package marking

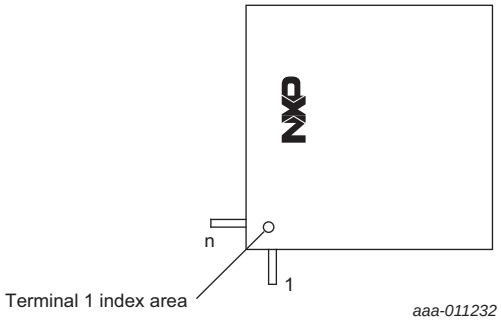

Fig 2. LQFP48 package marking

The LPC15xx devices typically have the following top-side marking for LQFP100 packages:

LPC15xxJxxx
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP64 packages:

LPC15xxJ
Xxxxxx xx
xxxyywwxxx

The LPC15xx devices typically have the following top-side marking for LQFP48 packages:

LPC15xxJ
Xxxxxx
Xxxyy
wwxxx

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

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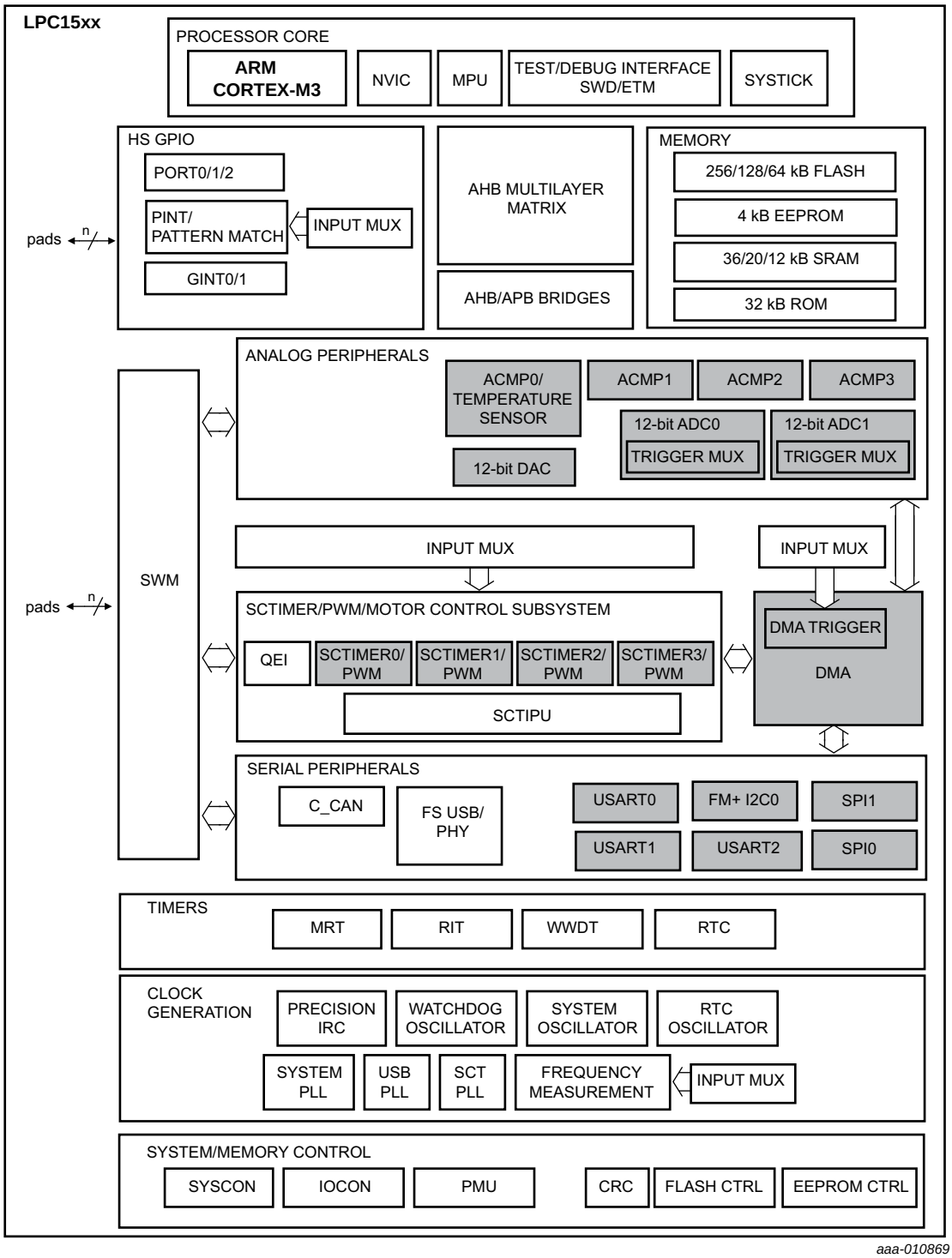
6. Block diagram



Grey-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

Fig 3. LPC15xx Block diagram

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7. Pinning information

7.1 Pinning

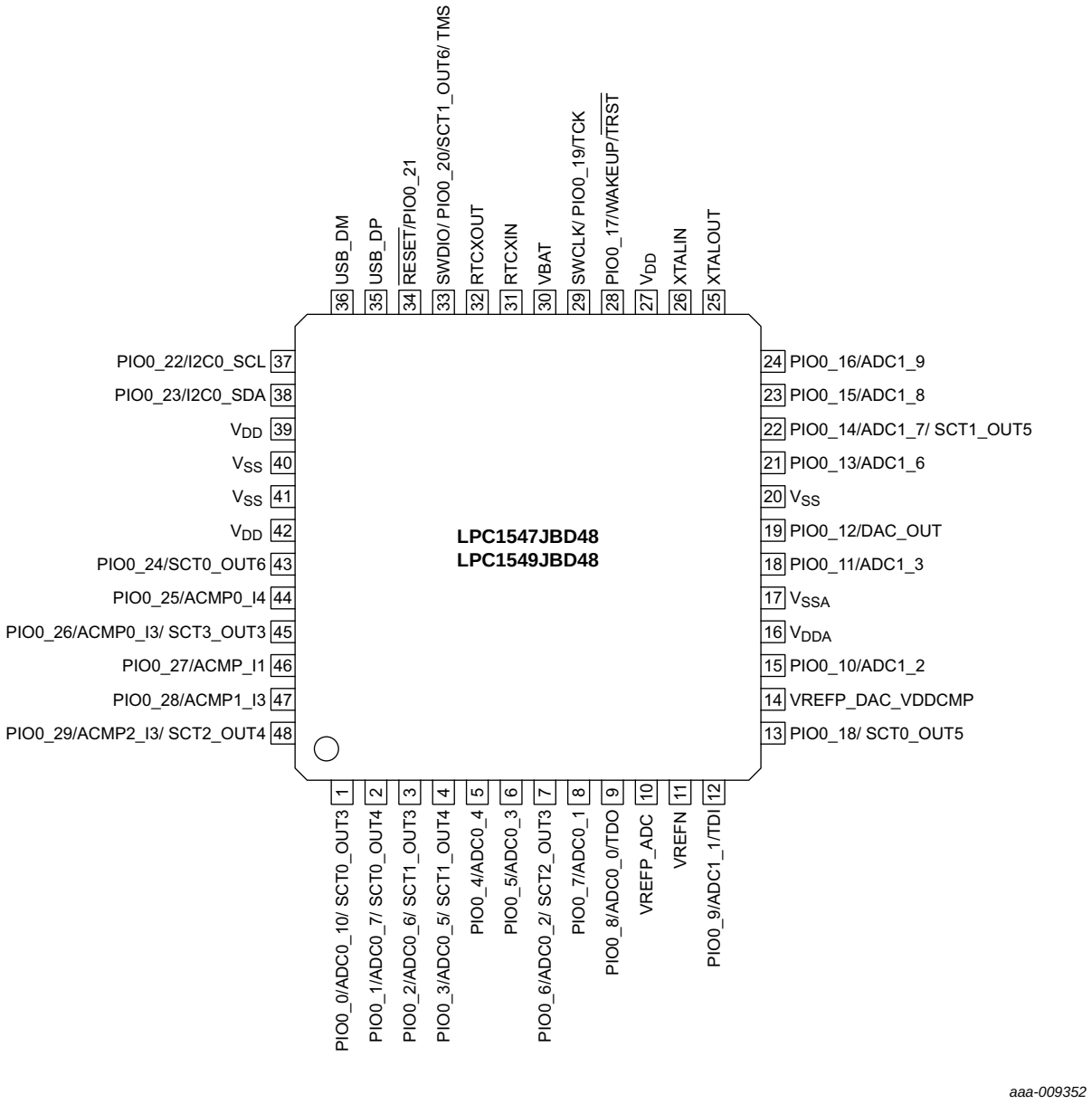

Fig 4. LQFP48 pin configuration (with USB)

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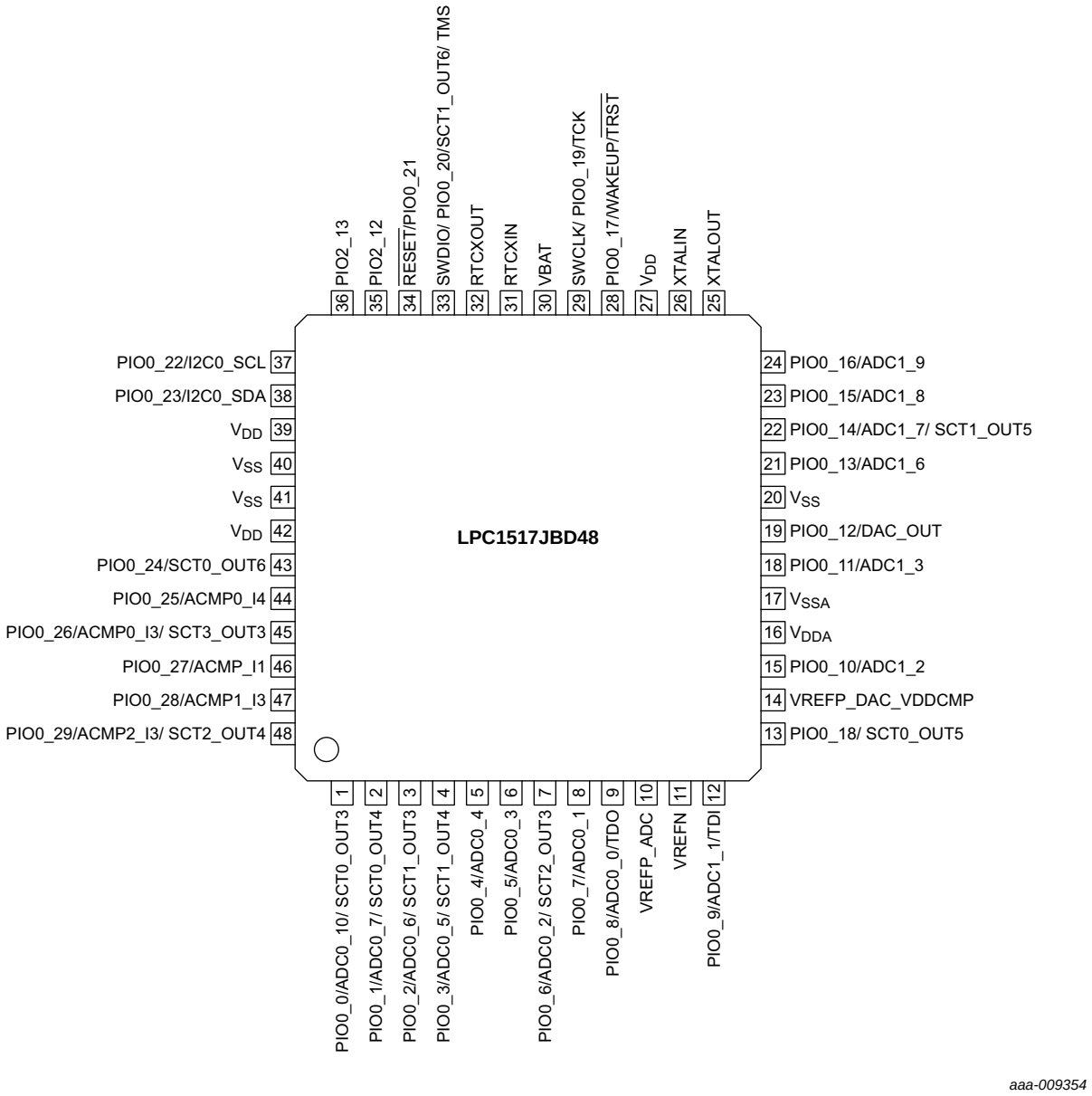

Fig 5. LQFP48 pin configuration (without USB)

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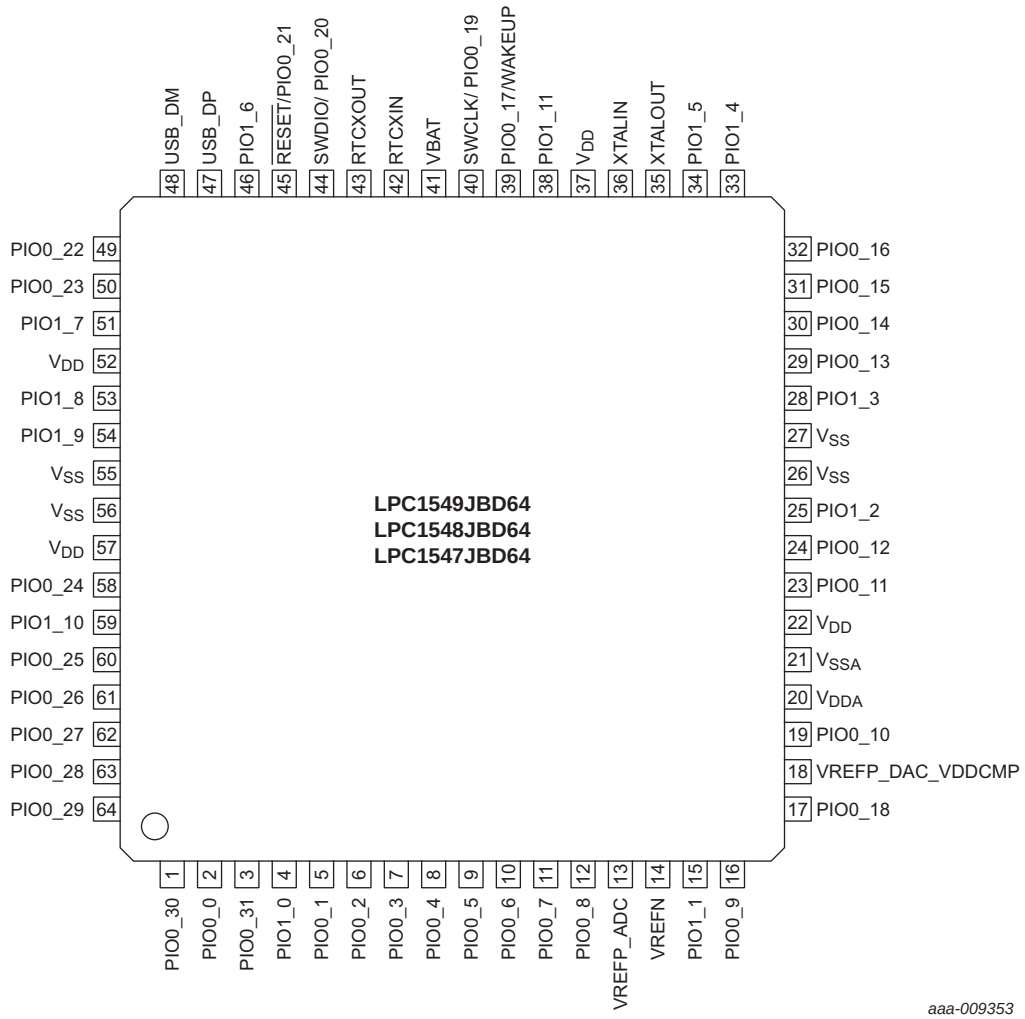

See Table 3 for the full pin name.

Fig 6. LQFP64 pin configuration (with USB)

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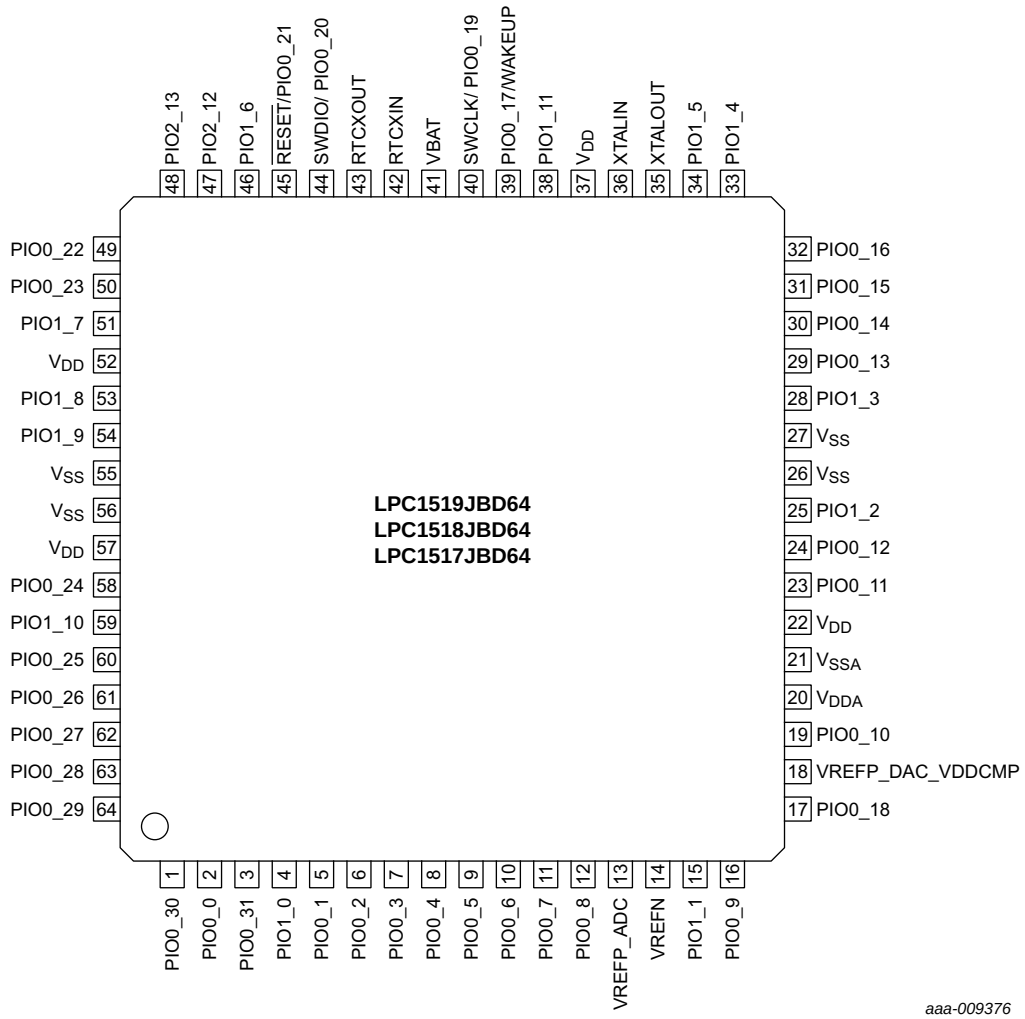

Fig 7. LQFP64 pin configuration (without USB)

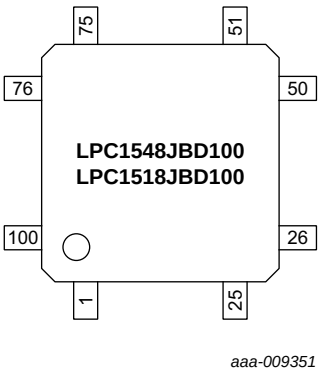

Fig 8. LQFP100 pin configuration

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7.2 Pin description

Most pins are configurable for multiple functions, which can be analog or digital. Digital inputs can be connected to several peripherals at once, however only one digital output or one analog function can be assigned to any on pin. The pin's connections to internal peripheral blocks are configured by the switch matrix (SWM), the input multiplexer (INPUT MUX), and the SCT Input Pre-processor Unit (SCTIPU).

The switch matrix enables certain fixed-pin functions that can only reside on specific pins (see Table 3) and assigns all other pin functions (movable functions) to any available pin (see Table 4), so that the pinout can be optimized for a given application.

The input multiplexer provides many choices (pins and internal signals) for selecting the inputs of the SCTimer/PWMs and the frequency measure block. Pins that are connected to the input multiplexer are listed in Table 5. If a pin is selected in the input multiplexer, it is directly connected to the peripheral input without being routed through the switch matrix. Independently of being selected in the input multiplexer, the same pin can also be assigned by the switch matrix to another peripheral input.

Four pins can also be connected directly to the SCTIPU and at the same time be inputs to the input multiplexer and the switch matrix (see Table 5).

Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_0/ADC0_10/ SCT0_OUT3	1	2	2	[2]	I; PU	IO	**PIO0_0 —** General purpose port 0 input/output 0.
						A	**ADC0_10 —** ADC0 input 10.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
PIO0_1/ADC0_7/ SCT0_OUT4	2	5	6	[2]	I; PU	IO	**PIO0_1 —** General purpose port 0 input/output 1.
						A	**ADC0_7 —** ADC0 input 7.
						O	**SCT0_OUT4 —** SCTimer0/PWM output 4.
PIO0_2/ADC0_6/ SCT1_OUT3	3	6	8	[2]	I; PU	IO	**PIO0_2 —** General purpose port 0 input/output 2.
							ADC0_6 — ADC0 input 6.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO0_3/ADC0_5/ SCT1_OUT4	4	7	10	[2]	I; PU	IO	**PIO0_3 —** General purpose port 0 input/output 3.
						A	**ADC0_5 —** ADC0 input 5.
						O	**SCT1_OUT4 —** SCTimer1/PWM output 4.
PIO0_4/ADC0_4	5	8	13	[2]	I; PU	IO	**PIO0_4 —** General purpose port 0 input/output 4. This is the ISP_0 boot pin for the LQFP48 package.
						A	**ADC0_4 —** ADC0 input 4.
PIO0_5/ADC0_3	6	9	14	[2]	I; PU	IO	**PIO0_5 —** General purpose port 0 input/output 5.
						A	**ADC0_3 —** ADC0 input 3.
PIO0_6/ADC0_2/ SCT2_OUT3	7	10	16	[2]	I; PU	IO	**PIO0_6 —** General purpose port 0 input/output 6.
						A	**ADC0_2 —** ADC0 input 2.
						O	**SCT2_OUT3 —** SCTimer2/PWM output 3.
PIO0_7/ADC0_1	8	11	17	[2]	I; PU	IO	**PIO0_7 —** General purpose port 0 input/output 7.
						A	**ADC0_1 —** ADC0 input 1.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_8/ADC0_0/TDO	9	12	19	[2]	I; PU	IO	**PIO0_8 —** General purpose port 0 input/output 8. In boundary scan mode: TDO (Test Data Out).
						A	**ADC0_0 —** ADC0 input 0.
PIO0_9/ADC1_1/TDI	12	16	24	[2]	I; PU	IO	**PIO0_9 —** General purpose port 0 input/output 9. In boundary scan mode: TDI (Test Data In).
						A	**ADC1_1 —** ADC1 input 1.
PIO0_10/ADC1_2	15	19	28	[2]	I; PU	IO	**PIO0_10 —** General purpose port 0 input/output 10.
						A	**ADC1_2 —** ADC1 input 2.
PIO0_11/ADC1_3	18	23	33	[2]	I; PU	IO	**PIO0_11 —** General purpose port 0 input/output 11. On the LQFP64 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_3 —** ADC1 input 3.
PIO0_12/DAC_OUT	19	24	35	[3]	I; PU	IO	**PIO0_12 —** General purpose port 0 input/output 12. If this pin is configured as a digital input, the input voltage level must not be higher than V_{DDA}.
						A	**DAC_OUT —** DAC analog output.
PIO0_13/ADC1_6	21	29	43	[2]	I; PU	IO	**PIO0_13 —** General purpose port 0 input/output 13. On the LQFP64 package, this pin is assigned to U0_RXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
						A	**ADC1_6 —** ADC1 input 6.
PIO0_14/ADC1_7/ SCT1_OUT5	22	30	45	[2]	I; PU	IO	**PIO0_14 —** General purpose port 0 input/output 14. On the LQFP48 package, this pin is assigned to U0_RXD in ISP USART mode.
						A	**ADC1_7 —** ADC1 input 7.
						O	**SCT1_OUT5 —** SCTimer1/PWM output 5.
PIO0_15/ADC1_8	23	31	47	[2]	I; PU	IO	**PIO0_15 —** General purpose port 0 input/output 15. On the LQFP48 package, this pin is assigned to U0_TXD in ISP USART mode.
						A	**ADC1_8 —** ADC1 input 8.
PIO0_16/ADC1_9	24	32	49	[2]	I; PU	IO	**PIO0_16 —** General purpose port 0 input/output 16. On the LQFP48 package, this is the ISP_1 boot pin.
						A	**ADC1_9 —** ADC1 input 9.
PIO0_17/WAKEUP/ $\overline{\text{TRST}}$	28	39	61	[4]	I; PU	IO	**PIO0_17 —** General purpose port 0 input/output 17. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. For wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally while in Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_18/ SCT0_OUT5	13	17	26	[5]	I; PU	IO	**PIO0_18 —** General purpose port 0 input/output 18. On the LQFP64 package, this pin is assigned to U0_TXD in ISP USART mode. On the LQFP48 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						O	**SCT0_OUT5 —** SCTimer0/PWM output 5.
SWCLK/ PIO0_19/TCK	29	40	63	[5]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_19 —** General purpose port 0 input/output 19.
SWDIO/ PIO0_20/SCT1_OUT6/ TMS	33	44	69	[5]	I; PU	I/O	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						I/O	**PIO0_20 —** General purpose port 0 input/output 20.
						O	**SCT1_OUT6 —** SCTimer1/PWM output 6.
$\overline{\text{RESET}}$/PIO0_21	34	45	71	[6]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{RESET}}$ function is not needed and the Deep power-down mode is not used.
						I/O	**PIO0_21 —** General purpose port 0 input/output 21.
PIO0_22/I2C0_SCL	37	49	78	[7]	IA	IO	**PIO0_22 —** General purpose port 0 input/output 22 (open-drain)
						I/O	**I2C0_SCL —** Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_23/I2C0_SDA	38	50	79	[7]	IA	IO	**PIO0_23 —** General purpose port 0 input/output 23 (open-drain).
						I/O	**I2C0_SDA —** I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_24/SCT0_OUT6	43	58	90	[8]	I; PU	IO	**PIO0_24 —** General purpose port 0 input/output 24. High-current output driver.
						O	**SCT0_OUT6 —** SCTimer0/PWM output 6.
PIO0_25/ACMP0_I4	44	60	93	[2]	I; PU	IO	**PIO0_25 —** General purpose port 0 input/output 25.
						A	**ACMP0_I4 —** Analog comparator 0 input 4.
PIO0_26/ACMP0_I3/ SCT3_OUT3	45	61	95	[2]	I; PU	IO	**PIO0_26 —** General purpose port 0 input/output 26.
						A	**ACMP0_I3 —** Analog comparator 0 input 3.
						O	**SCT3_OUT3 —** SCTimer3/PWM output 3.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO0_27/ACMP_I1	46	62	97	[2]	I; PU	IO	**PIO0_27 —** General purpose port 0 input/output 27.
						A	**ACMP_I1 —** Analog comparator common input 1.
PIO0_28/ACMP1_I3	47	63	98	[2]	I; PU	IO	**PIO0_28 —** General purpose port 0 input/output 28.
						A	**ACMP1_I3 —** Analog comparator 1 input 3.
PIO0_29/ACMP2_I3/ SCT2_OUT4	48	64	100	[2]	I; PU	IO	**PIO0_29 —** General purpose port 0 input/output 29.
						A	**ACMP2_I3 —** Analog comparator 2 input 3.
						O	**SCT2_OUT4 —** SCTimer2/PWM output 4.
PIO0_30/ADC0_11	-	1	1	[2]	I; PU	IO	**PIO0_30 —** General purpose port 0 input/output 30.
						A	**ADC0_11 —** ADC0 input 11.
PIO0_31/ADC0_9	-	3	3	[2]	I; PU	IO	**PIO0_31 —** General purpose port 0 input/output 31. On the LQFP64 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
						A	**ADC0_9 —** ADC0 input 9.
PIO1_0/ADC0_8	-	4	5	[2]	I; PU	IO	**PIO1_0 —** General purpose port 1 input/output 0.
						A	**ADC0_8 —** ADC0 input 8.
PIO1_1/ADC1_0	-	15	23	[2]	I; PU	IO	**PIO1_1 —** General purpose port 1 input/output 1.
						A	**ADC1_0 —** ADC1 input 0.
PIO1_2/ADC1_4	-	25	36	[2]	I; PU	IO	**PIO1_2 —** General purpose port 1 input/output 2.
						A	**ADC1_4 —** ADC1 input 4.
PIO1_3/ADC1_5	-	28	41	[2]	I; PU	IO	**PIO1_3 —** General purpose port 1 input/output 3.
						A	**ADC1_5 —** ADC1 input 5.
PIO1_4/ADC1_10	-	33	51	[2]	I; PU	IO	**PIO1_4 —** General purpose port 1 input/output 4.
						A	**ADC1_10 —** ADC1 input 10.
PIO1_5/ADC1_11	-	34	52	[2]	I; PU	IO	**PIO1_5 —** General purpose port 1 input/output 5.
						A	**ADC1_11 —** ADC1 input 11.
PIO1_6/ACMP_I2	-	46	73	[2]	I; PU	IO	**PIO1_6 —** General purpose port 1 input/output 6.
						A	**ACMP_I2 —** Analog comparator common input 2.
PIO1_7/ACMP3_I4	-	51	81	[2]	I; PU	IO	**PIO1_7 —** General purpose port 1 input/output 7.
						A	**ACMP3_I4 —** Analog comparator 3 input 4.
PIO1_8/ACMP3_I3/ SCT3_OUT4	-	53	84	[2]	I; PU	IO	**PIO1_8 —** General purpose port 1 input/output 8.
						A	**ACMP3_I3 —** Analog comparator 3 input 3.
						O	**SCT3_OUT4 —** SCTimer3/PWM output 4.
PIO1_9/ACMP2_I4	-	54	85	[2]	I; PU	IO	**PIO1_9 —** General purpose port 1 input/output 9. On the LQFP64 package, this is the ISP_0 boot pin.
						A	**ACMP2_I4 —** Analog comparator 2 input 4.
PIO1_10/ACMP1_I4	-	59	91	[2]	I; PU	IO	**PIO1_10 —** General purpose port 1 input/output 10.
						A	**ACMP1_I4 —** Analog comparator 1 input 4.
PIO1_11	-	38	58	[5]	I; PU	IO	**PIO1_11 —** General purpose port 1 input/output 11. On the LQFP64 package, this is the ISP_1 boot pin.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO1_12	-	-	9	[5]	I; PU	IO	**PIO1_12 —** General purpose port 1 input/output 12.
PIO1_13	-	-	11	[5]	I; PU	IO	**PIO1_13 —** General purpose port 1 input/output 13.
PIO1_14/SCT0_OUT7	-	-	12	[5]	I; PU	IO	**PIO1_14 —** General purpose port 1 input/output 14.
						O	**SCT0_OUT7 —** SCTimer0/PWM output 7.
PIO1_15	-	-	15	[5]	I; PU	IO	**PIO1_15 —** General purpose port 1 input/output 15.
PIO1_16	-	-	18	[5]	I; PU	IO	**PIO1_16 —** General purpose port 1 input/output 16.
PIO1_17/SCT1_OUT7	-	-	20	[5]	I; PU	IO	**PIO1_17 —** General purpose port 1 input/output 17.
						O	**SCT1_OUT7 —** SCTimer1/PWM output 7.
PIO1_18	-	-	25	[5]	I; PU	IO	**PIO1_18 —** General purpose port 1 input/output 18.
PIO1_19	-	-	29	[5]	I; PU	IO	**PIO1_19 —** General purpose port 1 input/output 19.
PIO1_20/SCT2_OUT5	-	-	34	[5]	I; PU	IO	**PIO1_20 —** General purpose port 1 input/output 20.
						O	**SCT2_OUT5 —** SCTimer2/PWM output 5.
PIO1_21	-	-	37	[5]	I; PU	IO	**PIO1_21 —** General purpose port 1 input/output 21.
PIO1_22	-	-	38	[5]	I; PU	IO	**PIO1_22 —** General purpose port 1 input/output 22.
PIO1_23	-	-	42	[5]	I; PU	IO	**PIO1_23 —** General purpose port 1 input/output 23.
PIO1_24/SCT3_OUT5	-	-	44	[5]	I; PU	IO	**PIO1_24 —** General purpose port 1 input/output 24.
						O	**SCT3_OUT5 —** SCTimer3/PWM output 5.
PIO1_25	-	-	46	[5]	I; PU	IO	**PIO1_25 —** General purpose port 1 input/output 25.
PIO1_26	-	-	48	[5]	I; PU	IO	**PIO1_26 —** General purpose port 1 input/output 26.
PIO1_27	-	-	50	[5]	I; PU	IO	**PIO1_27 —** General purpose port 1 input/output 27.
PIO1_28	-	-	55	[5]	I; PU	IO	**PIO1_28 —** General purpose port 1 input/output 28.
PIO1_29	-	-	56	[5]	I; PU	IO	**PIO1_29 —** General purpose port 1 input/output 29.
PIO1_30	-	-	59	[5]	I; PU	IO	**PIO1_30 —** General purpose port 1 input/output 30.
PIO1_31	-	-	60	[5]	I; PU	IO	**PIO1_31 —** General purpose port 1 input/output 31.
PIO2_0	-	-	62	[5]	I; PU	IO	**PIO2_0 —** General purpose port 2 input/output 0.
PIO2_1	-	-	64	[5]	I; PU	IO	**PIO2_1 —** General purpose port 2 input/output 1.
PIO2_2	-	-	72	[5]	I; PU	IO	**PIO2_2 —** General purpose port 2 input/output 2.
PIO2_3	-	-	76	[5]	I; PU	IO	**PIO2_3 —** General purpose port 2 input/output 3.
PIO2_4	-	-	77	[5]	I; PU	IO	**PIO2_4 —** General purpose port 2 input/output 4. On the LQFP100 package, this is the ISP_1 boot pin.
PIO2_5	-	-	80	[5]	I; PU	IO	**PIO2_5 —** General purpose port 2 input/output 5. On the LQFP100 package, this is the ISP_0 boot pin.
PIO2_6	-	-	82	[5]	I; PU	IO	**PIO2_6 —** General purpose port 2 input/output 6. On the LQFP100 package, this pin is assigned to U0_TXD in ISP USART mode.
PIO2_7	-	-	86	[5]	I; PU	IO	**PIO2_7 —** General purpose port 2 input/output 7. On the LQFP100 package, this pin is assigned to U0_RXD in ISP USART mode.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
PIO2_8	-	-	92	[5]	I; PU	IO	**PIO2_8 —** General purpose port 2 input/output 8. On the LQFP100 package, this pin is assigned to CAN0_TD in ISP C_CAN mode.
PIO2_9	-	-	94	[5]	I; PU	IO	**PIO2_9 —** General purpose port 2 input/output 9. On the LQFP100 package, this pin is assigned to CAN0_RD in ISP C_CAN mode.
PIO2_10	-	-	96	[5]	I; PU	IO	**PIO2_10 —** General purpose port 2 input/output 10.
PIO2_11	-	-	99	[5]	I; PU	IO	**PIO2_11 —** General purpose port 2 input/output 11.
PIO2_12	35	47	74	[5]	I; PU	IO	**PIO2_12 —** General purpose port 2 input/output 12. On parts LPC1519/17/18 only.
PIO2_13	36	48	75	[5]	I; PU	IO	**PIO2_13 —** General purpose port 2 input/output 13. On parts LPC1519/17/18 only.
USB_DP	35	47	74	[10]	-	IO	USB bidirectional D+ line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
USB_DM	36	48	75	[10]	-	IO	USB bidirectional D− line. Pad includes internal 33 Ω series termination resistor. On parts LPC1549/48/47 only.
RTCXIN	31	42	66	[9]	-		RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	32	43	67	[9]	-		RTC oscillator output.
XTALIN	26	36	54	[9] [11]	-		Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	25	35	53	[9] [11]	-		Output from the oscillator amplifier.
VBAT	30	41	65		-		Battery supply voltage. Supplies power to the RTC. If no battery is used, tie VBAT to VDD or to ground.
V_{DDA}	16	20	30		-		Analog supply voltage. V_{DD} and the analog reference voltages VREFP_ADC and VREFP_DAC_VDDCMP must not exceed the voltage level on V_{DDA}. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	39, 27, 42	22, 52, 37, 57	4, 32, 70, 83, 57, 89		-		3.3 V supply voltage (2.4 V to 3.6 V). The voltage level on V_{DD} must be equal or lower than the analog supply voltage V_{DDA}.
VREFP_DAC_VDDCMP	14	18	27	[9]	-		DAC positive reference voltage and analog comparator reference voltage. The voltage level on VREFP_DAC_VDDCMP must be equal to or lower than the voltage applied to V_{DDA}.
VREFN	11	14	22		-		ADC and DAC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.

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Table 3. Pin description with fixed-pin functions

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description
VREFP_ADC	10	13	21		-		ADC positive reference voltage. The voltage level on VREFP_ADC must be equal to or lower than the voltage applied to V_{DDA}. If the ADC is not used, tie VREFP_ADC to V_{DD}.
V_{SSA}	17	21	31		-		Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	41, 20, 40	56, 26, 27, 55	88, 7, 39, 40, 68, 87		-		Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled; F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[3] This pin is not 5 V tolerant due to special analog functionality. When configured for a digital function, this pin is 3 V tolerant and provides standard digital I/O functions with configurable internal pull-up and pull-down resistors and hysteresis. When configured for DAC_OUT, the digital section of the pin is disabled and this pin is a 3 V tolerant analog output. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, and configurable hysteresis. This pin includes a 10 ns on/off glitch filter. By default, the glitch filter is turned on. This pin is powered in deep power-down mode and can wake up the part. The wake-up pin function can be disabled and the pin can be used for other purposes, if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[9] Special analog pin.

[10] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[11] When the main oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

Table 4. Movable functions

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
$\overline{\text{U0_RTS}}$	O	Request To Send output for USART0.
$\overline{\text{U0_CTS}}$	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.

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Table 4. Movable functions *…continued*

Function name	Type	Description
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
$\overline{\text{U1_RTS}}$	O	Request To Send output for USART1.
$\overline{\text{U1_CTS}}$	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL0	I/O	Slave select 0 for SPI0.
SPI0_SSEL1	I/O	Slave select 1 for SPI0.
SPI0_SSEL2	I/O	Slave select 2 for SPI0.
SPI0_SSEL3	I/O	Slave select 3 for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL0	I/O	Slave select 0 for SPI1.
SPI1_SSEL1	I/O	Slave select 1 for SPI1.
CAN0_TD	O	CAN0 transmit.
CAN0_RD	I	CAN0 receive.
USB_VBUS	I	USB VBUS.
SCT0_OUT0	O	SCTimer0/PWM output 0.
SCT0_OUT1	O	SCTimer0/PWM output 1.
SCT0_OUT2	O	SCTimer0/PWM output 2.
SCT1_OUT0	O	SCTimer1/PWM output 0.
SCT1_OUT1	O	SCTimer1/PWM output 1.
SCT1_OUT2	O	SCTimer1/PWM output 2.
SCT2_OUT0	O	SCTimer2/PWM output 0.
SCT2_OUT1	O	SCTimer2/PWM output 1.
SCT2_OUT2	O	SCTimer2/PWM output 2.
SCT3_OUT0	O	SCTimer3/PWM output 0.
SCT3_OUT1	O	SCTimer3/PWM output 1.
SCT3_OUT2	O	SCTimer3/PWM output 2.
SCT_ABORT0	I	SCT abort 0.
SCT_ABORT1	I	SCT abort 1.
ADC0_PINTRIG0	I	ADC0 external pin trigger input 0.
ADC0_PINTRIG1	I	ADC0 external pin trigger input 1.
ADC1_PINTRIG0	I	ADC1 external pin trigger input 1.
ADC1_PINTRIG1	I	ADC1 external pin trigger input 1.

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Table 4. Movable functions *…continued*

Function name	Type	Description
DAC_PINTRIG	I	DAC external pin trigger input.
DAC_SHUTOFF	I	DAC shut-off external input.
ACMP0_O	O	Analog comparator 0 output.
ACMP1_O	O	Analog comparator 1 output.
ACMP2_O	O	Analog comparator 2 output.
ACMP3_O	O	Analog comparator 3 output.
CLKOUT	O	Clock output.
ROSC	O	Analog comparator ring oscillator output.
ROSC_RESET	I	Analog comparator ring oscillator reset.
USB_FTOGGLE	O	USB frame toggle. Do not assign this function to a pin until a USB device is connected and the first SOF interrupt has been received by the device.
QEI_PHA	I	QEI phase A input.
QEI_PHB	I	QEI phase B input.
QEI_IDX	I	QEI index input.
GPIO_INT_BMAT	O	Output of the pattern match engine.
SWO	O	Serial wire output.

Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO0_2/ADC0_6/SCT1_OUT3	3	6	8	SCT0 input multiplexer
PIO0_3/ADC0_5/SCT1_OUT4	4	7	10	SCT0 input multiplexer
PIO0_4/ADC0_4	5	8	13	SCT2 input multiplexer
PIO0_5/ADC0_3	6	9	14	FREQMEAS
PIO0_7/ADC0_1	8	11	17	SCT3 input multiplexer
PIO0_14/ADC1_7/SCT1_OUT5	22	30	45	SCTIPU input SAMPLE_IN_A0
PIO0_15/ADC1_8	23	31	47	SCT1 input multiplexer
PIO0_16/ADC1_9	24	32	49	SCT1 input multiplexer
PIO0_17/WAKEUP/$\overline{\text{TRST}}$	28	39	61	SCT0 input multiplexer
SWCLK/PIO0_19/TCK	29	40	63	FREQMEAS
$\overline{\text{RESET}}$/PIO0_21	34	45	71	SCT1 input multiplexer
PIO0_25/ACMP0_I4	44	60	93	SCTIPU input SAMPLE_IN_A1
PIO0_27/ACMP_I1	46	62	97	SCT2 input multiplexer
PIO0_30/ADC0_11	-	1	1	FREQMEAS
				SCT0 input multiplexer
PIO0_31/ADC0_9	-	3	3	SCT1 input multiplexer
PIO1_4/ADC1_10	-	33	51	SCT1 input multiplexer
PIO1_5/ADC1_11	-	34	52	SCT1 input multiplexer
PIO1_6/ACMP_I2	-	46	73	SCT0 input multiplexer

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Table 5. Pins connected to the INPUT multiplexer and SCT IPU

Symbol	LQFP48	LQFP64	LQFP100	Description
PIO1_7/ACMP3_I4	-	51	81	SCT0 input multiplexer
PIO1_11	-	38	58	SCT3 input multiplexer
				SCTIPU input SAMPLE_IN_A2
PIO1_12	-	-	9	SCT0 input multiplexer
PIO1_13	-	-	11	SCT0 input multiplexer
PIO1_15	-	-	12	SCT1 input multiplexer
PIO1_16	-	-	18	SCT1 input multiplexer
PIO1_18	-	-	25	SCT2 input multiplexer
PIO1_19	-	-	29	SCT2 input multiplexer
PIO1_21	-	-	37	SCT3 input multiplexer
PIO1_22	-	-	38	SCT3 input multiplexer
PIO1_26	-	-	48	SCTIPU input SAMPLE_IN_A3
PIO1_27	-	-	50	FREQMEAS

8. Functional description

8.1 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware division, hardware single-cycle multiply, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual*, which is available on the official ARM website.

8.2 Memory Protection Unit (MPU)

The LPC15xx have a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

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The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

8.3 On-chip flash programming memory

The LPC15xx contain up to 256 kB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software. Flash updates via USB are supported as well.

The flash memory is divided into 4 kB sectors with each sector consisting of 16 pages. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.3.1 ISP pin configuration

The LPC15xx supports ISP via the USART0, C_CAN, or USB interfaces. The ISP mode is determined by the state of two pins (ISP_0 and ISP_1) at boot time:

Table 6. ISP modes

Boot mode	ISP_0	ISP_1	Description
No ISP	HIGH	HIGH	ISP bypassed. Part attempts to boot from flash. If the user code in flash is not valid, then enters ISP via USB.
C_CAN	HIGH	LOW	Part enters ISP via C_CAN.
USB	LOW	HIGH	Part enters ISP via USB.
USART0	LOW	LOW	Part enters ISP via USART0.

The ISP pin assignment is different for each package, so that the fewest functions possible are blocked. No more than four pins must be set aside for entering ISP in any ISP mode. The boot code assigns two ISP pins for each package, which are probed when the part boots to determine whether or not to enter ISP mode. Once the ISP mode has been determined, the boot loader configures the necessary serial pins for each package.

Pins which are not configured by the boot loader for the selected boot mode (for example CAN0_RD and CAN0_TD in USART mode) can be assigned to any function through the switch matrix.

Table 7. Pin assignments for ISP modes

Boot pin	LQFP48	LQFP64	LQFP100
ISP_0	PIO0_4	PIO1_9	PIO2_5
ISP_1	PIO0_16	PIO1_11	PIO2_4
USART mode			
U0_TXD	PIO0_15	PIO0_18	PIO2_6
U0_RXD	PIO0_14	PIO0_13	PIO2_7
C_CAN mode			
CAN0_TD	PIO0_18	PIO0_31	PIO2_8
CAN0_RD	PIO0_13	PIO0_11	PIO2_9
USB mode			
USB_VBUS (same as ISP_1)	PIO0_16	PIO1_11	PIO2_4

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8.4 EEPROM

The LPC15xx contain 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip boot loader software.

8.5 SRAM

The LPC15xx contain a total 36 kB, 20 kB or 12 kB of contiguous, on-chip static RAM memory. For each SRAM configuration, the SRAM is divided into three blocks: 2 x 16 kB + 4 kB for 36 kB SRAM, 2 x 8 kB + 4 kB for 20 kB SRAM, and 2 x 4 kB + 4 kB for 12 kB SRAM. The bottom 16 kB, 8 kB, or 4 kB are enabled by the bootloader and cannot be disabled. The next two SRAM blocks in each configuration can be disabled or enabled individually in the SYSCON block to save power.

Table 8. LPC15xx SRAM configurations

	SRAM0	SRAM1	SRAM2
LPC1549/19 (total SRAM = 36 kB)			
address range	0x0200 0000 to 0x0200 3FFF	0x0200 4000 to 0x0200 7FFF	0x0200 8000 to 0x0200 8FFF
size	16 kB	16 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1548/18 (total SRAM = 20 kB)			
address range	0x0200 0000 to 0x0200 1FFF	0x0200 2000 to 0x0200 3FFF	0x0200 4000 to 0x0200 4FFF
size	8 kB	8 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled
LPC1547/17 (total SRAM = 12 kB)			
address range	0x0200 0000 to 0x0200 0FFF	0x0200 1000 to 0x0200 1FFF	0x0200 2000 to 0x0200 2FFF
size	4 kB	4 kB	4 kB
control	cannot be disabled	disable/enable	disable/enable
default	enabled	enabled	enabled

8.6 On-chip ROM

The on-chip ROM contains the boot loader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM.
- Flash updates via USB and C_CAN supported.
- USB API (HID, CDC, and MSC drivers).
- DMA, I2C, USART, SPI, and C_CAN drivers.
- Power profiles for configuring power consumption and PLL settings.

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- Power mode configuration for configuring deep-sleep, power-down, and deep power-down modes.
- ADC drivers for analog-to-digital conversion and ADC calibration.

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8.7 AHB multilayer matrix

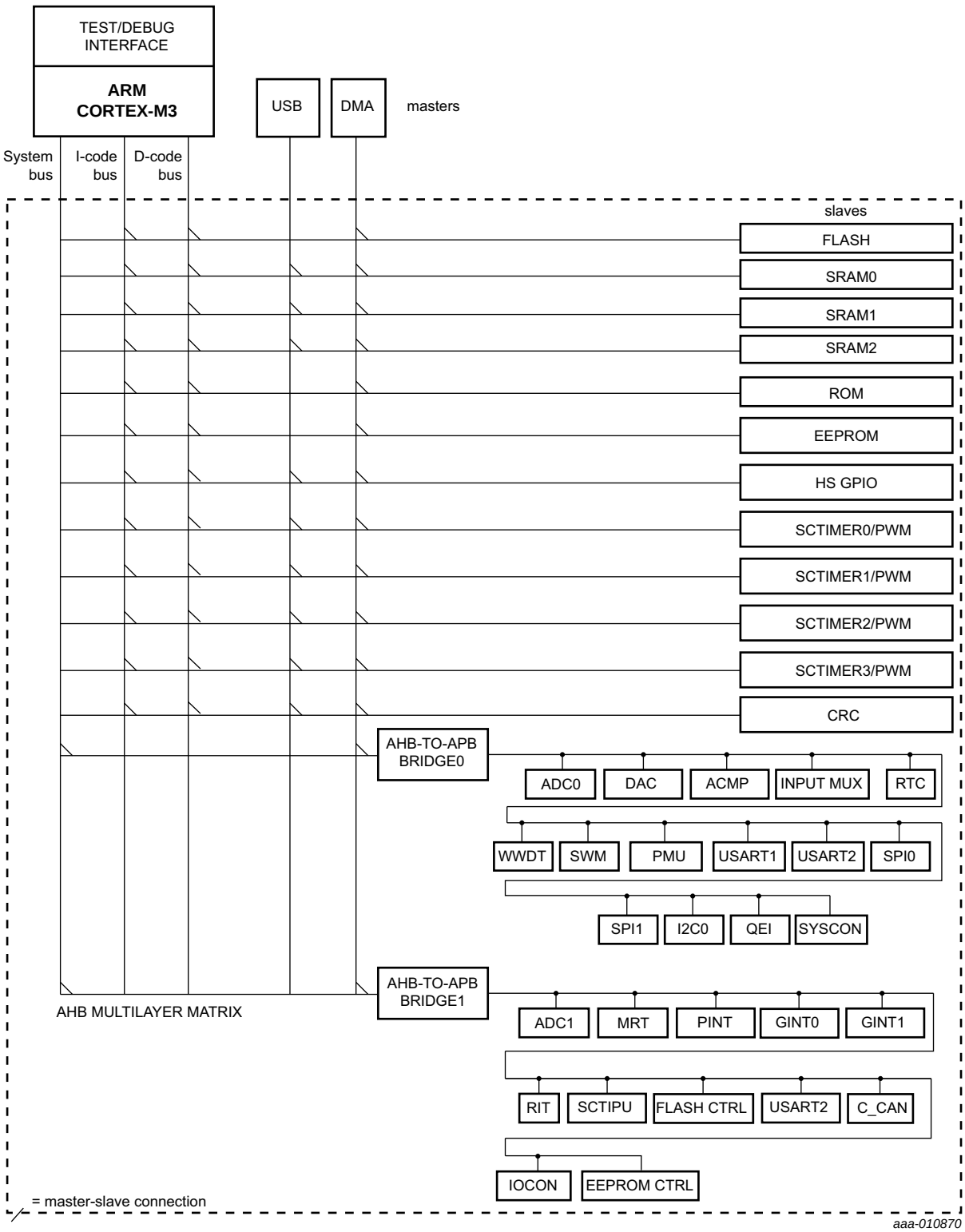

Fig 9. AHB multilayer matrix

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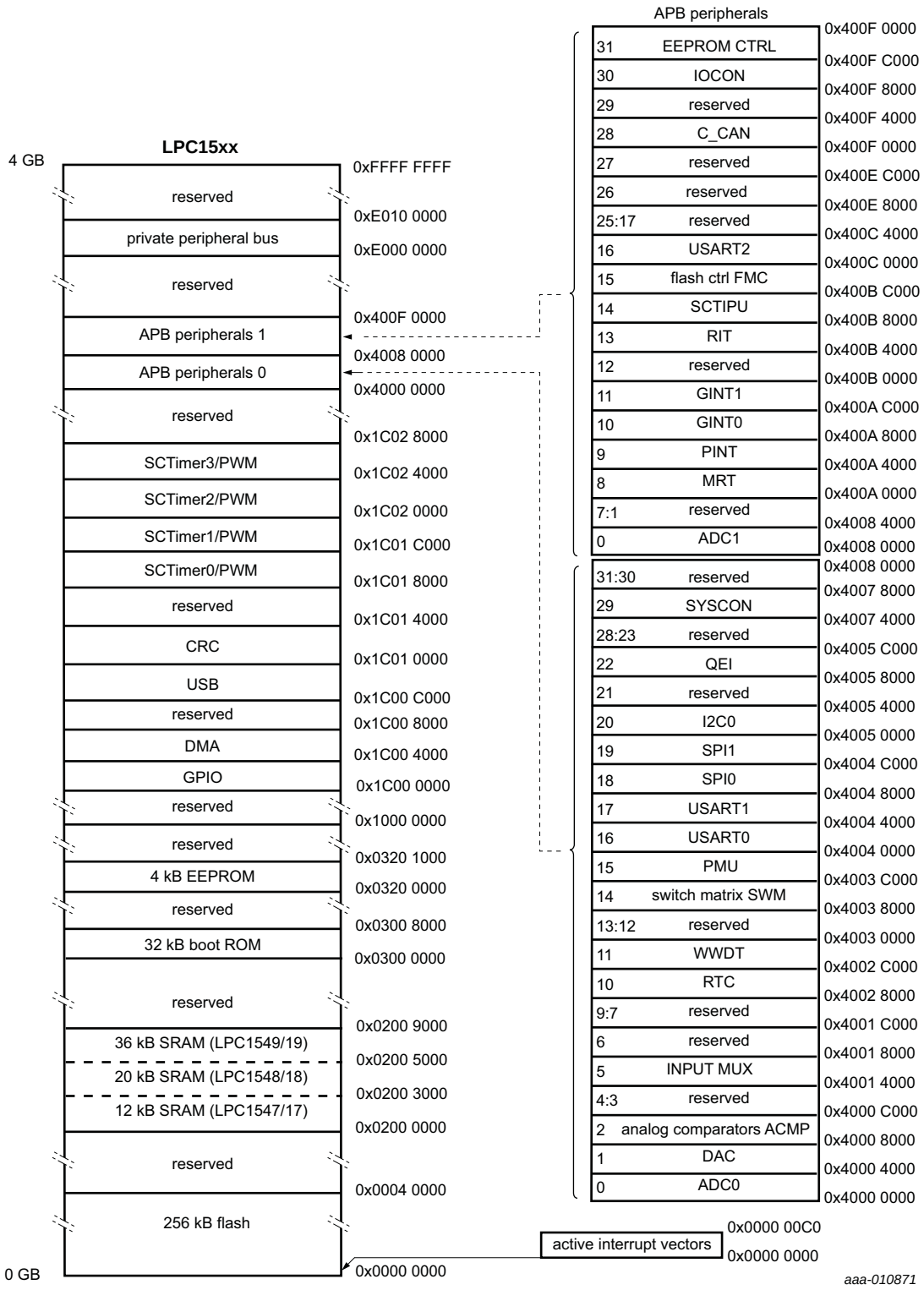
8.8 Memory map



See Section 8.5 “SRAM” for SRAM configuration.

Fig 10. Memory map

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8.9 Nested Vectored Interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.9.1 Features

- Nested Vectored Interrupt Controller that is an integral part of the ARM Cortex-M3.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- The NVIC supports 47 vectored interrupts.
- Eight programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCall and PendSV.
- Support for NMI.
- ARM Cortex-M3 Vector table offset register VTOR implemented.

8.9.2 Interrupt sources

Typically, each peripheral device has one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.10 IOCON block

The IOCON block configures the electrical properties of the pins such as pull-up and pull-down resistors, hysteresis, open-drain modes and input filters.

Remark: The pin function and whether the pin operates in digital or analog mode are entirely under the control of the switch matrix.

Enabling an analog function through the switch matrix disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.10.1 Features

- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_22 and PIO0_23) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on 36 pins (PIO0_0 to PIO0_17, PIO0_25 to PIO0_31, PIO1_0 to PIO1_10). The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.
- Digital filter with programmable filter constant on all pins.

8.10.2 Standard I/O pad configuration

Figure 11 shows the possible pin modes for standard I/O pins with analog input function:

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- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter configurable on all pins
- Digital input: Input glitch filter enabled/disabled on select pins
- Analog input

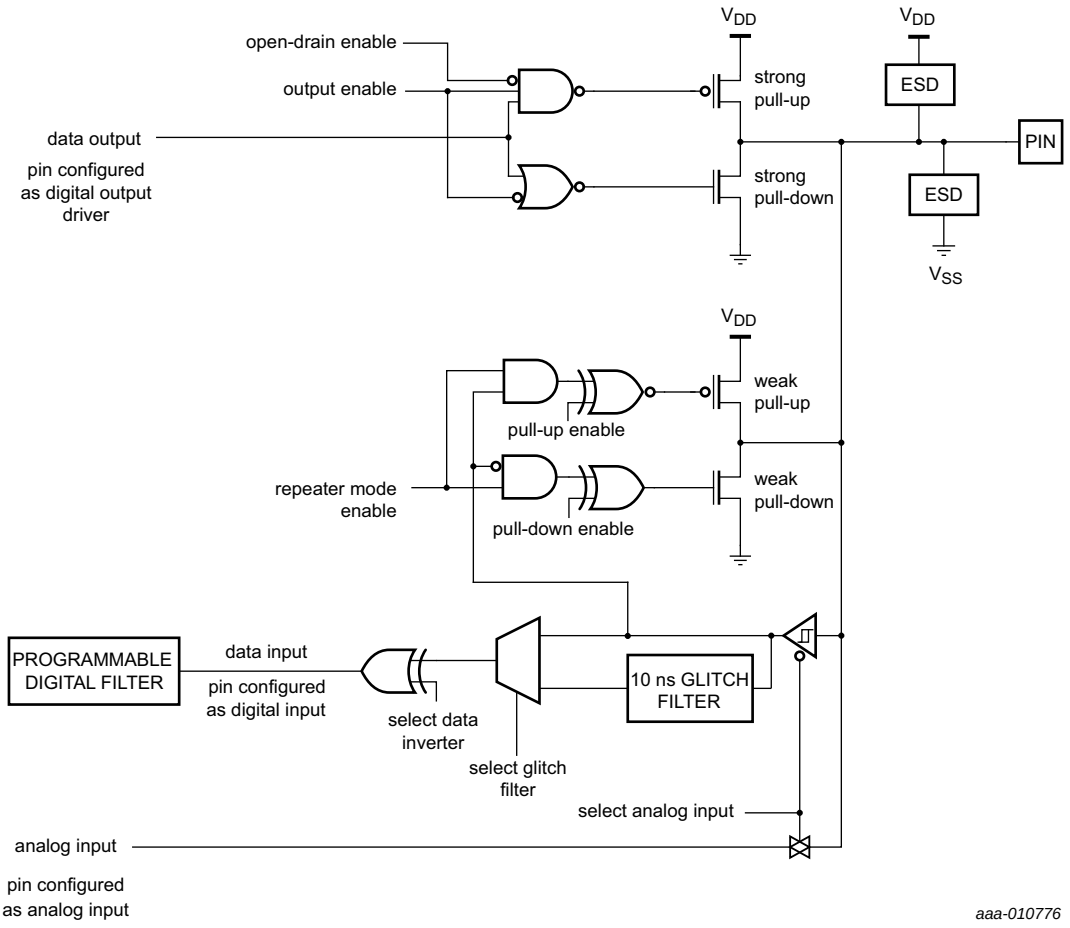

Fig 11. Standard I/O pin configuration

8.11 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 4.

Functions that need specialized pads like the ADC or analog comparator inputs can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 3. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

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8.12 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function through the switch matrix are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC15xx use accelerated GPIO functions.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.12.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.13 Pin interrupt/pattern match engine (PINT)

The pin interrupt block configures up to eight pins from the digital pins on ports 1 and 2 for providing eight external interrupts connected to the NVIC. The input multiplexer block is used to select the pins.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin on ports 0 and 1 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

8.13.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU.
  - The pattern match engine does not facilitate wake-up.

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8.14 GPIO group interrupts (GINT0/1)

The GPIO pins can be used in several ways to set pins as inputs or outputs and use the inputs as combinations of level and edge sensitive interrupts. For each port/pin connected to one of the two the GPIO Grouped Interrupt blocks (GINT0 and GINT1), the GPIO grouped interrupt registers determine which pins are enabled to generate interrupts and what the active polarities of each of those inputs are.

The GPIO grouped interrupt registers also select whether the interrupt output will be level or edge triggered and whether it will be based on the OR or the AND of all of the enabled inputs.

When the designated pattern is detected on the selected input pins, the GPIO grouped interrupt block generates an interrupt. If the part is in a power-savings mode, it first asynchronously wakes the part up prior to asserting the interrupt request. The interrupt request line can be cleared by writing a one to the interrupt status bit in the control register.

8.14.1 Features

- Two group interrupts are supported to reflect two distinct interrupt patterns.
- The inputs from any number of digital pins can be enabled to contribute to a combined group interrupt.
- The polarity of each input enabled for the group interrupt can be configured HIGH or LOW.
- Enabled interrupts can be logically combined through an OR or AND operation.
- The grouped interrupts can wake up the part from sleep, deep-sleep or power-down modes.

8.15 DMA controller

The DMA controller can access all memories and the USART, SPI, I2C, and DAC peripherals using DMA requests. DMA transfers can also be triggered by internal events like the ADC interrupts, the SCT DMA request signals, or the analog comparator outputs.

8.15.1 Features

- 18 channels with 14 channels connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events. Each DMA channel can select one trigger input from 24 sources through the input multiplexer.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

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8.16 Input multiplexing (Input mux)

The input multiplexer allows to select from multiple external and internal sources for the SCT inputs, DMA trigger inputs, and the frequency measure block. The input multiplexer is implemented as a register interface with one source selection register for each input. The input multiplexer can for example connect SCT outputs, the ADC interrupts, or the comparator outputs to the SCT inputs and thus enables the SCT to use a large variety of events to control the timing operation.

The ADCs and analog comparators also support input multiplexing using source selection registers as part of their configuration registers.

8.17 USB interface

Remark: The USB interface is available on parts LPC1549/48/47 only.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The USB interface consists of a full-speed device controller with on-chip PHY (PHYsical layer) for device functions.

Remark: Configure the part in default power mode with the power profiles before using the USB (see Section 8.40.1). Do not use the USB when the part runs in performance, efficiency, or low-power mode.

8.17.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

8.17.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints including one control endpoint.
- Single and double buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode and Power-down mode on USB activity and remote wake-up.
- Supports SoftConnect functionality through internal pull-up resistor.
- Internal 33 Ω series termination resistors on USB_DP and USB_DM lines eliminate the need for external series resistors.
- Supports Link Power Management (LPM).

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8.18 USART0/1/2

Remark: All USART functions are movable functions and are assigned to pins through the switch matrix. Do not connect USART functions to the open-drain pins PIO0_22 and PIO0_23.

Interrupts generated by the USART peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled.

8.18.1 Features

- Maximum bit rates of 4.5 Mbit/s in asynchronous mode, 15 Mbit/s in synchronous mode master mode, and 18 Mbit/s in synchronous slave mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

8.19 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix. Do not connect SPI functions to the open-drain pins PIO0_22 and PIO0_23.

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8.19.1 Features

- Maximum data rates of 17 Mbit/s in master mode and slave mode for SPI functions connected to all digital pins except PIO0_22 and PIO0_23.
- Data transmits of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- Up to four Slave Select input/outputs with selectable polarity and flexible usage.
- Supports DMA transfers: SPIn transmit and receive functions work with the system DMA controller.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.20 I2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are fixed-pin functions and must be enabled through the switch matrix on the open-drain pins PIO0_22 and PIO0_23.

8.20.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Fail-safe operation: When the power to an I^2C-bus device is switched off, the SDA and SCL pins connected to the I^2C-bus are floating and do not disturb the bus.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.

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8.21 C_CAN

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller can build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

The C_CAN functions are movable functions and are assigned to pins through the switch matrix. Do not connect C_CAN functions to the open-drain pins PIO0_22 and PIO0_23.

8.21.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

8.22 PWM/timer/motor control subsystem

The SCTimer/PWMs (State Configurable Timer/Pulse Width Modulators) and the analog peripherals support multiple ways of interconnecting their inputs and outputs and of interfacing to the pins and the DMA controller. Using the highly flexible and programmable connection scheme makes it easy to configure various subsystems for motor control and complex timing and tracking applications. Specifically, the inputs to the SCTs and the trigger inputs of the ADCs and DMA are selected through the input multiplexer which offers a choice of many possible sources for each input or trigger. SCT outputs are assigned to pins through the switch matrix allowing for many pinout solutions.

8.22.1 SCtimer/PWM subsystem

The SCTimer/PWMs can be configured to build a PWM controller with multiple outputs by programming the MATCH and MATCHRELOAD registers to control the base frequency and the duty cycle of each SCTimer/PWM output. More complex waveforms that span multiple counter cycles or change behavior across or within counter cycles can be generated using the state capability built into the SCTimer/PWMs.

Combining the PWM functions with the analog functions, the PWM output can react to control signals like comparator outputs or the ADC interrupts. The SCT IPU adds emergency shut-down functions and pre-processing of controlling events. For an overview of the PWM subsystem, see Figure 12 “PWM-Analog subsystem”.

For high-speed PWM functionality, use only outputs that are fixed-pin functions to minimize pin-to-pin differences in output skew. See also Table 22 “SCTimer/PWM output dynamic characteristics”. This reduces the number of PWM outputs to five for each large SCT.

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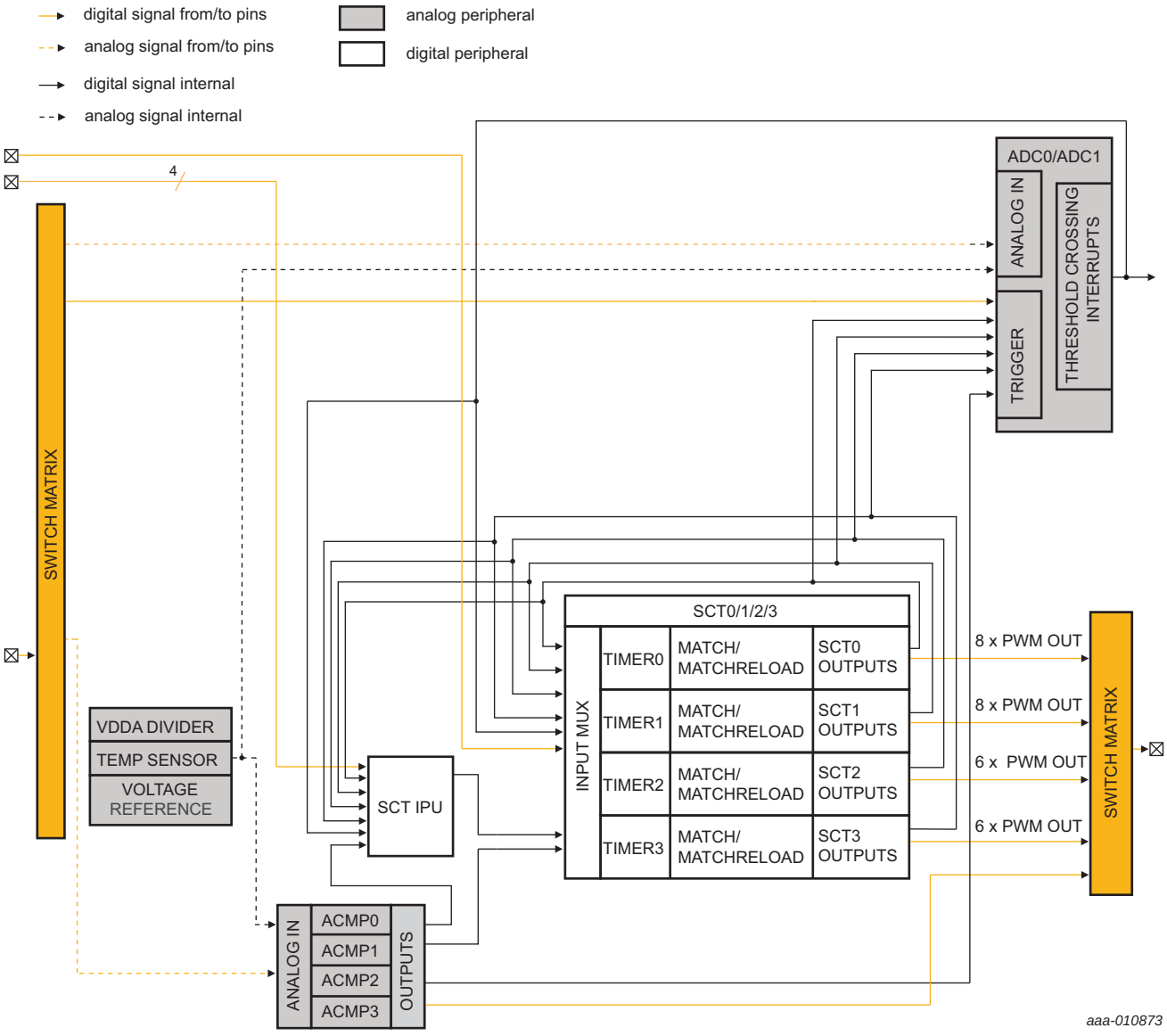

Fig 12. PWM-Analog subsystem

8.22.2 Timer controlled subsystem

The timers, the analog components, and the DMA can be configured to form a subsystem that can run independently of the main processor under the control of the SCTs and any events that are generated by the A/D converters, the comparators, the SCT output themselves, or the external pins. A/D conversions can be triggered by the timer outputs, the comparator outputs or by events from external pins. Data can be transferred from the ADCs to memory using the DMA controller, and the DMA transfers can be triggered by the ADCs, the comparator outputs, or by the timer outputs.

For an overview of the subsystem, see Figure 13 “Subsystem with timers, switch matrix, DMA, and analog components”.

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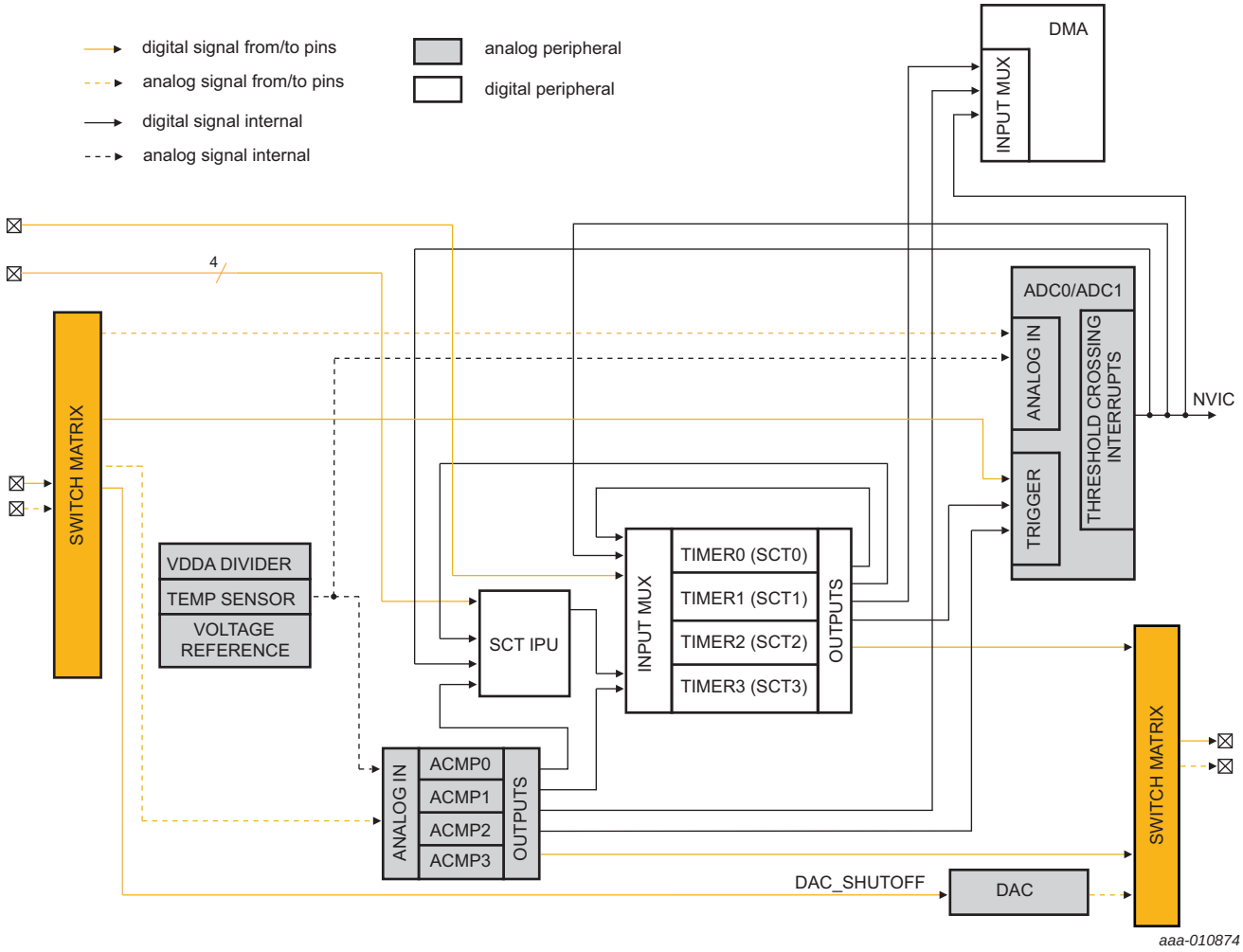

Fig 13. Subsystem with timers, switch matrix, DMA, and analog components

8.22.3 SCTimer/PWM in the large configuration (SCT0/1)

Remark: For applications that require exact timing of the SCT outputs (for example PWM), assign the outputs only to fixed-pin functions to ensure that the output skew is nearly the same for all outputs.

8.22.3.1 Features

The following feature list summarizes the configuration for the two large SCTs. Each large SCT has a companion small SCT (see Section 8.22.4) with fewer inputs and outputs and a reduced feature set.

- Each SCT supports:
  - 16 match/capture registers
  - 16 events
  - 16 states
  - Match register 0 to 5 support a fractional component for the dither engine

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- 8 inputs and 10 outputs
- DMA support

- Counter/timer features:
  - Configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to 16 match and capture registers total.
  - Upon match create the following events: stop, halt, limit counter or change counter direction; toggle outputs; create an interrupt; change the state.
  - Counter value can be loaded into capture register triggered by match or input/output toggle.
- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to eight single-edge or dual-edge controlled PWM outputs with up to eight independent duty cycles when configured as 32-bit timers.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition.
  - Events can only have an effect while the counter is running.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by the set of events that are allowed to happen in the state.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Dither engine.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer0/PWM and SCTimer1/PWM are configured as follows:

- 8 inputs
  - 7 inputs. Each input except input 7 can select one of 23 sources from an input multiplexer.
  - One input connected directly to the SCT PLL for a high-speed dedicated clock input.

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- 10 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Five outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCTIPU to sample or latch input events.
  - One output connected to the other large SCT
  - Four outputs connected to one small SCT
  - Two outputs connected to each ADC trigger input

8.22.4 State-Configurable Timers in the small configuration (SCT2/3)

Remark: For applications that require exact timing of the SCT outputs (for example PWM), assign the outputs only to fixed-pin functions to ensure that the output skew is nearly the same for all outputs.

8.22.4.1 Features

The following feature list summarizes the configuration for the two small SCTs. Each small SCT has a companion large SCT (see Section 8.22.3) with more inputs and outputs and a dither engine.

- Each SCT supports:
  - 8 match/capture registers
  - 10 events
  - 10 states
  - 3 inputs and 6 outputs
  - DMA support
- Counter/timer features:
  - Configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by bus clock or selected input.
  - Up counters or up-down counters.
  - Configurable number of match and capture registers. Up to 16 match and capture registers total.
  - Upon match create the following events: interrupt, stop, limit timer or change direction; toggle outputs; change state.
  - Counter value can be loaded into capture register triggered by match or input/output toggle.
- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge controlled PWM outputs with independent duty cycles if configured as 32-bit timers.
- Event creation features:

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- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Selected events can limit, halt, start, or stop a counter.
- Events control state changes, outputs, interrupts, and DMA requests.
- Match register 0 can be used as an automatic limit.
- In bi-directional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can take place in the state while the counter is running.
  - A state changes into another state as result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- Integrated with an input pre-processing unit (SCTIPU) to combine or delay input events.

Inputs and outputs on the SCTimer2/PWM and SCTimer3/PWM are configured as follows:

- 3 inputs. Each input selects one of 21 sources from a pin multiplexer.
- 6 outputs (some outputs are connected to multiple locations)
  - Three outputs connected to external pins through the switch matrix as movable functions.
  - Three outputs connected to external pins through the switch matrix as fixed-pin functions.
  - Two outputs connected to the SCT IPU to sample or latch input events.
  - Four outputs connected to the accompanying large SCT
  - Two outputs connected to each ADC trigger input

8.22.5 SCT Input processing unit (SCTIPU)

The SCTIPU allows to block or propagate signals to inputs of the SCT under the control of an SCT output. Using the SCTIPU in this way, allows signals to be blocked from entering the SCT inputs for a certain amount of time, for example while they are known to be invalid.

In addition, the SCTIPU can generate a common signal from several combined input sources that can be selected on all SCT inputs. Such a mechanism can be useful to create an abort signal that stops all timers.

8.22.5.1 Features

The SCTIPU pre-processes inputs to the State-Configurable Timers (SCT).

- Four outputs created from a selection of input transitions. Each output can be used as abort input to the SCTs or for any other application which requires a collection of multiple SCT inputs to trigger an identical SCT response.

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- Four registers to indicate which specific input sources caused the abort input to the SCTs.
- Four additional outputs which can be sampled at certain times and latched at others before being routed to SCT inputs.
- Nine abort inputs. Any combination of the abort inputs can trigger the dedicated abort input of each SCT.

8.23 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

8.23.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clock and direction).

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are internal connections to other on-chip peripherals such as the SCT and analog comparator outputs, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions.

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCT inputs for tight timing control between the ADC and the SCTs.

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8.24.1 Features

- 12-bit successive approximation analog-to-digital converter.
- 12-bit conversion rate of 2 MHz.
- Input multiplexing among 12 pins and up to 4 internal sources.
- Internal sources are the temperature sensor voltage, internal reference voltage, core voltage regulator output, and VDDA/2.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

8.25 Digital-to-Analog Converter (DAC)

The DAC supports a resolution of 12 bits. Conversions can be triggered by an external pin input or an internal timer.

The DAC includes an optional automatic hardware shut-off feature which forces the DAC output voltage to zero while a HIGH level on the external DAC_SHUTOFF pin is detected.

8.25.1 Features

- 12-bit digital-to-analog converter.
- Supports DMA.
- Internal timer or pin external trigger for staged, jitter-free DAC conversion sequencing.
- Automatic hardware shut-off triggered by an external pin.

8.26 Analog comparator (ACMP)

The LPC15xx include four analog comparators with seven selectable inputs each for each positive or negative input channel. Two analog inputs are common to all four comparators. Internal voltage inputs include a voltage ladder reference with selectable voltage supply source, the temperature sensor or the internal voltage reference.

The analog inputs to the comparators are fixed-pin functions and must be enabled through the switch matrix.

The outputs of each analog comparator are internally connected to the ADC trigger inputs and to the SCT inputs, so that the result of a voltage comparison can trigger a timer operation or an analog-to-digital conversion.

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8.26.1 Features

- Seven selectable inputs. Fully configurable on either the positive side or the negative input channel.
- 32-stage voltage ladder internal reference for selectable voltages on each comparator; configurable on either positive or negative comparator input.
- Voltage ladder source voltage is selectable from an external pin or the 3.3 V analog voltage supply.
- 0.9 V internal band gap reference voltage selectable as either positive or negative input on each comparator.
- Temperature sensor voltage selectable as either positive or negative input on each comparator.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Individual comparator outputs can be connected internally to the SCT and ADC trigger inputs or the external pins.
- Separate interrupt for each comparator.
- Pin filter included on each comparator output.
- Three propagation delay values are programmable to optimize between speed and power consumption.
- Relaxation oscillator circuitry output for a 555 style timer operation using comparator blocks 0 and 1.

8.27 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.28 Internal voltage reference

The internal voltage reference is an accurate 0.9 V and is the output of a low voltage band gap circuit. A typical value at T_{amb} = 25 °C is 0.905 V. The internal voltage reference can be used in the following applications:

- When the supply voltage V_{DD} is known accurately, the internal voltage reference can be used to reduce the offset error E_O of the ADC code output. The ADC error correction then increases the accuracy of temperature sensor voltage output measurements.

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- When the ADC is accurately calibrated, the internal voltage reference can be used to measure the power supply voltage. This requires calibration by recording the ADC code of the internal voltage reference at different power supply levels yielding a different ADC code value for each supply voltage level. In a particular application, the internal voltage reference can be measured and the actual power supply voltage can be determined from the stored calibration values. The calibration values can be stored in the EEPROM for easy access.

After power-up, the internal voltage reference must be allowed to settle to its stable value before it can be used as an ADC reference voltage input.

For an accurate measurement of the internal voltage reference by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

8.29 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.29.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

8.30 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

8.30.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WWDT is clocked by the dedicated watchdog oscillator (WDOsc) running at a fixed frequency.

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8.31 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

8.31.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.

8.32 System tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.33 Real-Time Clock (RTC)

The RTC resides in a separate, always-on voltage domain with battery back-up. The RTC uses an independent 32 kHz oscillator, also located in the always-on voltage domain.

8.33.1 Features

- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low power modes, including Deep power-down.

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8.34 Clock generation

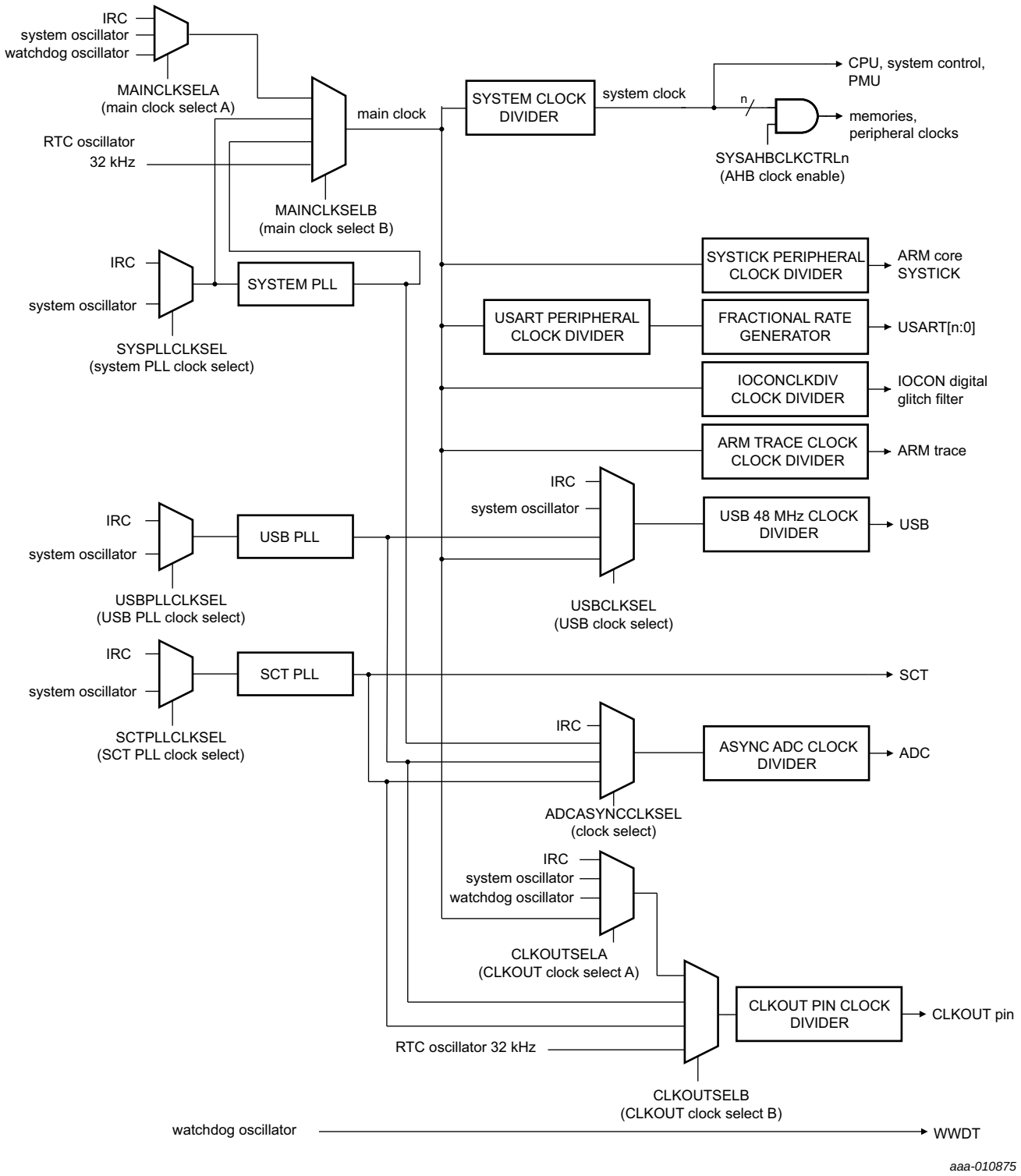

Fig 14. Clock generation

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8.35 Power domains

The LPC15xx provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup Registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is and V_{DD} >= VBAT + 0.3 V.

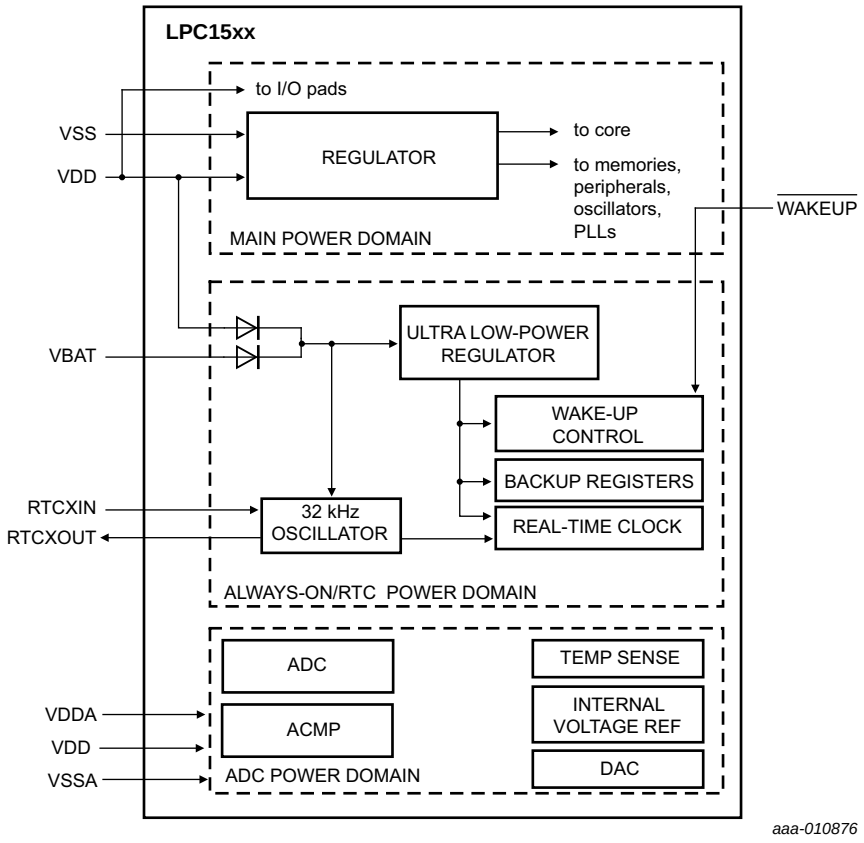

Fig 15. Power distribution

8.36 Integrated oscillators

The LPC15xx include the following independent oscillators: the system oscillator, the Internal RC oscillator (IRC), the watchdog oscillator, and the 32 kHz RTC oscillator. Each oscillator can be used for multiple purposes.

Following reset, the LPC15xx operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 14 for an overview of the LPC15xx clock generation.

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8.36.1 Internal RC oscillator

The IRC can be used as the clock that drives the system PLL and then the CPU. In addition, the IRC can be selected as input to various clock dividers and as the clock source for the USB PLL and the SCT PLL (see Figure 14). The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC15xx use the IRC as the clock source. Software can later switch to one of the other available clock sources.

8.36.2 System oscillator

The system oscillator can be used as a stable and accurate clock source for the CPU, with or without using the PLL. For USB applications, use the system oscillator to provide the clock source to USB PLL.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

The system oscillator has a wake-up time of approximately 500 µs.

8.36.3 Watchdog oscillator

The low-power watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is fixed at 503 kHz. The frequency spread over processing and temperature is ±40 %.

8.36.4 RTC oscillator

The low-power RTC oscillator provides a 1 Hz clock and a 1 kHz clock to the RTC and a 32 kHz clock output that can be used to obtain the main clock (see Figure 14).The 32 kHz oscillator output can be observed on the CLKOUT pin to allow trimming the RTC oscillator without interference from a probe.

8.37 System PLL, USB PLL, and SCT PLL

The LPC15xx contain a three identical PLLs for generating the system clock, the 48 MHz USB clock, and an asynchronous clock for the ADCs and SCTs. The system PLL is used to create the main clock. The SCT and USB PLLs create dedicated clocks for the asynchronous ADC, the asynchronous SCT clock input, and the USB.

Remark: The USB PLL is available on parts LPC1549/48/47 only.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

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8.38 Clock output

The LPC15xx feature a clock output function that routes the internal oscillator outputs, the PLL outputs, or the main clock an output pin where they can be observed directly.

8.39 Wake-up process

The LPC15xx begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the system oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and system oscillator as a clock source.

8.40 Power control

The LPC15xx support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides additional power control.

8.40.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC15xx for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock and to easily set the configuration options for Deep-sleep and power-down modes.

Remark: When using the USB, configure the LPC15xx in Default mode.

8.40.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

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8.40.3 Deep-sleep mode

In Deep-sleep mode, the LPC15xx is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC15xx can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, an interrupt generating USB port activity, an RTC interrupt, or any interrupts that the USART, SPI, or I2C interfaces can create in Deep-sleep mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Deep-sleep mode saves power and allows for short wake-up times.

8.40.4 Power-down mode

In Power-down mode, the LPC15xx is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

The LPC15xx can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, an interrupt generating USB port activity, an RTC interrupt, or any interrupts that the USART, SPI, or I2C interfaces can create in Power-down mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.40.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the always-on RTC power-domain. The LPC15xx can wake up from Deep power-down mode via the WAKEUP pin or a wake-up signal generated by the RTC interrupt.

The LPC15xx can be blocked from entering Deep power-down mode by setting a lock bit in the PMU block. Blocking the Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the WAKEUP pin is used in the application, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH while the part is in deep power-down mode. Pulling the WAKEUP pin LOW wakes up the part from deep power-down mode. In addition, pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

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8.41 System control

8.41.1 Reset

Reset has four sources on the LPC15xx: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

The $\overline{\text{RESET}}$ pin is operational in active, sleep, deep-sleep, and power-down modes if the $\overline{\text{RESET}}$ function is selected through the switch matrix for pin PIO0_21 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and thereby wakes up the part to its active state. The $\overline{\text{RESET}}$ pin is not functional in Deep power-down mode and must be pulled HIGH externally while the part is in Deep power-down mode.

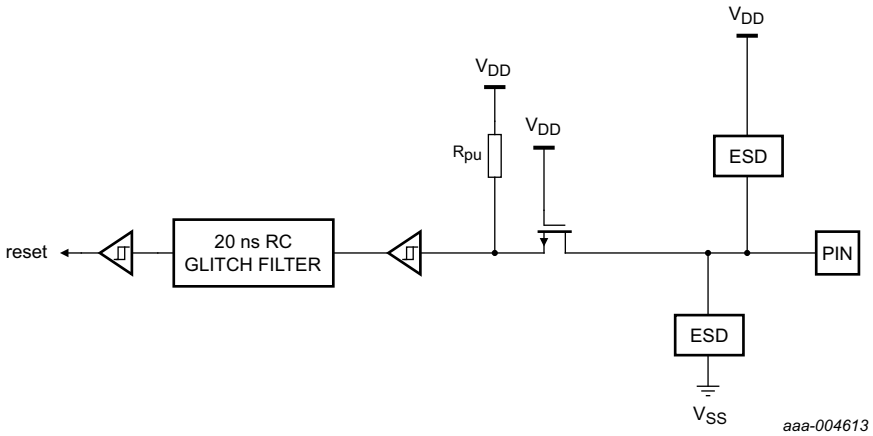

Fig 16. $\overline{\text{RESET}}$ pin configuration

8.41.2 Brownout detection

The LPC15xx includes brown-out detection (BOD) with two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of two selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.41.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

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In addition, ISP entry the external pins can be disabled without enabling CRP. For details, see the LPC15xx *user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using ISP pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP pins for valid user code can be disabled. For details, see the LPC15xx *user manual*.

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8.42 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M3 is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC15xx is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage (3.3 V)	[2]	–0.5	V_{DDA}	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	–0.5	V_{DDA}	V
		on pin VREFP_ADC	–0.5	V_{DDA}	V
V_{BAT}	battery supply voltage		–0.5	+4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present [3][4]	–0.5	+5.5	V
		on I2C open-drain pins PIO0_22, PIO0_23 [5]	–0.5	+5.5	V
		3 V tolerant I/O pin without over-voltage protection. Applies to PIO0_12. [6]	–0.5	V_{DDA}	V
		USB_DM, USB_DP pins	–0.5	V_{DD} + 0.5	V
V_{IA}	analog input voltage	[7][8][9]	–0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage	[2]	–0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	[2]	–0.5	+4.6	V
I_{DD}	supply current	per supply pin	-	100	mA
I_{SS}	ground current	per ground pin	-	100	mA

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Table 9. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C	-	100	mA
T_{stg}	storage temperature	[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins [11]	-	5	kV

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 11) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_22 and PIO0_23 and except the 3 V tolerant pin PIO0_12.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

[6] Applies to 3 V tolerant pin PIO0_12.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

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Table 10. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP48				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	64	°C/W
		1 m/s	55	°C/W
		2.5 m/s	50	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	96	°C/W
		1 m/s	76	°C/W
		2.5 m/s	67	°C/W
θjc	thermal resistance junction-to-case		13	°C/W
θjb	thermal resistance junction-to-board		16	°C/W
LQFP64				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	51	°C/W
		1 m/s	45	°C/W
		2.5 m/s	41	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	75	°C/W
		1 m/s	60	°C/W
		2.5 m/s	54	°C/W
θjc	thermal resistance junction-to-case		13	°C/W
θjb	thermal resistance junction-to-board		17	°C/W
LQFP100				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	42	°C/W
		1 m/s	37	°C/W
		2.5 m/s	34	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	59	°C/W
		1 m/s	48	°C/W
		2.5 m/s	44	°C/W
θjc	thermal resistance junction-to-case		12	°C/W
θjb	thermal resistance junction-to-board		17	°C/W

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The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

11. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)	[2]	2.4	3.3	V_{DDA}	V
V_{DDA}	analog supply voltage		2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP_DAC_VDDCMP	2.4	-	V_{DDA}	V
		on pin VREFP_ADC	-	-	V_{DDA}	V
V_{BAT}	battery supply voltage		2.4	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	4.3	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.7	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	19.3	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][7][8][10]	-	18	-	mA
		Sleep mode;				
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	2.1	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V [3][4][5][7][8]	-	1.5	-	mA
		system clock = 72 MHz; default mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	8.0	-	mA
		system clock = 72 MHz; low-current mode; V_{DD} = 3.3 V [3][4][10][7][8]	-	7.3	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; [3][4][11]	-			
		T_{amb} = 25 °C		310	380	µA
		T_{amb} = 105 °C	-	-	620	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V [3][4][11]	-			
		T_{amb} = 25 °C		3.8	15	µA
		T_{amb} = 105 °C	-	-	163	µA

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Table 11. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; VBAT = 0 or VBAT = 3.0 V [3][12][13]				
		RTC oscillator running				
		T_{amb} = 25 °C	-	1.1	1.3[14]	µA
		T_{amb} = 105 °C	-	-	15	µA
		RTC oscillator input grounded; T_{amb} = 25 °C [3][12]	-	560	-	nA
I_{BAT}	battery supply current	Deep power-down mode; V_{DD} = V_{DDA} = 3.3 V; VBAT = 3.0 V [13]		0	-	nA
		V_{DD} and V_{DDA} tied to ground; VBAT = 3.0 V [13]		1	-	µA
Standard port pins configured as digital pins, RESET; see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq$ 2.4 V; 5 V tolerant pins except PIO0_12 [16][18]	0	-	5	V
		$V_{DD} \geq$ 2.4 V; on 3 V tolerant pin PIO0_12	0	-	V_{DDA}	
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V	4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [19]	-	-	-45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD} [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V;	−10	−50	−85	µA
		V_{DD} < V_I < 5 V	0	0	0	µA

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Table 11. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
High-drive output pin configured as digital pin (PIO0_24); see Figure 17						
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled	-	0.5	10[14]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10[14]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10[14]	nA
V_I	input voltage	$V_{DD} \geq 2.4$ V [16] [18]	0	-	5.0	V
		V_{DD} = 0 V	0	-	3.6	V
V_O	output voltage	output active	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage	2.4 V <= V_{DD} < 3.0 V	0.30	-	-	V
		3.0 V <= V_{DD} <= 3.6 V	0.35	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.7 V <= V_{DD} < 3.6 V	$V_{DD} - 0.4$	-	-	V
		I_{OH} = 12 mA; 2.4 V <= V_{DD} < 2.7 V	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		$V_{OH} = V_{DD} - 0.4$ V; 2.4 V <= V_{DD} < 2.7 V	12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	4	-	-	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$ [19]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [20]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V [20]	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V	0	0	0	µA
I^2C-bus pins (PIO0_22 and PIO0_23); see Figure 17						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage		-	$0.05V_{DD}$	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins	3.5	-	-	mA

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Table 11. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.7 V <= V_{DD} < 3.6 V	20	-	-	mA
		V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.4 V <= V_{DD} < 2.7 V	16	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD} [21]	-	2	4	µA
		V_I = 5 V	-	10	22	µA
USB_DM and USB_DP pins						
V_I	input voltage	[2]	0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage		1.8	-	-	V
V_{IL}	LOW-level input voltage		-	-	1.0	V
V_{hys}	hysteresis voltage		0.32	-	-	V
Z_{out}	output impedance		28	-	44	Ω
V_{OH}	HIGH-level output voltage		2.9	-	-	V
V_{OL}	LOW-level output voltage		-	-	0.18	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.3 V [22]	4.8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.3 V [22]	5.0	-	-	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; pad connected to ground	-	-	125	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; pad connected to ground	-	-	125	mA
Oscillator pins						
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN	−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT	−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN [23]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT [23]	−0.5	-	3.6	V
Pin capacitance						
C_{io}	input/output capacitance	pins with analog and digital functions [24]	-	-	7.1	pF
		I^2C-bus pins (PIO0_22 and PIO0_23) [24]	-	-	2.5	pF
		pins with digital functions only [24]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] For USB operation: 3.0 V ≤ V_{DD} ≤ 3.6 V.

[3] T_{amb} = 25 °C.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

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[5] IRC enabled; system oscillator disabled; system PLL disabled.

[6] System oscillator enabled; IRC disabled; system PLL disabled.

[7] BOD disabled.

[8] All peripherals disabled in the SYSAHBCLKCTRL0/1 registers. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[9] IRC enabled; system oscillator disabled; system PLL enabled.

[10] IRC disabled; system oscillator enabled; system PLL enabled.

[11] All oscillators and analog blocks turned off: Use API power_mode_configure() with mode parameter set to DEEP_SLEEP or POWER_DOWN and peripheral parameter set to 0xFF.

[12] WAKEUP pin pulled HIGH externally.

[13] RTC running or not running.

[14] Characterized on samples. Not tested in production.

[15] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[16] Including voltage on outputs in tri-state mode.

[17] V_{DD} supply voltage must be present.

[18] Tri-state outputs go into tri-state mode in Deep power-down mode.

[19] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[20] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 17.

[21] To V_{SS}.

[22] The parameter values specified are simulated and absolute values.

[23] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)}$ < max(VBAT, V_{DD}).

[24] Including bonding pad capacitance.

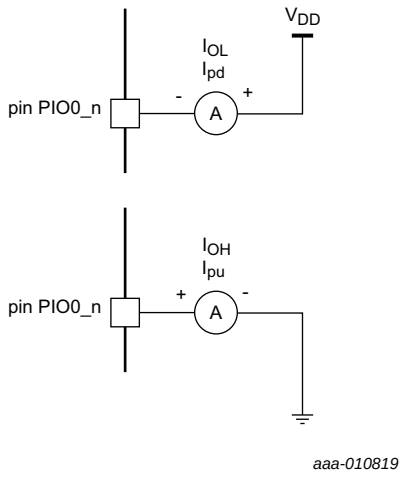

Fig 17. Pin input/output current measurement

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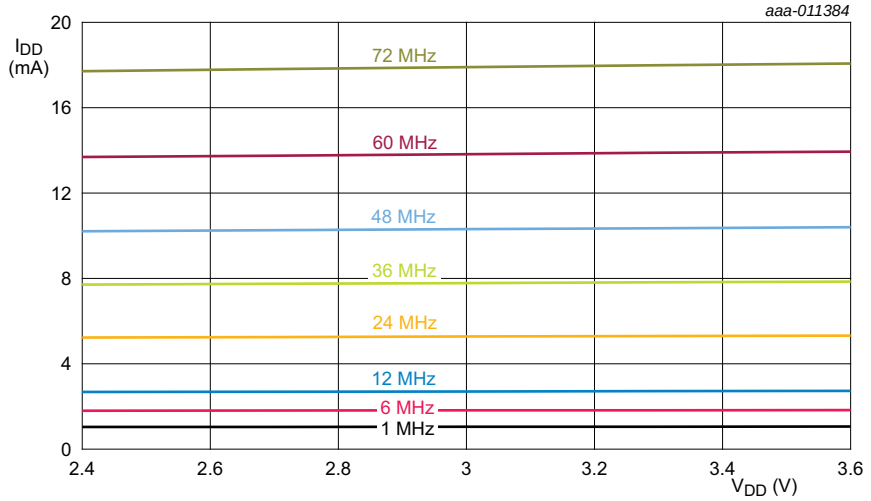
11.1 Power consumption

Power measurements in Active, Sleep, Deep-sleep, and Power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 18. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}

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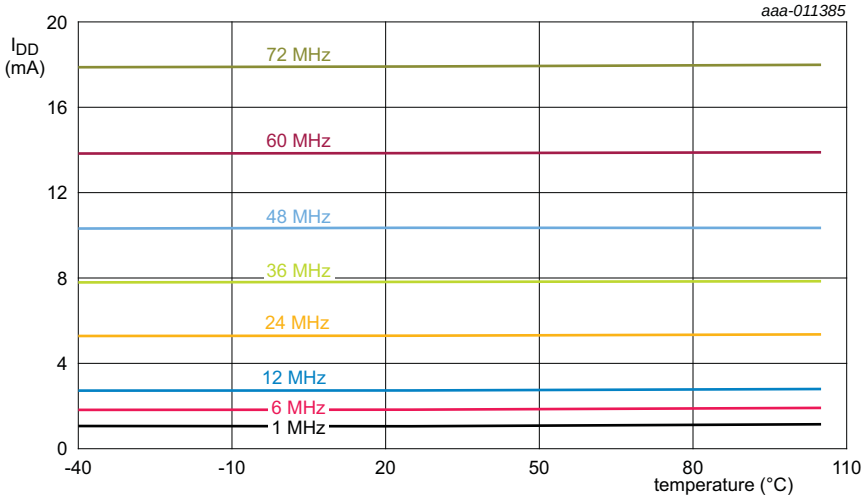


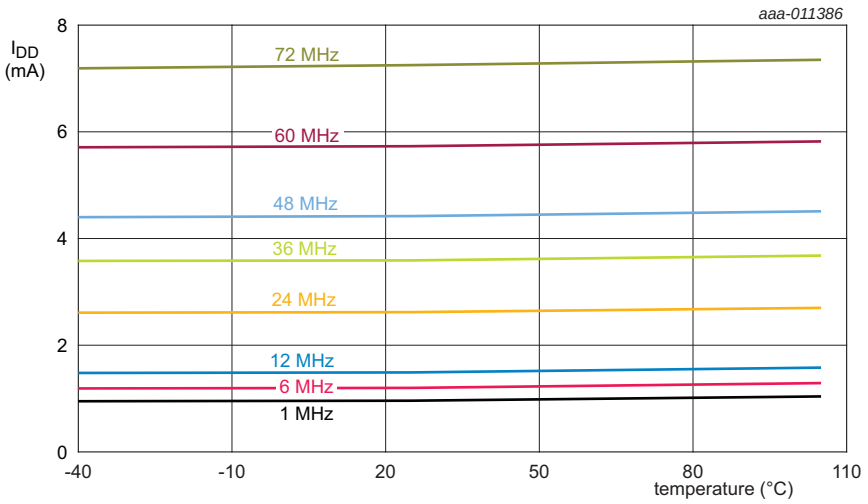
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 19. Active mode: Typical supply current I_{DD} versus temperature



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL0/1 registers; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 72 MHz: IRC enabled; PLL enabled.

Fig 20. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

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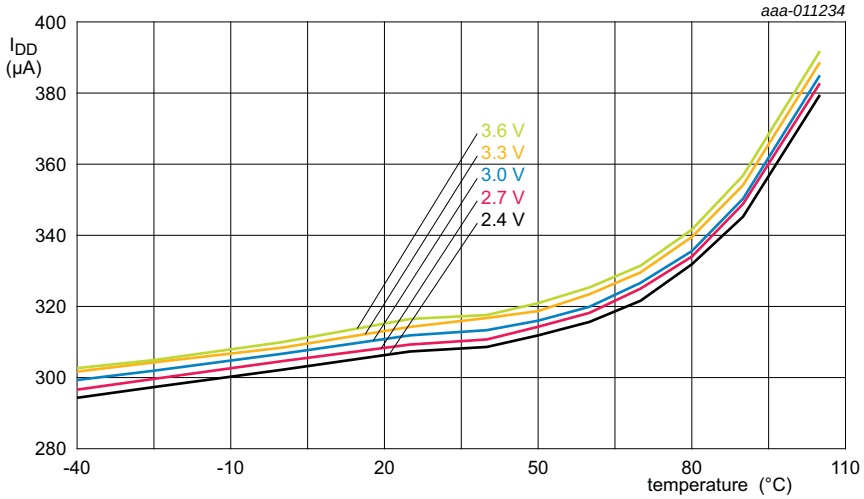
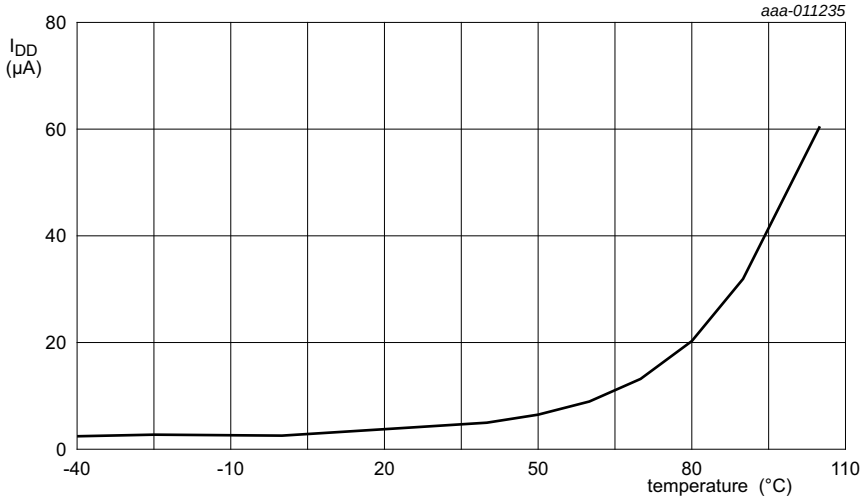


Conditions: BOD disabled; all oscillators and analog blocks disabled. Use API power_mode_configure() with mode parameter set to DEEP_SLEEP and peripheral parameter set to 0xFF.

Fig 21. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V. Use API power_mode_configure() with mode parameter set to POWER_DOWN and peripheral parameter set to 0xFF.

Fig 22. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

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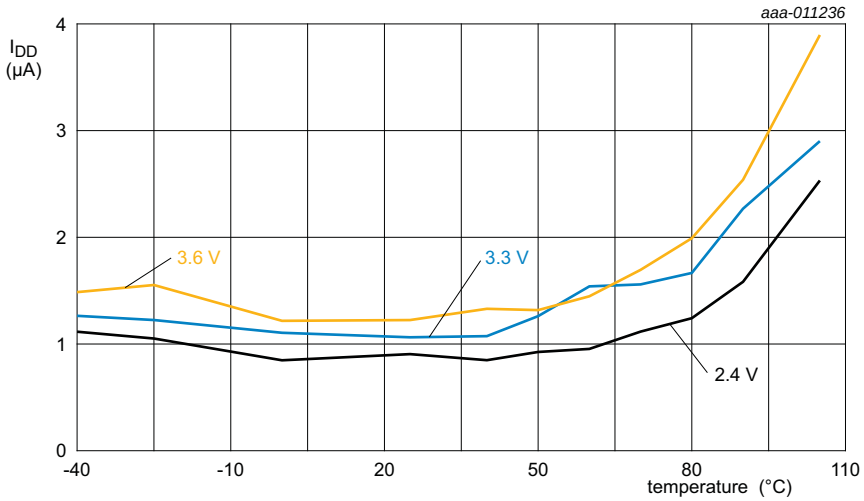
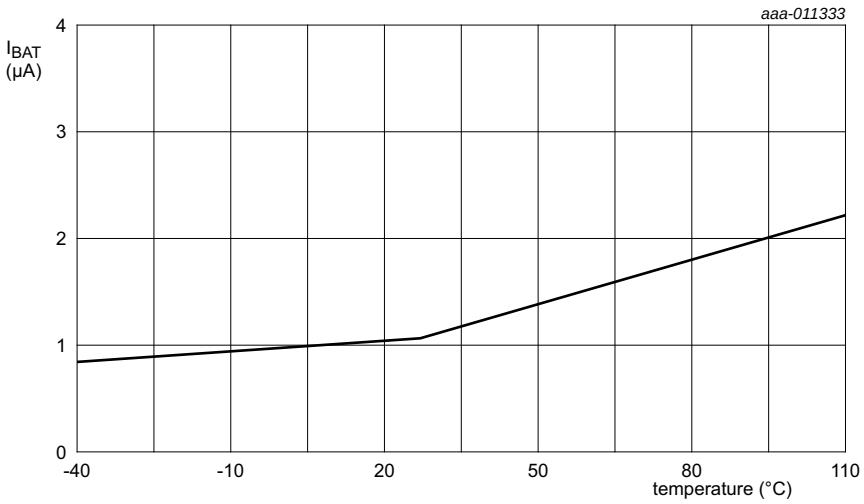


VBAT = 0 V.

Fig 23. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



VBAT = 3.3 V; V_{DD} floating.

Fig 24. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

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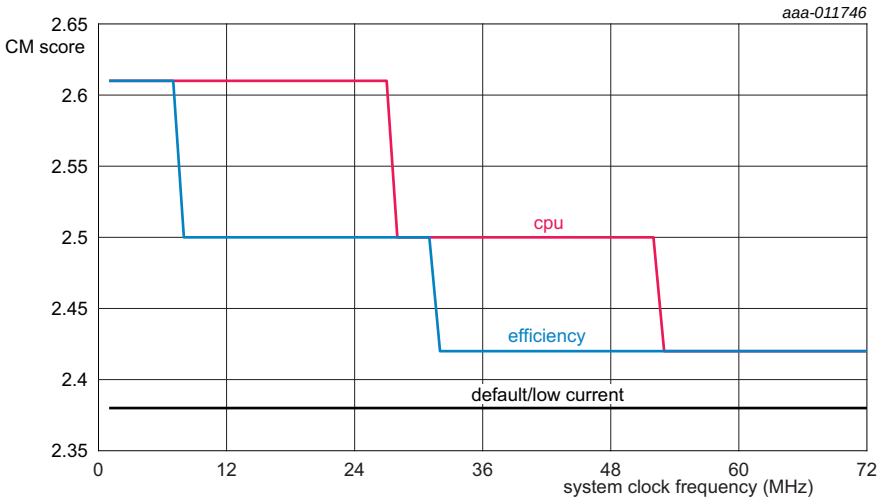
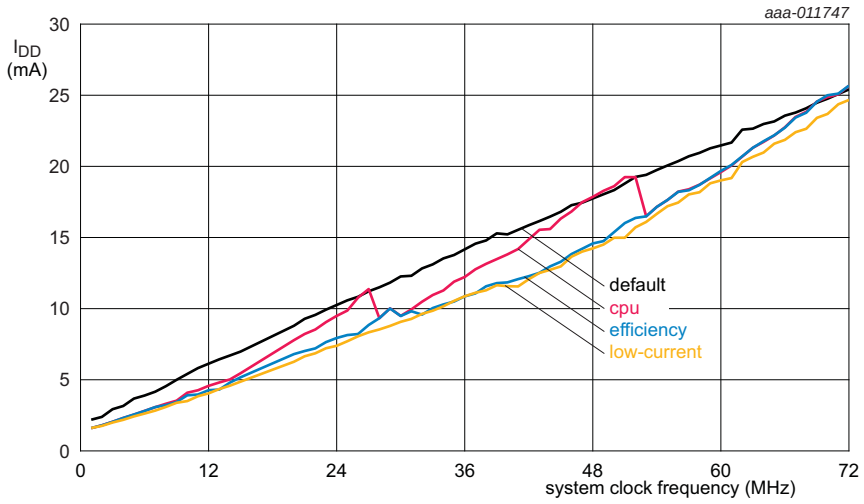
11.2 CoreMark data



Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL0/1 register; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.73.0.0, C compiler v.5.03.0.76.

Fig 25. CoreMark score



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals except one UART and the SCT disabled in the SYSAHBCLKCTRL0/1 registers; system clock derived from the IRC; system oscillator disabled; internal pull-up resistors enabled; BOD disabled. Measured with Keil uVision v.4.73.0.0, C compiler v.5.03.0.76.

Fig 26. Active mode: CoreMark power consumption I_{DD}

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11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 72 MHz.

Table 12. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
IRC	0.008	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.220	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator	0.002	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.045	-	-	Independent of main clock frequency.
Main PLL	-	0.085	-	-
USB PLL		0.100		
SCT PLL		0.110		
CLKOUT	-	0.005	0.01	Main clock divided by 4 in the CLKOUTDIV register.
ROM	-	0.015	0.02	-
GPIO + pin interrupt/pattern match	-	0.55	0.60	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	0.04	0.29	-
INPUT MUX		0.05	0.30	
IOCON	-	0.06	0.40	-
SCTimer0/PWM	-	0.18	1.10	-
SCTimer1/PWM	-	0.19	1.10	-
SCTimer2/PWM	-	0.13	0.70	-
SCTimer3/PWM	-	0.16	0.90	-
SCT IPU		0.02	0.1	
RTC	-	0.01	0.05	-
MRT	-	0.03	0.10	-
WWDT	-	0.01	0.10	Main clock selected as clock source for the WDT.
RIT		0.07	0.20	
QEI		0.12	0.80	
I2C0	-	0.02	0.12	-
SPI0	-	0.03	0.3	-
SPI1	-	0.01	0.28	-

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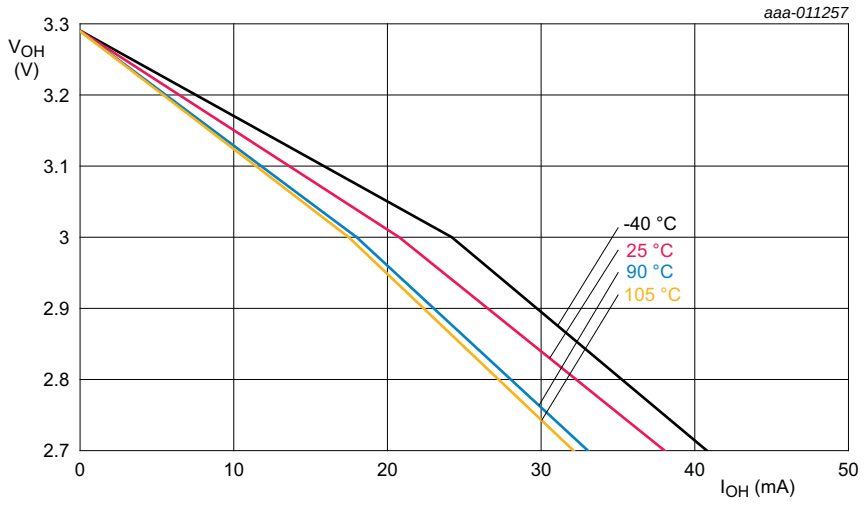
Table 12. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	72 MHz	
USART0	-	0.02	0.15	-
USART1	-	0.02	0.16	-
USART2	-	0.02	0.15	-
C_CAN	-	0.50	3.00	
USB	-	0.10	0.50	
Comparator ACMP0/1/2/3	-	0.01	0.03	-
ADC0	-	0.05	0.33	-
ADC1	-	0.04	0.33	-
temperature sensor	-	0.03	0.03	
internal voltage reference/band gap	-	0.03	0.04	
DAC	-	0.02	0.09	-
DMA	-	0.36	1.5	
CRC	-	0.01	0.08	-

11.4 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_24.

Fig 27. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}

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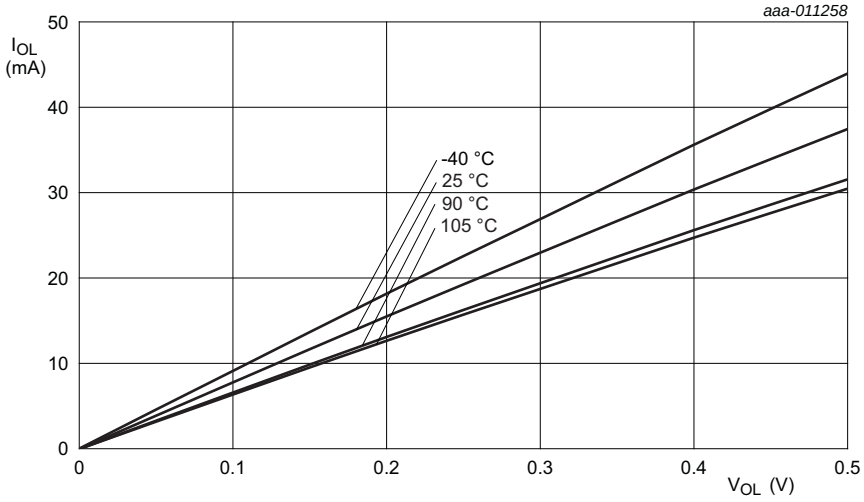
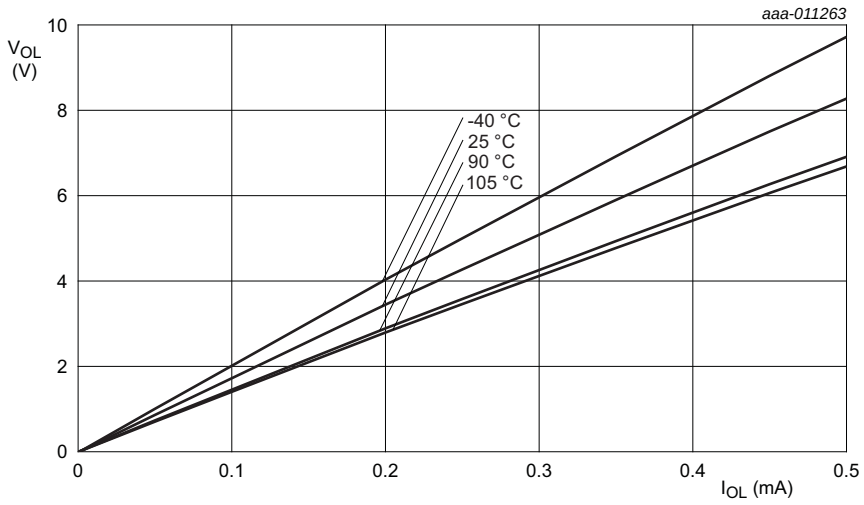


Conditions: V_{DD} = 3.3 V; on pins PIO0_22 and PIO0_23.

Fig 28. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_24.

Fig 29. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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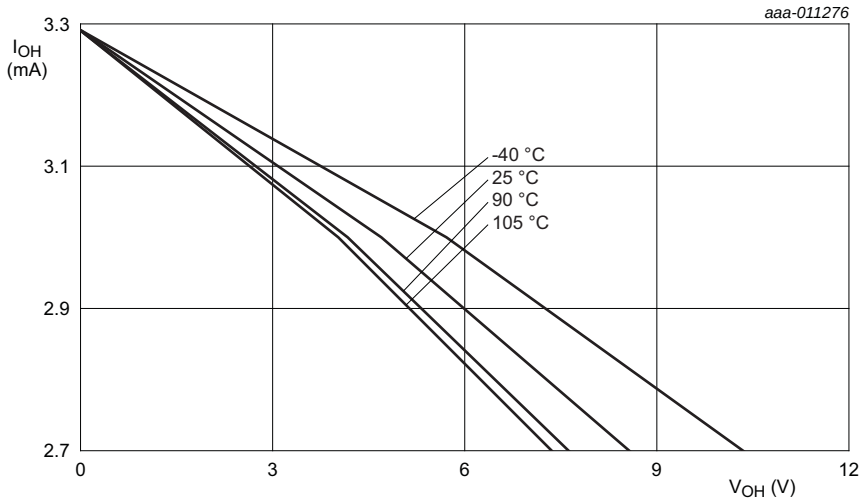
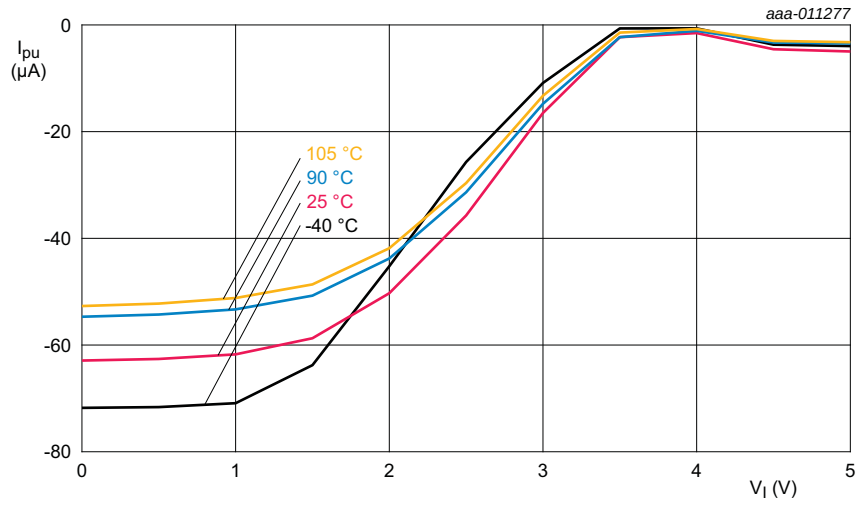


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 30. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 31. Typical pull-up current I_{pu} versus input voltage V_I

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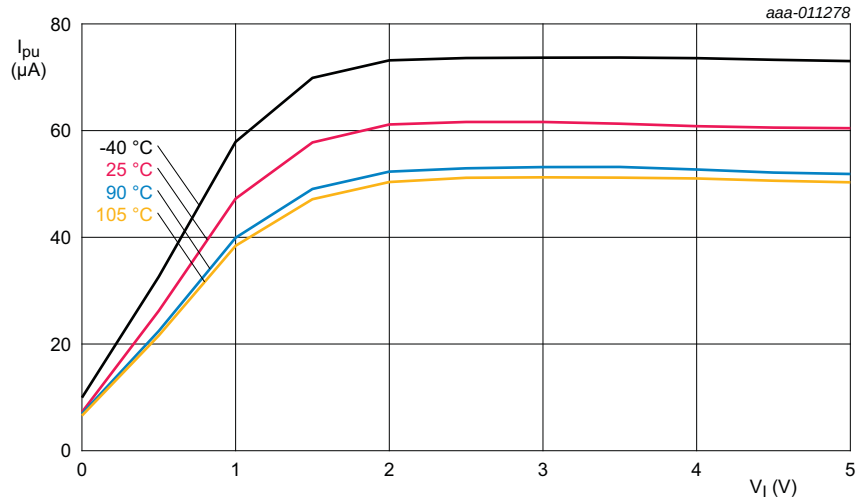

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 32. Typical pull-down current I_{pd} versus input voltage V_I

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12. Dynamic characteristics

12.1 Flash/EEPROM memory

Table 13. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered	10	20	-	years
		not powered	20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors	95	100	105	ms
t_{prog}	programming time	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC15xx user manual*).

Table 14. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		100000	1000000	-	cycles
t_{ret}	retention time	powered	100	200	-	years
		not powered	150	300	-	years
t_{prog}	programming time	64 bytes	-	2.9	-	ms

12.2 External clock for the oscillator in slave mode

Remark: The input voltage on the XTALIN and XTALOUT pins must be ≤ 1.95 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 14.3.

Table 15. Dynamic characteristic: external clock (XTALIN input)

T_{amb} = −40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

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[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

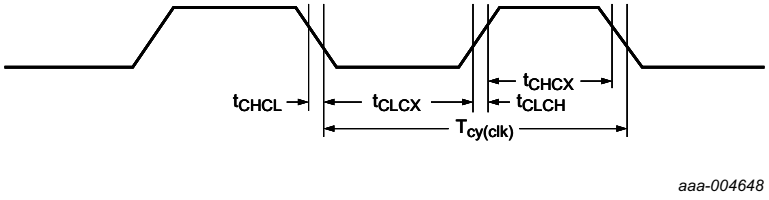


Fig 33. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

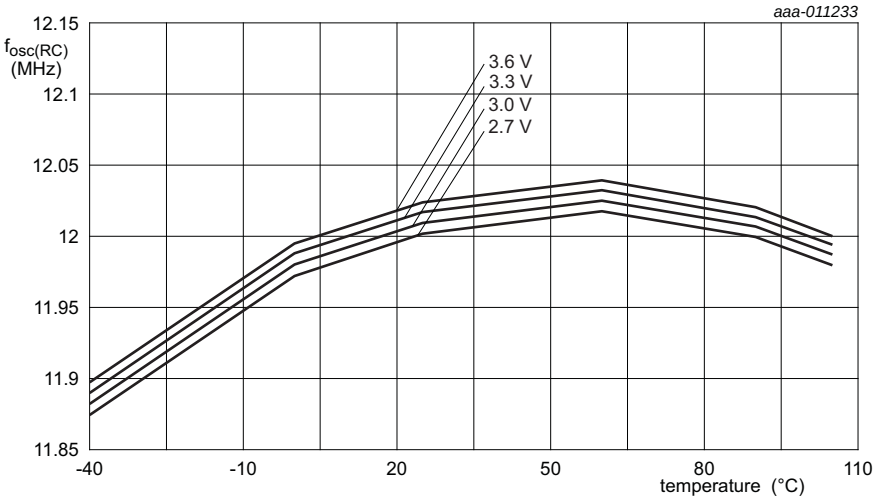
Table 16. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1%	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2%	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 34. Typical Internal RC oscillator frequency versus temperature

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Table 17. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	- [2]	-	503	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

12.4 I/O pins

Table 18. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0	1	MHz
t_f	fall time [4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
		Fast-mode	20 + 0.1 × C_b	300	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	µs
		Fast-mode	1.3	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	µs
		Fast-mode	0.6	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0.26	-	µs
$t_{HD;DAT}$	data hold time [3][4][8]	Standard-mode	0	-	µs
		Fast-mode	0	-	µs
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	0	-	µs

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Table 19. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{SU;DAT}$	data set-up time [9][10]	Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_22 and PIO0_23	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

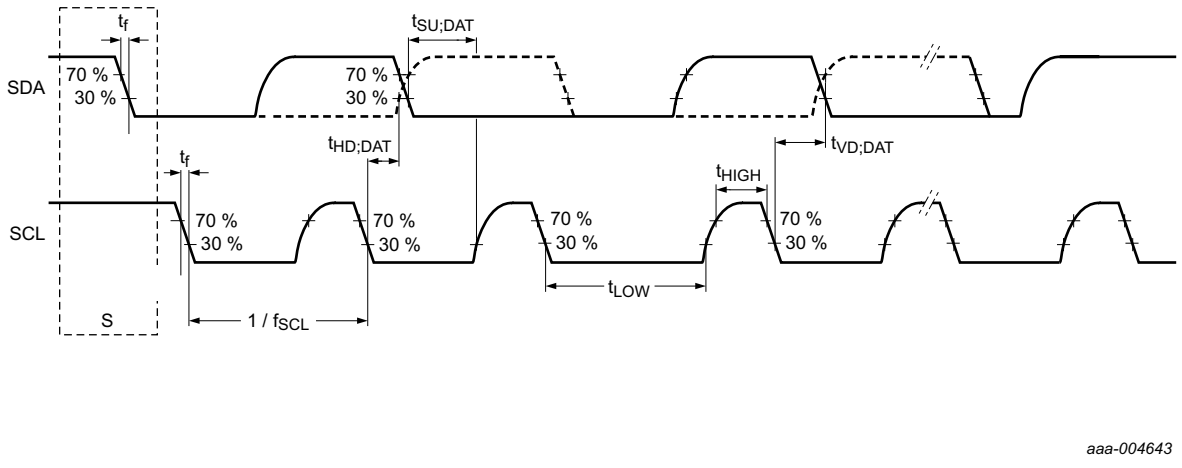

Fig 35. I²C-bus pins clock timing

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12.6 SPI interfaces

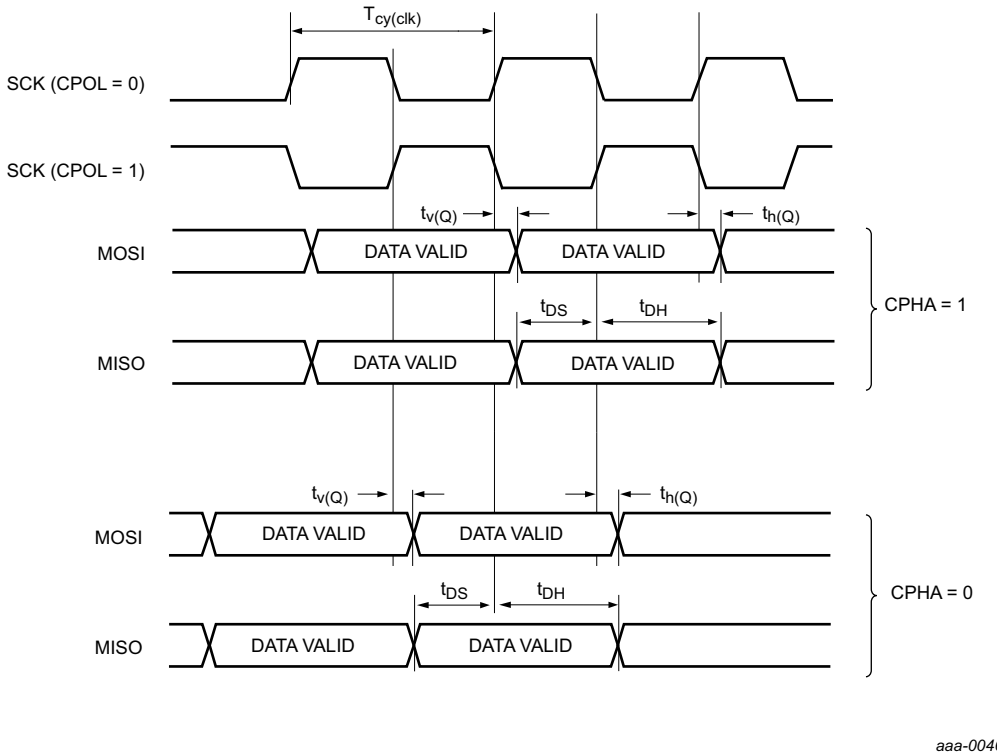
The maximum data bit rate is 17 Mbit/s in master mode and in slave mode.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_22 and PIO0_23.

Table 20. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF; input slew = 1 ns. Simulated parameters sampled at the 50 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
SPI master				
t_{DS}	data set-up time	30	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	4	ns
$t_{h(Q)}$	data output hold time	2	-	ns
SPI slave				
t_{DS}	data set-up time	6	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	29	ns
$t_{h(Q)}$	data output hold time	12	-	ns



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC15xx *User manual UM10736*.

Fig 36. SPI master timing

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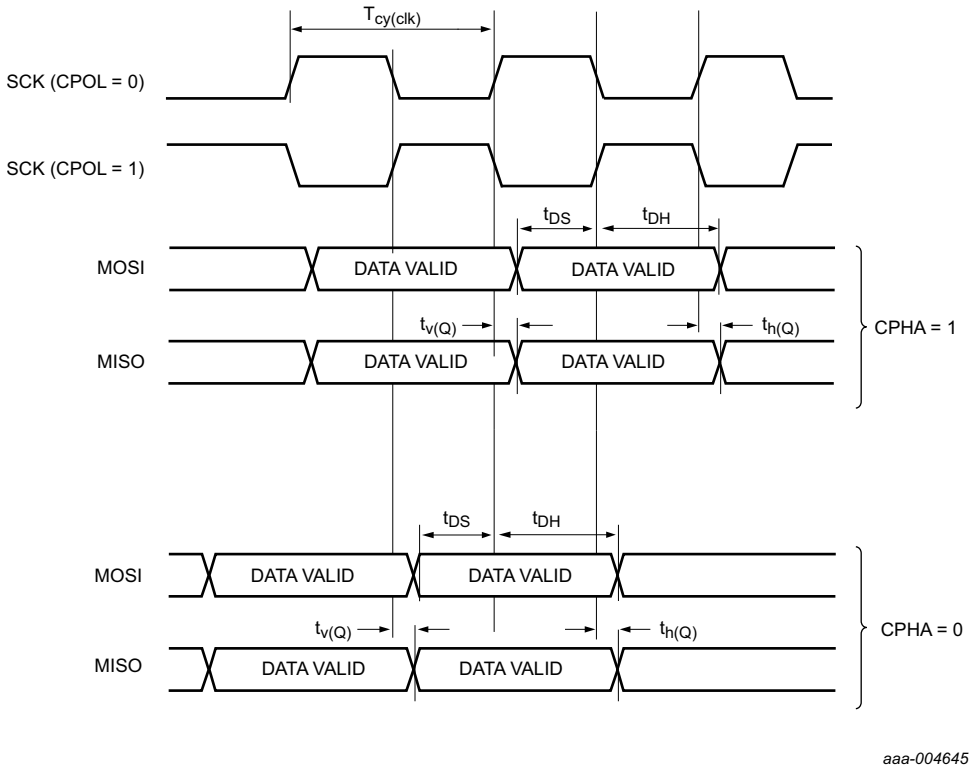

Fig 37. SPI slave timing

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12.7 USART interface

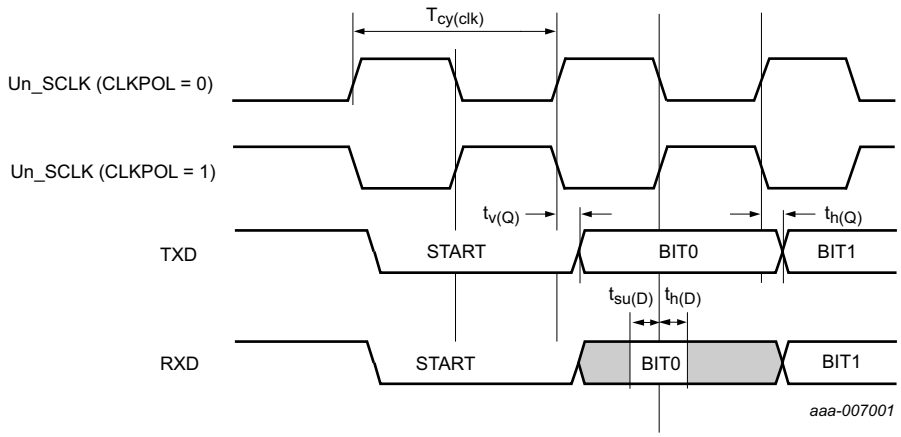
The maximum USART bit rate is 15 Mbit/s in synchronous mode master mode and 18 Mbit/s in synchronous slave mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_22 and PIO0_23.

Table 21. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	33	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	7	ns
$t_{h(Q)}$	data output hold time	2	-	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	13	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	28	ns
$t_{h(Q)}$	data output hold time	12	-	ns



In master mode, $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the LPC15xx *User manual UM10736*.

Fig 38. USART timing

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12.8 SCTimer/PWM output timing

Table 22. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V C_l = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	SCTimer0/PWM	-	-	4	ns
		SCTimer1/PWM	-	-	3	ns
		SCTimer2/PWM	-	-	1	ns
		SCTimer3/PWM	-	-	2	ns

13. Characteristics of analog peripherals

Table 23. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2				
		assertion	-	2.55	-	V
		de-assertion	-	2.69	-	V
		interrupt level 3				
		assertion	-	2.83	-	V
		de-assertion	-	2.96	-	V
		reset level 2				
		assertion	-	2.34	-	V
		de-assertion	-	2.49	-	V
		reset level 3				
		assertion	-	2.64	-	V
		de-assertion	-	2.79	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC15xx *user manual*.

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Table 24. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IA}	analog input voltage	[1]	0	V_{DDA}	V
C_{ia}	analog input capacitance		-	0.32	pF
$f_{clk(ADC)}$	ADC clock frequency	V_{DDA} ≥ 2.7 V		50	MHz
		V_{DDA} ≥ 2.4 V		25	MHz
f_s	sampling frequency	V_{DDA} ≥ 2.7 V	-	2	Msamples/s
		V_{DDA} ≥ 2.4 V	-	1	Msamples/s
E_D	differential linearity error	[2]	-	+/- 2	LSB
$E_{L(adj)}$	integral non-linearity	[3]	-	+/- 2	LSB
E_O	offset error	[4]	-	+/- 3	LSB
$V_{err(fs)}$	full-scale error voltage	2 Msamples/s [5]	-	+/- 0.12	%
		1 Msamples/s		+/- 0.07	%
Z_i	input impedance	f_s = 2 Msamples/s [6][7]	0.1	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

[5] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 40.

[6] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.~~1~~32 pF.

[7] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 11 for C_{io}.

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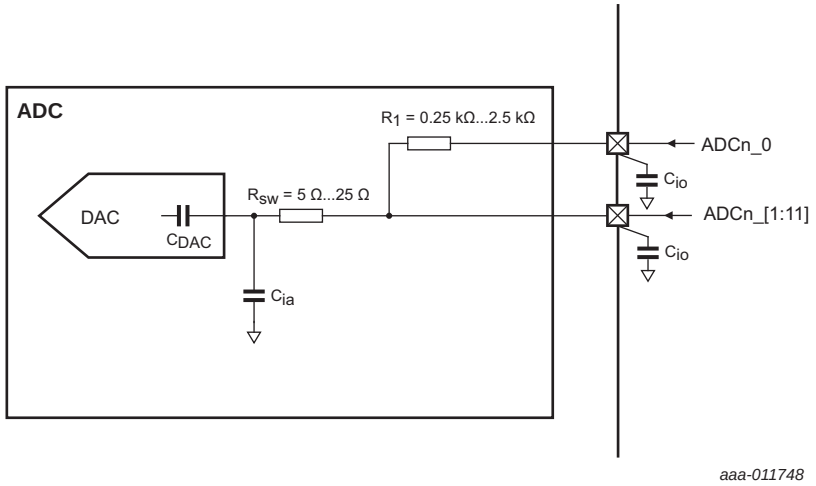

Fig 39. ADC input impedance

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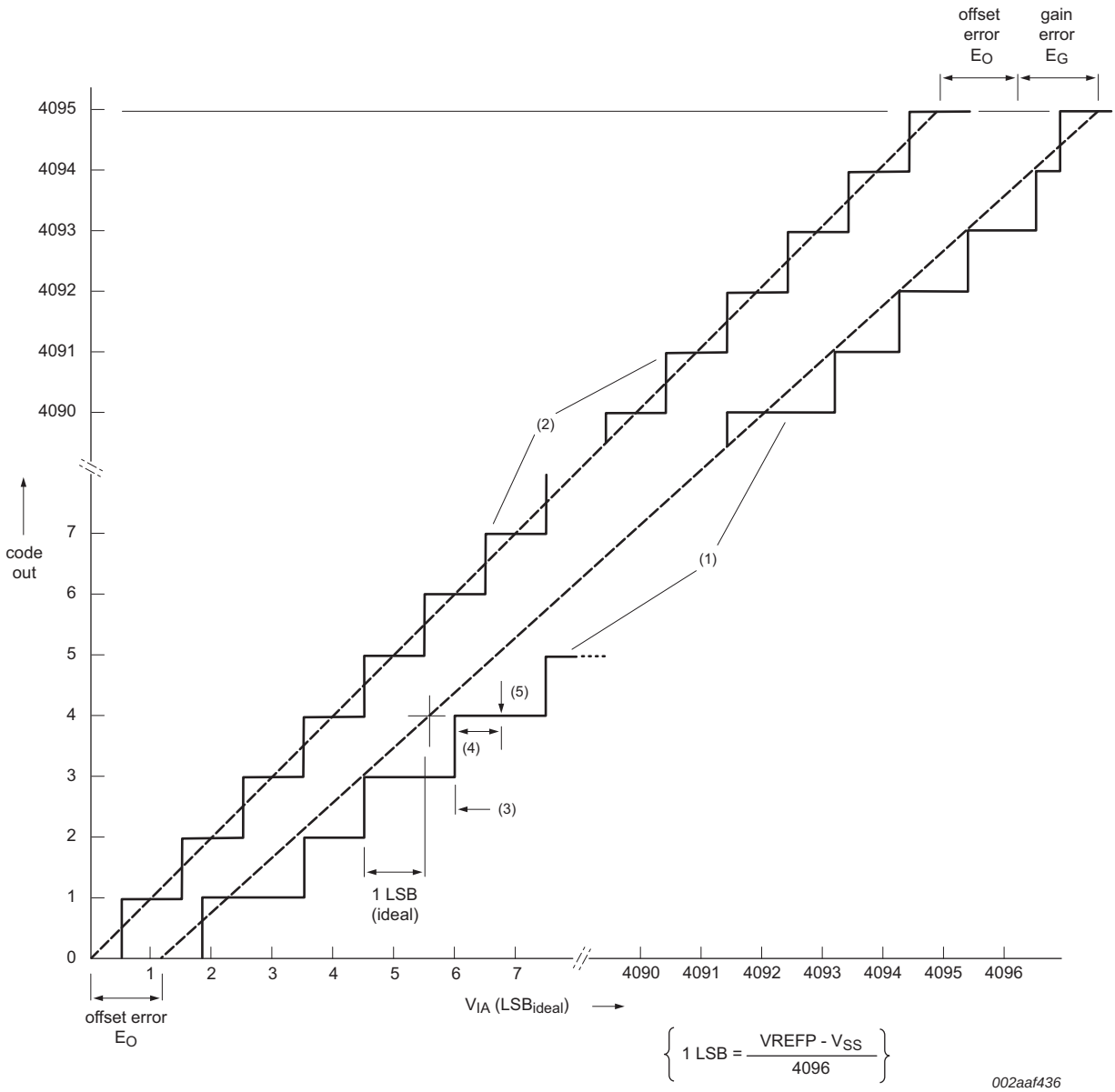

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 40. 12-bit ADC characteristics

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Table 25. DAC static and dynamic characteristics

V_{DDA} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified; C_L = 100 pF; R_L = 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
$f_{c(DAC)}$	DAC conversion frequency		-	-	500	kSamples/s
R_O	output resistance		-	300		Ω
t_s	settling time		-	-	2.5	µs
E_D	differential linearity error		-	-	+/-0.4	LSB
$E_{L(adj)}$	integral non-linearity		-	-	+/-3	LSB
E_O	offset error	VDDA = 3.3 V	-	-	+/-9	LSB
		VDDA = 2.4 V	-	-	+/-8	LSB
E_G	gain error		-	-	+/- 0.1	%
V_O	output voltage	Output voltage range with less than 1 LSB deviation; with minimum R_L connected to ground or power supply	-	-	V_{DDA} - 0.3	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

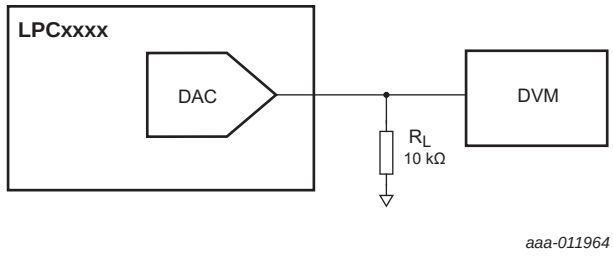

Fig 41. DAC test circuit

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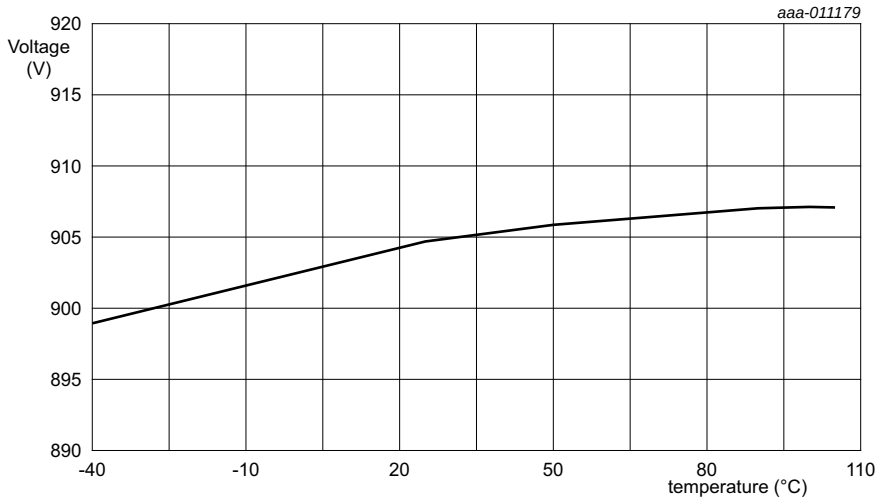
Table 26. Internal voltage reference static and dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = −40 °C to +105 °C [1]	875	-	925	mV
		T_{amb} = 25 °C		905		mV
$t_{s(pu)}$	power-up settling time	to 99% of V_O	-	-	125	µs

[1] Maximum and minimum values are measured on samples from the corners of the process matrix lot.



V_{DDA} = 3.3 V; averaged over process corners

Fig 42. Average internal voltage reference output voltage

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Table 27. Temperature sensor static and dynamic characteristics

V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = –40 °C to +105 °C [1]	-	-	5	°C
E_L	linearity error	T_{amb} = –40 °C to +105 °C	-	-	5	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value [2][3]	-	81	110	µs

[1] Absolute temperature accuracy.

[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models). Maximum values are derived from worst case simulation (V_{DDA} = 2.6 V; T_{amb} = 105 °C; slow process models).

[3] Internal voltage reference must be powered before the temperature sensor can be turned on.

[4] Settling time applies to switching between comparator and ADC channels.

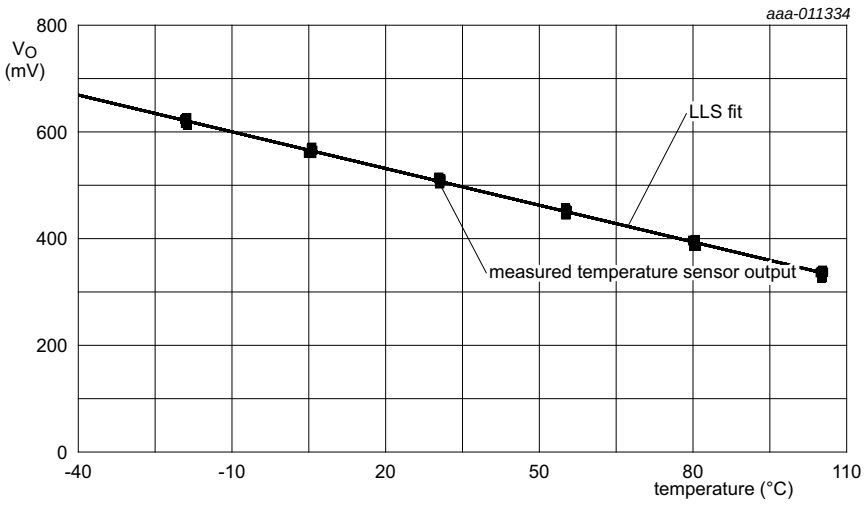
Table 28. Temperature sensor Linear-Least-Square (LLS) fit parameters

V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range	Min	Typ	Max	Unit
LLS slope	T_{amb} = –40 °C to +105 °C [1]	-	-2.29	-	mV/°C
LLS intercept at 0 °C	T_{amb} = –40 °C to +105 °C [1]	-	577.3	-	mV
Value at 30 °C	[2]	502	-	514	mV

[1] Measured over matrix samples.

[2] Measured for samples over process corners.



V_{DDA} = 3.3 V; measured on matrix samples.

Fig 43. LLS fit of the temperature sensor output voltage

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Table 29. Comparator characteristics

V_{DDA} = 3.0 V. DLY = 0x0 in the analog comparator CTRL register for shortest propagation delay setting. See the LPC15xx user manual UM10736.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{DD}	supply current	VP > VM	-	48	-	µA
		VM > VP	-	38	-	µA
V_{IC}	common-mode input voltage		0	-	V_{DDA}	V
DV_O	output voltage variation		0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V	-	+/- 3	-	mV
		V_{IC} = 1.5 V	-	+/- 3	-	mV
		V_{IC} = 2.9 V	-	+/- 6	-	mV
Dynamic characteristics						
$t_{startup}$	start-up time	nominal process	-	4.5	6	µs
t_{PD}	propagation delay	HIGH to LOW; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	196	250	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	68	110	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	64	90	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	86	130	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	48	80	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DDA} = 3.0 V;				
		V_{IC} = 0.1 V; 50 mV overdrive input [1]	-	98	130	ns
		V_{IC} = 0.1 V; rail-to-rail input [1]	-	24	40	ns
		V_{IC} = 1.5 V; 50 mV overdrive input [1]	-	88	130	ns
		V_{IC} = 1.5 V; rail-to-rail input [1]	-	68	120	ns
		V_{IC} = 2.9 V; 50 mV overdrive input [1]	-	84	110	ns
		V_{IC} = 2.9 V; rail-to-rail input [1]	-	98	180	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [2]				
		5 mV	3	-	8	mV
		10 mV	8	-	13	mV
		15 mV	17	-	25	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DDA} = 3.0 V; V_{IC} = 1.5 V; settings: [1][2]				
		5 mV	3	-	9	mV
		10 mV	8	-	18	mV
		15 mV	18	-	27	mV
R_{lad}	ladder resistance	-	-	1	-	MΩ

[1] C_L = 10 pF; results from measurements on silicon samples over process corners and over the full temperature range T_{amb} = -40 °C to +105 °C.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

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Table 30. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	-	-	30	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	-	-	20	µs

Table 31. Comparator voltage ladder reference static characteristics

V_{DDA} = 3.3 V; T_{amb} = -40 °C to + 105 °C; external or internal reference.

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
$E_{V(O)}$	output voltage error	decimal code = 00 [2]	-	0	3	mV
		decimal code = 08	-1.5	0	+1.5	%
		decimal code = 16	-1.5	0	+1.5	%
		decimal code = 24	-1.5	0	+1.5	%
		decimal code = 30	-1.5	0	+1.5	%
		decimal code = 31	-1.5	0	+1.5	%

[1] Measured over a polyresistor matrix lot with a 2 kHz input signal and overdrive < 100 µV.

[2] All peripherals except comparator, temperature sensor, and IRC turned off.

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14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 24:

- The ADC input trace must be short and as close as possible to the LPC15xx chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 44) or bus-powered device (see Figure 45).

On the LPC15xx, the PIO0_3/USB_VBUS pin is 5 V tolerant only when V_{DD} is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when V_{DD} = 0 V.

If V_{DD} is always greater than 0 V while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where V_{DD} can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than $0.7V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

V_{DD} = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

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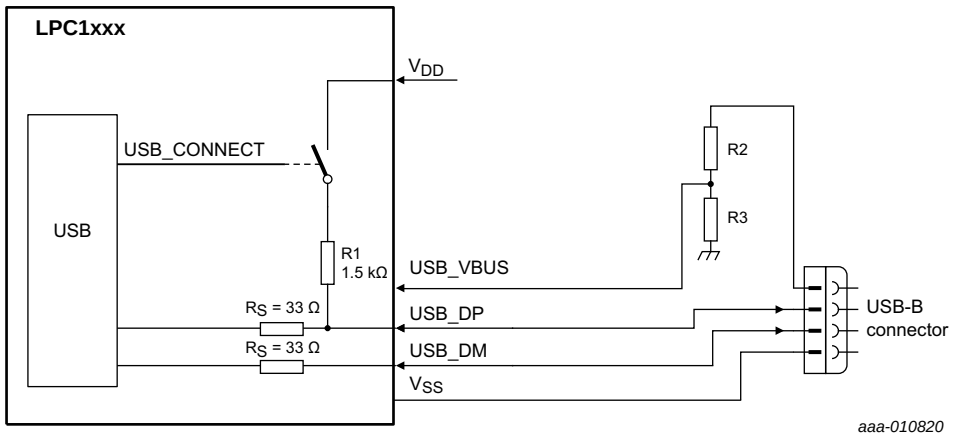

Fig 44. USB interface on a self-powered device where USB_VBUS = 5 V

For a bus-powered device, the VBUS signal does not need to be connected to the USB_VBUS pin (see Figure 45). The USB_CONNECT function can additionally be enabled internally by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required for the USB_CONNECT functionality.

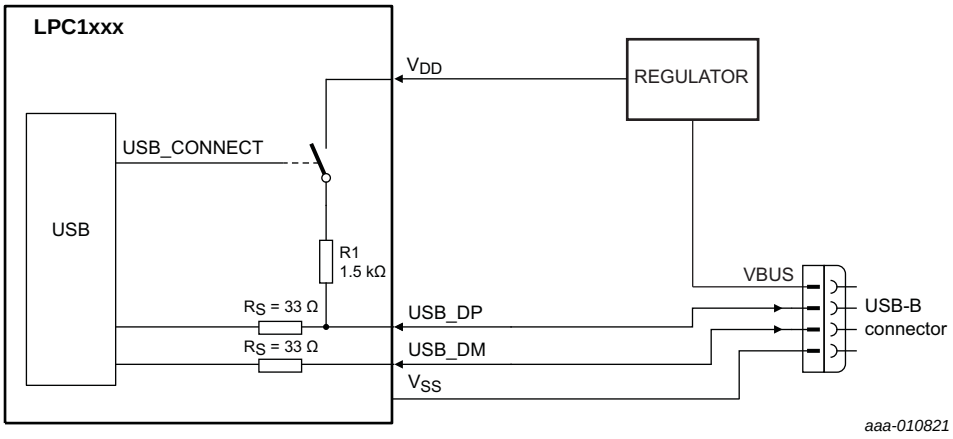

Fig 45. USB interface on a bus-powered device

Remark: When a bus-powered circuit as shown in Figure 45 is used or, for a self-powered device, when the VBUS pin is not connected, configure the PIO0_3/USB_VBUS pin for GPIO (PIO0_3) in the IOCON block. This ties the VBUS signal HIGH internally.

14.2.1 USB Low-speed operation

The USB device controller can be used in low-speed mode supporting 1.5 Mbit/s data exchange with a USB host controller.

Remark: To operate in low-speed mode, change the board connections as follows:

1. Connect USB_DP to the D- pin of the connector.
2. Connect USB_DM to the D+ pin of the connector.

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External 10 Ω resistors are recommended in low-speed mode to reduce over-shoots and accommodate for 5 m cable length required for USB-IF testing.

14.3 XTAL input and crystal oscillator component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

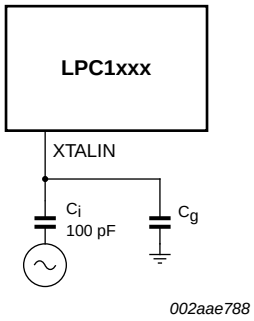

Fig 46. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 46), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 47 and in Table 32 and Table 33. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 47 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 32).

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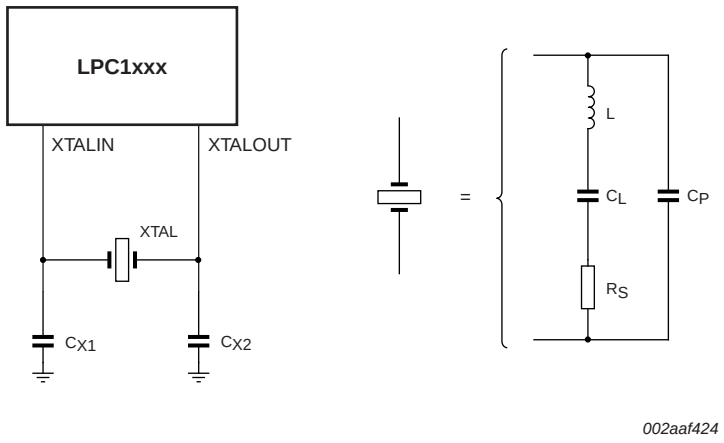

Fig 47. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 32. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 33. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.4 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in

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order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

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14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 48. If the RTC is not used, the RTCXIN pin can be grounded.

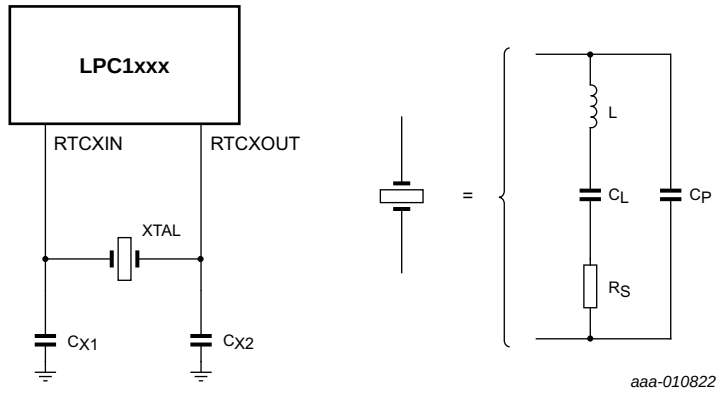

Fig 48. RTC oscillator components

Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry.The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If the external crystal's load capacitance is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$$C_{x1} = C_{x2} = 2 \times C_L - C_P$$

14.6 Connecting power, clocks, and debug functions

Figure 49 shows the basic board connections used to power the LPC15xx, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

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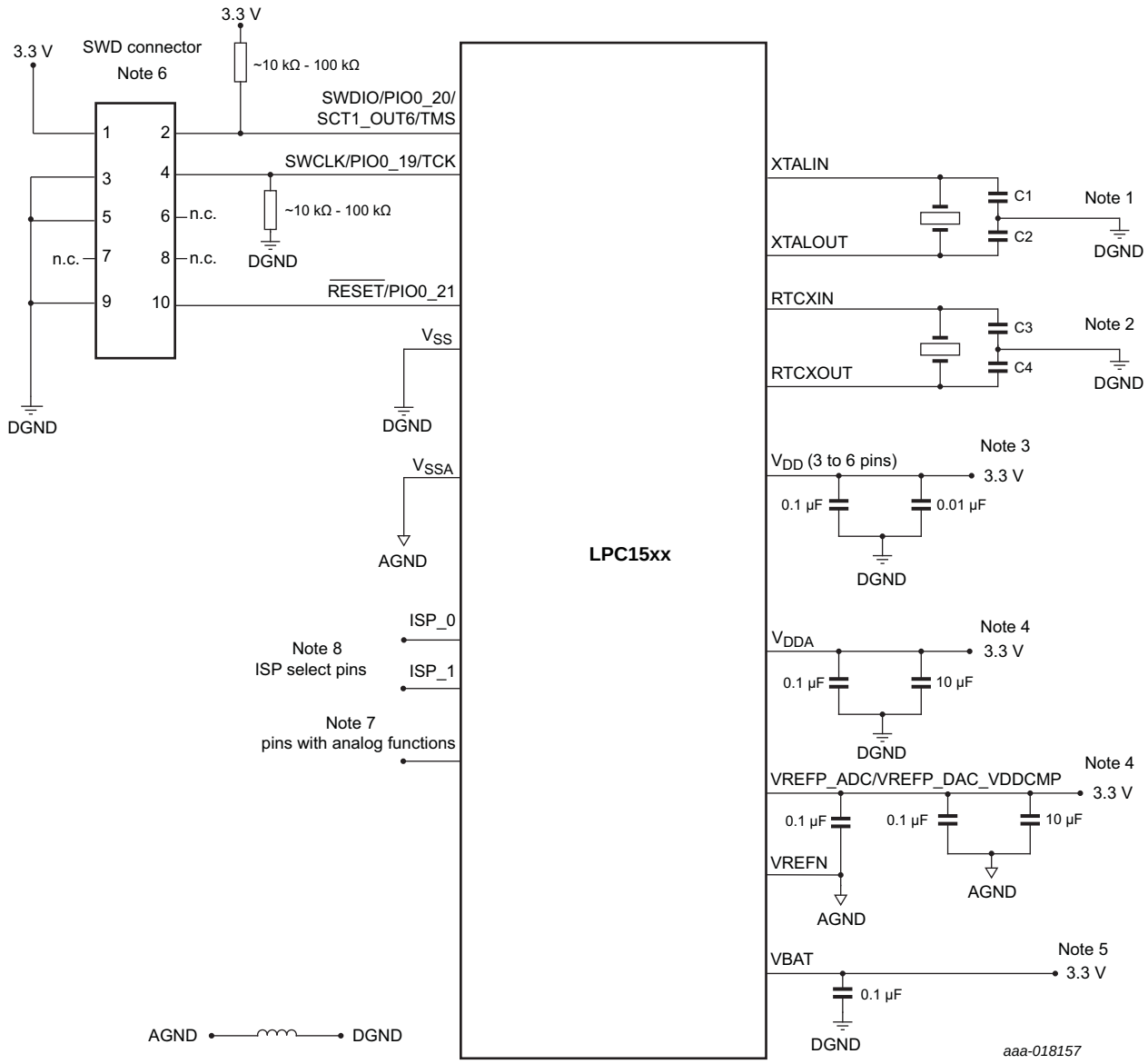

(1) See Section 14.3 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.5 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(8) ISP pin assignments is dependent on package type. See Table 7 “Pin assignments for ISP modes”.

Fig 49. Power, clock, and debug connections

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14.7 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as GPIO (switch matrix default) and setto outputs driving LOW with their internal pull-up disabled. To drive the output LOW, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_21	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
USB_DP/USB_DM	F	Can be left unconnected. When the USP PHY is disabled, the pins are LOW.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP_DAC_VDDCMP	-	Tie to VDD.
VREFP_ADC		Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VBAT	-	Tie to VDD if no external battery connected.
VSSA	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

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14.8 Pin states in different power modes

Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_22, PIO0_23 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$/PIO0_21	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, addan external pull-up to the $\overline{\text{RESET}}$ pin to reduce power consumption.
PIO0_17/ WAKEUP/$\overline{\text{TRST}}$	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

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14.9 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC1549JBD100.

Table 36. ElectroMagnetic Compatibility (EMC) for part LPC1549 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =						Unit
		12 MHz	24 MHz	36 MHz	48 MHz	60 MHz	72 MHz	
Input clock: IRC (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-5	-1	-5	-4	-3	0	dBµV
	30 MHz to 150 MHz	-1	+3	+6	+8	+11	+14	dBµV
	150 MHz to 1 GHz	-1	+2	+5	+10	+9	+11	dBµV
IEC level[1]	-	O	O	O	N	N	M	-
Input clock: crystal oscillator (12 MHz)								
maximum peak level	1 MHz to 30 MHz	-2	0	-5	-2	-2	2	dBµV
	30 MHz to 150 MHz	0	+3	+6	+8	+12	+14	dBµV
	150 MHz to 1 GHz	-1	+3	+5	+10	+10	+11	dBµV
IEC level[1]	-	O	O	O	N	N	M	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

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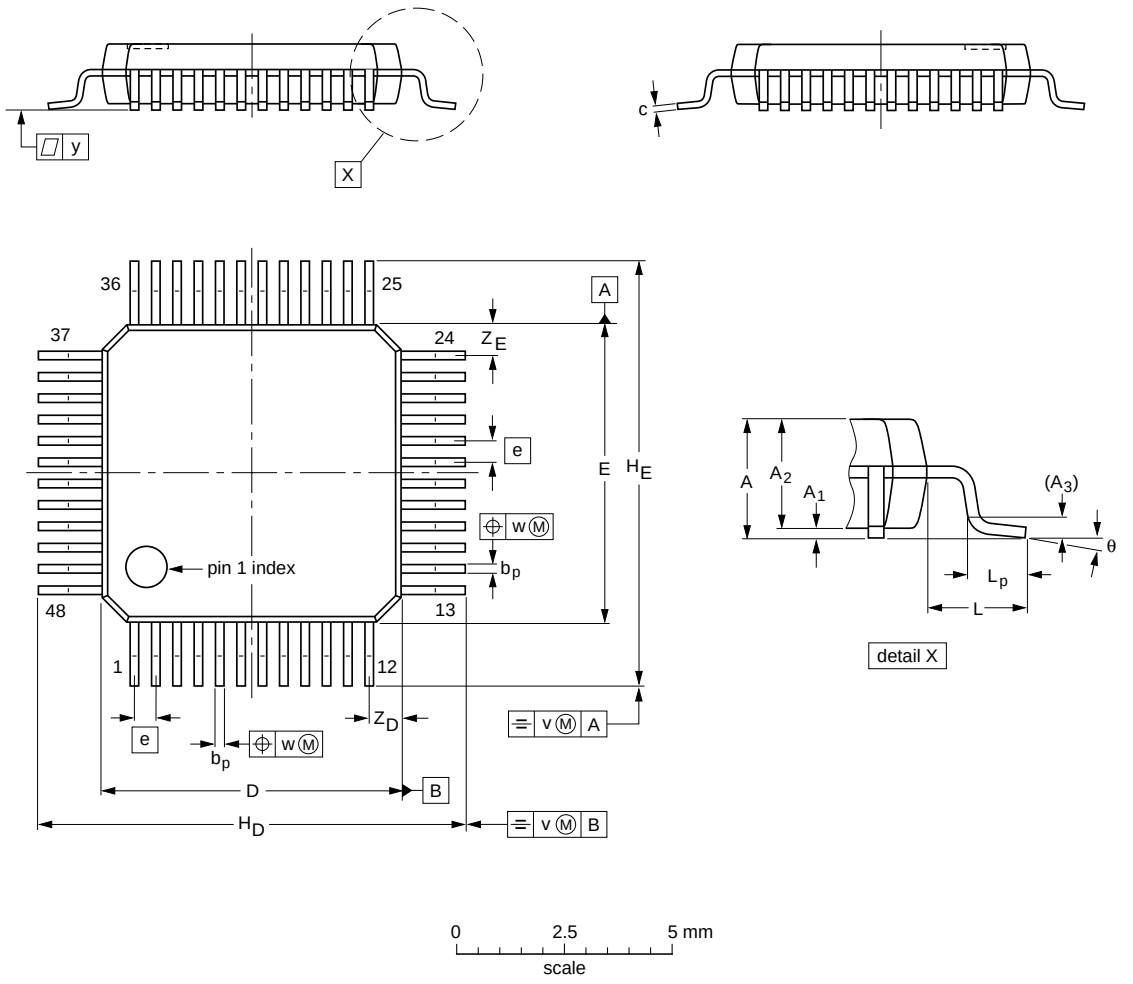
15. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 50. Package outline LQFP48 (SOT313-2)

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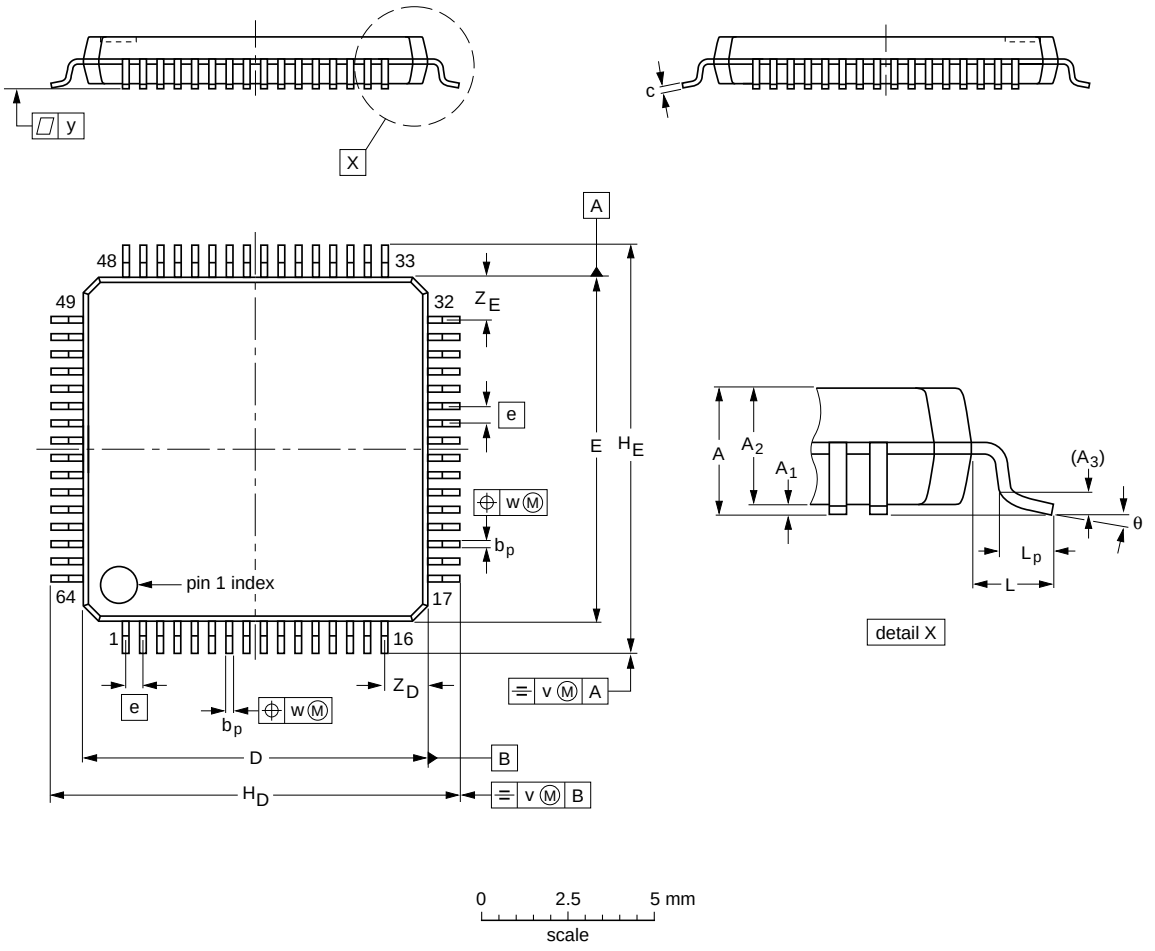
LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 51. Package outline LQFP64 (SOT314-2)

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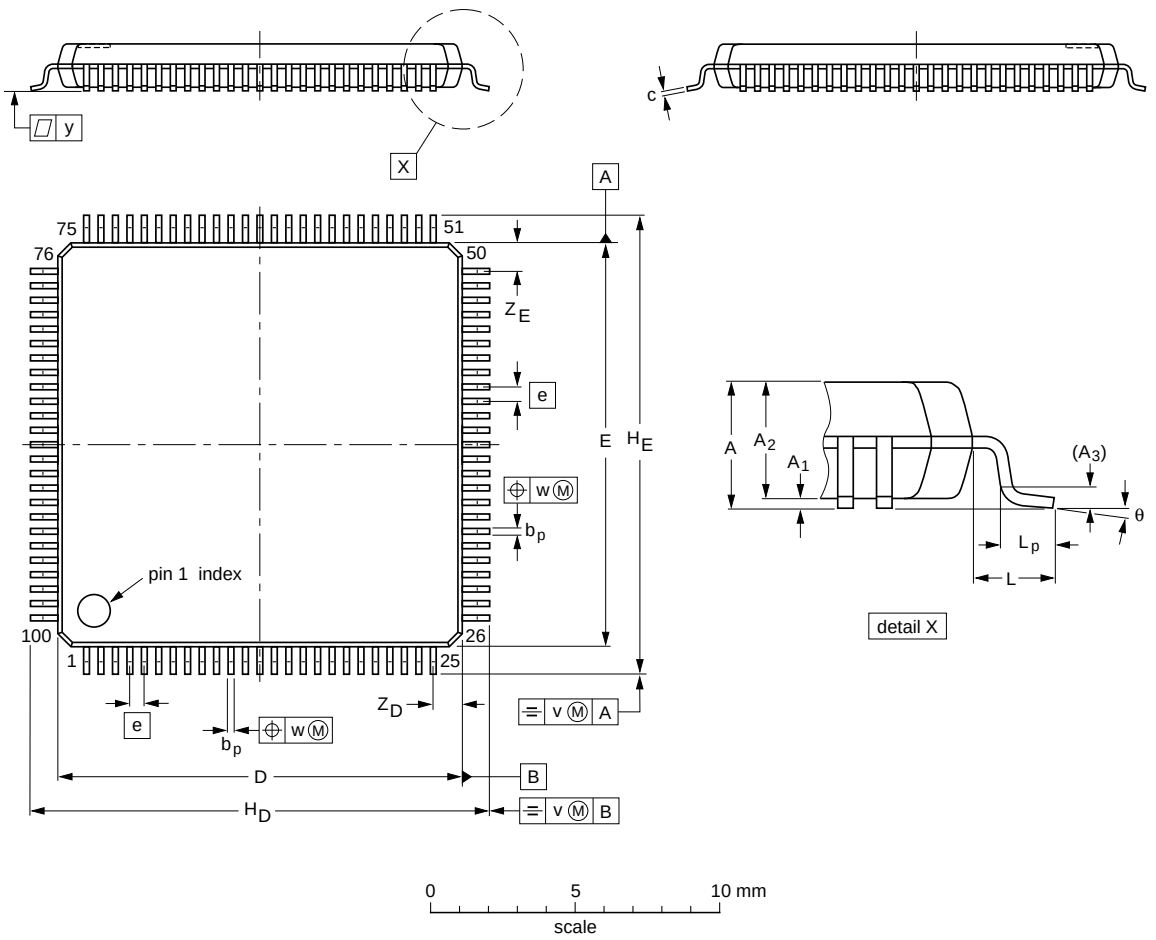
LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 52. Package outline LQFP100 (SOT407-1)

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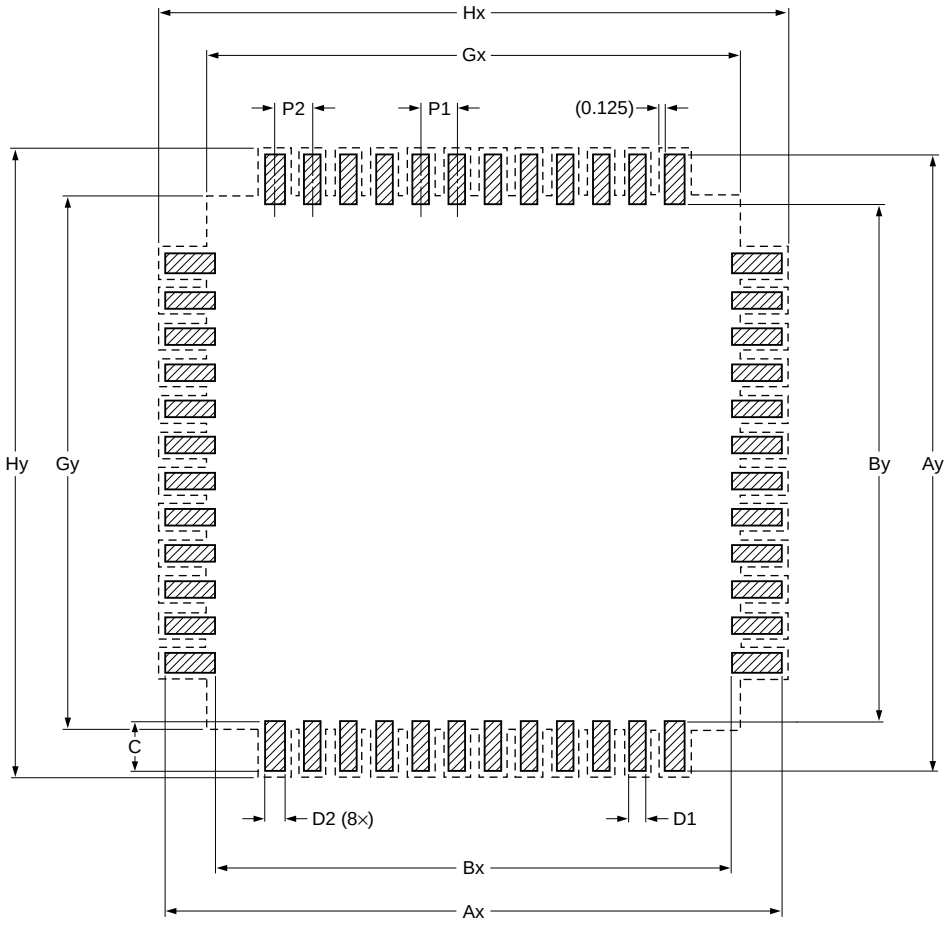
16. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 53. Reflow soldering for the LQFP48 package

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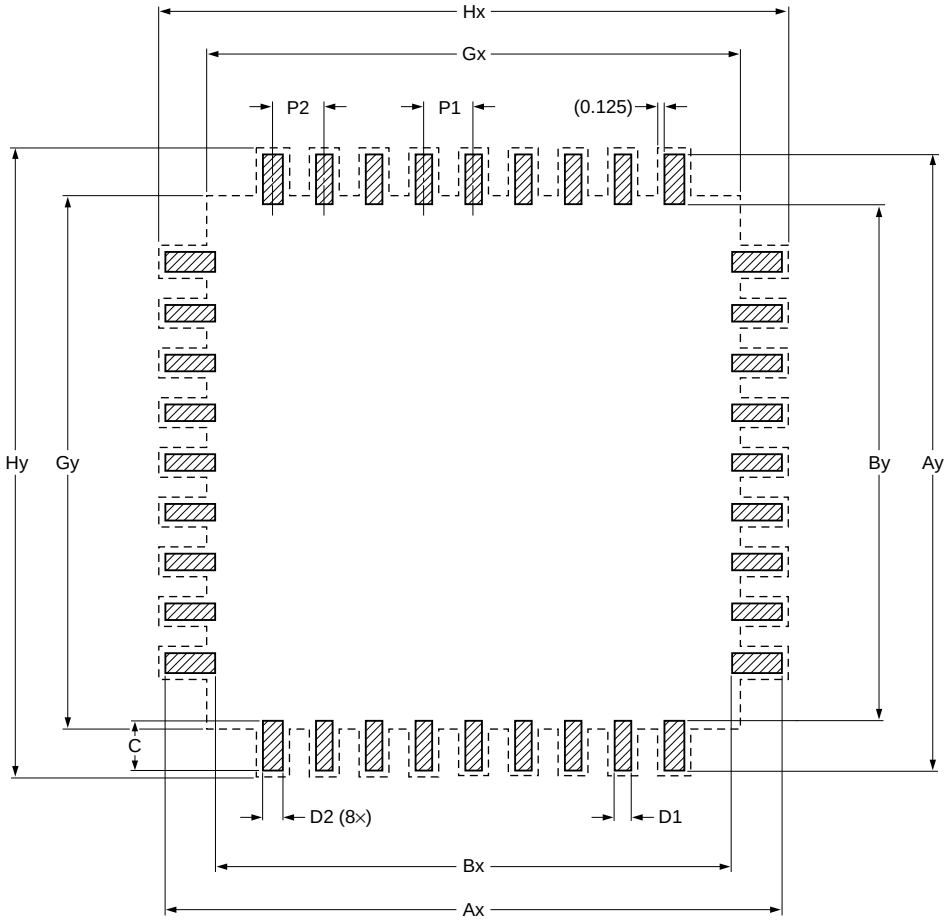
Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 54. Reflow soldering for the LQFP64 package

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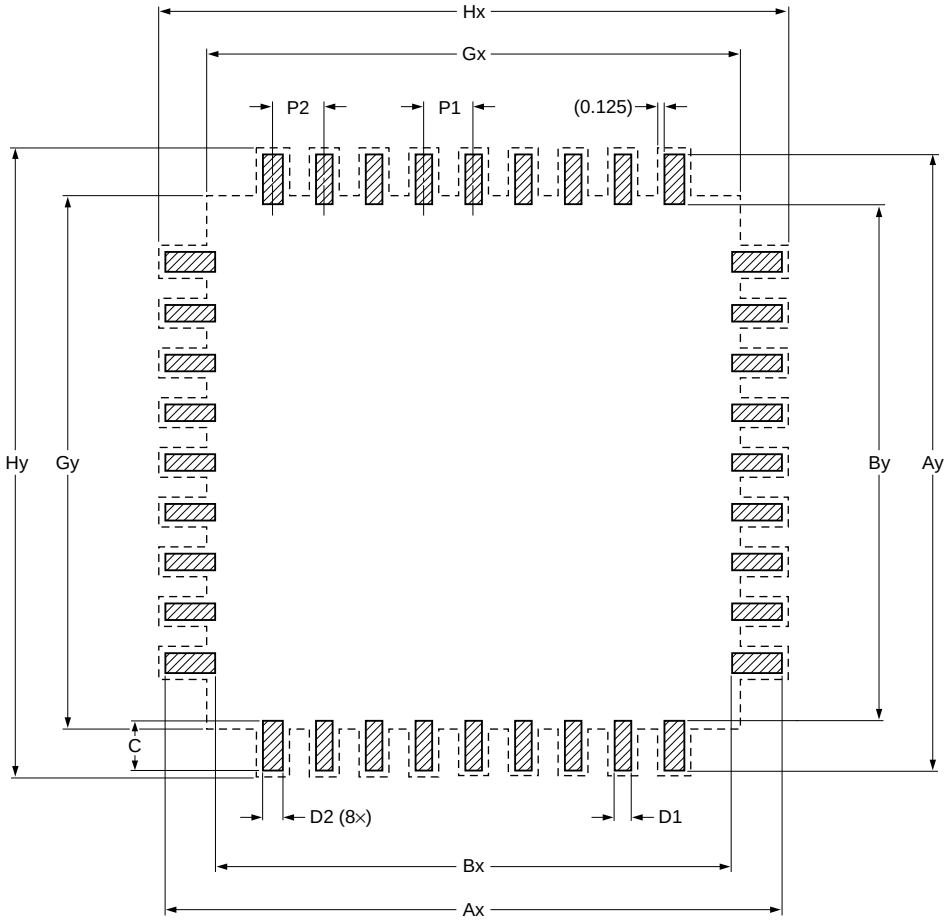
Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering for the LQFP100 package

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17. References

[1] LPC15xx User manual UM10736:
http://www.nxp.com/documents/user_manual/UM10736.pdf

[2] LPC15xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC15XX.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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18. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC15XX v.1.1	20150429	Product data sheet	-	LPC15XX v.1
Modifications:	• Pin description table updated for clarification (I2C-bus pins, VBAT, WAKEUP, RTCXIN/OUT). • Table note 11 added in Table 3. • Section 14.1 “ADC usage notes” added. • Section 14.6 “Connecting power, clocks, and debug functions” added. • Section 14.7 “Termination of unused pins” added. • Section 14.8 “Pin states in different power modes” added. • Section 14.9 “ElectroMagnetic Compatibility (EMC)” added. • Table 11 “Static characteristics”: Changed the power-down max specification value: I_{DD} Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C from 8 μA to 15 μA.			
LPC15XX v.1	<tbd>	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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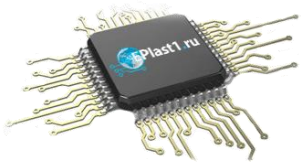

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